



GPL16218B

Advanced Game / ELA SoC with $\mu'nSP^{\text{®}}$ 2.0

Nov. 21, 2016

Version 1.0

Table of Contents

	<u>PAGE</u>
1. GENERAL DESCRIPTION	4
2. BLOCK DIAGRAM	4
3. FEATURES	4
4. SIGNAL DESCRIPTIONS	5
4.1. PAD ASSIGNMENT	9
4.2. PIN MAP	10
5. FUNCTIONAL DESCRIPTIONS	11
5.1. CPU	11
5.2. MEMORY	11
5.2.1. Internal SRAM	11
5.2.2. External memory	11
5.3. PLL, CLOCK, POWER MODE	11
5.3.1. PLL (Phase Lock Loop)	11
5.3.2. System Clock	11
5.4. POWER SAVINGS MODE	11
5.5. PICTURE PROCESS UNIT (PPU)	11
5.6. SOUND PROCESS UNIT	12
5.7. VIDEO OUTPUT INTERFACE	12
5.7.1. STN-LCD Interface	12
5.7.2. TFT-LCD Interface	12
5.7.3. TV encoder	12
5.8. INTERRUPT	12
5.9. GPIO	12
5.10. TIMER / COUNTER	12
5.11. WATCHDOG	12
5.12. SERIAL INTERFACE	13
5.12.1. Serial Peripheral Interface (SPI)	13
5.12.2. USB Device Function	13
5.13. IDE TOOLS FUNCTION	13
5.14. SD/MMC CONTROLLER	13
5.15. REAL TIME CLOCK (RTC)	13
5.16. ANALOG CONTROL	13
5.16.1. DAC Control	13
6. ELECTRICAL SPECIFICATIONS	14
6.1. ABSOLUTE MAXIMUM RATING	14
6.2. DC CHARACTERISTICS	14
6.3. VIDEO DAC CHARACTERISTICS	14
6.4. AUDIO DAC CHARACTERISTICS	15
6.5. REGULATOR CHARACTERISTICS	15
7. RECOMMENDED BOARD LAYOUT	16
7.1. POWER AND GROUND	16
7.2. CRYSTAL AND PLL	16

7.3. ANALOG SECTION	16
8. APPLICATION CIRCUIT	17
8.1. FOR TV PLUG-AND-PLAY SIMPLE ELA/GAME 2D APPLICATION	17
9. PACKAGE/PAD LOCATIONS	18
9.1. ORDERING INFORMATION	18
9.2. PACKAGE INFORMATION	18
10. DISCLAIMER	20
11. REVISION HISTORY	21

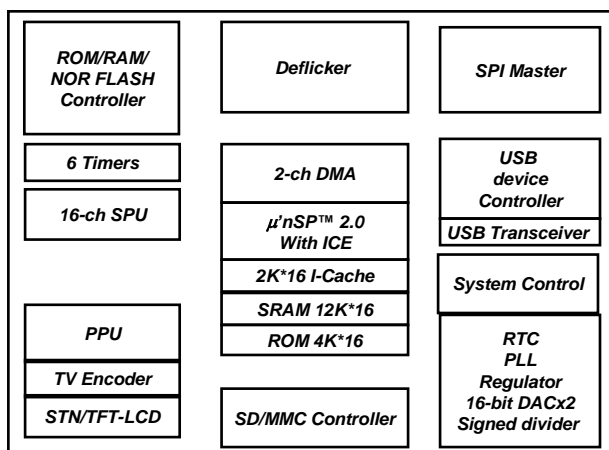
Advanced Game / ELA SoC with $\mu'nSP^{\circledR}$ 2.0

1. GENERAL DESCRIPTION

The Generalplus GPL16218B is highly integrated system-on-a-chip and it targets a cost-effective, high performance micro-controller solution for game, education and e-learning applications. It embeds $\mu'nSP^{\circledR}$ 2.0 (16-bit CPU developed by Sunplus Technology) with 4KB I-cache, picture process unit (PPU), TV encoder with QVGA output, 16 channels sound process unit (SPU), ROM/SRAM/NOR FLASH controller, two channel DMA controller, six-channel 16-bit timers, SD/MMC memory interface, USB device, mono STN-LCD and TFT-LCD interface, interrupt controller, SPI master controller, programmable I/O ports, 16-bit DAC for audio playback, PLL, de-flicker, divider and embedded 12K*16 bits SRAM, and 4K*16 ROM, all in a single compact Integrated circuit.

By providing a complete set of common system peripherals, the Generalplus GPL16218B chip minimizes overall system costs and eliminates the need to configure additional components. The GPL16218B provides not only the high-speed performance and low cost for a system, but it also integrates several powerful tools into the development system, such as development system with C language, assembly compiler, linker, source debugger functions and project management tools.

2. BLOCK DIAGRAM



3. FEATURES

- $\mu'nSP^{\circledR}$ 2.0 16-bit CPU with frequency up to 96MHz.
- 4K bytes I-cache.
- 12k*16 bits SRAM for programming or LCD frame buffers.
- 4K*16 bits ROM for boot code.
- Picture Process Unit (PPU)
 - Four Text layers + 256 Sprites
 - QVGA output
 - Line base or Frame base operation
 - De-flicker for TV output
 - Up-to 4096x4096 Text Size
 - Alpha-channel sprite
- Sound Process Unit (SPU)
 - Sixteen hardware PCM/ADPCM channels
 - Built-in sound compressor
- Static memory controller. (ROM/SRAM/NOR FLASH/Page Memory)
- Two-channel DMA controller.
- Mono and 16 gray STN-LCD controller.
- TFT-LCD controller which can be UPS051(serial RGB), UPS052(serial RGB dummy), parallel RGB, i80(8-bit/16-bit system bus) I/F type, and CCIR601/CCIR656.
- 29 sources Interrupt Controller.
- Universal Serial Bus (USB) 2.0 full speed compliant device with built-in transceiver.
- Watch-dog timer.
- 32-bit by 32-bit signed divider
- Real-time clock.
- Six 16-bit timers.
- SD/MMC memory interface.
- SPI master interface.
- 51 Programmable general I/O ports with pull-high/low control.
- Power manager.
- Built-in 3.0V to 1.8V Regulator.
- Low voltage reset.
- 96MHz, 27MHz and 12MHz PLL.
- 16-bit stereo DAC(2ch) for audio playback.
- TV encoder which support NTSC/PAL output.

4. SIGNAL DESCRIPTIONS

Left Side

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
1	2	DVSS	Digital GND	P	Digital ground	
2	3	BKCSB0	Memory I/F	I/O	External memory chip select 0	IOD0
3	4	XA3	Memory I/F	I/O	External memory address pin 3	
4	5	XA2	Memory I/F	I/O	External memory address pin 2	
5	6	XA1	Memory I/F	I/O	External memory address pin 1	
6	7	BKCSB1	Memory I/F	I/O	External memory chip select 1	IOD1
7	8	XA0	Memory I/F	I/O	External memory address pin 0	
8	9	XA10	Memory I/F	I/O	External memory address pin 10	
9	10	XA11	Memory I/F	I/O	External memory address pin 11	
10	11	BKCSB2	Memory I/F	I/O	External memory chip select 2	IOD2
11	12	XA12	Memory I/F	I/O	External memory address pin 12	
12	13	XA13	Memory I/F	I/O	External memory address pin 13	
13	14	XA14	Memory I/F	I/O	External memory address pin 14	
14	15	DVCC33	Digital PWR	P	3.3V digital power	
15	16	DVSS	Digital GND	P	Digital ground	
16	17	DVCC18	Digital PWR	P	1.8V digital power	
17	18	BKWEB	Memory I/F	I/O	External memory write enable pin	
18	19	BKOEB	Memory I/F	I/O	External memory output enable pin	
19	20	XA15	Memory I/F	I/O	External memory address pin 15	IOD7
20	21	XA16	Memory I/F	I/O	External memory address pin 16	IOD8
21	22	XA17	Memory I/F	I/O	External memory address pin 17	IOD9
22	23	XA18	Memory I/F	I/O	External memory address pin 18	IOD10
23	24	XA19	Memory I/F	I/O	External memory address pin 19	IOD11
24	25	XA20	Memory I/F	I/O	External memory address pin 20	IOD12
25	26	XA21	Memory I/F	I/O	External memory address pin 21	IOD13
26	27	XA22	Memory I/F	I/O	External memory address pin 22	IOD14
27	28	XA23	Memory I/F	I/O	External memory address pin 23	IOD15
28	29	DVSS	Digital GND	P	Digital ground	
29	30	TEST	MODE	I	Test mode control signal. Input floating; it must be tied with ground under normal operation.	

Bottom Side

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
30	31	RESETB	SYSTEM	I/O	Reset input pin. (Low active)	
31	32	IOB2	MODE	I/O	BM2: Boot mode selection pin 2. (0: use 6MHz crystal, usually for TV application, 1: use internal PLL, usually for other application w/o TV)	IOB2
32	33	IOB1	MODE	I/O	BM1: Boot mode selection pin 1. 1 : Internal ROM Boot (SPI boot) 0 : Chip Select 0 Memory Boot	IOB1
33	34	IOB0	MODE	I/O	BM0: Boot mode selection pin 0. (This pin must be pull low with a resistor)	IOB0
34	35	ICEDA	ICE	I/O	Embedded ICE data pin. Default is floating. In development phase, connect it with a capacitor to GND. In production phase, connect it with a resistor to GND.	
35	36	ICECK	ICE	O	Embedded ICE clock pin. Default is floating. In development phase, connect it with a capacitor to GND. In production phase, connect it with a resistor to GND.	
36	37	IOA7	Key/LCD	I/O	TFT-LCD's D7	IOA7
37	38	IOA6	Key/LCD	I/O	TFT-LCD's D6	IOA6
38	39	IOA5	Key/LCD	I/O	TFT-LCD's D5	IOA5
39	40	IOA4	Key/LCD	I/O	TFT-LCD's D4	IOA4
40	41	IOA3	Key/LCD	I/O	TFT-LCD's D3	IOA3
41	42	IOA2	Key/LCD	I/O	TFT-LCD's D2	IOA2
42	43	IOA1	Key/LCD	I/O	TFT-LCD's D1	IOA1
43	44	IOA0	Key/LCD	I/O	TFT-LCD's D0	IOA0
44	45	IOA8	Key/LCD	I/O	TFT-LCD's D8	IOA8
45	46	DVCC33	Digital PWR	PWR	3.3V digital power	
46	47	DVSS	Digital GND	PWR	Digital ground	
47	48	DVCC18	Digital PWR	PWR	1.8V digital power	
48	49	IOA9	Key/LCD	I/O	TFT-LCD's D9	IOA9
49	50	IOA10	Key/LCD	I/O	TFT-LCD's D10	IOA10
50	51	IOA11	Key/LCD	I/O	TFT-LCD's D11	IOA11
51	52	IOA12	Key/LCD	I/O	TFT-LCD's D12	IOA12
52	53	IOA13	Key/LCD	I/O	TFT-LCD's D13	IOA13
53	54	IOA14	Key/LCD	I/O	TFT-LCD's D14	IOA14
54	55	IOA15	Key/LCD	I/O	TFT-LCD's D15	IOA15
55	56	IOC8	SD2	I/O	SD2 data0	IOC8
56	57	IOC7	SD2	I/O	SD2 clock	IOC7
57	58	IOC6	SD2	I/O	SD2 command	IOC6
58	59	IOC10	SD2	I/O	SD2 data2	IOC10
59	60	IOC9	SD2	I/O	SD2 data1	IOC9
60	61	IOC5	SD2	I/O	SD2 data3	IOC5
61	62	IOC11	Key change A	I/O	Key change A input	IOC11
62	63	IOC12	Key change B	I/O	Key change B input	IOC12
63	64	PLLV33	PLL	PWR	3.3V PLL power	
64	65	X32KO	PLL	O	32768 Hz crystal output pin	
65	66	X32KI	PLL	I	32768 Hz crystal input pin	

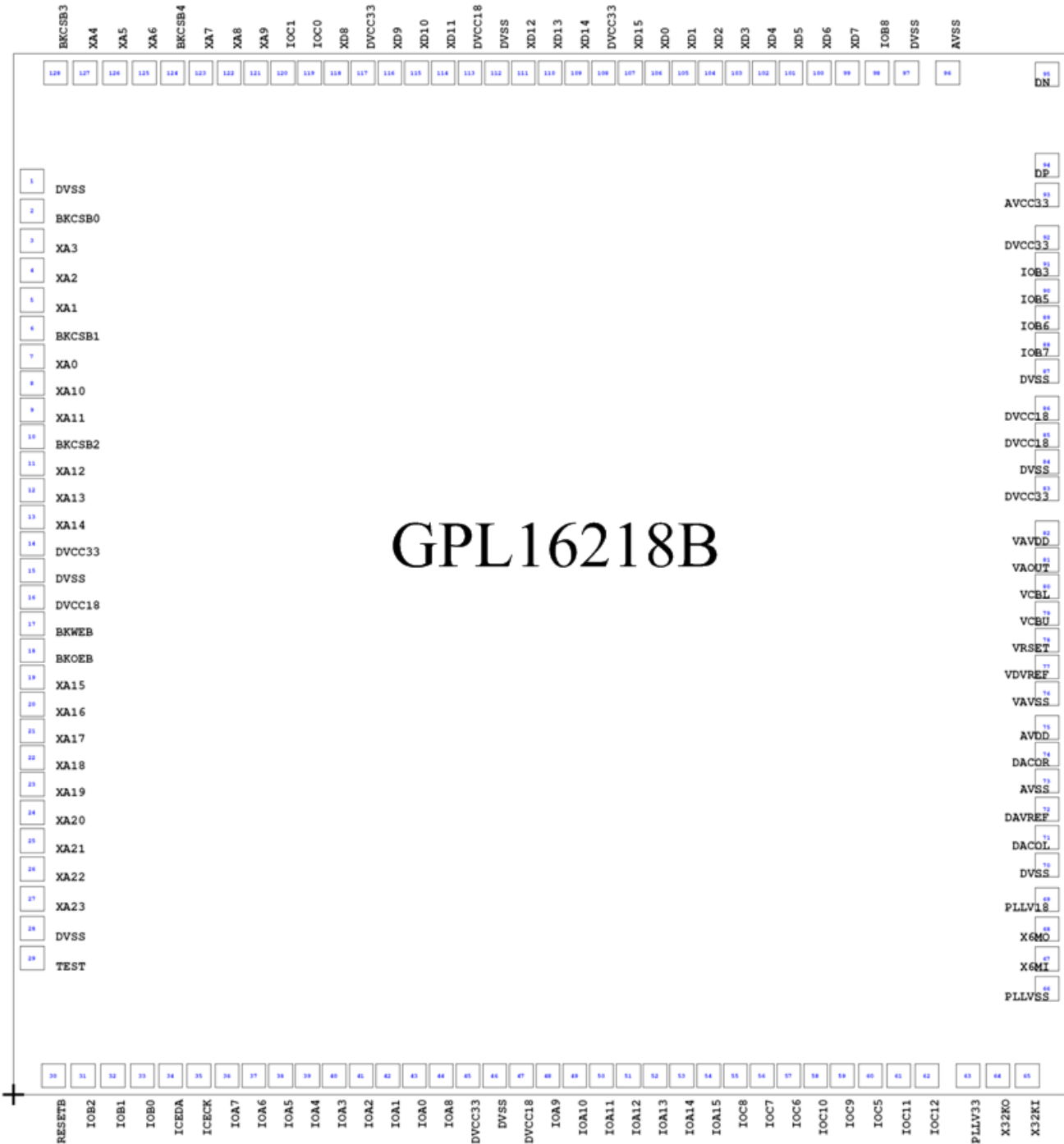
Right Side

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
66	67	PLLSS	PLL	PWR	PLL ground	
67	68	X6MI	PLL	A/I	6MHz crystal input pin or 12M PLL filter pin	
68	69	X6MO	PLL	O	6MHz crystal output pin	
69	70	PLL18	PLL	P	1.8V power for PLL	
70	71	DVSS	Digital GND	PWR	Digital ground	
71	72	DACOL	DAC	A/O	Left channel audio output	
72	73	DAVREF	DAC	A/O	DAC reference voltage pin	
73	74	AVSS	DAC	PWR	DAC ground	
74	75	DACOR	DAC	A/O	Right channel audio output	
75	76	AVDD	DAC	PWR	3.3V DAC power	
76	77	VAVSS	VDAC	PWR	VDAC ground	
77	78	VDVREF	VDAC	A/I	Video DAC reference voltage	IOE2
78	79	VRSET	VDAC	A/I	Video DAC current source adjustment	IOE1
79	80	VCBU	VDAC	A/I	Video DAC reference voltage	
80	81	VCBL	VDAC	A/I	Video DAC reference voltage	
81	82	VAOUT	VDAC	A/O	Video DAC output	IOE0
82	83	VAVDD	VDAC	PWR	3.3V VDAC power	
83	84	DVCC33	Regulator	PWR	3.3V Regulator power	
84	85	DVSS	Regulator	PWR	Regulator ground	
85	86	DVCC18	Regulator	A/O	Regulator 1.8V output	
86	87	DVCC18	Digital PWR	PWR	1.8V digital power	
87	88	DVSS	Digital GND	PWR	Digital ground	
88	89	IOB7	SPI	I/O	SPIRX: SPI data input	IOB7
89	90	IOB6	SPI	I/O	SPITXD: SPI data output	IOB6
90	91	IOB5	SPI	I/O	SPICLK: SPI clock	IOB5
91	92	IOB3	LCD	I/O	TFT DCLK	IOB3
92	93	DVCC33	Digital PWR	PWR	3.3V digital power	
93	94	AVCC33	USB	PWR	3.3V USB power	
94	95	DP	USB	I/O	DP pin of USB PHY	
95	96	DN	USB	I/O	DN pin of USB PHY	

Top Side

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
96	97	AVSS	USB	PWR	USB ground	
97	98	DVSS	Digital GND	PWR	Digital ground	
98	99	IOB8	EINT	I/O	External INT0; Light gun input	IOB8
99	100	XD7	Memory I/F	I/O	External memory data pin 7	
100	101	XD6	Memory I/F	I/O	External memory data pin 6	
101	102	XD5	Memory I/F	I/O	External memory data pin 5	
102	103	XD4	Memory I/F	I/O	External memory data pin 4	
103	104	XD3	Memory I/F	I/O	External memory data pin 3	
104	105	XD2	Memory I/F	I/O	External memory data pin 2	
105	106	XD1	Memory I/F	I/O	External memory data pin 1	
106	107	XD0	Memory I/F	I/O	External memory data pin 0	
107	108	XD15	Memory I/F	I/O	External memory data pin 15	
108	109	DVCC33	Digital PWR	PWR	3.3V digital power	
109	110	XD14	Memory I/F	I/O	External memory data pin 14	
110	111	XD13	Memory I/F	I/O	External memory data pin 13	
111	112	XD12	Memory I/F	I/O	External memory data pin 12	
112	113	DVSS	Digital GND	PWR	Digital ground	
113	114	DVCC18	Digital PWR	PWR	1.8V digital power	
114	115	XD11	Memory I/F	I/O	External memory data pin 11	
115	116	XD10	Memory I/F	I/O	External memory data pin 10	
116	117	XD9	Memory I/F	I/O	External memory data pin 9	
117	118	DVCC33	Digital PWR	PWR	3.3V digital power	
118	119	XD8	Memory I/F	I/O	External memory data pin 8	
119	120	IOC0	General I/O	I/O	General-purposed I/O C0	IOC0
120	121	IOC1	General I/O	I/O	General-purposed I/O C1	IOC1
121	122	XA9	Memory I/F	I/O	External memory address pin 9	
122	123	XA8	Memory I/F	I/O	External memory address pin 8	
123	124	XA7	Memory I/F	I/O	External memory address pin 7	
124	125	BKCSB4	Memory I/F	I/O	External memory chip select 4	IOD4
125	126	XA6	Memory I/F	I/O	External memory address pin 6	
126	127	XA5	Memory I/F	I/O	External memory address pin 5	
127	128	XA4	Memory I/F	I/O	External memory address pin 4	
128	1	BKCSB3	Memory I/F	I/O	External memory chip select 3	IOD3

4.1. PAD Assignment



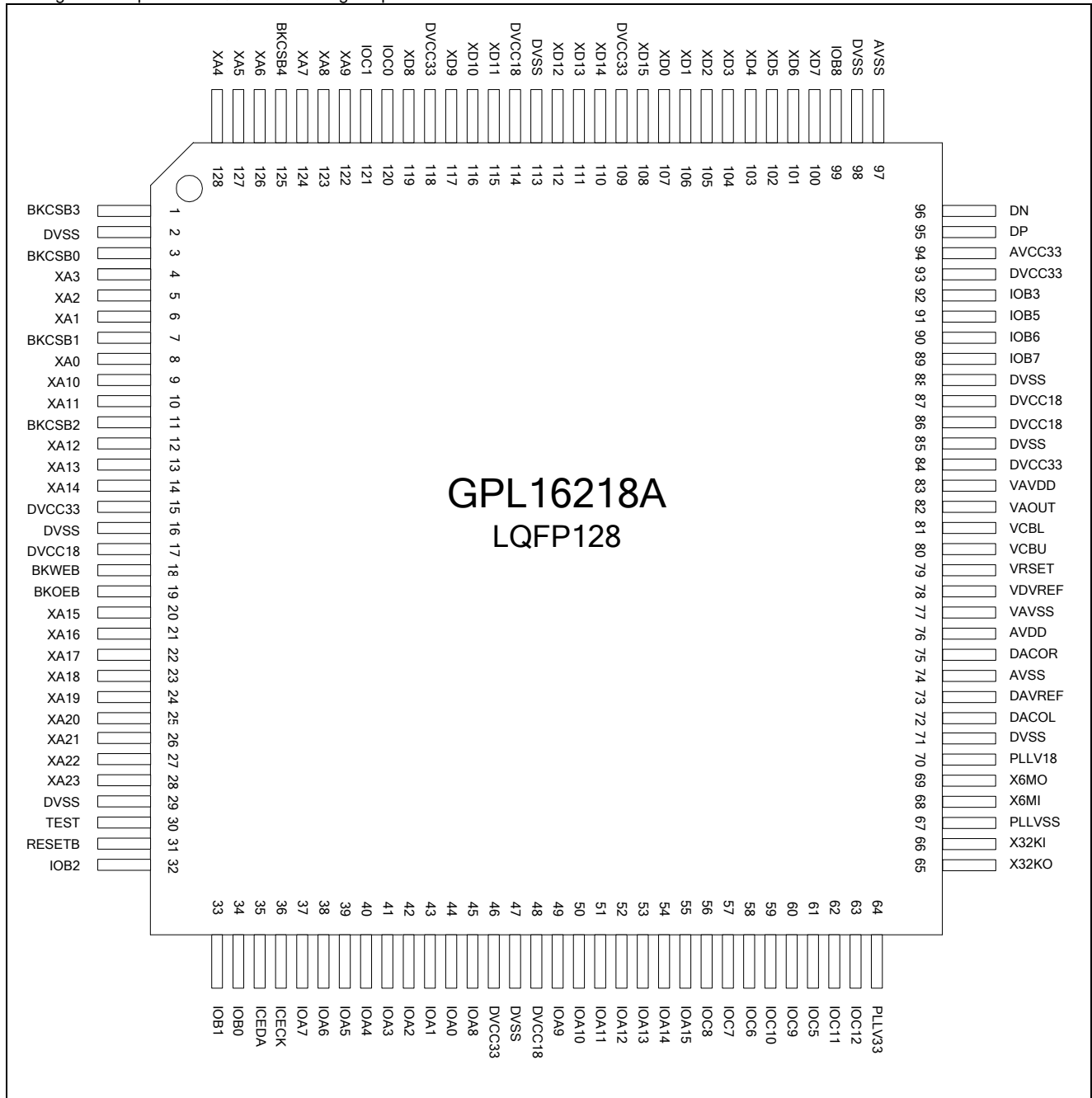
This IC substrate should be connected to VSS

Note1: To assure IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as closed as possible.

4.2. Pin Map

Package Pin Sequence - LQFP 128 Package Top View



5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The GPL16218B is equipped with a 16-bit $\mu'nSP^{\text{TM}}$ 2.0, a powerful 16-bit microprocessor by SUNPLUS and pronounced as *micro-n-SP*. Sixteen registers are involved in $\mu'nSP^{\text{TM}}$ 2.0: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP), SR (Segment Register) and R8 - R15 (General-purpose register). The interrupts include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK. GPL16218B is also built-in a 4K bytes I-cache which is able to boost the performance significantly.

5.2. Memory

5.2.1. Internal SRAM

The amount of SRAM is a 12K-word (stack included), ranged from 0x0000 through 0x2FFF with access speed of one CPU clock cycle. Since this SRAM is located in CPU's local bus, the system bus will not be taken over when this SRAM is accessed by CPU. This SRAM can be accessed freely by CPU/PPU/DMA /LCD.

5.2.2. External memory

The memory space is separated into 5 banks; each bank can be up to 256 pages, and 64K words per page. The controller can support up to 80M words of NOR flash memories. Each bank can be programmed as ROM/SRAM/NOR Flash.

5.3. PLL, Clock, Power Mode

5.3.1. PLL (Phase Lock Loop)

There are three PLLs embedded in GPL16218B: 1st PLL pumping up to 96MHz, 2nd to 27MHz, and 3rd PLL up to 12MHz. The output frequency of fast PLL is programmable and ranged from 15MHz ~ 96MHz (3MHz per step).

5.3.2. System Clock

The system clock can be selected from 32768 or 12M or 96M (determined by fast PLL's output frequency) by register setting. Furthermore, a clock divider, which can divide clocks up to 1/128, is provided to reduce power consumption.

5.4. Power Savings Mode

The GPL16218B provide four power savings modes: Normal, Wait, Halt and Sleep. The following table indicates the function operating status in these modes.

Mode	CPU	System	RTC	POWEREN	After wakeup
Normal	ON	ON	ON	ON	-
Wait	OFF	ON	ON	ON	Next Instruction
Halt	OFF	OFF	ON	OFF	Reset CPU
Halt2	OFF	OFF	ON	OFF	Next Instruction
Sleep	OFF	OFF	OFF	OFF	Reset System

Enter the Wait/Halt/Halt2/Sleep mode, is done by writing designated value to specific port. Possible wake-up triggers are interrupt, timer, or key-status changes.

5.5. Picture Process Unit (PPU)

GPL16218B equips a powerful process engine which has the following features.

Item	Features
Text Layer	<ol style="list-style-type: none"> 1. Maximum 4 text layers at the same time. 2. Supports text size up to 4096x4096. 3. Supports Text rotate and scale effect. 4. Supports horizontal/vertical compression effect. 5. Supports horizontal movement effect. 6. Supports 64-level alpha blending.
Sprite	<ol style="list-style-type: none"> 1. Maximum 256 sprites at the same time. 2. Each sprite supports 64-level rotate function. 3. Each sprite supports 64-level zoom in/out function from 1/32 to 8.75 times. 4. Each sprite supports 64-level alpha blending. 5. Each sprite supports 3 kinds of mosaic effect. 6. Supports alpha channel function. 7. All above functions can combine at the same time.
Color	<ol style="list-style-type: none"> 1. Text layer and sprites support 4/16/64/256-color palette and RGB1555/RGB565/YUYV/RGBG bitmap mode. 2. 1024 palette entry for text layers and sprites. 3. Supports 16/24-bit level of palette index color.
Operation Mode	<ol style="list-style-type: none"> 1. Supports QVGA at line/frame base mode.
Other Features	<ol style="list-style-type: none"> 1. Supports light gun interface. 2. Supports sprite DMA function. 3. Supports de-flicker for TV output.

5.6. Sound Process Unit

GPL16218B equips a 16-channel SPU and each channel of SPU supports PCM8/PCM16/ADPCM36. A dynamic volume compressor is also embedded to magnify the overall volume. For software application, GPL16218B is also capable for wide-band (sample rate \geq 16kHz) low bit rate algorithm.

5.7. Video Output Interface

5.7.1. STN-LCD Interface

The STN-LCD driver interface built-in GPL16218B supports up-to 320 X 240 LCD panel and supports 1/4 bits data bus for monochrome/gray-scale STN. Memory interface type CSTN is also supported.

5.7.2. TFT-LCD Interface

The GPL16218B supports TFT-LCD controller. The LCM interface includes parallel RGB (5-6-5), serial delta RGB, serial stripe RGB, CPU (MPU) type, and CCIR601/CCIR656. The horizontal resolution reaches up to 320 pixels, and the vertical resolution up to 240 pixels. The TFT controller mainly provides 4 timing control pins and 8 or 16 data pins to control external TFT panel and they are VSYNC, HSYNC, DE, DCLK, and DATA.

5.7.3. TV encoder

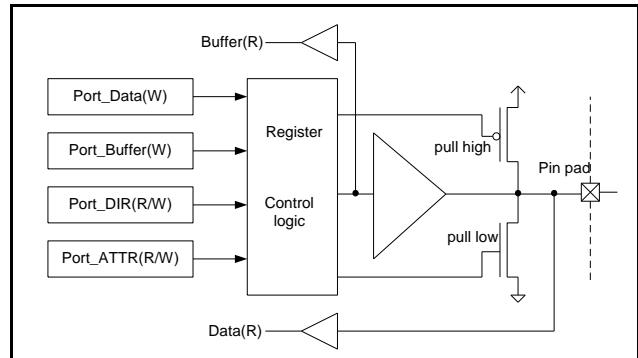
The GPL16218B supports TV composite output. Both NTSC and PAL outputs are supported. The output resolution can be up to 640 x 480. A 10-bit video DAC is also embedded in GPL16218B which can utilize minimum system cost and best performance.

5.8. Interrupt

The GPL16218B has 29 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources. Some of the interrupt sources can be programmed as FIQ or IRQ via register settings.

5.9. GPIO

Five I/O ports are built in GPL16218B: IOA, IOB, IOC, IOD, and IOE. Each I/O pin has its normal function and is described in the signal description section. When the normal function of the I/O is disabled, it will switch to GPIO function automatically. The following diagram is a GPIO schematic.



5.10. Timer / Counter

The GPL16218B provides six 16-bit timers/counters, TimerA to TimerF. The clock source of each timer can be set individually. For Timer A to TimerD, an INT will be sent to CPU when timer overflows. Besides, Capture, Comparison and PWM functions are also provided by TimerA/TimerB/TimerC.

Clock Source A	Clock Source B
Fosc/2	2048Hz
Fosc/256	1024Hz
32768Hz	256Hz
8192Hz	Time Base B
4096Hz	Time Base A
1	0
Another Timer	1
INT1	INT2

The GPL16218B is embedded with a time base controller which is used to generate the slow and precisely interrupt form 32768Hz crystal. The following table shows the available time base.

TimeBase A	TimeBase B	TimeBase C
--	8Hz	128Hz
1Hz	16Hz	256Hz
2Hz	32Hz	512Hz
4Hz	64Hz	1024Hz

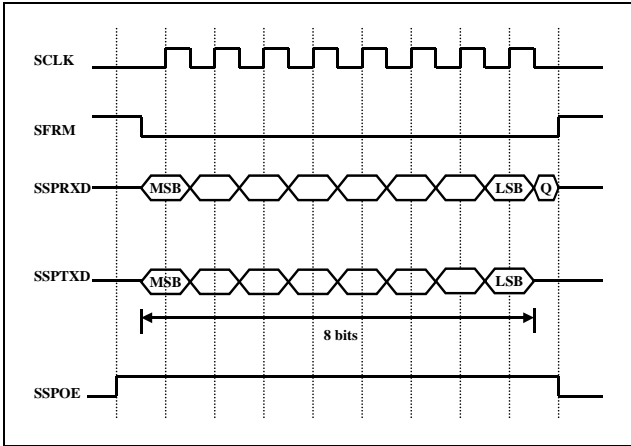
5.11. Watchdog

The purpose of watchdog is to monitor if the system operates normally. Within a certain period of time, watchdog must be cleared. If not, CPU assumes the program has been running into an abnormal condition. Thus, CPU will reset the system to the initial state and start running the program all over again. In GPL16218B, the clear period is software programmable. If watchdog is cleared before expired, the system will not be reset.

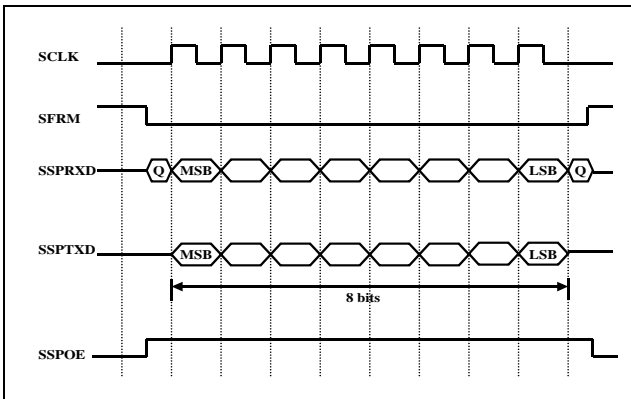
5.12. Serial Interface

5.12.1. Serial Peripheral Interface (SPI)

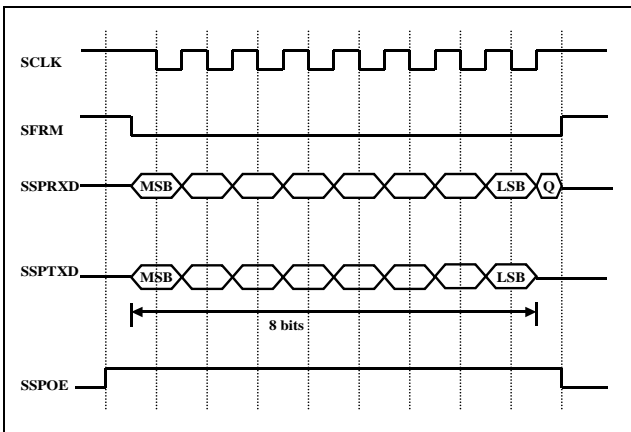
The SPI interface is a master interface that enables synchronous serial communication with slave/master peripherals. Two 8-byte FIFOs are used for transmitting and receiving data. Four types of timings are supported and shown in the following diagram.



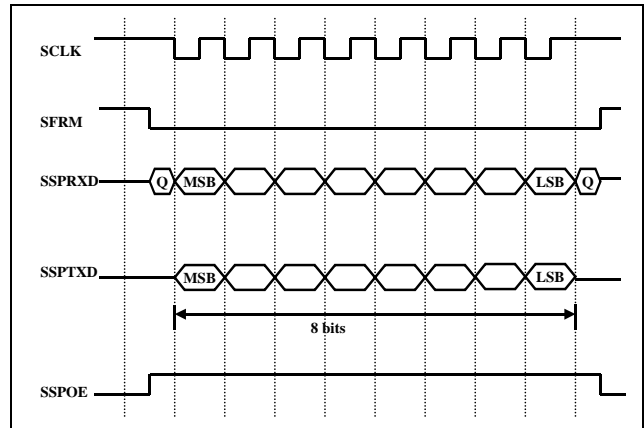
SPO = 0, SPH = 0



SPO = 0, SPH = 1



SPO = 1, SPH = 0



SPO = 1, SPH = 1

5.12.2. USB Device Function

GPL16218B provides USB device function which is compatible with USB 1.1 and USB 2.0 full speed standard. An USB transceiver is built-in for devices function. A FIFO with size of 128x8 is used for bulk-in and bulk-out transfer and an 8-byte FIFO is used for pipe transfer control. Interrupt IN/OUT pipes are also supported. The DMA transfer is enabled for bulk-in/out to maximize the transfer performance.

5.13. IDE Tools Function

The functions of IDE include the follows:

- 1). C compiler, Assembly, and Linker
- 2). Single step trace
- 3). Break point (break point for debugging)
- 4). Run (execute)

5.14. SD/MMC Controller

GPL16218B provides SD/MMC controllers which is compatible with MMC system specification version 2.3 and SD Memory Card specification 1.1. The controller supports automatically CRC generation and check, 1-bit and 4-bit transfer, interrupt generation when buffer empty/full, DMA transfer for page read/write.

5.15. Real Time Clock (RTC)

The RTC block provides the alarm function, schedule function, and hour/minute/second/half-second interrupt function.

5.16. Analog Control

5.16.1. DAC Control

A 16-bit stereo DAC (2ch) is embedded in GPL16218B. For both left and right channels, a 16x16 FIFO is used to prevent sound glitch when CPU is busy. The left and right channels do not need to have the same sample rate. A single DMA channel can utilize the stereo playback.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	DVCC33 PLL_V33	-0.3 to 4.0	V
Supply Voltage 2	AVDD	-0.3 to 4.0	V
Supply Voltage 3	DVCC18 PLL_V18	-0.3 to 2.16	V
Input Voltage	V _{IN}	-0.3 to 4.0	V
Operating Temperature	T _A	0 to 70	°C
Storage Temperature	T _{STG}	-40 to +150	°C

6.2. DC Characteristics

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage 1	DVCC33 PLL_V33	2.7/3.0 ¹	3.0	3.6	V	-
Operating Voltage 2	AVDD	2.7	3.0	3.3	V	-
Operating Voltage 3	DVCC18 PLL_V18	1.62	1.8	1.98	V	-
Operating Current	I _{OP}	-	100 ²	-	mA	@96MHz, 3.3V, all clocks on
Power Down Current	I _{PD}	-	80 ³	100 ³	μA	Sleep Mode@1.5V
High Input Voltage	V _{IH}	0.7DVDD33	-	DVDD33	V	-
Low Input Voltage	V _{IL}	VSS	-	0.8	V	-
Crystal Frequency 1	-	-	32768	-	Hz	-
Crystal Frequency 2	F _{CRYSTAL}	-	6.0 ⁴	-	MHz	-
System Clock	F _{SYS}	256Hz ⁵	48	96	MHz	-

Note1: When USB function is enabled, the minimum voltage of DVCC33/PLL_V33 is 3.0V.

Note2: Operating current depends on software code. In this test case, the following macro is turned on: Video DAC, Audio DAC, 96MHz PLL and 27MHz PLL.

Note3: Regulator is in sleep mode.

Note4: 6M Crystal is needed when USB function or TV function is enabled.

Note5: By setting clock divider and changing system clock to 32768 mode.

6.3. Video DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	10	-	Bit	-
INL	-	±1	-	LSB max	-
DNL	-	±0.5	-	LSB max	-
Input Capacitor	-	10	-	pF	-
Voltage Reference Range	1.14	1.235	1.33	V	-
VRSET	0.570	0.617	0.665	V	-
Offset Error	-	0	-	V	-
Gain Error	-	25	-	LSB	-
Glitch Energy	-	50	-	pV	-
Conversion Rate	-	30	-	ns	-

6.4. Audio DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	16	-	Bit	-
Full Scale Output Voltage	-	0.6*VDDDA	-	Vp-p	-
THD+N (f = 1kHz)	-	0.1	-	%	-
Noise at No Signal	-85	90	-	dBv	-
Frequency Response	20	-	19200	Hz	-

6.5. Regulator Characteristics

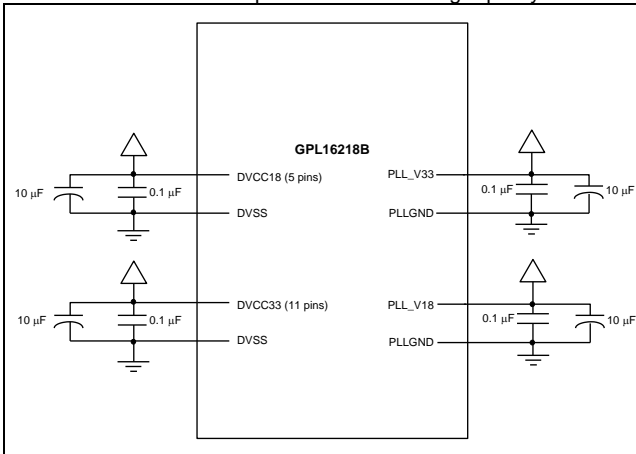
Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.7	3.0	3.6	V
Maximum Current Output	IREGO	-	70	100	mA
Output Voltage	VREGO	1.5 ¹	1.8	1.89	V
Standby Current	IREGS	-	10	-	uA

Note1: To save more power, it is recommended switching to 1.5V before entering the halt/sleep mode and switching to 1.8V in normal operation mode.

7. RECOMMENDED BOARD LAYOUT

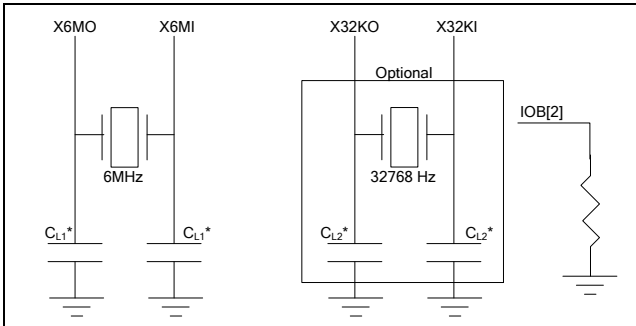
7.1. Power and Ground

All digital power and ground should be connected. The decoupling capacitor of 0.1μF and 10μF should be connected to each power pin of the IC as the following diagram. The power of analog parts should be connected from power source with high quality.



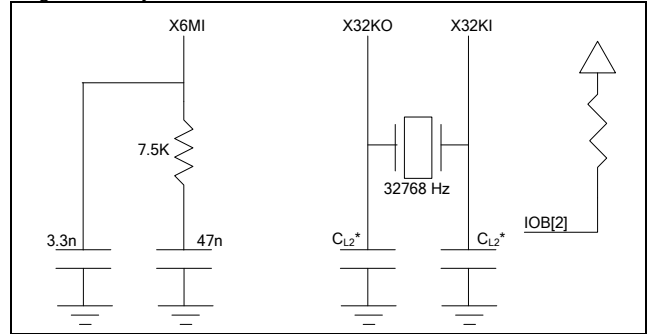
7.2. Crystal and PLL

When the 32768Hz crystal is disabled, usually for TV and USB applications, please refer to the following diagram for the crystal circuit scheme.



Note*: Please refer to the crystal's application circuit.

When the 6MHz crystal is disabled, please refer to the following diagram for crystal circuit scheme.

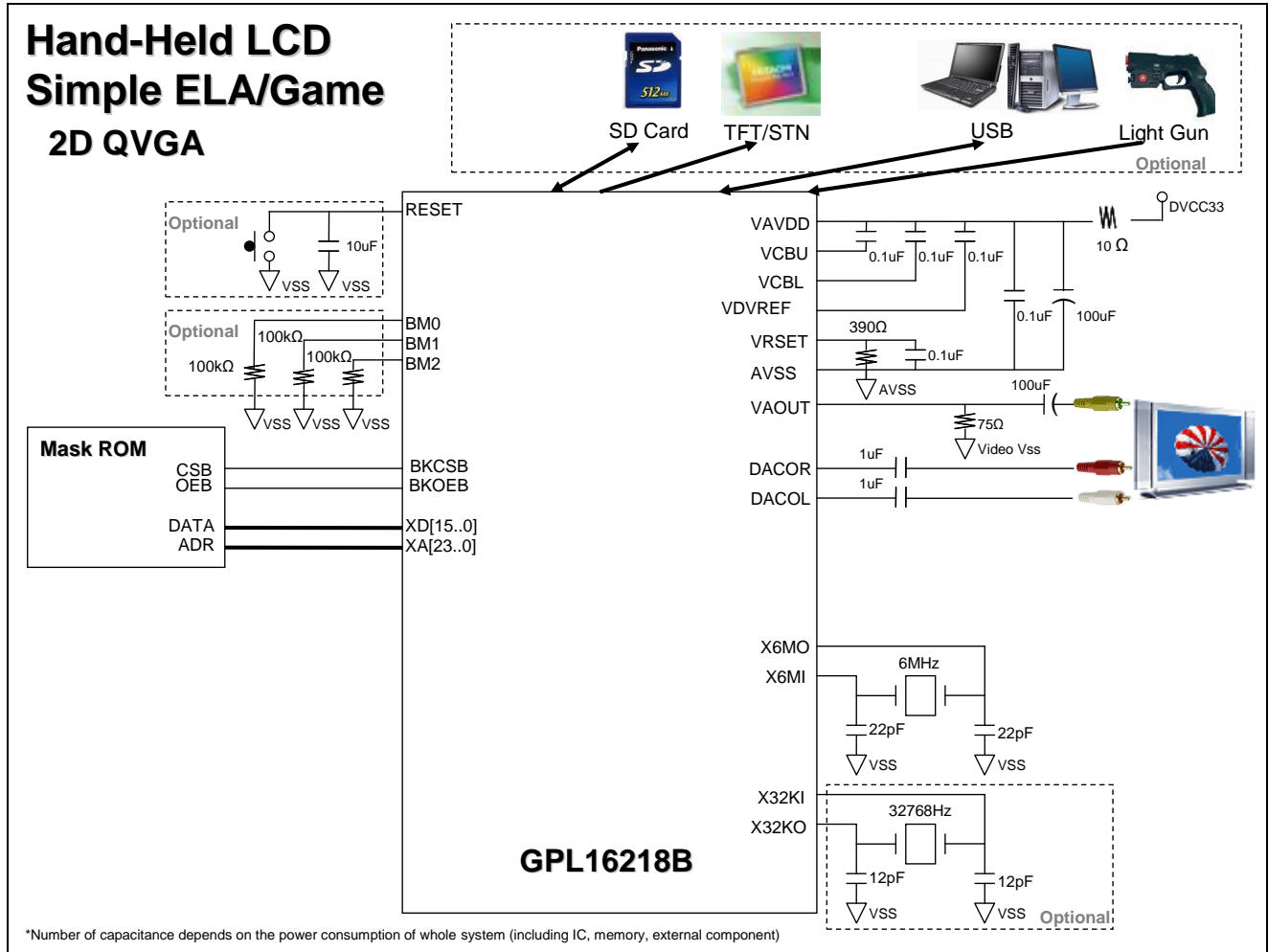


7.3. Analog Section

A specific AGND ground plane, connected via a signal trace to GND ground, should be provided. No digital signal should cross the AGND plane. DAVREF should be connected to a 1μF capacitor and VDVREF should be connected to a 0.1μF capacitor.

8. Application Circuit

8.1. For TV Plug-and-Play Simple ELA/Game 2D Application



9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPL16218B - NnnV - C	Chip Form
GPL16218B - NnnV - QL09x	Halogen Free Package

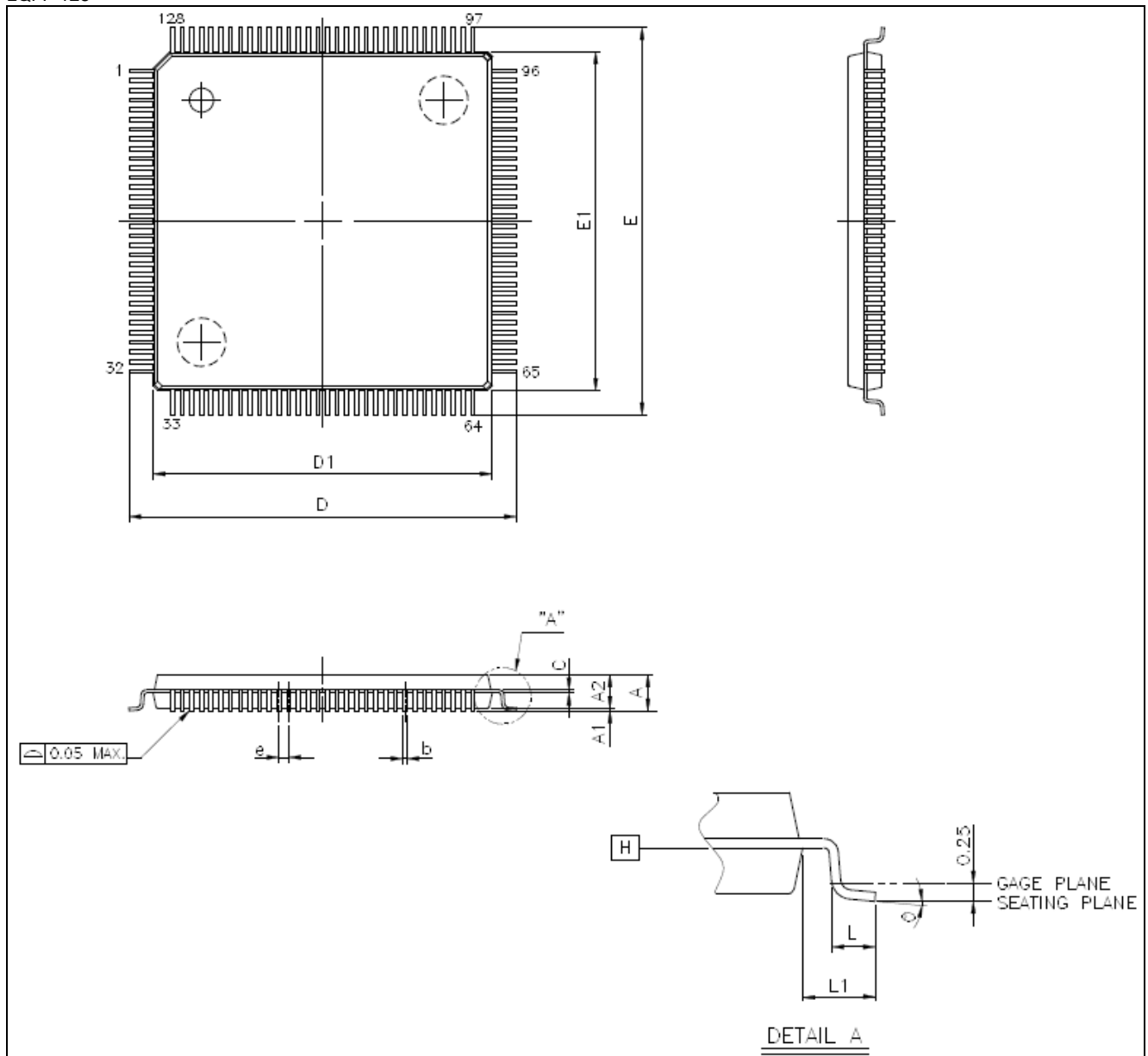
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

9.2. Package Information

LQFP 128



Symbol	Millimeter		
	Min.	Nom.	Max.
A	--	--	1.60

Symbol	Millimeter		
	Min.	Nom.	Max.
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
C	0.09	--	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

10. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Generalplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. GENERALPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, GENERALPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. GENERALPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by GENERALPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

11. REVISION HISTORY

Date	Revision #	Description	Page
Nov. 21, 2016	1.0	Add ICEDA, ICECK pin description in 4.SIGNAL DESCRIPTION.	5
Nov. 19, 2008	0.4	1. Modify pin descriptions.	5
		2. Modify pad assignment.	9
Jul. 01, 2008	0.3	1. Modify test pin descriptions.	5
		2. Modify package number.	5-8
Jun. 03, 2008	0.2	1. Modify operating current and power down current.	12
		2. Modify application circuit.	16
May. 05, 2008	0.1	Preliminary version.	19