DATA SHEET

GPL16258VB

Advanced Virtual 3D Game / ELA SoC with *μ'nSP*® 2.0

Nov. 24, 2016

Version 1.0

Table of Contents

PAGE

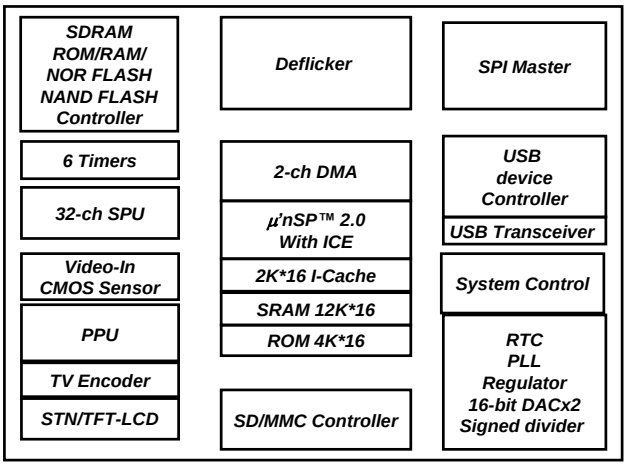
Advanced Virtual 3D Game / ELA SoC with μ'nSP® 2.0

1. GENERAL DESCRIPTION

The Generalplus GPL16258VB is highly integrated system-on-a chip and targets a cost-effective, high performance micro-controller solution for game, education and learning applications. It embedded μ'nSP® 2.0 (16-bit CPU developed by Sunplus Technology) with 4KB I-cache, picture process unit (PPU), TV encoder with QVGA or VGA output, 32-channel sound process unit (SPU), SDRAM controller, ROM/SRAM/NOR FLASH/NAND FLASH with ECC Memory controller, two channel DMA controller, six-channel 16-bit timers, SD/MMC memory interface, USB device, mono STN-LCD and TFT-LCD interface, interrupt controller, SPI master controller, programmable I/O ports, 16-bit DAC for audio playback, PLL, de-flicker, divider and embedded 12K*16-bit SRAM and 4K*16 ROM.

By providing a complete set of common system peripherals, the GPL16258VB minimizes overall system costs and eliminates the need to configure additional components. The GPL16258VB provides not only the high-speed performance and low cost for a system, but it also integrates several powerful tools into the development system, such as development system with C language, assembly compiler, linker, source debugger functions and project management tools.

2. BLOCK DIAGRAM



3. FEATURES

- μ'nSP® 2.0 16-bit CPU with frequency up to 96MHz.
- 4K bytes I-cache.
- 12k*16-bit SRAM for programming or LCD frame buffers.
- 4K*16- bit ROM for boot code.
- Picture Process Unit (PPU)
  - 4 Text layers + 256 Sprites + 4096 Extended Sprites
  - Virtual 3D Effect for text and sprite
  - QVGA/VGA output
  - Line base or Frame base operation
  - De-flicker for TV output
  - Up-to 4096 x 4096 Text Size
  - Alpha-channel sprite
- Sound Process Unit (SPU)
  - 32 hardware PCM/ADPCM channels
  - Built-in sound compressor
- Video-in/CMOS sensor interface supports CCIR601/CCIR656 standard.
- 96 MHz SDRAM with maximum size 64M bytes for single chip selection.
- Static memory controller. (ROM/SRAM/NOR FLASH/Page Memory/NAND FLASH with ECC)
- Two-channel DMA controller.
- Mono and 16-gray STN-LCD controller.
- TFT-LCD controller which can be UPS051 (serial RGB), UPS052 (serial RGB dummy), parallel RGB, i80 (8-bit/16-bit system bus) I/F type, and CCIR601/CCIR656.
- 29 sources Interrupt Controller.
- Universal Serial Bus (USB) 2.0 full speed compliant device with built-in transceiver.
- Watchdog timer.
- 32-bit by 32-bit signed divider
- Real-time clock.
- Six 16-bit timers.
- SD/MMC memory interface.
- SPI master interface.
- 51 Programmable general I/O ports with pull-high/low control.
- Power manager.
- Built-in 3.0V to 1.8V Regulator.
- Low voltage reset.
- 96MHz, 27MHz and 12MHz PLL.
- 16-bit stereo DAC (2ch) for audio playback.
- TV encoder: supports NTSC/PAL output.

4. SIGNAL DESCRIPTIONS

Left Side

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
1	2	DVSS	Digital GND	P	Digital ground	
2	3	BKCSB0	Memory I/F	I/O	External memory chip select 0	IOD0
3	4	XA3	Memory I/F	I/O	External memory address pin 3	
4	5	XA2	Memory I/F	I/O	External memory address pin 2	
5	6	XA1	Memory I/F	I/O	External memory address pin 1	
6	7	BKCSB1	Memory I/F	I/O	External memory chip select 1	IOD1
7	8	XA0	Memory I/F	I/O	External memory address pin 0	
8	9	XA10	Memory I/F	I/O	External memory address pin 10	
9	10	XA11	Memory I/F	I/O	External memory address pin 11	
10	11	BKCSB2	Memory I/F	I/O	External memory chip select 2	IOD2
11	12	XA12	Memory I/F	I/O	External memory address pin 12	
12	13	XA13	Memory I/F	I/O	External memory address pin 13	
13	14	XA14	Memory I/F	I/O	External memory address pin 14	
14	15	DVCC33	Digital PWR	P	3.3V digital power	
15	16	DVSS	Digital GND	P	Digital ground	
16	17	DVCC18	Digital PWR	P	1.8V digital power	
17	18	BKWEB	Memory I/F	I/O	External memory write enable pin	
18	19	BKOEB	Memory I/F	I/O	External memory output enable pin	
19	20	XA15	Memory I/F	I/O	External memory address pin 15	IOD7
20	21	XA16	Memory I/F	I/O	External memory address pin 16	IOD8
21	22	XA17	Memory I/F	I/O	External memory address pin 17	IOD9
22	23	XA18	Memory I/F	I/O	External memory address pin 18	IOD10
23	24	XA19	Memory I/F	I/O	External memory address pin 19	IOD11
24	25	XA20	Memory I/F	I/O	External memory address pin 20	IOD12
25	26	XA21	Memory I/F	I/O	External memory address pin 21	IOD13
26	27	XA22	Memory I/F	I/O	External memory address pin 22	IOD14
27	28	XA23	Memory I/F	I/O	External memory address pin 23	IOD15
28	29	DVSS	Digital GND	P	Digital ground	
29	30	TEST	MODE	I	Test mode control signal. Input floating; it must be tied with ground under normal operation.	

Bottom Side

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
30	31	RESETB	SYSTEM	I/O	Reset input pin. (Low active)	
31	32	IOB2	MODE	I/O	BM2: Boot mode selection pin 2. (0: use 6MHz crystal, usually for TV application, 1: use internal PLL, usually for other application w/o TV)	IOB2
32	33	IOB1	MODE	I/O	BM1: Boot mode selection pin 1. 1: Internal ROM Boot (SPI boot, NAND boot) 0: Chip Select 0 Memory Boot	IOB1
33	34	IOB0	MODE	I/O	BM0: Boot mode selection pin 0. (This pin must be pull low with a resistor)	IOB0
34	35	ICEDA	ICE	I/O	Embedded ICE data pin. Default is floating. In development phase, connect it with a capacitor to GND. In production phase, connect it with a resistor to GND.	
35	36	ICECK	ICE	O	Embedded ICE clock pin. Default is floating. In development phase, connect it with a capacitor to GND. In production phase, connect it with a resistor to GND.	
36	37	IOA7	LCD	I/O	TFT-LCD's D7	IOA7
37	38	IOA6	LCD	I/O	TFT-LCD's D6	IOA6
38	39	IOA5	LCD	I/O	TFT-LCD's D5	IOA5
39	40	IOA4	LCD	I/O	TFT-LCD's D4	IOA4
40	41	IOA3	LCD	I/O	TFT-LCD's D3	IOA3
41	42	IOA2	LCD	I/O	TFT-LCD's D2	IOA2
42	43	IOA1	LCD	I/O	TFT-LCD's D1	IOA1
43	44	IOA0	LCD	I/O	TFT-LCD's D0	IOA0
44	45	IOA8	LCD	I/O	TFT-LCD's D8	IOA8
45	46	DVCC33	Digital PWR	PWR	3.3V digital power	
46	47	DVSS	Digital GND	PWR	Digital ground	
47	48	DVCC18	Digital PWR	PWR	1.8V digital power	
48	49	IOA9	LCD	I/O	TFT-LCD's D9	IOA9
49	50	IOA10	LCD	I/O	TFT-LCD's D10	IOA10
50	51	IOA11	LCD	I/O	TFT-LCD's D11	IOA11
51	52	IOA12	LCD	I/O	TFT-LCD's D12	IOA12
52	53	IOA13	LCD	I/O	TFT-LCD's D13	IOA13
53	54	IOA14	LCD	I/O	TFT-LCD's D14	IOA14
54	55	IOA15	LCD	I/O	TFT-LCD's D15	IOA15
55	56	IOC8	SD2	I/O	SD2 data0	IOC8
56	57	IOC7	SD2	I/O	SD2 clock	IOC7
57	58	IOC6	SD2	I/O	SD2 command	IOC6
58	59	IOC10	SD2	I/O	SD2 data2	IOC10
59	60	IOC9	SD2	I/O	SD2 data1	IOC9
60	61	IOC5	SD2	I/O	SD2 data3	IOC5
61	62	IOC11	Key change A	I/O	Key change A input	IOC11
62	63	IOC12	Key change B	I/O	Key change B input	IOC12
63	64	PLLV33	PLL	PWR	3.3V PLL power	
64	65	X32KO	PLL	O	32768 Hz crystal output pin	

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
65	66	X32KI	PLL	I	32768 Hz crystal input pin	

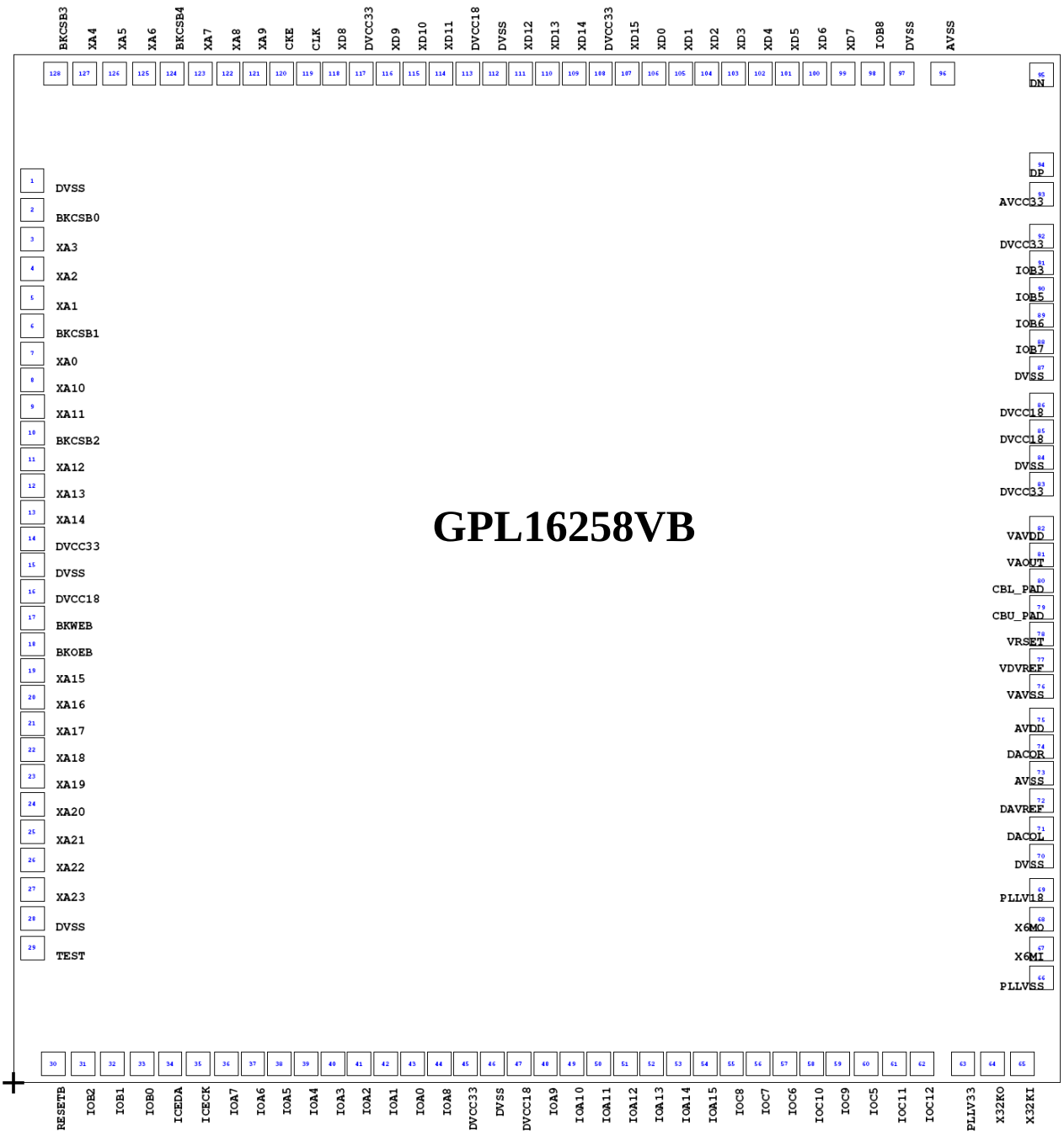
Right Side

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
66	67	PLLVSS	PLL	PWR	PLL ground	
67	68	X6MI	PLL	A/I	6MHz crystal input pin or 12M PLL filter pin	
68	69	X6MO	PLL	O	6MHz crystal output pin	
69	70	PLLV18	PLL	P	1.8V power for PLL	
70	71	DVSS	Digital GND	PWR	Digital ground	
71	72	DACOL	DAC	A/O	Left channel audio output	
72	73	DAVREF	DAC	A/O	DAC reference voltage pin	
73	74	AVSS	DAC	PWR	DAC ground	
74	75	DACOR	DAC	A/O	Right channel audio output	
75	76	AVDD	DAC	PWR	3.3V DAC power	
76	77	VAVSS	VDAC	PWR	VDAC ground	
77	78	VDVREF	VDAC	A/I	Video DAC reference voltage	IOE2
78	79	VRSET	VDAC	A/I	Video DAC current source adjustment	IOE1
79	80	VCBU	VDAC	A/I	Video DAC reference voltage	
80	81	VCBL	VDAC	A/I	Video DAC reference voltage	
81	82	VAOUT	VDAC	A/O	Video DAC output	IOE0
82	83	VAVDD	VDAC	PWR	3.3V VDAC power	
83	84	DVCC33	Regulator	PWR	3.3V Regulator power	
84	85	DVSS	Regulator	PWR	Regulator ground	
85	86	DVCC18	Regulator	A/O	Regulator 1.8V output	
86	87	DVCC18	Digital PWR	PWR	1.8V digital power	
87	88	DVSS	Digital GND	PWR	Digital ground	
88	89	IOB7	SPI	I/O	SPIRX: SPI data input	IOB7
89	90	IOB6	SPI	I/O	SPITXD: SPI data output	IOB6
90	91	IOB5	SPI	I/O	SPICLK: SPI clock	IOB5
91	92	IOB3	LCD	I/O	TFT DCLK	IOB3
92	93	DVCC33	Digital PWR	PWR	3.3V digital power	
93	94	AVCC33	USB	PWR	3.3V USB power	
94	95	DP	USB	I/O	DP pin of USB PHY	
95	96	DN	USB	I/O	DN pin of USB PHY	

Top Side

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
96	97	AVSS	USB	PWR	USB ground	
97	98	DVSS	Digital GND	PWR	Digital ground	
98	99	IOB8	EINT	I/O	External INT0; Light gun input	IOB8
99	100	XD7	Memory I/F	I/O	External memory data pin 7	
100	101	XD6	Memory I/F	I/O	External memory data pin 6	
101	102	XD5	Memory I/F	I/O	External memory data pin 5	
102	103	XD4	Memory I/F	I/O	External memory data pin 4	
103	104	XD3	Memory I/F	I/O	External memory data pin 3	
104	105	XD2	Memory I/F	I/O	External memory data pin 2	
105	106	XD1	Memory I/F	I/O	External memory data pin 1	
106	107	XD0	Memory I/F	I/O	External memory data pin 0	
107	108	XD15	Memory I/F	I/O	External memory data pin 15	
108	109	DVCC33	Digital PWR	PWR	3.3V digital power	
109	110	XD14	Memory I/F	I/O	External memory data pin 14	
110	111	XD13	Memory I/F	I/O	External memory data pin 13	
111	112	XD12	Memory I/F	I/O	External memory data pin 12	
112	113	DVSS	Digital GND	PWR	Digital ground	
113	114	DVCC18	Digital PWR	PWR	1.8V digital power	
114	115	XD11	Memory I/F	I/O	External memory data pin 11	
115	116	XD10	Memory I/F	I/O	External memory data pin 10	
116	117	XD9	Memory I/F	I/O	External memory data pin 9	
117	118	DVCC33	Digital PWR	PWR	3.3V digital power	
118	119	XD8	Memory I/F	I/O	External memory data pin 8	
119	120	CLK	SDRAM	I/O	SDRAM clock	IOC0
120	121	CKE	SDRAM	I/O	SDRAM clock enable	IOC1
121	122	XA9	Memory I/F	I/O	External memory address pin 9	
122	123	XA8	Memory I/F	I/O	External memory address pin 8	
123	124	XA7	Memory I/F	I/O	External memory address pin 7	
124	125	BKCSB4	Memory I/F	I/O	External memory chip select 4	IOD4
125	126	XA6	Memory I/F	I/O	External memory address pin 6	
126	127	XA5	Memory I/F	I/O	External memory address pin 5	
127	128	XA4	Memory I/F	I/O	External memory address pin 4	
128	1	BKCSB3	Memory I/F	I/O	External memory chip select 3	IOD3

4.1. PAD Assignment



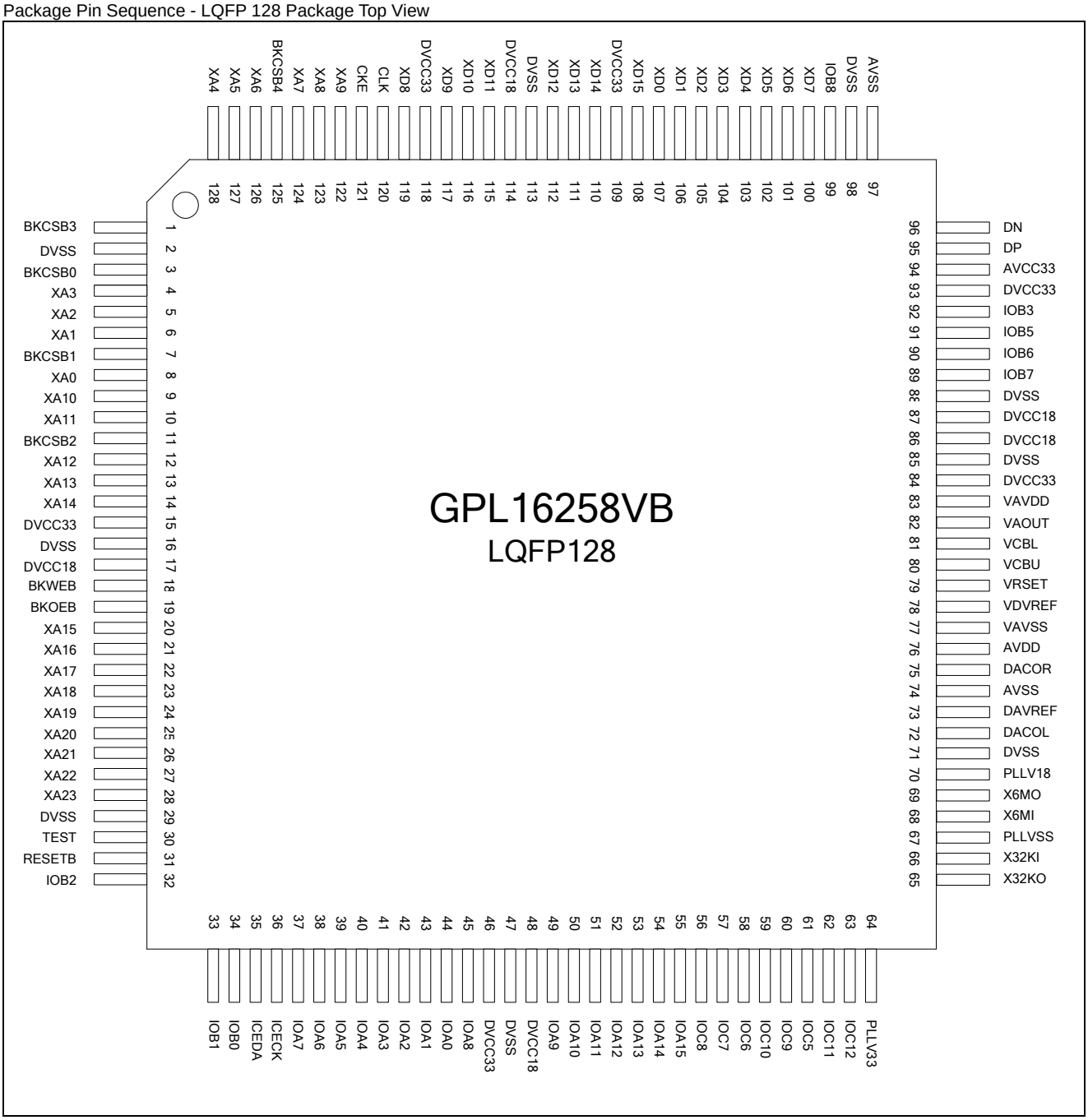
This IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

4.2. Pin Map

Package Pin Sequence - LQFP 128 Package Top View



5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The GPL16258VB is equipped with a 16-bit *μ'nSP*™ 2.0, the newest 16-bit microprocessor by SUNPLUS and pronounced as *micro-n-SP*. Sixteen registers are involved in *μ'nSP*™ 2.0: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP), SR (Segment Register) and R8 - R15 (General-purpose register). The interrupt include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK. GPL16258VB is also built-in a 4K bytes I-cache which can increase the performance significantly.

5.2. Memory

5.2.1. Internal SRAM

The amount of SRAM is 12K-word (including Stack), ranged from 0x0000 through 0x2FFF with access speed of one CPU clock. Since this SRAM is located in CPU's locale bus, the system bus will not be occupied when this SRAM is accessed by CPU. This SRAM can be access freely by CPU/PPU/DMA /LCD.

5.2.2. External memory

The memory space is separated into 5 banks and each bank can be up to 256 pages with 64K words per page. It supports up to 80M words NOR type flash memories. Each bank can be programmed as SDRAM/ROM/SRAM/NOR Flash/NAND Flash. GPL16258VB can support up-to 64M bytes (512Mb) SDRAM with single chip selection. 8-bit NAND flash is supported with an embedded 1/4/8 bits ECC calculation circuit which recognizes the error correction mechanism on SLC/MLC NAND flash.

5.3. PLL, Clock, Power Mode

5.3.1. PLL (Phase Lock Loop)

There are three PLLs embedded in GPL16258VB. 1st PLL can pump up to 96MHz, 2nd PLL can generate 27MHz, and 3rd PLL can pump 12MHz. The output frequency of fast PLL is programmable and has range from 15MHz ~ 96MHz (3MHz per step).

5.3.2. System clock

The system clock can be selected from 32768 or 12M or 96M (determined by fast PLL's output frequency) by register setting. Furthermore, a clock divider which can divide clock up to 1/128 is provided to reduce the power consumption.

5.4. Power Savings Mode

The GPL16258VB provide 4 power modes, Normal, Wait, Halt and Sleep.

Mode	CPU	System	RTC	POWEREN	After wakeup
Normal	ON	ON	ON	ON	-
Wait	OFF	ON	ON	ON	Next Instruction
Halt	OFF	OFF	ON	OFF	Reset CPU
Halt2	OFF	OFF	ON	OFF	Next Instruction
Sleep	OFF	OFF	OFF	OFF	Reset System

Enter the Wait/Halt/Halt2/Sleep mode, is done by write designated value to designated port. The wake-up source can be interrupt or timer or key-change.

5.5. Picture Process Unit

GPL16258VB equips a powerful process engine which has the following features.

Item	Features
Text Layer	1. Maximum 4 text layers at the same time. 2. Supports text size up to 4096x4096. 3. Supports virtual 3D effect. 4. Supports Text rotate and scale effect. 5. Supports horizontal/vertical compression effect. 6. Supports horizontal movement effect. 7. Supports 64-level alpha blending. 8. Supports vertical compression under 2.5D mode.
Sprite	1. Maximum 256 sprites at the same time. 2. Maximum 4096 extended sprite at the same time. 3. Each sprite supports virtual 3D texture mapping 4. Each sprite support 64-level rotate function. 5. Each sprite supports 64-level zoom in/out function from 1/32 to 8.75 times. 6. Each sprite supports 64-level alpha blending. 7. Each sprite supports 3 kinds of mosaic effect. 8. Supports alpha channel function. 9. All above function can combine at the same time.
Color	1. Text layer and sprites support 4/16/64/256-color palette and RGB1555/ RGB565/ YUYV/ RGBG bitmap mode. 2. 1024 palette entry for text layers and sprites. 3. Supports 16/24-bit level of palette index color.
Operation Mode	1. Supports QVGA at line/frame base mode. 2. Supports VGA at line/frame base mode.
Other Features	1. Supports light gun interface. 2. Supports sprite DMA function. 3. Supports de-flicker for TV output.

5.6. Video Input Interface

GPL16258VB supports video input from sensor or TV decoder. The maximum input resolution is 4095 x 4095. A built-in scalar can be used to scale input data from arbitrary resolution to VGA or QVGA mode. A motion detecting engine is also built-in GPL16258VB to recognize the interactive game with sensor input. The video-in interface supports CCIR601/CCIR656 format with YUV or RGB format. The output format is frame-based and the input frame rate does not need to synchronize with GPL16258VB's system clock.

5.7. Sound Process Unit

GPL16258VB equips a 32-channel SPU. Each channel of SPU can support PCM8/ PCM16/ ADPCM36. A dynamic volume compressor is also embedded to enlarge the overall volume. For software application, GPL16258VB is also capable of the wide-band (sample rate >= 16KHz) low bit rate algorithm.

5.8. Video Output Interface

5.8.1. STN-LCD Interface

The STN-LCD driver interface built-in GPL16258VB supports up-to 320X240 LCD panel and supports 1/4 bits data bus for monochrome/gray-scale STN. Memory interface type CSTN is also supported.

5.8.2. TFT-LCD Interface

The GPL16258VB supports TFT-LCD controller. The LCM interface including parallel RGB (5-6-5), serial delta RGB, serial stripe RGB, CPU (MPU) type, and CCIR601/CCIR656. The horizontal resolution of TFT controller maximum reaches 640 pixels, and the vertical resolution of TFT controller maximum reaches 480 pixels. The TFT controller mainly provides four timing control pins and 8 or 16 data pins to control external TFT panel. Those are VSYNC, HSYNC, DE, DCLK, and DATA.

5.8.3. TV encoder

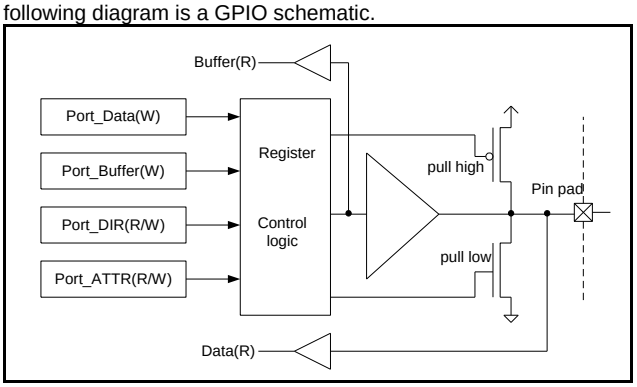
The GPL16258VB supports TV composite output. Both NTSC and PAL output are supported. The output resolution can up-to 640x480. A 10-bit video DAC is also embedded in GPL16258VB which can utilize minimum system cost and best performance.

5.9. Interrupt

The GPL16258VB has 29 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources. Some of the interrupt source can be programmed as FIQ or IRQ by register setting.

5.10. GPIO

Five I/O ports are built in GPL16258VB, IOA, IOB, IOC, IOD and IOE. Each I/O pin has its normal function and is described in the signal description section. When the normal function of the I/O is disabled, it will switch to GPIO function automatically. The following diagram is a GPIO schematic.



5.11. Timer / Counter

The GPL16258VB provides six 16-bit timers/counters, TimerA to TimerF. The clock source of each timer can be set individually. For Timer A to TimerD, an INT will be sent to CPU when timer overflows. Besides, Capture, Comparison and PWM functions are also provided by TimerA/TimerB/TimerC.

Clock Source A	Clock Source B
Fosc/2	2048Hz
Fosc/256	1024Hz
32768Hz	256Hz
8192Hz	Time Base B
4096Hz	Time Base A
1	0
Another Timer	1
INT1	INT2

The GPL16258VB is embedded with a time base controller which is used to generate the slow and precisely interrupt form 32768Hz crystal. The following table shows the available time base.

TimeBase A	TimeBase B	TimeBase C
--	8Hz	128Hz
1Hz	16Hz	256Hz
2Hz	32Hz	512Hz
4Hz	64Hz	1024Hz

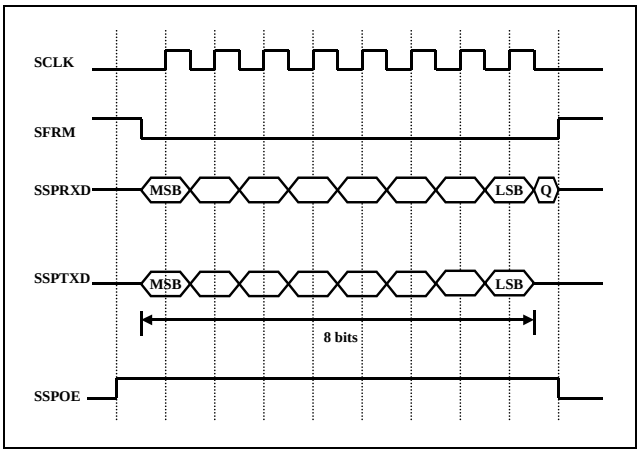
5.12. Watchdog

The purpose of watchdog is to monitor if the system operates normally. Within a specific period, watchdog must be cleared. If not, CPU assumes that the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again. In GPL16258VB, the clear period is software programmable. If watchdog is cleared before expiration, the system will not be reset.

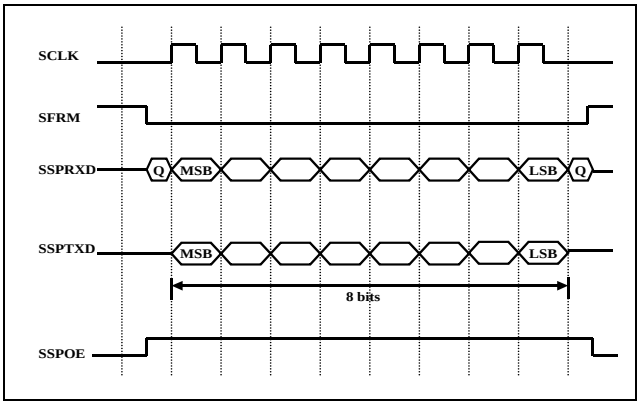
5.13. Serial Interface

5.13.1. Serial Peripheral Interface (SPI)

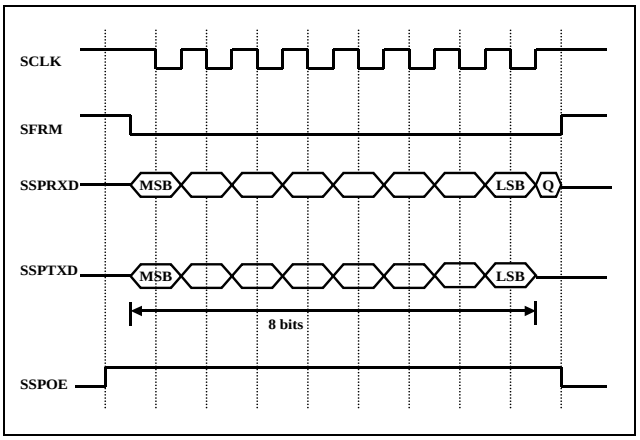
The SPI interface is a master interface that enables synchronous serial communication with slave/master peripherals. Two 8-byte FIFOs are used for transmitting and receiving data. Four types of timing are supported and shown in the following diagram.



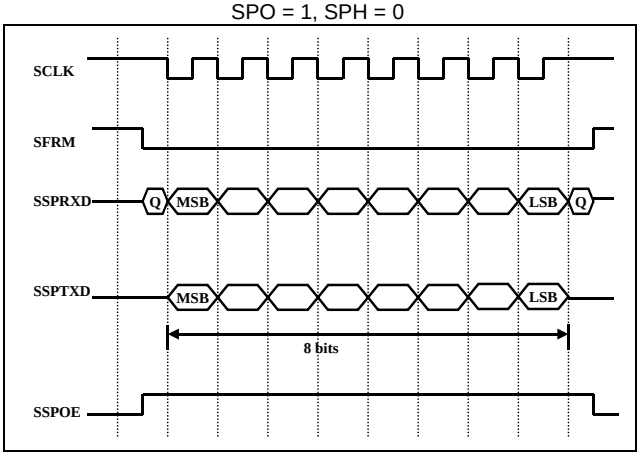
SPO = 0, SPH = 0



SPO = 0, SPH = 1



SPO = 1, SPH = 0



SPO = 1, SPH = 1

5.13.2. USB Device Function

GPL16258VB provides USB device function which is compatible with USB 1.1 and USB 2.0 full speed standard. An USB transceiver is built-in for devices function. A FIFO with size of 128x8 is used for bulk-in and bulk-out transfer and an 8-byte FIFO is used for pipe transferring control. Interrupt IN/OUT pipes are also supported. The DMA transferring is enabled for bulk-in/out to maximize the transfer performance.

5.14. IDE Tools Function

The functions of IDE include the follows:

1). C compiler, Assembly and Linker
2). Single step trace
3). Break point (break point for debugging)
4). Run (execute)

5.15. SD/MMC Controller

GPL16258VB provides SD/MMC controllers which is compatible with MMC system specification version 2.3 and SD Memory Card specification 1.1. The controller supports automatically CRC generation and check, 1-bit and 4-bit transfer, interrupt generation when buffer empty/full, DMA transfer for page read/write.

5.16. Real Time Clock (RTC)

The RTC block provides the alarm function, schedule function, and hour/minute/second/half-second interrupt function.

5.17. Analog Control

5.17.1. DAC control

A 16-bit stereo DAC (2ch) is embedded in GPL16258VB. For both left and right channels, a 16x16 FIFO is used to avoid sound glitch when CPU is busy. The left and right channels do not need to have the same sample rate. A single DMA channel can use the stereo playback.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	DVCC33 PLL_V33	-0.3 to 4.0	V
Supply Voltage 2	AVDD	-0.3 to 4.0	V
Supply Voltage 3	DVCC18 PLL_V18	-0.3 to 2.16	V
Input Voltage	V_{IN}	-0.3 to 4.0	V
Operating Temperature	T_A	0 to 70	℃
Storage Temperature	T_{STG}	-40 to +150	℃

6.2. DC Characteristics

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage 1	DVCC33 PLL_V33	2.7 3.0[1]	3.0	3.6	V	-
Operating Voltage 2	AVDD	2.7	3.0	3.3	V	-
Operating Voltage 3	DVCC18 PLL_V18	1.62	1.8	1.98	V	-
Operating Current	I_{OP}	-	100[2]	-	mA	@96MHz, 3.3V, all clocks on
Power Down Current	I_{PD}	-	80[3]	100[3]	μA	Sleep Mode@1.5V
High Input Voltage	V_{IH}	0.7DVDD33	-	DVDD33	V	-
Low Input Voltage	V_{IL}	VSS	-	0.8	V	-
Crystal Frequency 1	-	-	32768	-	Hz	-
Crystal Frequency 2	$F_{CRYSTAL}$	-	6.0[4]	-	MHz	-
System Clock	F_{SYS}	256Hz[5]	48	96	MHz	-

Note1: When USB function is enabled, the minimum voltage of DVCC33 is 3.0V.

Note2: Operating current depends on software code. In this test case, the following macro is turned on: Video DAC, Audio DAC, 96MHz PLL and 27MHz PLL.

Note3: Regulator is in sleep mode.

Note4: 6M Crystal is needed when USB function or TV function is enabled.

Note5: By setting clock divider and changing system clock to 32768Hz mode.

6.3. Video DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	10	-	Bit	-
INL	-	±1	-	LSB max	-
DNL	-	±0.5	-	LSB max	-
Input Capacitor	-	10	-	pF	-
Voltage Reference Range	1.14	1.235	1.33	V	-
VRSET	0.570	0.617	0.665	V	-
Offset Error	-	0	-	V	-
Gain Error	-	25	-	LSB	-
Glitch Energy	-	50	-	pV	-
Conversion Rate	-	30	-	ns	-

6.4. Audio DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	16	-	Bit	-
Full Scale Output Voltage	-	0.6*VDDDA	-	Vp-p	-
THD+N (f = 1kHz)	-	0.1	-	%	-
Noise at No Signal	-85	90	-	dBv	-
Frequency Response	20	-	19200	Hz	-

6.5. Regulator Characteristics

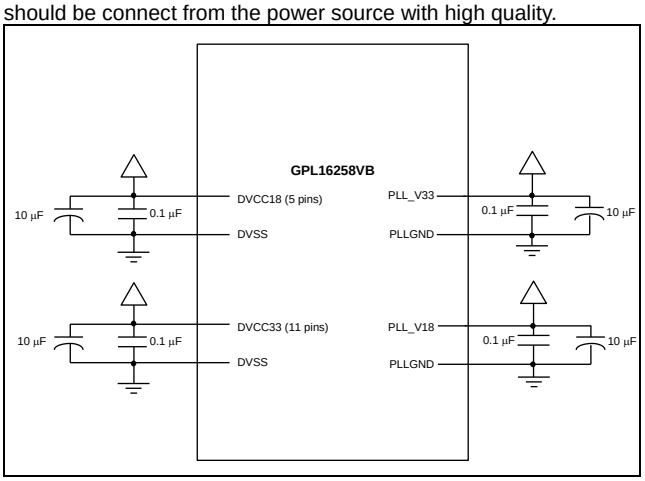
Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.7	3.0	3.6	V
Maximum Current Output	IREGO	-	70	100	mA
Output Voltage	VREGO	1.5[1]	1.8	1.89	V
Standby Current	IREGS	-	10	-	-

Note1: To save more power, it is recommended switching to 1.5V before entering the halt/sleep mode and switching to 1.8V in normal operation mode.

7. RECOMMENDED BOARD LAYOUT

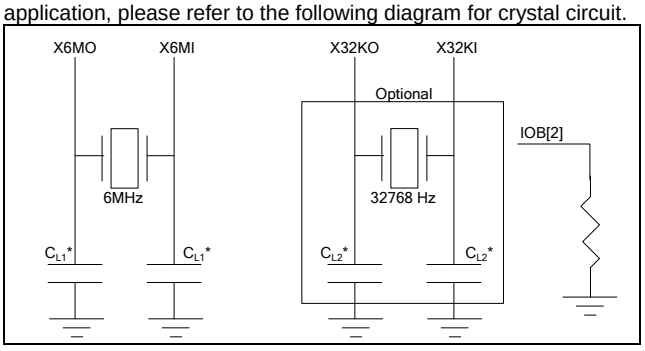
7.1. Power and Ground

All digital power and ground should be connected. The decoupling capacitor of 0.1μF and 10μF should be connected to each power pin of the IC as the following diagram. The power of analog parts should be connect from the power source with high quality.



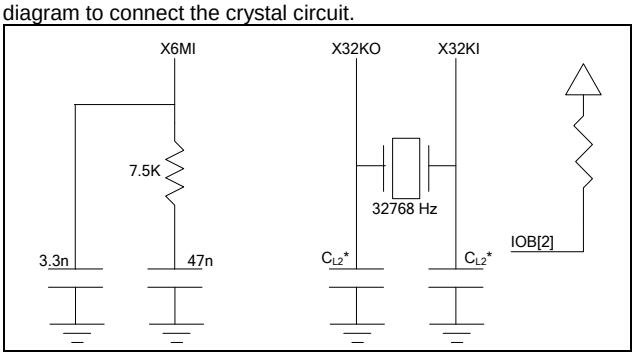
7.2. Crystal and PLL

When the 32768Hz crystal is disabled, usually for TV and USB application, please refer to the following diagram for crystal circuit.



Note*: Please refer to the crystal's application circuit.

When the 6MHz crystal is disabled, please refer to the following diagram to connect the crystal circuit.

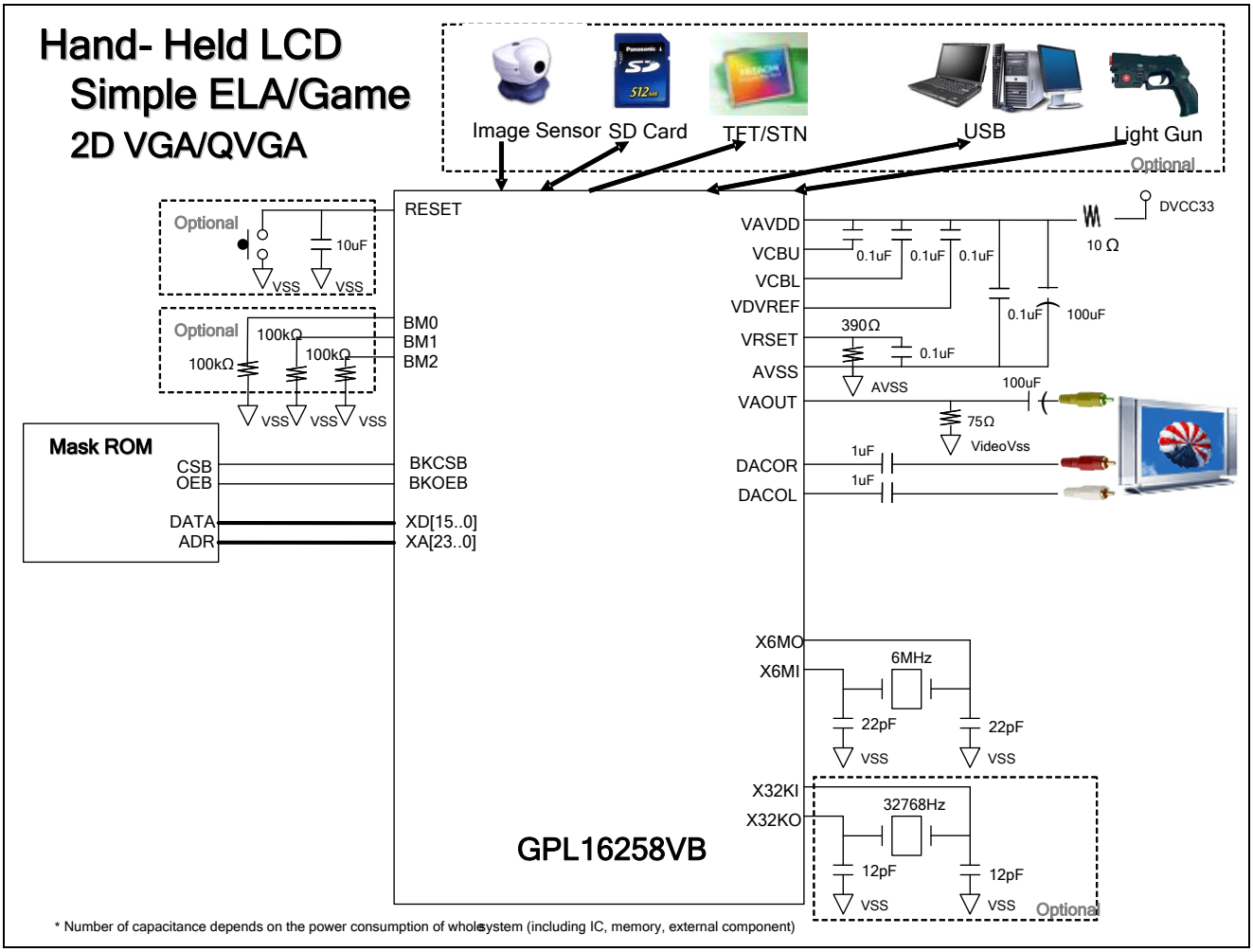


7.3. Analog Section

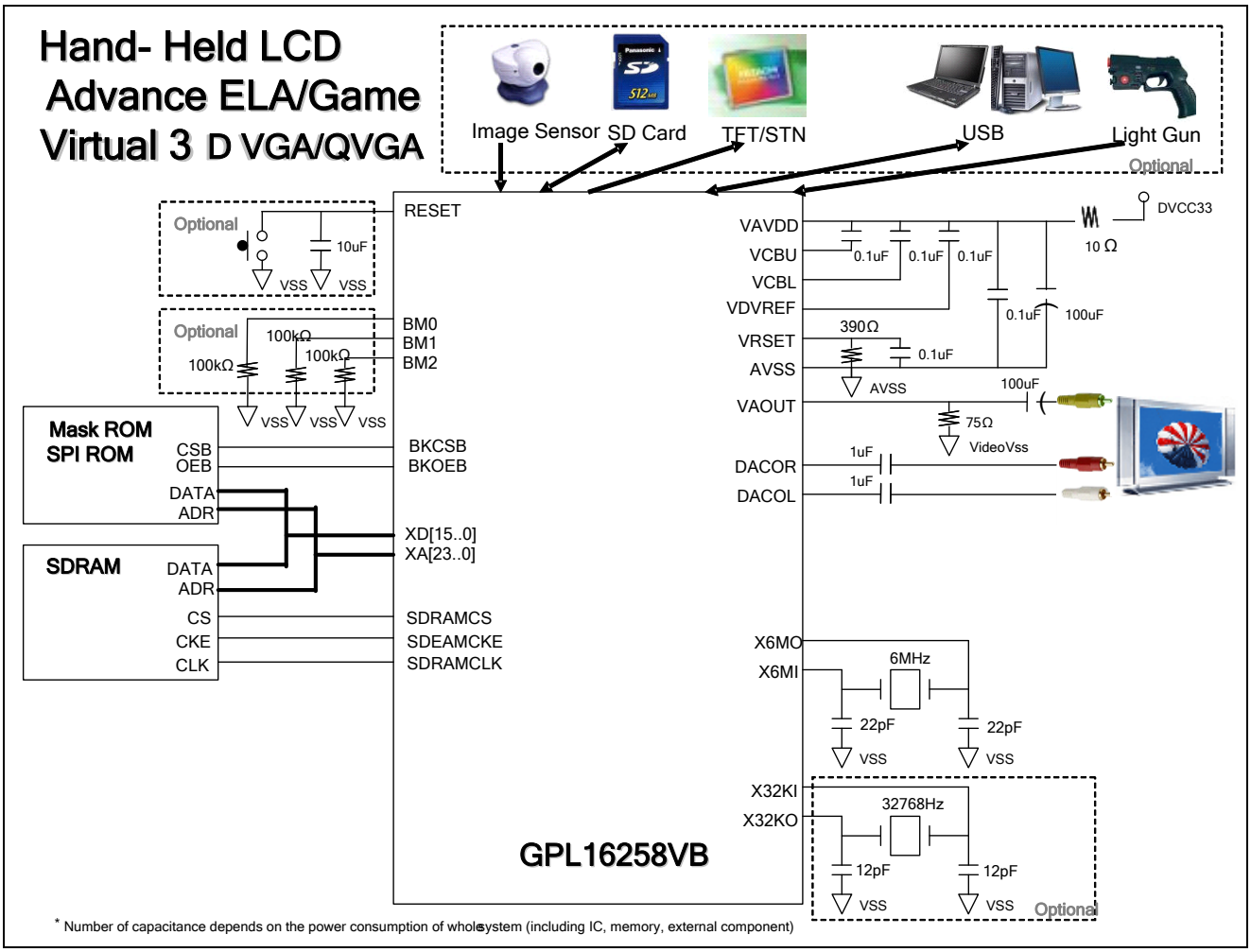
A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. DAVREF should be connected to a 1μF capacitor. VDVREF should be connected to a 0.1μF capacitor.

8. APPLICATION CIRCUIT

8.1. For TV Plug-and-Play Simple ELA/Game 2D Application



8.2. For TV Plug-and-Play Advance ELA/Game Virtual 3D Application



9. ORDERING INFORMATION

9.1. Ordering Information

Product Number	Package Type
GPL16258VB - NnnV - C	Chip Form
GPL16258VB - NnnV - QL09x	Halogen Free Package

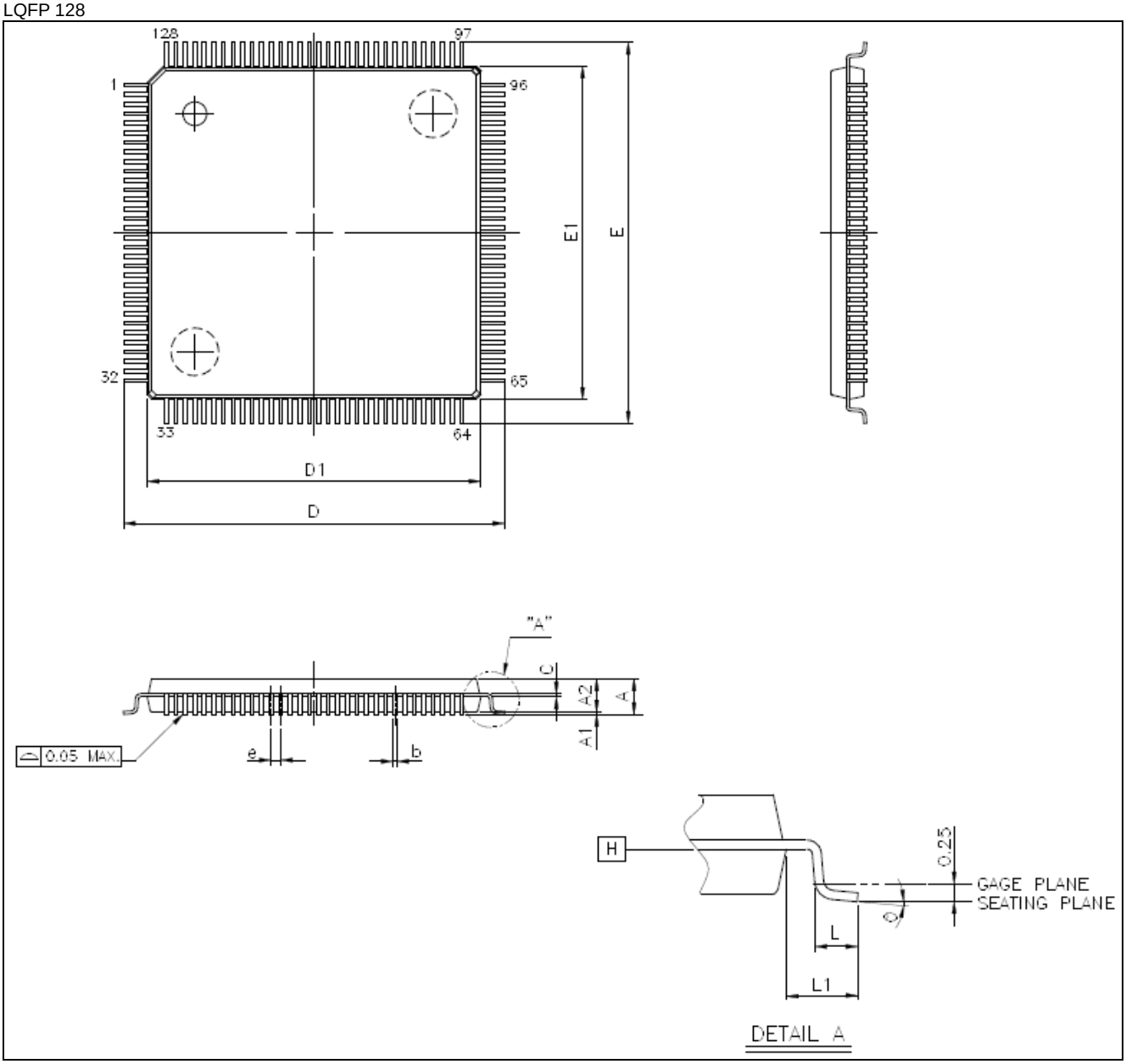
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

9.2. Package Information

LQFP 128



Symbol	Millimeter		
	Min.	Nom.	Max.
A	--	--	1.60

Symbol	Millimeter		
	Min.	Nom.	Max.
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
C	0.09	--	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
Nov. 24, 2016	1.0	Add ICEDA, ICECK pin description in 4.SIGNAL DESCRIPTION.	5
Jun. 30, 2009	0.4	1. Modify IOD2 assignment to BKCSB2.	5
		2. Remove key scan description.	6
		3. Modify TFT resolution to 640x480.	12
Jul. 01, 2008	0.3	1. Modify test pin descriptions.	5
		2. Modify package number.	5-8
Jun. 02, 2008	0.2	1. Modify 4Kx16 ROM descriptions.	3
		2. Modify operating current and power down current.	14
		3. Modify regulator characteristic.	15
		4. Modify application circuit.	16,17
		5. Package information is not available.	18
Mar. 05, 2008	0.1	Preliminary version.	22