DATA SHEET

GPL169256A

16-bit LCD Controller with 2368 Dots Driver

Dec. 19, 2013

Version 1.4

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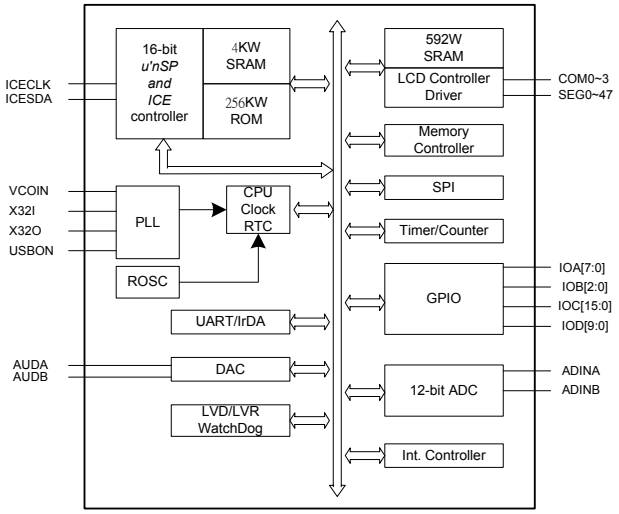
16-BIT LCD CONTROLLER WITH 2368 DOTS DRIVER

1. GENERAL DESCRIPTION

The GPL169256A, a 16-bit architecture LCD controller product, carries the SUNPLUS's newest 16-bit microprocessor, *μ'nSP* (pronounced as *micro-n-SP*) and also has LCD driver built-in. The high processing speed assures the *μ'nSP*™ is capable of handling complex digital signal processes easily and rapidly. The GPL169256A is applicable to digital sound processing application. In addition, Liquid Crystal Display (LCD) capability strengthens the GPL169256A to be used in variety of visual applications. The memory capacity includes 4K-word SRAM for system and 592-word SRAM for LCD frame buffer and 256K-word ROM. The GPL169256A provides single-chip solution with built-in driver to support maximum resolution up to 32x74. Other features include 8 programmable multi-functional I/Os, three 16-bit timers/counters, 32768Hz Real Time Clock, Low Voltage Reset/Detection and many others.

2. BLOCK DIAGRAM



NOTE: PB[2:0] shared with VMIC/ADINA/ADINB; PC[15:0] shared with COM[31:16]; PD[9:0] shared with COM[73:64]

3. FEATURES

- Built-in 16-bit *μ'nSP* 1.3 microprocessor
  - 256K-word ROM
  - 4K-word SRAM
  - 592-word SRAM for LCD frame buffer
  - CPU clock: Max. 48MHz
  - 18 INT sources can be selected as IRQ or FIQ
- Three power saving modes:
  Standby mode/Halt mode/Wait mode
  Max. 5μA @ 3.6V in standby mode
  Max. 30μA @ 3.6V in halt mode(without LCD display)
  Max. 180μA @ 3.6V in halt mode(with mono LCD display)
  Max. 2mA @3.6V in wait mode
- Programmable LCD driver
  - Up to 74 segments, up to 32 commons, maximum 2368 dots
    Unused commons and segments can be set as I/O
  - 1/3~1/7 bias, 1/4, 1/6, 1/8,1/12, 1/16, 1/18, 1/32 duty
  - Adjustable LCD voltage (32 level)
  - 592 words dedicated LCD RAM
  - Selectable black/white or 16-gray display
- Built-in 12-bit ADC with AGC
- Asynchronous serial interface (UART)
- Supports SPI interface
- Three 16-bit timers/counters
- Two-channel 16-bit DAC audio outputs
- Maximum up to 37 general I/Os (8 dedicate I/Os, 29 shared with commons/segments)
- Key wakeup/interrupt function
- PLL feature for system clock
- 32768Hz Real Time Clock (RTC)
- Low voltage reset and low voltage detection
- Watchdog, system bus/address error reset
- Software-based audio processing

4. APPLICATION FIELD

- Advanced educational toys or ELAs
- Handheld LCD game with sound synthesizer

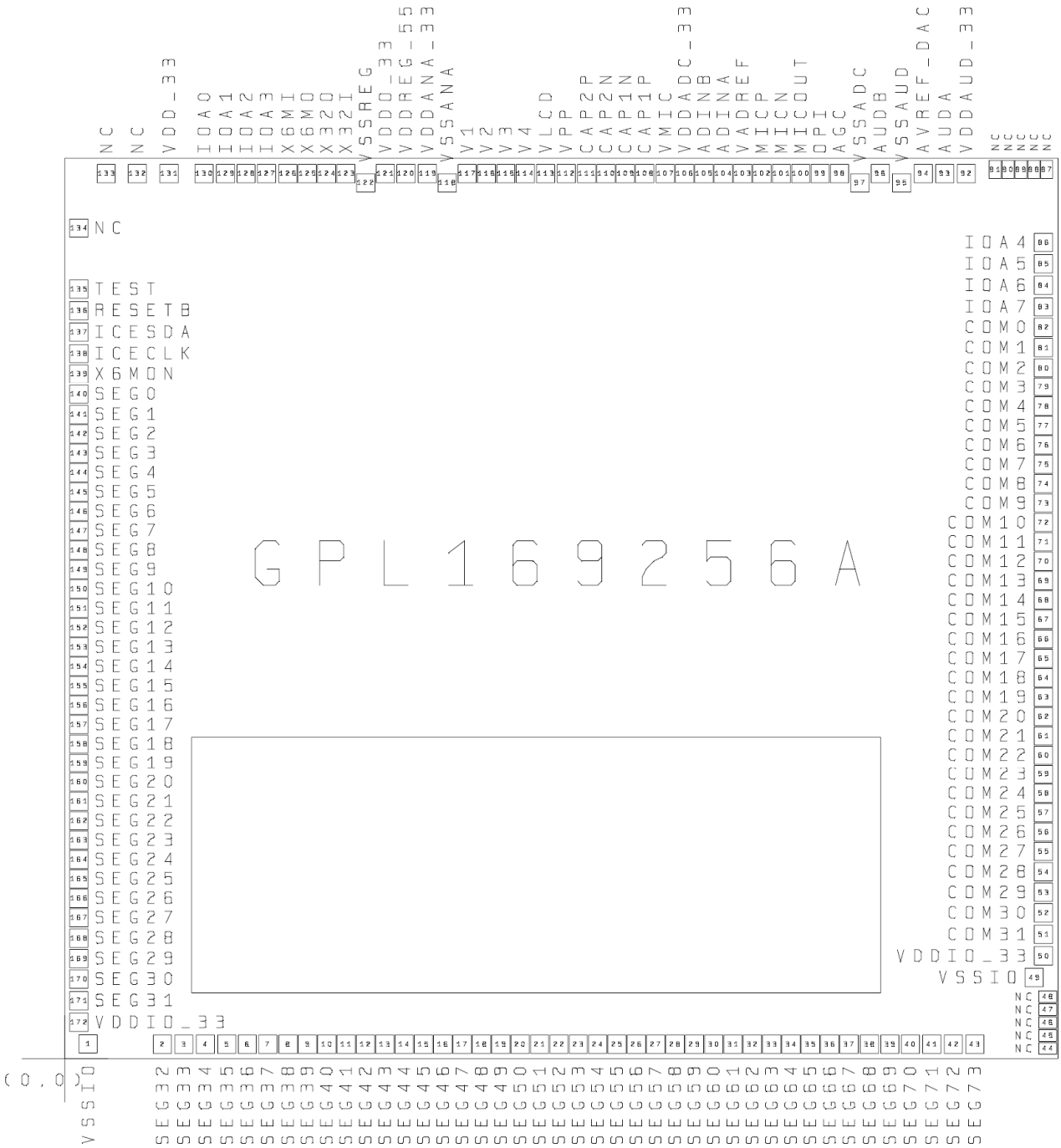
5. SIGNAL DESCRIPTIONS

Mnemonic	Pin No.	Type	Description
SEG[15:0]	155-140	O	LCD driver segment output Can be shared with key scan port
SEG[63:16]	33-2, 171-156	O	LCD driver segment output
SEG[73:64]	43-34	O	LCD driver segment output SEG[73:64] also shared pins with PD[9:0]
COM[31:0]	51-82	O	LCD driver common output COM[31:16] also shared pins with PC[15:0]
IOA[7:0]	83-86, 127-130	I/O	IOA[7:0]: bi-directional I/O ports IOA[7:0] can be software programmed to wakeup I/O pins and key strobe inputs IOA[7] can be selected as Timer clock input or external interrupt input IOA[6] can be selected as Timer input/output of CCP function IOA[5:4] can be selected as UART RX/TX pins IOA[3:1] can be selected as SPI interface signals SCK/SDO/SDI
RESETB	136	I	External reset pin
X6MON	139	I	This pin will control the ON/OFF of the 6MHz crystal and must be connected as VDD or GND.
ICECLK	138	I	ICE clock input pin should be connected to ground if not in development mode.
ICESDA	137	I/O	ICE data pin should be connected to ground if not in development mode.
AUDA	93	O	Audio DAC output
AUDB	96	O	Audio DAC output
X32I	123	I	32768Hz crystal input
X32O	124	O	32768Hz crystal output
TEST	135	I	Test pin
CAP1P, CAP1N	108, 109	P	LCD voltage generation. Charge pump capacitor interconnection pins.
CAP2P, CAP2N	111, 110	P	LCD voltage generation. Charge pump capacitor interconnection pins.
VPP	112	P	LCD voltage generation
VLCD	113	P	VLCD highest voltage
V1	117	P	LCD bias voltage
V2	116	P	LCD bias voltage
V3	115	P	LCD bias voltage
V4	114	P	LCD bias voltage
VDDIO_33	50, 172	P	Power supply voltage input
VSSIO	1, 49	P	Ground reference
VDDANA_33	119	P	Power supply voltage input for analog circuit
VSSANA	118	P	Ground reference for analog circuit
VDDAUD_33	92	P	Power supply voltage input for DAC
VSSAUD	95	P	Ground reference for DAC
VDDREG_55	120	P	Power supply voltage input for core
VSSREG	122	P	Ground reference for core
VDDO_33	121	O	Regulator output voltage for core
AVREF_DAC	94		DAC reference voltage pin
MICP	102	A	Microphone differential input (positive)
MICN	101	A	Microphone differential input (negative)

Mnemonic	Pin No.	Type	Description
VMIC	107	I/O	Output VDDADC when microphone enabled or used as GPIO. VMIC also shared pins with PB[2]
MICOUT	100	A	Microphone 1st amplifier output
OPI	99	A	Microphone 2nd amplifier input
AGC	98	A	AGC control pin
VADREF	103	A	ADC reference pin
ADINA	104	A/I	ADC input ADINA also shared pins with PB[1]
ADINB	105	A/I	ADC input ADINB also shared pins with PB[0]
VDDADC_33	106	P	Power supply voltage input for ADC
VSSADC	97	P	Ground reference for ADC
X6MI	126	I	6MHz crystal input or RC filter connection for PLL
X6MO	125	O	6MHz crystal output
VDD_33	131	P	Power supply voltage input
NC	44-48, 87-91, 132-134		Non-used pin for user

Legend: I = Input, O = Output, P = Power
Total 172pins

5.1. Pad Assignment



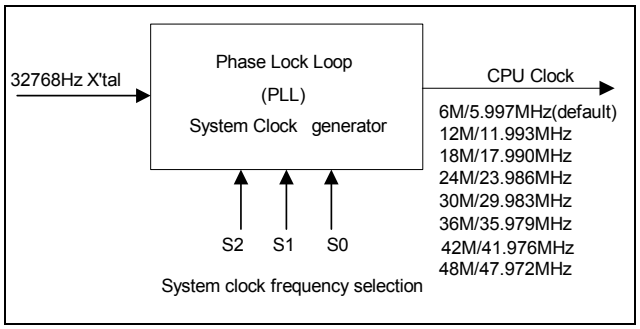
Note1: To ensure IC functions properly, please bond all of VDD and VSS pins.
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The GPL169256A is equipped with a 16-bit *μ'nSP*™, the newest 16-bit microprocessor by SUNPLUS and pronounced as *micro-n-SP*. Eight registers are involved in *μ'nSP*™*:* R1 ~ R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP) and SR (Segment Register). The new version of *μ'nSP*™ 1.3 contains four secondary registers and supports many DSP functions and bit-operation instructions.

The interrupts include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK. Moreover, a high performance hardware multiplier with capability of FIR filter is also built in to reduce software multiplication loading. Besides, nested IRQ is also supported.



6.2. Memory

The GPL169256A contains 4KW SRAM and 592W dual-port SRAM dedicated to support LCD display. The frame buffer is able to support maximum 32x74 16-gray display.

6.3. Regulator

There is a built-in regulator that provides approximate 3V core power from 3-battery power system. The regulator could also be code-optioned to mark-off in 2-battery applications.

6.4. PLL, Clock, Power Mode

6.4.1. PLL (Phase Lock Loop)

There are two PLLs built-in in GPL169256A to provide the system clock. The 6MHz crystal or boost-up from 32768Hz clock could be selected to provide the clock source of fast PLL to generate 48MHz clock. The slow PLL is to generate the 5.997MHz clock from 32768Hz crystal and could be the clock source of the fast PLL.

6.4.1.1. System clock

Basically, the system clock is provided by PLL to determine the system clock frequency. The clock source could be selected either from 6MHz crystal or 32KHz crystal. The default CPU clock is around 6MHz after reset. The CPU clock can be adjusted to desired CPU clock by software.

6.4.1.2. 32768Hz RTC

The RTC, Real Time Clock, is normally used in watch, clock or other time related products. A 2Hz-RTC (0.5 seconds) function is featured in GPL169256A. The RTC is to compute timing and wake CPU up whenever RTC occurs. The timing can be traced by number of RTC occurrences. In addition, GPL169256A supports 32768Hz oscillator in strong mode and auto mode. In strong mode, 32768Hz OSC always runs at the highest power consumption. In auto mode, however, it runs in strong mode for the first 7.5 seconds and switches back to weak mode automatically to save powers.

6.5. Power Saving Mode

The GPL169256A features three power saving modes: WAIT mode, HALT mode, and STANDBY mode.

	Wait	Halt	Standby
CPU	OFF	OFF	OFF
PLL	ON	OFF	OFF
RTC	ON	ON	OFF

6.5.1. Wait mode

In WAIT mode, only CPU is disabled. The PLL and RTC are still active to keep LCD display function. After GPL169256A is awakened from wait mode, CPU will continue to execute the program from previous state.

6.5.2. Halt mode

In HALT mode, both CPU and PLL are OFF and only RTC is keeping active. After GPL169256A is awakened form Halt mode, the CPU will execute the program from reset state.

6.5.3. Standby mode

While in STANDY mode, all modules are OFF to keep at the lowest power consumption. In such mode, RAM and I/Os remain in the previous states till CPU being awakened. The wakeup sources in GPL169256A can be IOA/IOB/IOC/IOD. After GPL169256A is awakened from standby mode, the CPU will execute the program from reset state.

6.6. LCD Controller

The GPL169256A contains a powerful LCD controller, which can support up to 16 gray levels for monochrome STN. With built-in LCD driver function, GPL169256A provides a single-chip solution, which supports maximum resolution up to 32x74 with 16 gray levels.

6.6.1. LCD Voltage Generation

To achieve highly integrated circuit and save external components as possible, the GPL169256A has built-in charge pump circuit and operational amplifiers to generate LCD's bias voltages VLCD, V4, V3, V2 and V1. The charge pump circuit can generate VPP approx. to 8V. With VPP as power source, an operational amplifier is further to provide LCD panel's power supply, VLCD. The level of VLCD can be adjusted by software. It is suggested that VLCD must be higher than VDD by 0.7V, otherwise, abnormal operation will occur.

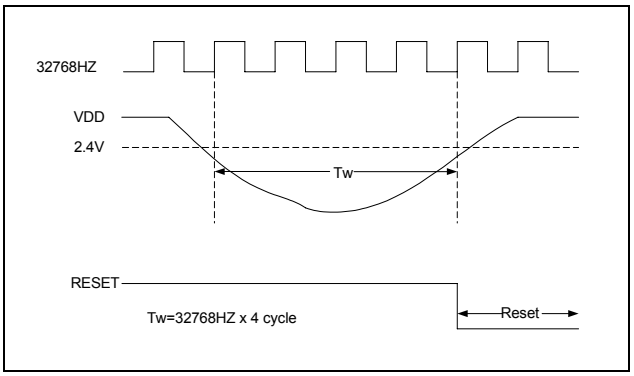
6.7. Low Voltage Detection and Low Voltage Reset

6.7.1. Low Voltage Detection (LVD)

The Low Voltage Detection (LVD) reports the circumstance of present voltage. There are four LVD levels to be selected: 2.2V, 2.4V, 2.6V and 2.8V. Those levels can be programmed via 0x7009 (W). As an example, suppose LVD is given to 2.8V. When the voltage drops below 2.8V, the b15 of 0x7009 is read as HIGH. In such state, program is designed to handle this situation.

6.7.2. Low Voltage Reset (LVR)

In addition to LVD, the GPL169256A offers another important feature, Low Voltage Reset (LVR). The level of LVR voltage is 2.4V. The LVR detects whether the power input of regulator is below the voltage. With the LVR function, a reset signal is generated to reset system when the operating voltage drops below predetermined voltage for four consecutive clock cycles. Without LVR, the CPU becomes unstable and malfunctions when the operating voltage drops below 2.4V. Using LVR, it will reset all functions to the initial operational (stable) states when the voltage drops below 2.4V. A LVR timing diagram is given as follows:



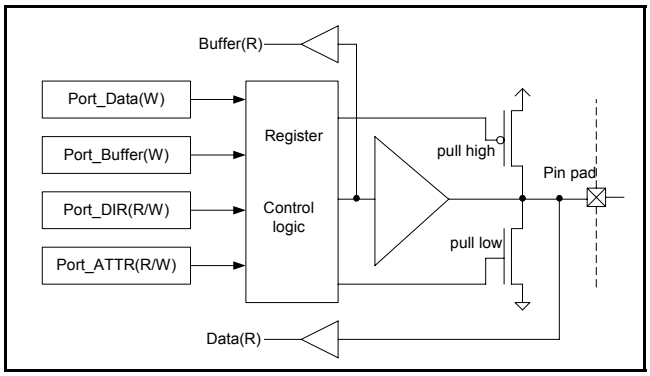
6.8. Interrupt

The GPL169256A has 18 interrupt sources. Some of the interrupt sources could be programmed as FIQ (Fast Interrupt Request) or IRQ (Interrupt Request) individually. The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is the low-priority one. When IRQ and FIQ happen simultaneous, IRQ has the lower priority than FIQ and so do the IRQ7 ~ IRQ0. IRQ7 is the lowest priority interrupt.

Interrupt Source	Interrupt Group	Priority
Audio ChannelA	FIQ/IRQ0	Highest
Audio ChannelB	FIQ/IRQ0	Highest
EXT1	FIQ/IRQ2	High
DMA	FIQ/IRQ3	High
UART	FIQ/IRQ3	High
SPI	FIQ/IRQ3	High
TimerC	FIQ/IRQ4	High
TimerB	FIQ/IRQ4	High
TimerA	FIQ/IRQ4	High
LCD Frame Pulse	FIQ/IRQ5	High
Key Change	FIQ/IRQ5	High
LVD	FIQ/IRQ6	High
Schedule	IRQ6	Low
Time Base C	IRQ6	Low
Time Base B	IRQ7	Lowest
Time Base A	IRQ7	Lowest
Alarm	IRQ7	Lowest
RTC	IRQ7	Lowest

6.9. I/O

Maximum four I/O ports are provided in GPL169256A: IOA, IOB, IOC and IOD. In addition to regular IO function, all I/Os are shared with special function pins. The following diagram is an I/O schematic.



Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer (R) and Data (R). The IOA is software programmable for key wakeup capability. To activate key wakeup function, latch data on PORT_IOA_RL and enable the key wakeup function. Wakeup is triggered when the IOA state is different from at the time latched.

6.10. ADC (Analog to Digital Converter)

The GPL169256A has built-in three 12-bit A/Ds (Analog to Digital Converter) channels; one is the microphone input channel and two are line-in channels. The function of an A/D converter is to convert analog quality signal, e.g. a voltage, into a digital word. Or convert from an input source which can be line-in from ADINA/ADINB or microphone input through amplifier and AGC controller. The MIC amplifier circuit is capable of reducing common mode noise by transmitting signals through MIC's fully differential input. Moreover, an external resistor can be applied to adjust microphone gain and time of AGC operating. The AD needs to select source of line-in before converting. The ADC chooses internal power (=AVDD) as top reference voltage.

6.11. DAC

The GPL169256A imposes two 16-bit DACs and therefore superior sound effect can be generated with less distortion.

6.12. Timer/Counter

The GPL169256A has three 16-bit timers/counters: TimerA, TimerB and TimerC. The clock source of TimerA comes from the combination of clock source A and clock source B. In TimerB and TimerC, the clock source is given from source C. When timer overflows, an INT signal is sent to CPU to generate a time-out signal.

Clock of Source A	Clock of Source B	Clock of Source C
SYSCLK/2	2048Hz	SYSCLK/2
SYSCLK/256	1024Hz	SYSCLK/256
32768Hz	256Hz	32768Hz
8192Hz	TMBB	8192Hz
4096Hz	TMBA	4096Hz
1	0	1
TimerB overflow	1	0
EXTA	0	EXTA
PWM service rate	-	PWM service rate

TimerA and TimerB can operate in timer mode, counter mode, capture mode, compare mode and PWM mode. TimerC can operate in timer mode and counter mode.

6.12.1. Timer mode

Initially, write a value of N into a timer and select a desired clock source, timer will start counting from N, N+1, N+2…, through FFFF. An INT (TimerA/TimerB/TimerC) signal is generated at the next clock after reaching "FFFF" and the INT signal is transmitted to INT controller for further processing. At the same time, N will be reloaded into timer and start all over again. The clock source A is a high frequency source and clock source B is a low frequency source. The combination of clock source A and B provides a variety of speed to TimerA. A "1" represents pass signal and not gating. In contrast, "0" indicates deactivating timer.

6.12.2. Counter mode

The EXTA is the external clock source (shared with IOA[7]). The external clock source can be divided by 1, 4 or 16 pre-scaler divider and capable of selecting clock edge.

6.12.3. Capture mode

In capture mode, the content of timer/counter is stored in register at the selected edge of pins CCP (special function of IOA[6]) by the selected rate. This could be used to detect the pulse width of CCP.

6.12.4. Comparison mode

In comparison mode, CCP will be programmed as output automatically. The initial value is loaded from pre-load register and after count to the pre-set value, hardware will set or clear CCP or leave it unaffected. When timer/counter overflows, initial value will not be reloaded but interrupt flag will be generated.

6.12.5. PWM mode

In PWM mode, the operation is similar to comparison mode except that the initial value will reloaded whenever timer/counter overflow is.

Generally, the clock source A and C are fast clock sources and source B comes from RTC system (32768Hz). Therefore, clock source B can be utilized as a punctual counter for time count, e.g., the 2Hz clock can be used for real time counting.

6.12.6. Timebase

Timebase, generated by 32768Hz, is a combination of frequency selections. The outputs of timebase module are named TMBA, TMBB, and TMBC. TMBA and TMBB can be clock source for TimerA (clock source B). The TMBA and TMBB are the sources for Interrupt (IRQ7) whereas TMBC is the source for interrupt (IRQ6).

TMBC	TMBB	TMB1
128Hz	8Hz	Reserved
256Hz	16Hz	1Hz
512Hz	32Hz	2Hz
1024Hz	64Hz	4Hz
Default: 128Hz	Default: 8Hz	Default: 2Hz

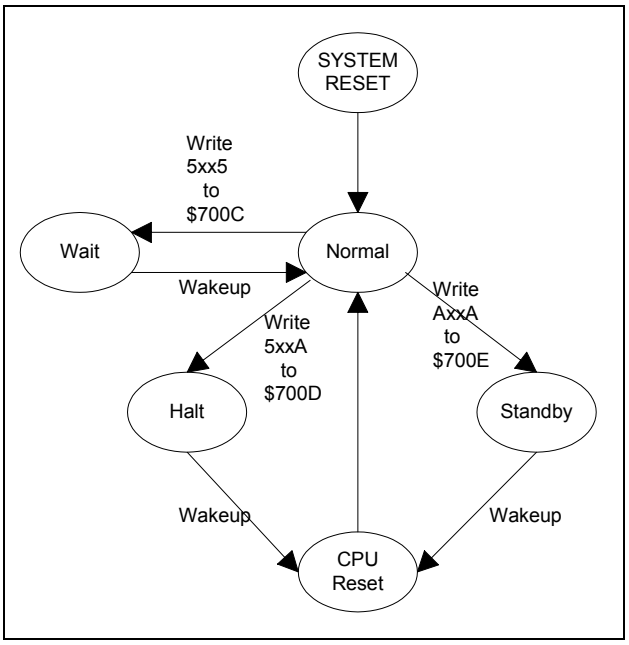
6.13. Power saving, Wakeup and Watchdog

6.13.1. Power saving and Wakeup

1). Power saving: In GPL169256A, CPU has three power saving mode, Wait/Halt/Standby mode. After reset, IC starts running until a power saving signal occurs.

2). Wakeup: If any interrupt happens, GPL169256A is awakened.

3). The following diagram shows the three conditions:



Note1: When GPL169256A enters Wait mode, any interrupt will awake GPL169256A. After GPL169256A is awoken, CPU continues to execute next instruction.

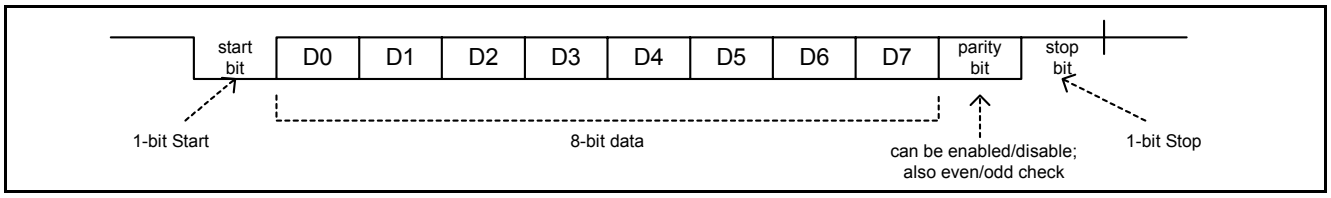
Note2: When GPL169256A enters Halt or Standby mode, any interrupt will awake GPL169256A. After GPL169256A is awoken, CPU will be reset to initial state.

6.13.2. Watchdog

The purpose of watchdog is to monitor if the system operates normally. Within a certain period of time, watchdog must be cleared. If watchdog is not cleared, CPU assumes the program has been running in an abnormal condition. As a result, system or CPU will be reset according to register setting and the program will be executed all over again. The watchdog function can be disabled by software. In GPL169256A, the clear period can be programmed from 62.5ms to 2 seconds (default). If watchdog is cleared within the given time period, the system or CPU will not be reset. To clear watchdog, simply write “Axx5(h)” to Port_Watchdog_Clear(W). The watchdog function remains enabled during wait mode and halt mode where the 32768Hz is still turned on.

6.14. UART

The UART module provides a full-duplex standard interface that is able to communicate with other devices. With this interface, GPL169256A can transmit and receive simultaneously. The maximum baud-rate can be up to 115200bps. This function can be accomplished by using IOA and Interrupt (UART IRQ). The Rx and Tx of UART are shared with IOA[5] and IOA[4]. The UART has two 16-byte FIFOs to store transmitted and received data. The UART status register will indicate status when the FIFOs are empty, half-full or full.



6.15. Serial Peripheral Interface (SPI)

The SPI interface is a master/slave interface that enables synchronous serial communication with peripherals. Two 16-byte FIFOs are used for transmitting and receiving data. Four modes with programmable phase and polarity of master clock are also supported.

6.16. Audio Algorithm

The following speech types can be used in GPL169256A: PCM, LOG PCM, SACM_A1600, SACM_1601, SACM_S200, SACM_S480, SACM_S530, SACM_S720, SACM_S320, SACM_S880, SACM_DVR1800, SACM_DVR520, SACM_DVR1600, SACM_DVR4800, and SACM_DVR3200. For melody synthesis, the GPL169256A provides a SACM_MS01 (FM synthesizer) and SACM_MS02 wave-table synthesizer.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	VDD	< 3.6V
Input Voltage Range	V_{IN}	-0.5V to VDD + 0.5V
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD VDDREG_55	2.4 2.4	- -	3.6 5.5	V	All VDD pins except VDDREG_55
Operating Current	I_{OP}	-	40	-	mA	VDD = 3.6V, F_{OSC} = 47.9232MHz, The wait cycle of internal ROM is 1 ($704c.b3~b0)
Wait Current	I_{WAIT1}	-	-	2	mA	VDD = 3.6V, 32K X'tal ON, The wait cycle of internal ROM is 1 ($704c.b3~b0), clock source OSC 1MHz. LCD ON, no LCD panel, PLL ON
Halt Current	I_{HALT1}	-	-	30	μA	VDD = 3.6V, 32K X'tal & RTC ON
Halt Current	I_{HALT2}	-	-	180	μA	VDD = 3.6V, 32K X'tal & RTC ON, mono LCD ON
Standby Current	I_{STB}	-	-	5 10	μA	VDD = 3.6V, all off, disable regulator VDD = 3.6V, all off, enable regulator
LCD Driver Voltage	VLCD	3.0	-	6.0		VDD = 3.0V, 1/5 bias, no load
		3.19	-	6.6	V	VDD = 3.0V, 1/6 bias, no load
		3.48	-	7.2	V	VDD = 3.0V, 1/7 bias, no load
Input High Level	V_{IH}	0.7 VDD	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.3 VDD	V	VDD = 3.0V
Output High Current	I_{OH2}	-2.0	-	-	mA	VDD = 3.0V, V_{OH} = 2.4V IOA[7:0]
Output Low Current	I_{OL2}	-2.0	-	-	mA	VDD = 3.0V, V_{OL} = 0.8V IOA[7:0]
Input Pull-Low Resistor (IOA)	R_{PL}	-	100	-	KΩ	VDD = 3.0V V_{IN} = 3.0V
Input Pull-High Resistor (IOA)	R_{PH}	-	100	-	KΩ	VDD = 3.0V V_{IN} = VSS

7.2.1. PLL Characteristics (T_A = 25℃, VDD=3.0V, 6MHz crystal disable)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
VCO Operating Frequency	F_{vco}	11.993	-	95.945	MHz	
Input Reference Clock Freq.	F_{ref}	-	32768	-	Hz	
Output Clock Freq.		5.997	-	47.972	MHz	
Start-up Time		-	-	5	ms	
Lock-in Time		-	-	5	ms	
Jitter (cycle-cycle)		-	1.5	-	%	
Duty Cycle		-	50	-	%	

7.2.2. ADC Characteristics (T_A = 25℃, VDD=3.0V)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
ADC Resolution	RESO	-	-	12	Bits	
Signal-to-noise Ratio +distortion	SINDR @fin=1KHz	-	-	57	dB	
ADC Input Voltage	VIN	VSS	-	VDD	V	
INL(Integral Non-linearity)	INL	-	±4.0	-	LSB	
DNL(Differential Non-linearity)	DNL	-	±0.8	-	LSB	
No Missing Code		10	11	-	Bits	
AD Conversion Rate	F_{CONV}	-	-	F_{CPU}/512	KHz	

7.2.3. DAC Characteristics (T_A = 25℃, VDD=3.0V)

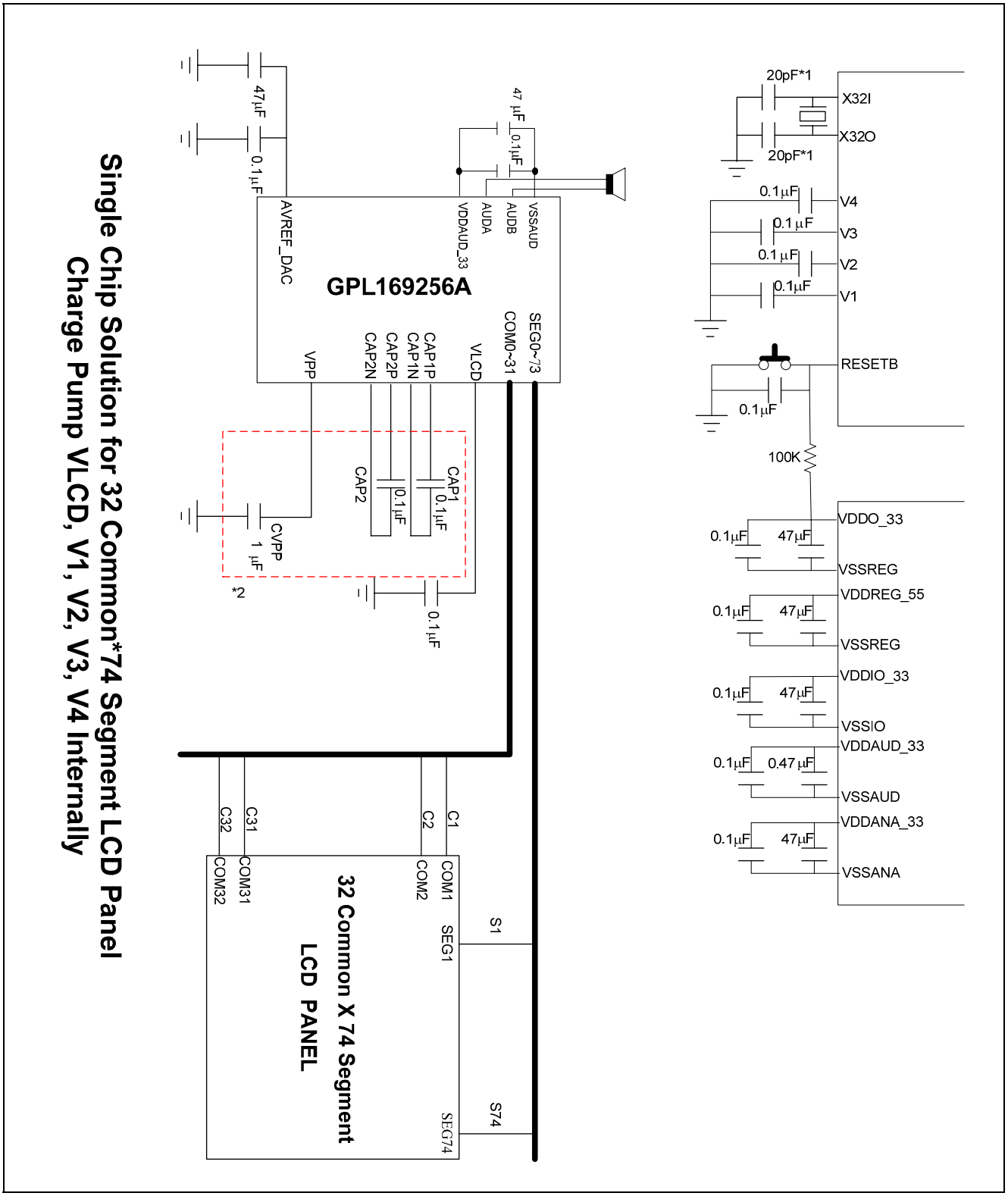
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Resolution		-	16	-	Bits	
Input Data Sampling Freq.		-	-	192	KHz	
Output Range		0.2	-	0.8	Vdd	
Output Loading	R_{LOAD}	125	-	-	ohm	
THD+N at FS		-	0.1(-60dB)	-	%	
Dynamic Range		-	80	-	dB	

7.2.4. OSC Characteristics (T_A = 25℃, VDD=3.0V)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output Clock Frequency	CLK32768	-	32768	-	Hz	
Duty Cycle		40	-	50	%	
Start-up Time		-	-	10000x T_{32768}	μs	

8. APPLICATION CIRCUITS

8.1. Application Circuit - (1)



Note*1: These capacitor values are for design guidance only. We recommend user select the ESR < 35K as well as CL1=CL=20~30pF(including PCB parasitic loading). Note that the environment humidity may affect the equivalent resistances on the two end points. To avoid the humidity effect, we recommend user to apply 20pF(assume PCB parasitic loading is 6pF) on XI and XO. Note that a larger CL capacitance will cause a longer time for XTAL to oscillate.

Note*2: These capacitor values are for design guidance only. The ratio of capacitance of CVPP to the capacitance of CAP1 and CAP2 is recommended to be ten or more.

9. PACKAGE/ORDERING INFORMATION

9.1. Ordering Information

Product Number	Package Type
GPL169256A-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
DEC 19, 2013	1.4	Modify 8.1. Application Circuit.	14
SEP 16, 2013	1.3	Modify 8.1. Application Circuit.	14
OCT. 11, 2012	1.2	Modify 8.1. Application Circuit.	14
JUL. 29, 2010	1.1	Modify 8.1. Application Circuit and add notes.	15
AUG. 20, 2009	1.0	1. Add description about ICECLK & ICESDA pin. 2. Add 2nd I_{STB} condition on DC characteristics table.	5 13
MAR. 13, 2008	0.1	Original	18