DATA SHEET

GPL191B2

1024 Dots LCD Controller/Driver with 256KB ROM

Mar. 08, 2010

Version 1.1

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1024-dot LCD Controller/Driver with 256KB ROM

1. GENERAL DESCRIPTION

The GPL191B2 is an 8-bit CMOS microprocessor containing 704 bytes working RAM, 256K bytes ROM, 12 I/Os, interrupt/wakeup controller, UART for serial communication, and automatic display controller/driver for LCD. It has one PWM driver with two audio channel outputs. Attractive sound effects can easily be generated. Its large ROM area can be used to store both program and audio data (speech duration is approx. 80 seconds at a 6KHz sampling rate using 4-bit ADPCM). The built-in UART speeds up data transmission between two chips. Furthermore, a SLEEP (power-down) feature is also built-in to reduce power consumption. The GPL191B2 is designed with state-of-the-art technology to fulfill LCD application requirements, especially hand-held products.

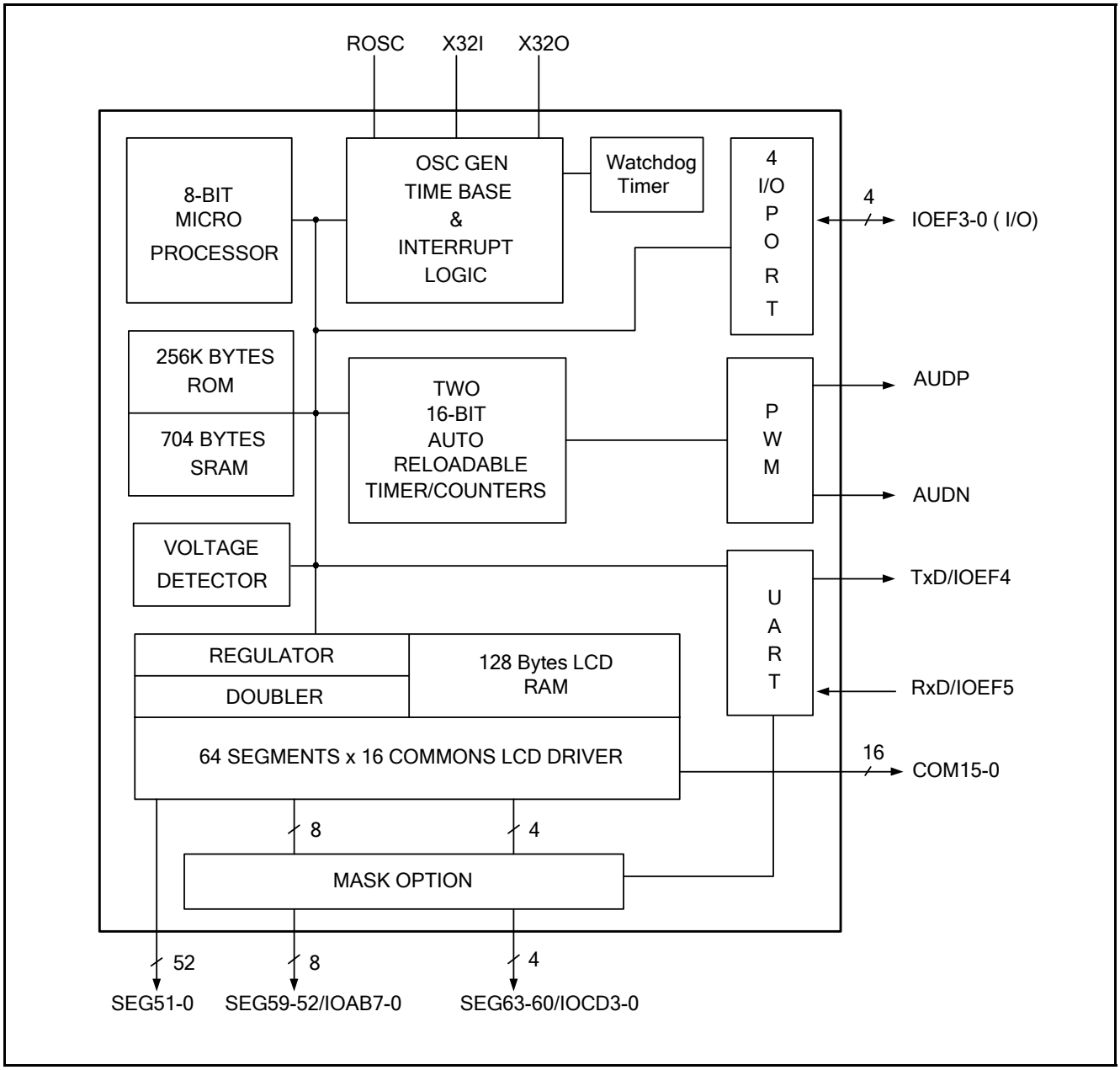
2. FEATURES

- Built-in 8-bit processor
  - **704 bytes SRAM**
  - **256K bytes ROM**
  - Max. Operating Speed: 4.0MHz @ 2.4V
  - CPU clock is software programmable, can be 1/2, 1/4, 1/8 or 1/16 R-oscillator clock frequency
  - Key wake-up function
  - Provides 8 interrupt sources
- Asynchronous serial interface (UART)
  - Supports bit rate up to 115.2 Kbps
- Programmable LCD Driver
  - **Up to 64 segments, up to 16 commons, maximum 1024 dots**
  - 1/4 or 1/5 bias capability
  - 1/8, 1/12 or 1/16 duty
  - **128 bytes dedicated LCD RAM**
  - Built-in voltage doubler and voltage regulator to generate VLCD for LCD driver
  - 16-level VLCD adjustable
- Power saving SLEEP mode (wakeup source: key input, 2Hz, 16Hz, and timer)
- **Low Voltage Detector**
  - 2.6V and 2.4V detection
- Wide Operating Voltage:
  - 2.4V - 3.6V
  - 3.6V - 5.5V
- Peripherals
  - **12 I/O pins shared with LCD segments (mask option)**
  - **4 I/O pins (IOEF3 - 0)**
  - **Extra two general I/O pins (IOEF5 - 4) or 2 UART pins (TXD - RXD) (mask option)**
  - **Extra 2 I/O pins (IOEF7 - 6) if LCD is 1/8 or 1/12 duty (mask option)**
  - Built-in 32.768KHz oscillator circuit for real time clock Function
  - Built-in R-oscillator (only one resistor required)
  - Internal time base generator
  - Two 16-bit reloadable timer/counters(TM0 & TM1)
  - **2-channel 8-bit audio decoders**
  - **One PWM output (can drive speaker or buzzer directly)**
  - Watchdog Timer for reliable operation
- Low-power consumption

3. APPICATION FIELD

- Hand held Games
- Scientific Calculator
- Talking Calculator, Talking Clock
- Talking Instrument Controller
- General Speech Synthesizer
- Data Bank

4. BLOCK DIAGRAM



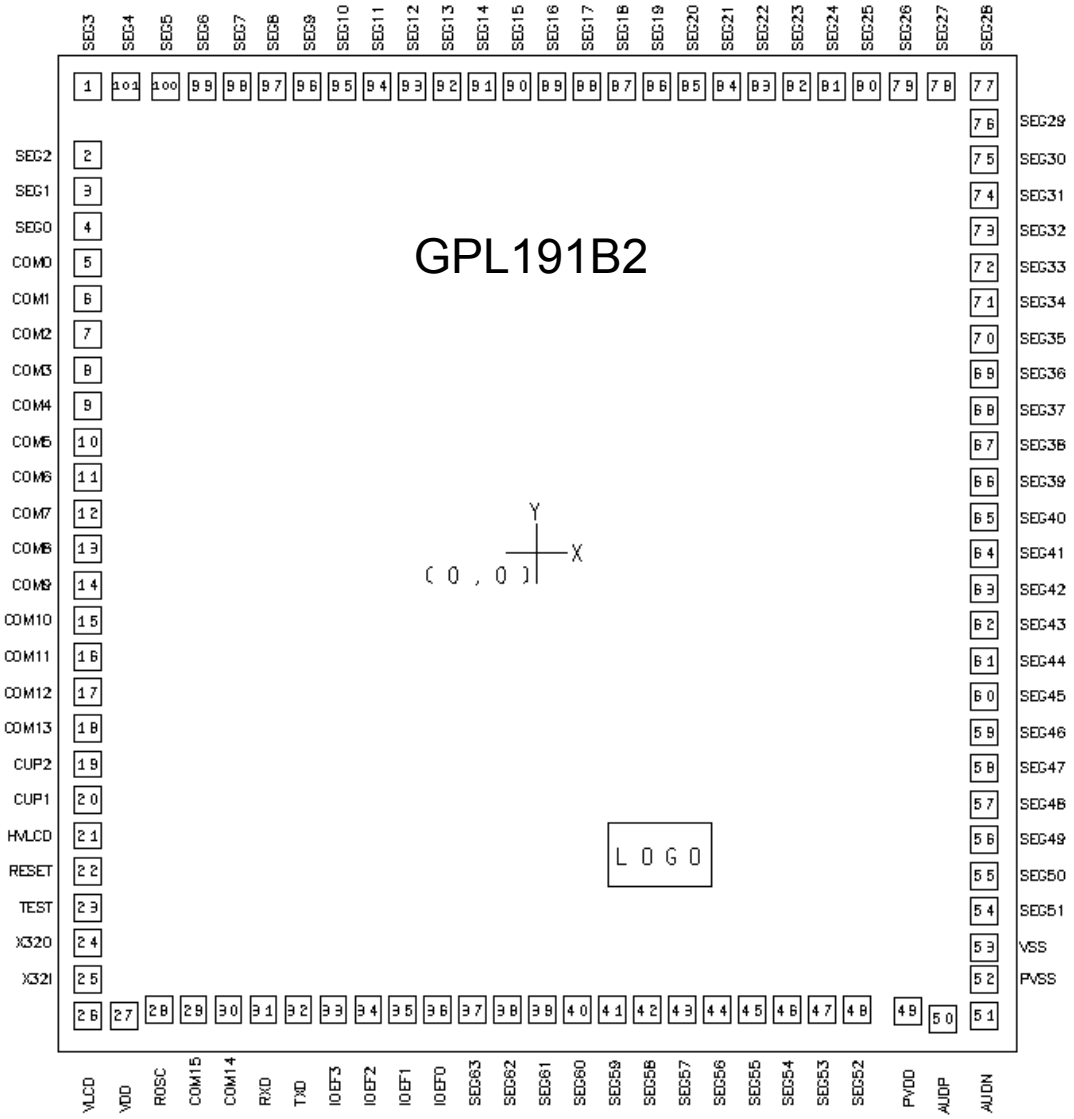
Note1: IOAB7 - 0 can be enabled by mask option from Segment 59 - 52. Each I/O (segment) can be mask optioned individually.
Note2: IOCD3 - 0 can be applied as segment 63 - 60 by mask option. Each I/O corresponds to one segment.
Note3: Common 15 - 12 can be optioned to IOEF7 - 6 when LCD driving type is selected as 1/8 duty or 1/12 duty.
Note4: TxD and RxD can be optioned to IOEF5 - 4 when UART is not used.

5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
SEG3 - 0 SEG51 - 4 SEG63 - 52	4 - 1 54 - 101 37 - 48	O	LCD driver segment output. SEG59 - 52 can be re-assigned as IOAB7 - 0 bi-directional I/O ports. Also, SEG60 - 63 can be re-assigned as IOCD0 - 3 bi-directional I/O port. (mask option)
COM13 - 0 COM15 - 14	18 - 5 29 - 30	O	LCD driver common output. COM15 - 14 can be re-assigned as IOEF7 - 6 bi-directional I/O port. (mask option)
IOEF3 - 0	33 - 36	I/O	Port EF is a bi-directional I/O port, can be software programmed as wake up I/O.
RxD	31	I	UART input, optioned to IOEF5.
TxD	32	O	UART output, optioned to IOEF4.
ROSC	28	I	ROSC input, connect to VDD through a resistor.
RESET	22	I	System reset input, low active.
AUDP AUDN	50 51	O	PWM audio output.
X32I	25	I	32.768KHz crystal input or connects to VDD through a resistor. (option)
X32O	24	O	32.768KHz crystal output.
TEST	23	I	Test input
VLCD	26	P	LCD voltage. Connect to VSS through a capacitor if voltage doubler is enabled.
HVLCD	21	P	LCD voltage generation. Connect to VSS through a capacitor if voltage regulator is enabled.
CUP1 CUP2	20 19	P	LCD voltage generation. Charge pump capacitor interconnection pins.
VDD	27	P	Power supply voltage input.
VSS	53	P	Ground reference.
PVDD	49	P	PWM driver power.
PVSS	52	P	PWM driver ground reference.

Legend: I = Input, O = Output, P = Power

5.1. PAD Assignment



This IC substrate should be connected to VSS or floated

Note1: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

6. FUNCTIONAL DESCRIPTIONS

6.1. ROM Area

The GPL191B2 is a large ROM based micro-controller with 1024 dots LCD driver. The large ROM can be defined as program ROM, LCD fonts and audio data continuously without any limitation. To access ROM, users should program the Bank Selection register, choose bank, and then access bank address to fetch data.

6.2. Map of Memory and I/Os

***I/O PORT:**

- PORT IOAB $0002
- PORT IOCD $0003
- PORT IOEF $0004
- I/O AB_CTRL $0001
- I/O CD_CTRL $0000
- I/O EF_CTRL $0006

***NMI SOURCE:**

- INT1 (from TIMER 1)

***INT SOURCE:**

- INT0 (from TIMER 0)
- INT1 (from TIMER 1)
- 2 KHz
- T2 Hz (2Hz / 1 Hz)
- T16 Hz (4Hz/8Hz/16Hz/32Hz)
- 128 Hz
- EXT INT (from IOCD1 pin)
- UART

***MEMORY MAP**

$00000 $0003F $00040	H/W registers , I/Os
$000FF $00100	WORKING SRAM (192 bytes)
$002FF $00300	SRAM for STACK and Data Storage (512 bytes)
$0037F $00400	LCD Buffer (128 bytes)
$007FF $00800	GENERALPLUS TEST PROGRAM
$07FFF $08000	USER's PROGRAM DATA AREA ROM BANK #0
$0FFFF $10000	ROM BANK #1
$17FFF $18000	ROM BANK #2
$1FFFF $20000	ROM BANK #3
$27FFF $28000	ROM BANK #4
$2FFFF $30000	ROM BANK #5
$37FFF $38000	ROM BANK #6
$3FFFF	ROM BANK #7

Note: $7FFA - $7FFF in ROM bank#0, and $FFFA - $FFFF in bank#1 - 7 are reserved for reset vectors.
$7FF2 - $7FF7 in bank#0, and $FFF2 - $FFF7 in bank#1 - 7 are reserved for GENERALPLUS testing.

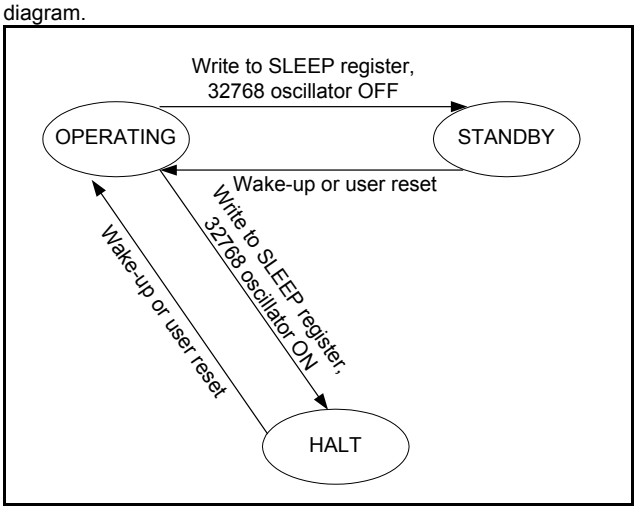
6.3. Operating States

The GPL191B2 supports three operating states: standby, halt, and operating. Following table shows the differences between the three operating states.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768 oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

In the operating state, all modules (CPU, 32768Hz oscillator, timer/counter, LCD drive, etc.) are activated. The halt/standby state is entered by writing to the SLEEP register. There are four wake-up sources in GPL191B2: port IOEF wake-up, Timer0 wake-up, 4Hz/8Hz/16Hz/32Hz wake-up and 2Hz/1Hz wake-up. If any wake-up event occurs, execution of the next instruction continues in the operating state.

When in standby, all modules are shut down, and RAM and I/Os remain in their previous states. Current consumption is minimized in standby. By writing to the SLEEP register while the 32768Hz oscillator running, the system is in halt state. In halt state, CPU clock is halted while it waits for an event (key press, or timer overflow) to generate a wake-up signal. The 32768Hz related modules (timer/counter, LCD drive, etc.) may remain active in the halt state. The following figure is the GPL191B2 state diagram.



GPL191B2 State Diagram

6.4. Speech and Melody

Since the GPL191B2 provides large ROM and wide range of CPU operating speed, it is very suitable for speech and melody synthesis. For speech synthesis, GPL191B2 provides several timer interrupts for precise sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound then can be played back in the sequence assigned by the users' programs. Several algorithms are recommended for high fidelity and good compression of sound: such as PCM and ADPCM.

For melody synthesis, the GPL191B2 provides a dual tone mode. Once in the dual tone mode, users need only to program the tone frequency for each channel by writing to the timer/counter TM0 and TM1, and set the envelope for each channel. The hardware will toggle the tone wave automatically.

6.5. LCD Controller/Driver

GPL191B2 contains a 1024-dot LCD driver. Programmers can set the LCD configuration (bias, duty, voltage doubler) by writing to LCD control register ($20). Once the LCD configuration is initialized, the desired pattern can be displayed by filling the LCD buffer with appropriate data. The LCD driver can also operate during sleep by keeping 32768Hz oscillator running. The LCD driver in GPL191B2 is designed to fit most LCD specifications. It can either be programmed as 1/4 or 1/5 bias and the duty is also programmable as 1/8, 1/12, or 1/16 duty.

6.6. Voltage Doubler/Regulator

The GPL191B2 also contains a built-in voltage doubler and a voltage regulator. The voltage regulator provides a reference voltage (HVLCD) for the voltage doubler to generate VLCD (by charge-pumping). Users can get desired VLCD by changing the output reference voltage (writing to register) of the voltage regulator. By enabling the voltage doubler and regulator, users can get a stable VLCD that will not be affected by VDD. The three possible configurations of voltage doubler and regulator are shown in the following table:

Regulator	Doubler	VLCD
OFF	OFF	VDD (not regulated)
OFF	ON	2*VDD (not regulated)
ON	OFF	N/A
ON	ON	Adjustable

Note that when voltage regulator and voltage doubler are enabled, VDD should be lower than V_{LCD}-0.5V to prevent forward biasing the p-n junction of I/O's output PMOS.

6.7. PWM Output

Internally, the GPL191B2 has one PWM output with two sound channels. Each channel can be set to play speech or tone individually. GPL191B2 uses Pulse Width Modulation that could directly drive speaker or buzzer without any buffer or amplification circuit.

6.8. Asynchronous Serial Interface (UART)

The GPL191B2 supports a 1-channel UART for serial communications. It supports bit-rate up to 115.2kbps. UART operation is controlled by UART command registers. Configurations such as Tx/Rx interrupt, parity check, parity even/odd and clock source can be set in command registers. Two interrupts are generated by Rx and Tx. The Rx or Tx interrupt activates when a byte is received or transmitted. By reading the status register, user knows whether the interrupt is generated by Rx or Tx. Framing, overrun and parity errors are detected as each byte is received. All error status can be read from status register.

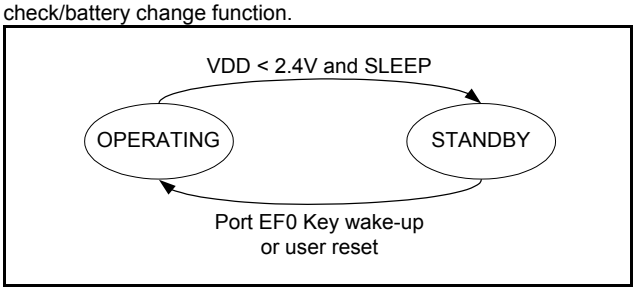
The UART supports clock auto calibration. If this clocking scheme is selected, standard baud rates from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to baud rate control registers. The supported standard baud rates and their minimum R-oscillator clock frequency required are shown in the following table:

Baud Rate(bps)	Min. Frosc(Hz)
1200	24000
2400	48000
4800	96000
9600	192000
19200	384000
38400	768000
51200	1024000
57600	1152000
102400	2048000
115200	2304000

If the auto calibration clocking scheme is not selected, users can get desired baud rates by writing appropriate values to pre-scalar registers. Non-standard baud rates can be obtained this way. When using the non-calibration mode, one should be aware that the frequency of R-oscillator may alter due to manufacturing process variations, supply voltage, operating temperature and tolerance of external R components used.

6.9. Low Voltage Detection

The GPL191B2 provides a 2.6V/2.4V voltage detector to detect a low voltage event. Users can turn on 2.6V detection and read bit1 of the port periodically to monitor whether VDD is lower than 2.6V. In addition, if 2.4V detection is turned on and VDD drops below 2.4V, after a SLEEP command is issued, system will shut down all activities (LCD bias, LCD display, 32768Hz oscillator) and enters standby mode to reduce current consumption. This low voltage power-down can be awakened by a PEF0 key change or RESET. Users can use this feature to implement the low battery check/battery change function.



State Diagram of Low Voltage Power Down

6.10. Watchdog Timer (WDT)

An on chip watchdog timer(WDT) is available in the GPL191B2. The WDT is designed to recover the system from abnormal operation. If the system is stalled, the WDT will generate a system reset to restart system after one second. If WDT is enabled, the WDT should be cleared every 0.5 seconds to avoid accidental reset. The WDT can be cleared by writing to WDT clear register. Note that the WDT only works when 32768 Hz clock is available.

6.11. Mask Options

6.11.1. 32768 oscillator

1). X'TAL

2). R-oscillator

6.11.2. Watchdog timer

1). Enable

2). Disable

6.11.3. TxD/RxD selection

1). TxD as UART transmit output, RxD as UART receive input

2). TxD as I/O port EF4, RxD as I/O port EF5

6.11.4. Port EF bit7 - 0 with 600K, Pull-Low

Each bit can be optioned to Enable/Disable individually.

6.11.5. I/O and LCD driver

There are some examples shown as below:

Dots	Segment	Common	Input/Output	Input/Output	Input/Output
1024	64	16	4 IOEF3 - 0	-	-
960	60	16	4 IOEF3 - 0	4 IOCD3 - 0	-
832	52	16	4 IOEF3 - 0	4 IOCD3 - 0	8 IOAB7 - 0
768	64	12	8 IOEF3 - 0	-	-

Each input/output port, IOAB7 - 0 and IOCD3 - 0, can be optioned to LCD segments independently, and LCD commons (COM15 - 12) can be optioned to IOEF7 - 6 when LCD mode is 1/8 duty or 1/12 duty. If UART is not used, two more I/O ports (TxD/IOEF4, RxD/IOEF5) can be used.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics

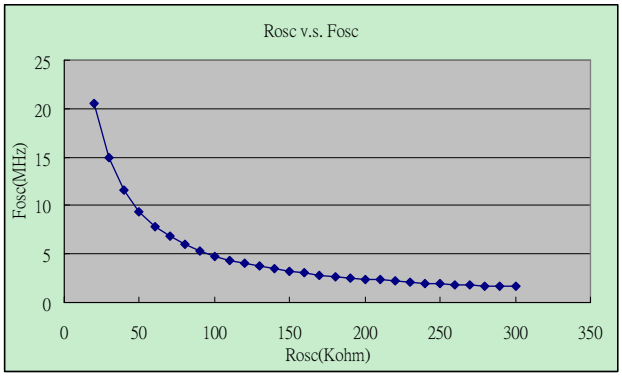
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
		3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	650	-	μA	F_{OSC} = 4.0MHz, F_{CPU} = 1.0MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, ALL OFF
Halt Current	I_{HALT}	-	16	-	μA	VDD = 3.0V, 32K X'tal ON, LCD ON, VLCD = 4.8V, no LCD panel
Audio Output Current	I_{OH}	-	-45	-	mA	VDD = 3.0V, V_{OH} = 2.5V
		-	-75	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Audio Output Current	I_{OL}	-	65	-	mA	VDD = 3.0V, V_{OL} = 0.5V
		-	110	-	mA	VDD = 3.0V, V_{OL} = 1.0V
VLCD Variation	V_{LCD_VAR}	-	±0.2	-	V	VDD = 2.4V - 5.4V, V_{LCD} = 4.8V No LCD panel applied
Low Voltage Detection Level	V_{LV26}	2.50	2.60	2.70	V	-
Voltage difference of 2.6V and 2.4V detection level	V_{DIF}	0.1	-	-	V	-
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (I/O)	I_{OH}	-	-3.3	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (I/O)	I_{OL}	-	10.0	-	mA	VDD = 3.0V, V_{OL} = 0.8V
CPU Clock	F_{CPU}	-	-	4.0	MHz	F_{CPU} = F_{OSC}/2 @ 2.4V

Note1: VLCD variation is subject to change due to the variation of process, temperature, supply voltage and loadings.

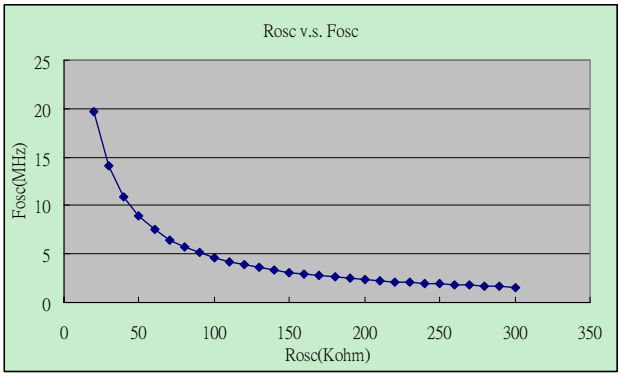
Note2: When voltage regulator and voltage doubler are enabled, VDD should be lower than VLCD-0.5V to prevent forward biasing the p-n junction of I/O's output PMOS.

7.3. The Relationship between the R_{OSC} and the F_{CPU}

7.3.1. VDD = 3.0V, T_A = 25℃

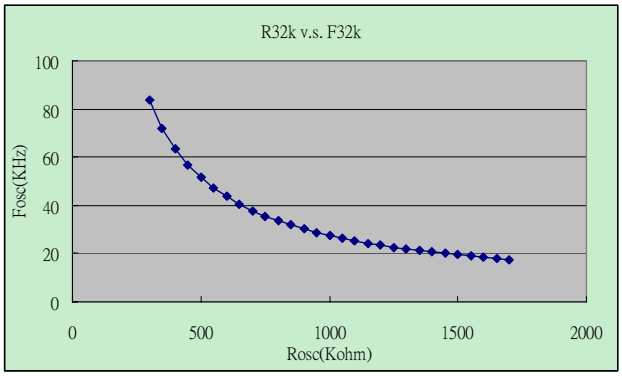


7.3.2. VDD = 4.5V, TA = 25℃

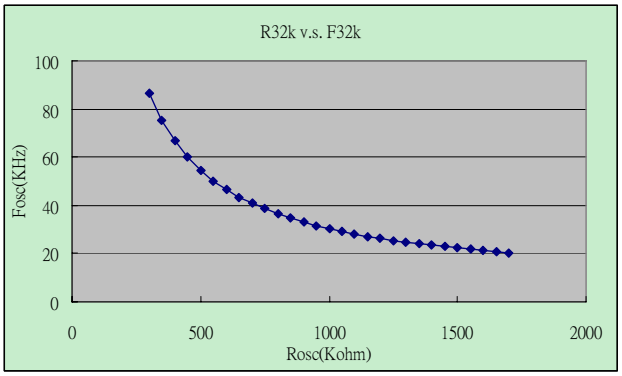


7.4. The Relationship between the R_{32K} and the F_{32K}

7.4.1. VDD = 3.0V, TA = 25℃

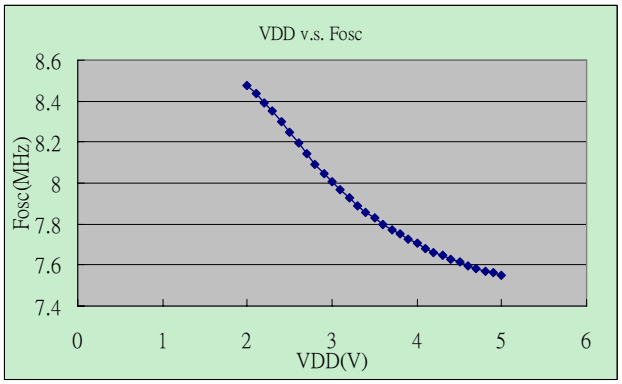


7.4.2. VDD = 4.5V, TA = 25℃

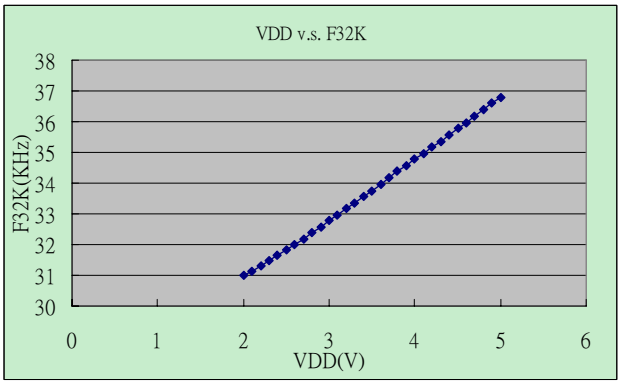


7.5. The Relationship between the VDD and the Frequency

7.5.1. VDD vs. F_{OSC} @R_{OSC}=59kohm, T_A = 25℃

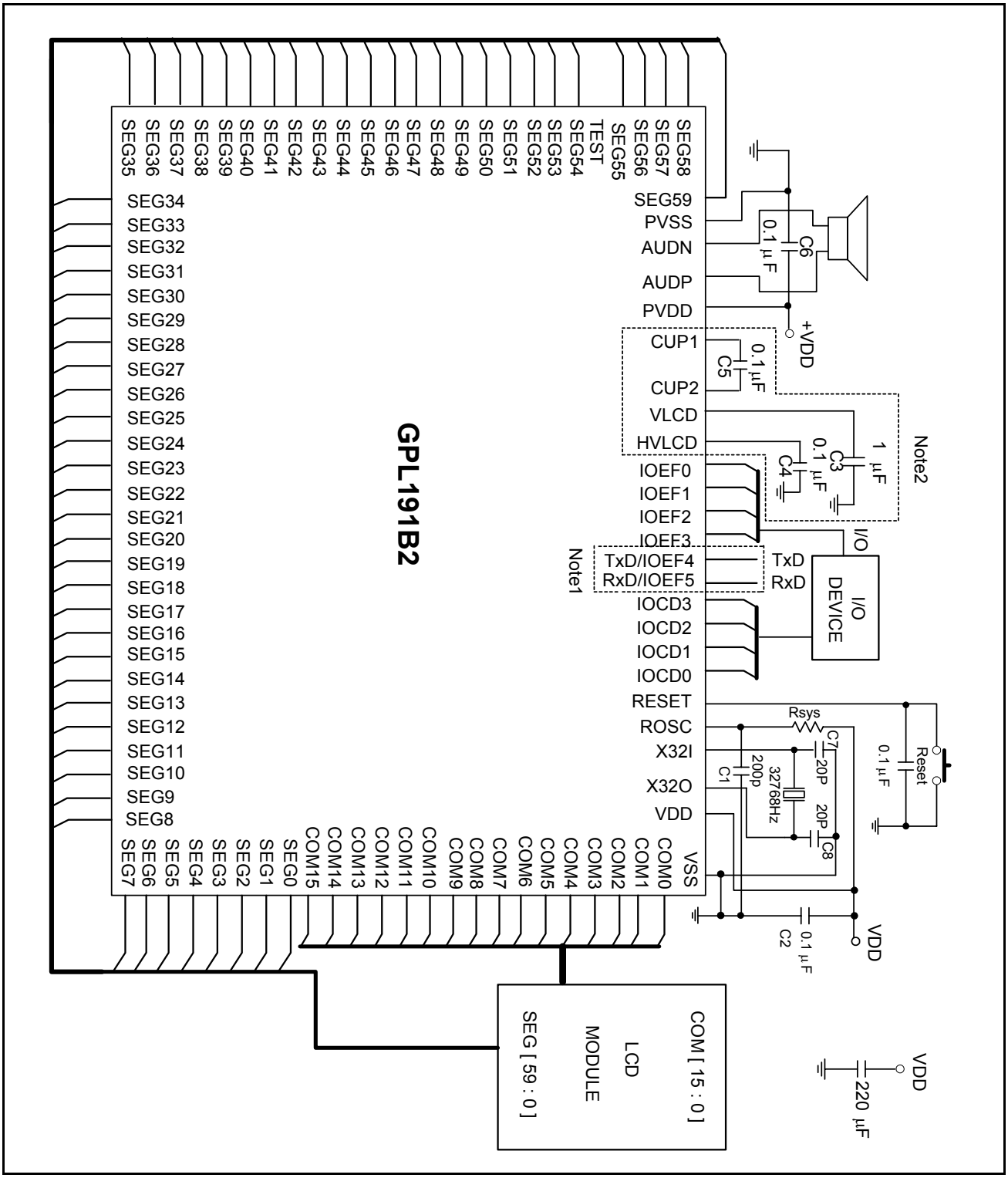


7.5.2. VDD vs. F_{32k}@R_{32K}=820Kohm, T_A = 25℃



8. APPLICATION CIRCUITS

8.1. 960 Points LCD Driver, 60 Segments × 16 Commons



Note1: IOEF4, IOEF5 are shared with TxD, RxD(UART), if UART is not used, these two pins can be used as I/O ports

Note2: These capacitors must be connected if voltage doubler and voltage regulator are used.

Note3: Wire route path from capacitors (C6 - 1) to chip should be as close as possible.

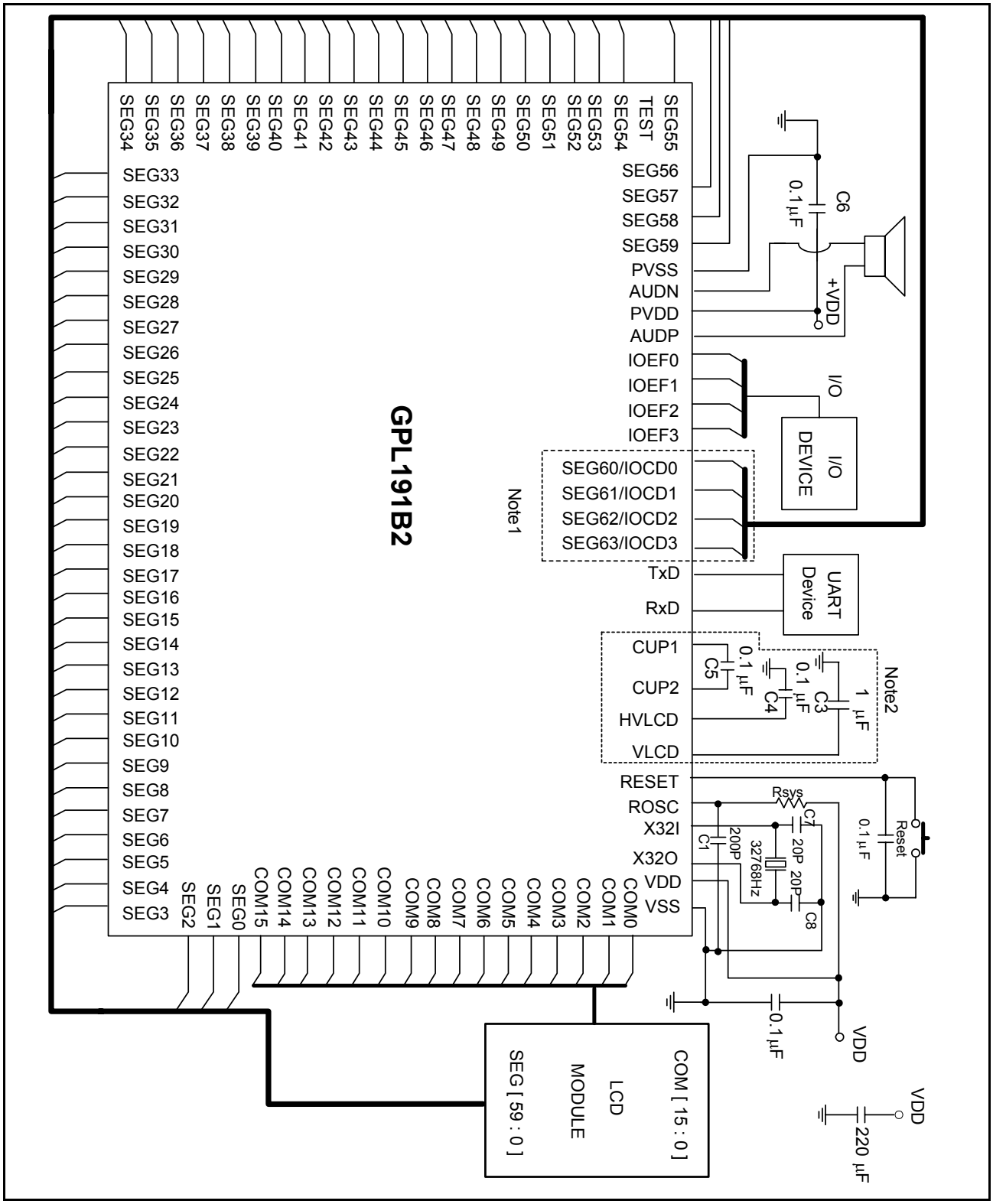
Note4: If voltage doubler and voltage regulator are not used, VLCD should be connected to VDD.

Note5: C7, C8 and crystal should be placed as close as possible to X32I and X32O. A shielding by ground is suggested.

Note6: The value of C7 and C8 are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note7: The capacitor value of C1 is from 30pF to 200pF, according to system noise level.

8.2. 1024 Points LCD Driver, 64 Segments × 16 Commons



Note1: IOCD3 - 0 can be mask-option for segment 63 - 60.

Note2: These capacitors must be connected if voltage doubler and voltage regulator are used.

Note3: Wire route path from capacitors (C6 - 1) to chip should be as close as possible.

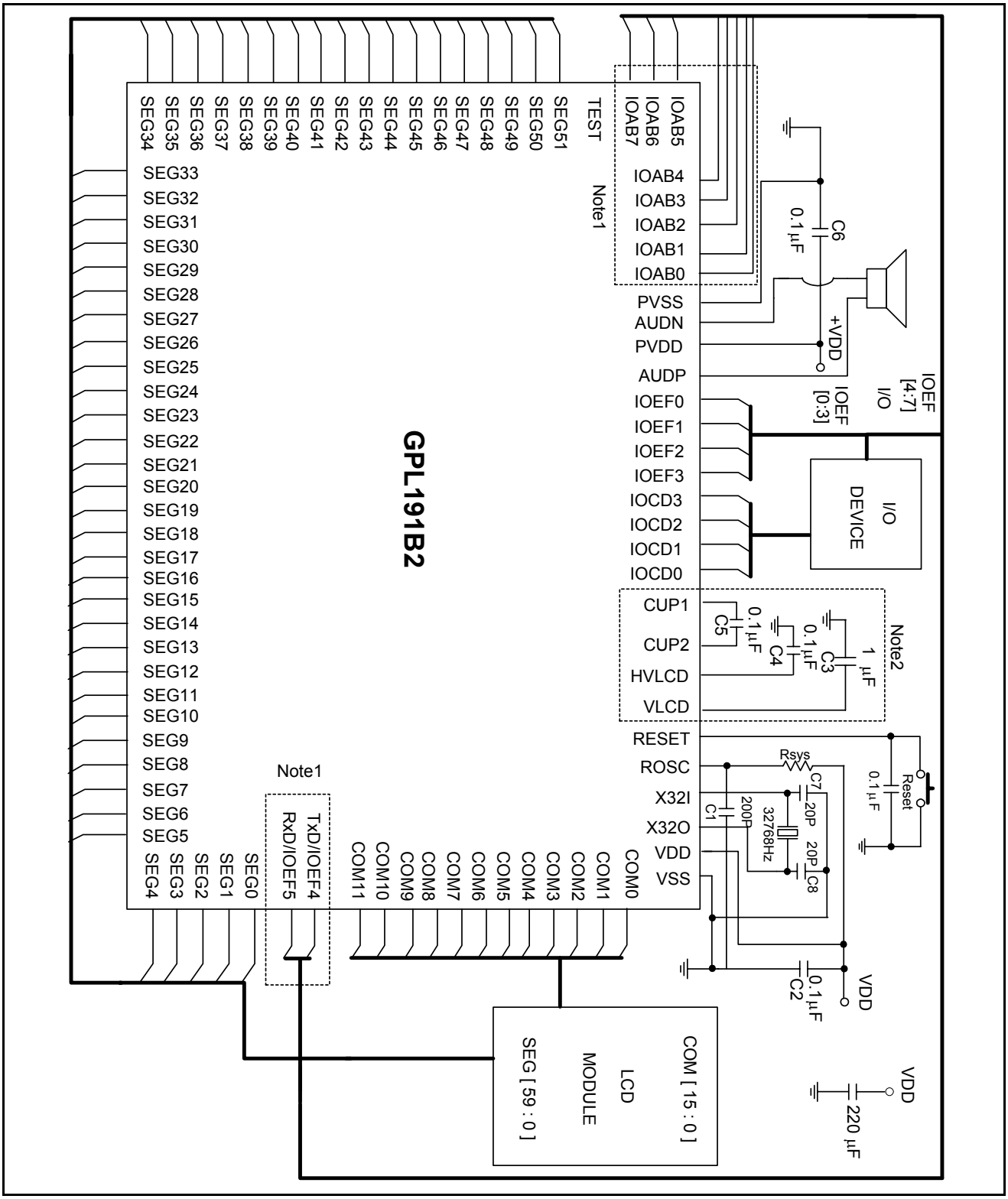
Note4: If voltage doubler and voltage regulator are not used, VLCD should be connected to VDD.

Note5: C7, C8 and crystal should be placed as close as possible to X32I and X32O. A shielding by ground is suggested.

Note6: The value of C7 and C8 are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note7: The capacitor value of C1 is from 30pF to 200pF, according to system noise level.

8.3. LCD in 1/8 Duty or 1/12 Duty, IOAB7 - 0, IOCD3 - 0, IOEF5 - 0



Note1: SEG59 - 52 can be mask-option for IOAB7 - 0. TxD and RxD can be used for IOEF4, IOEF5 when UART is not used.

Note2: These capacitors must be connected if voltage doubler and voltage regulator are used.

Note3: Wire route path from capacitors (C6 - 1) to chip should be as close as possible.

Note4: If voltage doubler and voltage regulator are not used, VLCD should be connected to VDD.

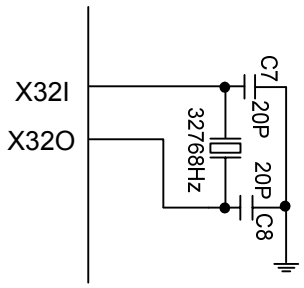
Note5: C7, C8 and crystal should be placed as close as possible to X32I and X32O. A shielding by ground is suggested.

Note6: The value of C7 and C8 are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

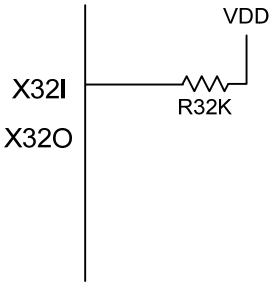
Note7: The capacitor value of C1 is from 30pF to 200pF, according to system noise level.

8.4. 32K Frequency Option Connection

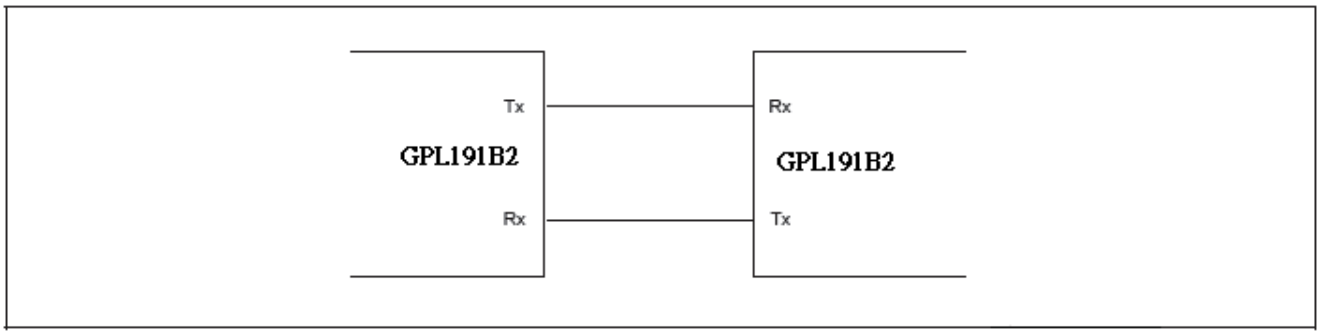
8.4.1. Crystal option



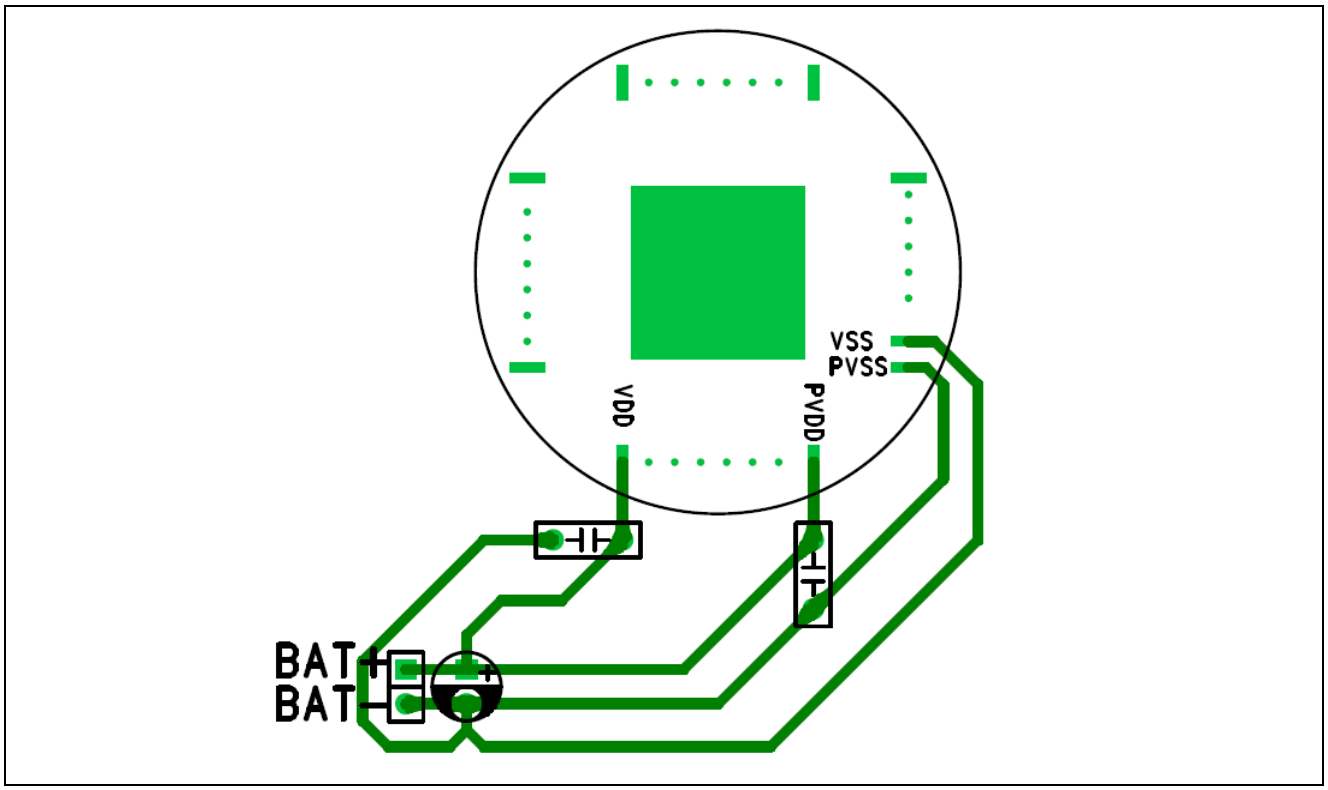
8.4.2. External resistor option



8.5. Serial Communications between two GPL191B2s



8.6. Power-Ground Layout Illustration



Note1: PVDD and VDD are branched from the power source. Do not connect in series.
Note2: PVSS and VSS are branched from the power source. Do not connect in series.

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPL191B2-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
Mar. 08, 2010	1.1	1. Modify 1.GENERAL DESCRIPTION. 2. Modify 2.FEATURES. 3. Modify 6.7. PWM Output.	3 3 8
May 06, 2009	1.0	1. Add chapter 7. ELECTRICAL SPECIFICATIONS. 2. Modify chapter 8. APPLICAION CIRCUITS.	10-15
Nov. 11, 2008	0.1	Preliminary version	16