DATA SHEET

GPL30A1

144KB LCD Controller/Driver

FEB. 25, 2010

Version 1.1

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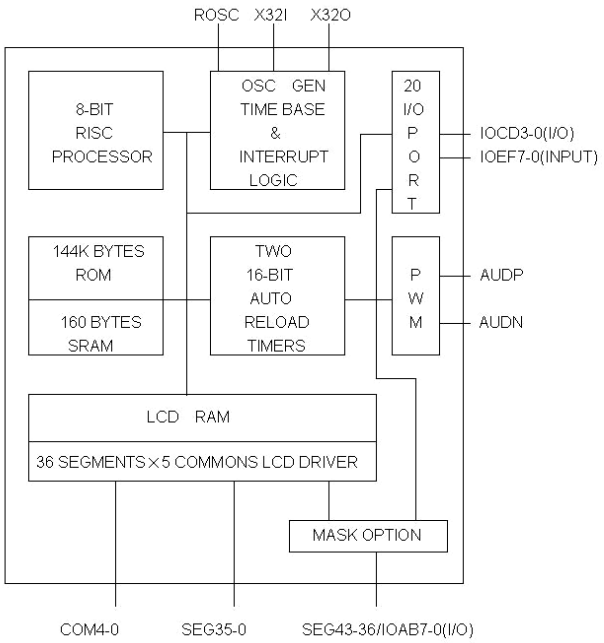
144KB LCD CONTROLLER/DRIVER

1. GENERAL DESCRIPTION

The GPL30A1 is a CMOS 8-bit single chip microprocessor which contains RAM, ROM, I/Os, interrupt controller, 8-bit PWM audio output and automatic display controller/driver for LCD. For power saving, a software controllable standby switch is also built-in. This chip is implemented with advanced design and process technology. It is very suitable for LCD type handheld products. The ROM space of this chip can be used to store program or audio data. (The speech data is about 38 seconds at 7 KHz sampling rate by using 4bit-ADPCM).

2. BLOCK DIAGRAM



Note: IOAB7 - 0 can be mask option for segment 43 - 36. The mask option can be used as one I/O for one segment.

Note: Patent Circuit Included.
Taiwan Patent No. 68824.

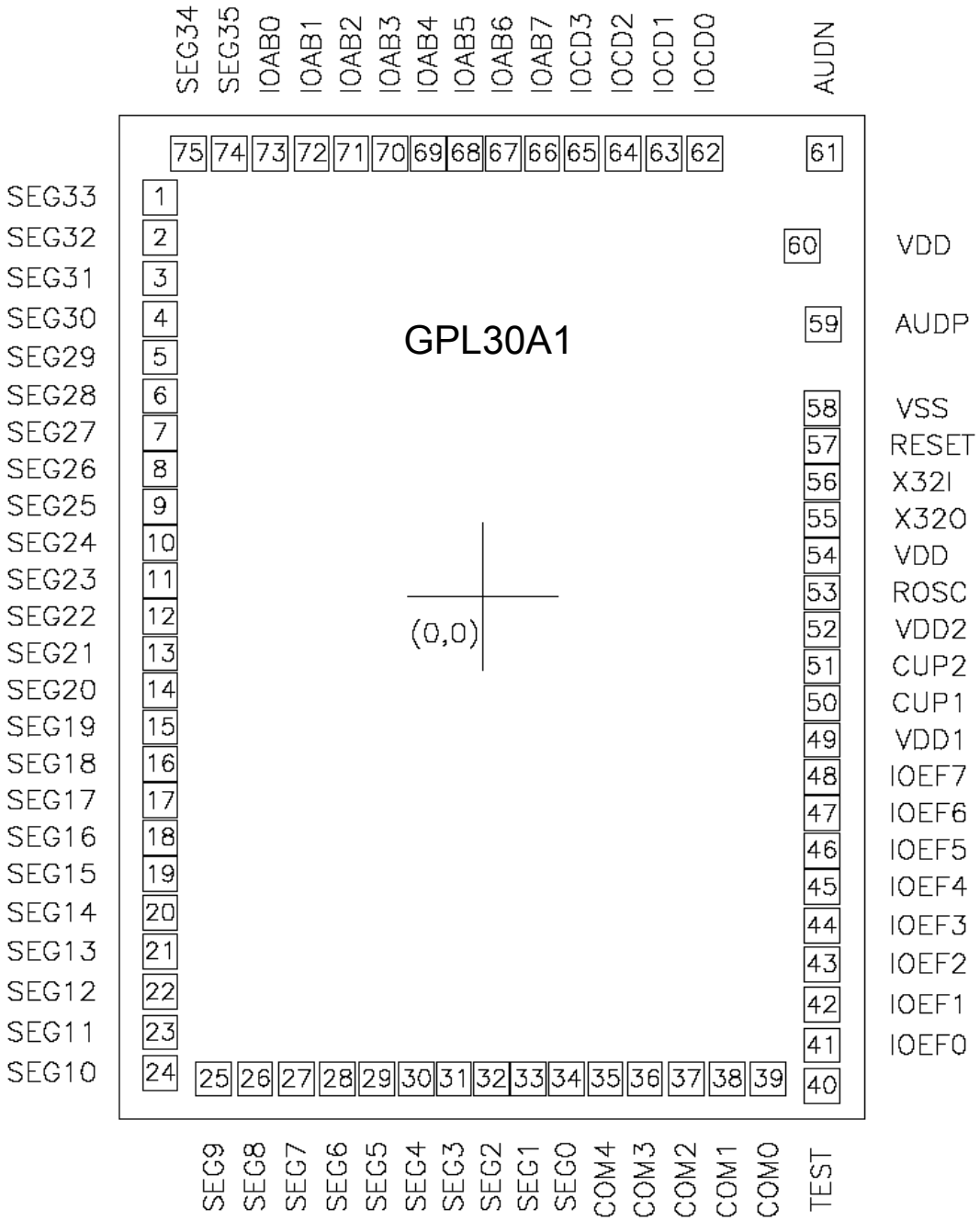
3. FEATURES

- Built-in 8-bit CPU
- 160 bytes SRAM
- 144K bytes ROM
- Max. CPU frequency: 2.0MHz @ 3.0V
- Wide operating voltage: 2.4V - 3.6V
  3.6V - 5.5V
- Built-in 32.768KHz oscillator circuit for real clock function
- Built-in RC oscillator (only one resistor is needed)
- Internal time base generator
- Key wake-up mode
- Provide 7 INT sources
- Operating current: 400μA/600KHz @ 3.0V
- Very low standby current
  In standby mode: I_{STBY} < 1μA
- LCD matrix: 44 segments x 5 commons
- LCD 1/2, 1/3 bias; 1/2, 1/3, 1/4,1/5 duty
- Two 16-bit timers
- 12 general I/O pins, 8 input pins
- Provide standby function (stop osc)
- Built-in 8-bit PWM output (directly drive a speaker)

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
SEG33 - 0 SEG35 - 34	1 - 34 74 - 75	O	LCD driver segment output
COM4 - 0	35 - 39	O	LCD driver common output
IOAB7 - 0	66 - 73	I/O	I/O port or LCD driver segment 43 - 36
IOEF7 - 0	48 - 41	I	INPUT port (also for key wakeup input).
IOCD3 - 0	65 - 62	I/O	I/O port
ROSC	53	I	ROSC input, connect to VDD through resistor
RESET	57	I	System reset input
AUDP	59	O	PWM Audio output
AUDN	61	O	PWM Audio output
X32I	56	I	32.768KHz crystal input (provide LCD frequency)
X32O	55	O	32.768KHz crystal output
TEST	40	I	Test input
VDD	54, 60	I	Positive supply voltage input
VSS	58	I	Ground input
VDD1, VDD2	49, 52	I	Inputs for setting LCD bias
CUP1, CUP2	50, 51	I	Inputs for setting LCD bias

4.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

5. FUNCTIONAL DESCRIPTIONS

5.1. ROM Area

GPL30A1 is a large ROM based micro-controller with 220 dots LCD driver. The large ROM can be defined as a program ROM, LCD font and audio data continuously without any limitation. To access the ROM area, user should program the BANK SELECT register ($07) first, then access the bank #1 or bank #2 by addressing the higher bank address ($8000 - $FFFF) to fetch data.

5.2. Stop Clock Mode

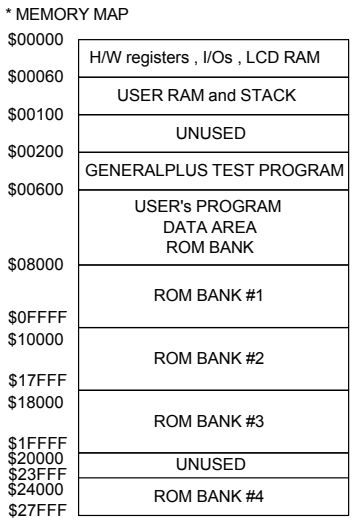
GPL30A1 supports power saving mode for those applications requiring very low standby current. User can simply enable the wake-up sources to stop the CPU clock by writing the STOP CLOCK register ($09). Thus, CPU will enter standby mode and the RAM and I/O retain in their previous state until awake. There are four sources of wake-up in this chip: PORT IOEF wake-up, TIMER 0 wake-up, 4Hz/8Hz/16Hz/32Hz wake-up and 2Hz/1Hz wake-up. After the chip is awakened, the internal CPU will go to the RESET state. The RAM and I/O are not affected by this wake-up reset.

5.3. Map of Memory and I/Os

*I/O PORT:
- PORT IOAB $0002
  IOCD $0003
  IOEF $0004
- I/O CONFIG $0000
- I/O CONFIG $001E

*NMI SOURCE:
- INT1 (from TIMER 1)

*INT SOURCE
- INT0 (from TIMER 0)
- INT1 (from TIMER 1)
- 2KHz
- LCDL (1/3, 1/4 duty 256Hz; 1/2 duty 128Hz)
- 128Hz
- EXT INT
- 2Hz



5.4. Time-Setting Register Related

The basic time base of CPU wake-up and interrupt can be changed by writing to TIME-SETTING register. For example, the programmer can change 2Hz wake-up and interrupt into 1Hz wake-up and interrupt by writing 80H into $0A. Therefore, this system will wake-up to service every second. Also, T16Hz (one of counter's clock source and wake-up & interrupt) can be one of 4Hz, 8Hz, 16Hz or 32Hz by setting bit0 and bit1 of TIME-SETTING register ($0A). At power on state, T16Hz selects 4Hz, and T2Hz chooses 2Hz.

5.5. PWM Output

Internally, GPL30A1 has two sets of PWMs (one for each channel). GPL30A1 uses Pulse Width Modulation that could directly drive speaker or buzzer without any buffer or AMP circuit.

5.6. Speech and Melody

Since GPL30A1 carries a large ROM size and wide CPU operating speed range, it is the most suitable device for speech and melody application. For speech synthesis, this chip provides INT for precise sampling frequency. Users can record or synthesize the sound and digitize it into ROM. The sound can be played back in the sequence of the control functions as designed by the internal user's program. Several algorithms are suggested to be used for high fidelity and good compression of sound: PCM, LOG PCM, DM and ADPCM. For melody synthesis, GPL30A1 features dual tone mode. Once entered into the dual tone mode, users only need to program the TM0 and TM1 to tone frequency for each channel, count the envelope of each channel, and the hardware can toggle the tone wave automatically without using INT to handle it.

5.7. LCD Controller

GPL30A1 contains a total of 220 segments LCD controller and drivers. In the power-on state, LCD display is all on state. The programmer can set the LCD status (bias, duty, normal scan) by writing to LCD option ($1F), update the LCD content by writing to LCD registers. After the power-on state, LCD option is defined only one time and then fills the LCD registers to display the desired pattern. The LCD driver is designed to fit most LCD's specifications in GPL30A1. It can either be programmed as 1/2 or 1/3 bias. The duty is also programmable from 1/2, 1/3, 1/4 or 1/5 duty.

5.8. Timer/Counter

GPL30A1 features two 16-bit timer/counters, TM0 and TM1 respectively. In the timer mode, TM0 and TM1 are reloaded up-counters. When timer overflows from $FFFF to $0000, the carry signal will generate the INT signal if the corresponding bit is enabled in INT ENABLE register ($0d), and the timer will auto reload to the user setup value and up count again. If TM0 is specified as a counter, user can reset the counter by loading 0 into register $15 and $16 and loading 0 into the counter by writing to $17. After the counter is activated, the count value can also be read from above registers ($15 and $16) on-the-fly and the read instruction will not affect the counter's value or reset it.

The clock source of the timer/counter is selected as the following:

Timer/Counter		Address	Clock Source
TM0	16-BIT TIMER	$0015 $0016 $0017	CPU CLOCK X 2, the CARRY of timer 1
	16-BIT COUNTER	$0015 $0016 $0017	Clock source 1: IOCD1, VDD, T16Hz, 128Hz Clock source 2: IOCD0, CPU CLOCK x 2, 32768Hz **Note:** T16Hz can be one of 4Hz, 8Hz, 16Hz or 32Hz by setting $0A (time-setting register)
TM1	16-BIT TIMER	$0025 $0026 $0027	CPU CLOCK X 2, 32768 Hz
MODE SELECT REGISTER		$000B	Select TM0 & TM1 configuration

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

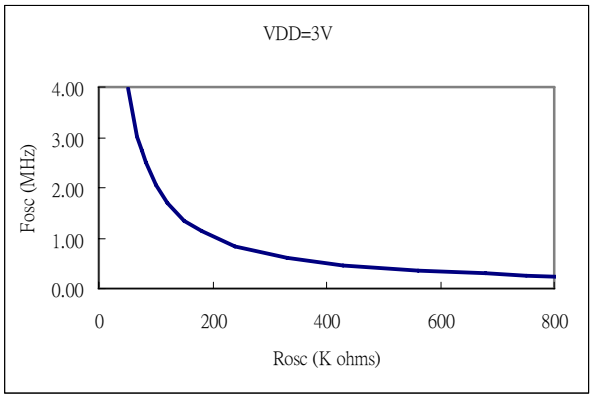
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics

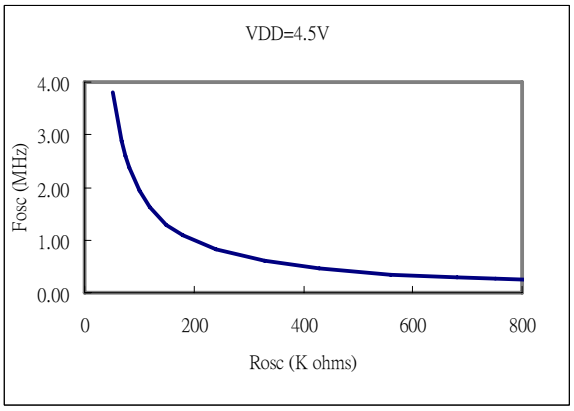
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
		3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	400	-	μA	F_{CPU} = 600KHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, 32768 Hz OFF
OSC Frequency	F_{OSC2}	-	-	4.0	MHz	VDD = 3.0V
Audio Output Current	I_{OH}	-	-16	-	mA	VDD = 3.0V
	I_{OL}	-	24	-	mA	VDD = 3.0V
Input High level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I (I/O)	I_{OH}	-200	-	-	μA	VDD = 3.0V, V_{OH} = 2.1V
Output Sink I (I/O)	I_{OL}	500	-	-	μA	VDD = 3.0V, V_{OL} = 0.9V
Input Resistor	R_{IN}	-	50K	-	Ω	For input only
OSC Resistor	R_{OSC}	-	180K	-	Ω	F_{OSC2} = 1.0MHz @ 3.0V
CPU Clock	F_{CPU}	-	-	2.0	MHz	F_{CPU} = F_{OSC2}/2 @ 3.0V

6.3. The Relationships between the R_{OSC} and the F_{OSC}

6.3.1. VDD = 3.0V, T_A = 25℃

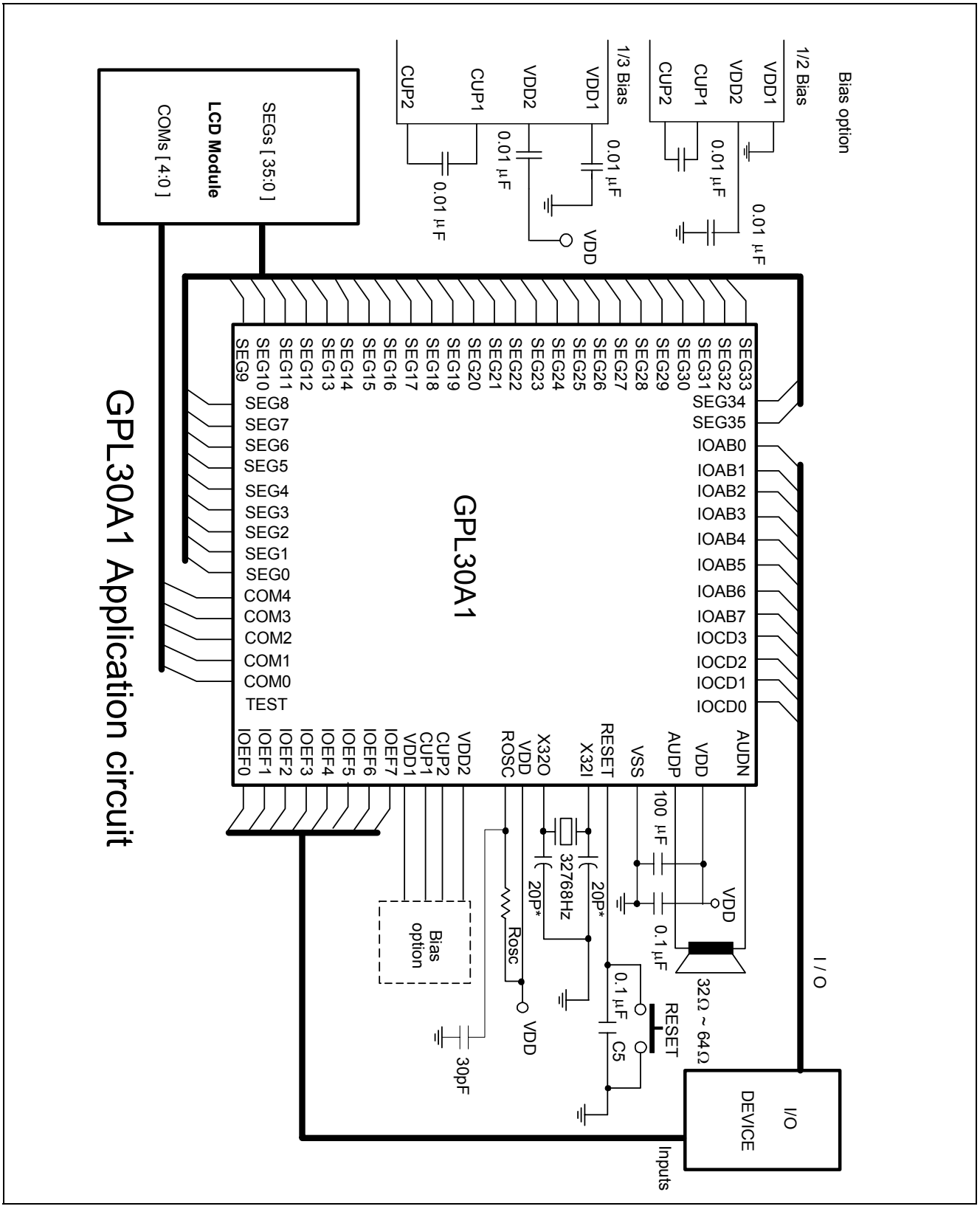


6.3.2. VDD = 4.5V, T_A = 25℃



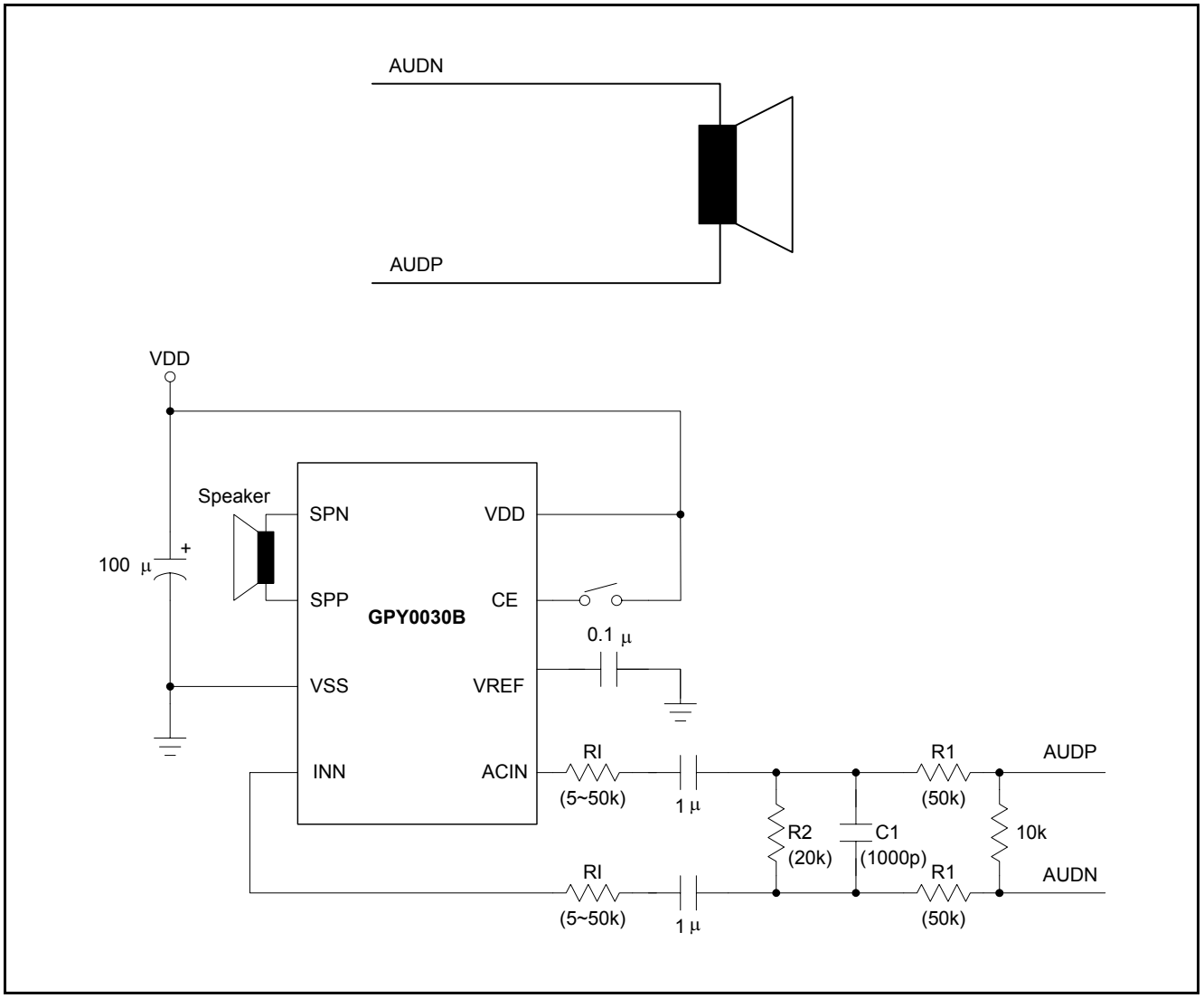
7. APPLICATION CIRCUITS

7.1. Application Circuit



Note*: These capacitor values are for design guidelines only. Different capacitor values may be required for different crystal/resonator used.

7.2. Audio Driver/Amplifier for PWM Mode



8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL30A1-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
FEB. 25, 2010	1.1	1. IOEF7-0 description modified. 2. Clock source2 “Crystal oscillator” removed.	4 7
JUN. 20, 2006	1.0	Original	10