DATA SHEET

GPL31C

160 Dots LCD Controller with 64KB ROM

Nov. 30, 2016

Version 2.0

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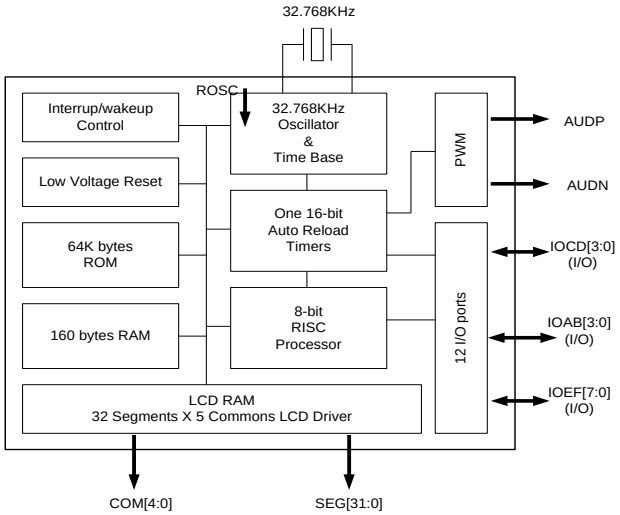
160 DOTS LCD CONTROLLER WITH 64KB ROM

1. GENERAL DESCRIPTION

The GPL31C, an 8-bit CMOS single chip microprocessor, contains RAM, ROM, I/Os, interrupt/wakeup controller, timer, 8-bit PWM audio output and automatic display controller/ driver for LCD. With a dual channel PWM driver, attractive sound effects can be generated easily. Furthermore, a software controllable standby mode is also implemented for power saving.

2. BLOCK DIAGRAM



3. FEATURES

- Built-in 8-bit CPU
  - 160 bytes SRAM
  - 64K bytes ROM
  - Max. CPU clock: 2.0MHz @ 2.0V – 5.5V
  - Programmable CPU clock frequency, 1/2, 1/4, 1/8, 1/16, 1/32 or 1/64 of R-oscillator's clock frequency is available
  - R-oscillator's clock frequency can be set to 3.0MHz or 4.0MHz (mask option)
  - Provides 7 interrupt sources
- Built-in 8-bit 1-channel PWM outputs
- Built-in 32.768KHz Crystal / R-oscillator
  - Crystal or R-oscillator (mask option)
  - Crystal oscillator switches from strong to Weak mode automatically
  - Internal time base generator
- Built-in System R-oscillator
  - No resistor is needed
- One 16-bit timer/counters
- Low Voltage Reset
  - Provides 1.9V low voltage reset function
- Low power consumption
  - Operating current: 500uA/1.0MHz @ 3.0V
  - Very low standby current : ISTBY < 1.0μA @ 3.0V
    In standby mode: stop all oscillators
- Max. 16 general purpose I/O
  - SEG[31:28] can be optioned to IOAB[0:3]
  - 8 IO pins IOEF[7:0] support Key wake-up mode
- LCD controller / driver
  - 32 segments x 5 commons, max. 160 dots
  - LCD bias: 1/3
  - LCD duty: 1/3,1/4,1/5

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
SEG[31 : 28] / IOAB[0 : 3] SEG[27 : 0]	33-36, 37-59, 1-5	O	LCD driver segment output. Can also be optioned to IOAB[0:3] LCD driver segment output
COM[4 : 0]	6-10	O	LCD driver common output
IOEF[7 : 0]	31-24	I/O	I/O port (provide key wake-up function)
IOCD[3 : 0]	23-20	I/O	I/O port
RESETB	11	I	System reset input
AVDD	18	P	PWM power supply input
AUDP	19	O	PWM audio output
AUDN	16	O	PWM audio output
AVSS	17	P	PWM ground input
X32I	13	I	32.768KHz crystal input, or connect to VDD through resistor as R-oscillator input (Mask option)
X32O	12	O	32.768KHz crystal output
TEST	14	I	Test mode input
VDD	32	P	Power supply voltage input
VSS	15	P	Ground input

Total: 59 pins

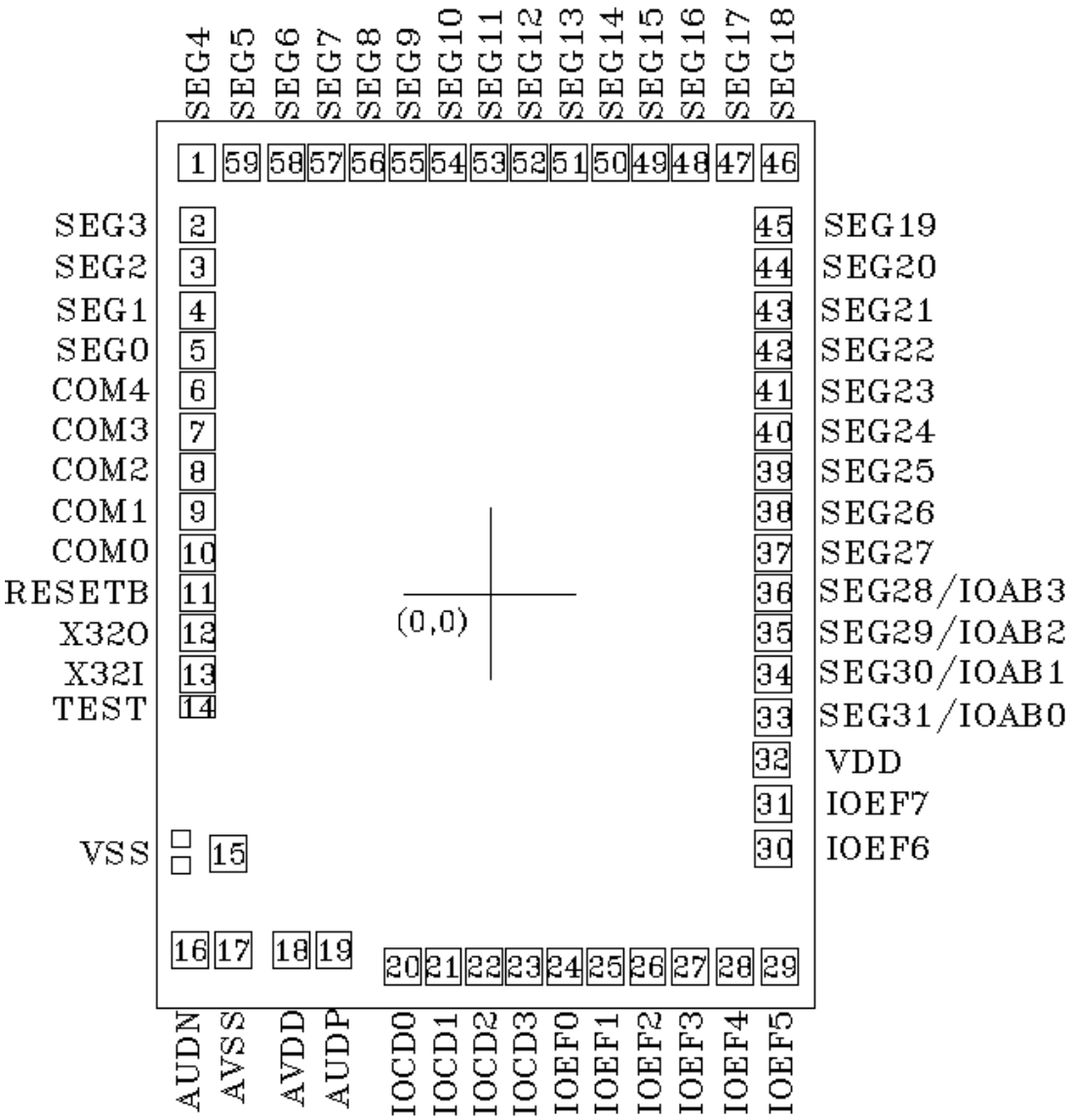
Note1: Legend: I = Input, O = Output, P = Power

Note2: SEG[31:28]/IOAB[0:3] can be optioned to IOAB[0:3] or SEG[31:28] separately

Note3: Provides 160 bits read/writable LCD RAM buffer.

Note4: 32.768KHz Crystal oscillator can be optioned to R-oscillator (connected to VDD through resistor).

4.1. PAD Assignment



This IC substrate should be connected to VSS or floated

Note1: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

5. FUNCTIONAL DESCRIPTIONS

5.1. Map of Memory and I/Os

*I/O PORT:
- IOCD Port $0004
- IOEF Port $0005
- IOAB Port $0003

* I/O CONFIG
- IOCD_Config $0000
- IOEF_Config $0006
- IOAB_Config $001E

* NMI SOURCE:
- INT1 (from TIMER 1)

* INT SOURCE
- INT0 (from TIMER 0)
- INT1 (from TIMER 1)
- T16Hz (4Hz /8Hz /16Hz /32Hz)
- T2Hz (2Hz /1Hz)
- 128Hz
- 2KHz
- EXTINT (from IOCD1 pin)

* WAKEUP SOURCE
- IOEF Port Change
- TIMER 0 Overflow
- T16Hz (4Hz /8Hz /16Hz /32Hz)
- T2 Hz (2Hz /1Hz)

* MEMORY MAP

$0000	I/O & Registers
$001F	
$0020	LCD RAM Buffer
$003B	
	reserved
$0060	SRAM
$00FF	
	reserved
$0200	Test Program
$05FF	
$0600	Program ROM Bank #0
$7FFA	
$7FFF	NMI/Reset/IRQ Vector
	Program ROM Bank #1
$FFFA	
$FFFF	NMI/Reset/IRQ Vector

5.2. ROM Area

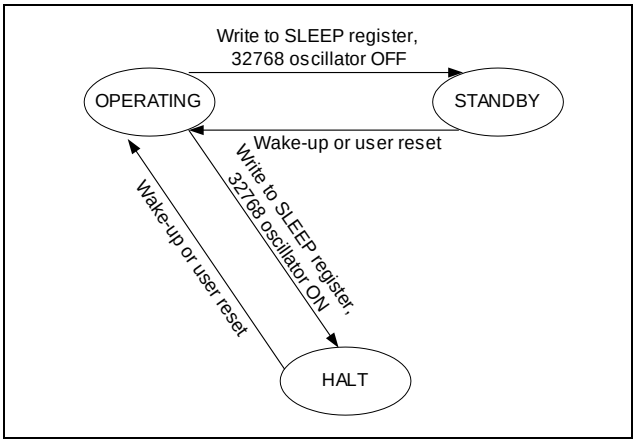
GPL31C is a ROM based micro-controller with 160 dots LCD driver. The large ROM space can be defined as a program ROM, LCD font and audio data continuously without any limitation. To access the higher bank ROM area, it is allowed to program the BANK SELECT register ($07) to 1 and then fetch the data from address $8000 to $FFFF.

5.3. Operating States

The GPL31C provides three operating states: standby, halt, and operating state. Following table shows the differences between these three states.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768 oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

In operating mode, all modules (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated. The halt/standby state is entered by writing the SLEEP register ($09). There are four wake-up sources in GPL31C: port IOEF wake-up, TIMR0 wake-up, 4Hz/8Hz/ 16Hz/32Hz wake-up and 2Hz/1Hz wake-up. If any wake-up event occurs, execution of the next instruction continues in the operating state. In standby mode, all modules will be shut down, and RAM and I/Os remain in their previous states. Therefore current consumption is minimized. By writing to SLEEP register but keeps 32768 oscillator running, the system is in HALT state. CPU clock is halted while it waits for an event (key press, timer overflow) to generate a wake-up in HALT state. The 32768 related modules (timer/counter, LCD driver…) may remain active in the halt state. Following figure is a state diagram for the GPL31C.



State Diagram of GPL31C

After the chip is awaken from halt/standby state, CPU will continue to execute the next instruction. The RAM and I/O status will not be changed by wake-up.

5.4. Time-Base-Setting Register

Writing to TIME-SETTING register can program the time source of CPU wake-up and interrupt. For example, the programmer can change 2Hz wake-up and interrupt into 1Hz wake-up and interrupt by writing 80H into $0A.

Thus, the system awakes every second to operate services. Also, T16Hz (one of counter's clock source and wake-up & interrupt) can be one of 4Hz, 8Hz, 16Hz or 32Hz, selected by bit0 and bit1 of TIME-SETTING register ($0A). At power on state, the default value of T16Hz is 4Hz and T2Hz is 2Hz.

5.5. Timer/Counter

GPL31C contains one 16-bit timer/counters TM0. In the timer mode, TM0 is a reloadable up-counter. When the timer overflows from $FFFF to $0000, the carry signal will generate the INT signal if the corresponding bit is enabled in INT ENABLE register ($0D). The timer will automatically reload the value assigned by the program and up count continuously. If TM0 is specified as a counter, the user can reset the counter by loading 0 into register $10 and $11 and loading 0 into the counter by writing any data to $12. After the counter is activated, the counter's value can also be read from above registers ($10 and $11) and the read instruction will not neither affect the counter's value nor reset it.

The clock sources of the timer/counter are selected as the following:

Timer/Counter		Address	Clock Source
TM0	16-BIT Timer	$0010 $0011 $0012	R-oscillator Output
	16-BIT Counter	$0010 $0011 $0012	Clock source A: IOCD0, R-oscillator Output, VDD, 32768Hz. Clock source B: IOCD1, VDD, T16Hz, 128Hz. **Note:** T16Hz can be one of 4Hz, 8Hz, 16Hz and 32Hz by setting $0A (time-setting register)

5.6. Speech and Melody

Since GPL31C features a large ROM size and wide CPU operating speed, it is suitable for speech and melody synthesis. For speech synthesis, it offers INT for precise sampling frequency. Users can record or synthesize the sound and digitize the data into the ROM. The sound can be played back in the sequence designed by the internal user's program. Some algorithms are recommended for high fidelity and good compression of sound, e.g. PCM and ADPCM. For melody synthesis, GPL31C provides tone mode. Once in the tone mode, users only need to program the tone frequency of each channel by writing to timer/counter TM0, and set the channel envelope. The hardware will toggle the tone wave automatically.

5.7. LCD Controller/Driver

GPL31C contains a LCD controller and driver for 160 dots display. Users can set the LCD configuration (display mode) by writing LCD control register ($18). Once the LCD configuration is initialized, the designated pattern can be displayed by filling the LCD buffer with appropriate data. The LCD driver can still operate during halt mode by keeping 32768Hz oscillator running. Furthermore, programmer can turn off the LCD display through LCD control register for power savings. The LCD driver in GPL31C is designed to fit LCD panel for 1/3 bias 1/3,1/4 and 1/5 duty.

5.8. PWM Output

Internally, GPL31C has one pair of PWM outputs supporting one sound channel. The sound channel is selectable to play speech or tone. GPL31C uses Pulse Width Modulation (PWM) that is able to drive speaker or buzzer directly without any buffer or amplification circuit.

5.9. Low Voltage Reset

The GPL31C provides a low voltage reset function. The system will enter into LVRST state if and only if the power supply voltage VDD drops lower than 1.9V.

5.10. Watchdog Timer (WDT)

An on-chip watchdog timer is available on GPL31C. The WDT is designed for recovering from system abnormal operation. If the system is hanged, WDT will generate a system reset to restart system after 1 second. If WDT is enabled, the WDT should be cleared every two seconds to avoid accidental reset. The WDT can be cleared by writing the specified value 0FH to port $0F. Note that the WDT only works when 32768Hz clock is available.

5.11. Mask Options

5.11.1. 32768 crystal oscillator

1). X'TAL
2). R-oscillator

5.11.2 Built-in R-oscillator clock frequency

Can be optioned to 3.0MHz or 4.0MHz

5.11.3 SEG[31:28] Can be Optioned to IOAB[0:3]

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (VDD = 3.0V, T_A = 25℃)

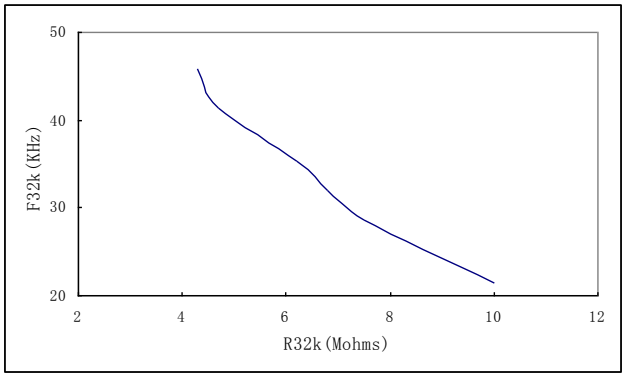
Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.0	-	3.6	V	For 2-battery application
Operating Current	I_{OP}	-	500	-	uA	VDD = 3.0V, F_{CPU} = 1MHz
Halt Current	Ihalt1	-	10	-	uA	VDD = 3.0V, LCD ON, Maximum VLCD level
	Ihalt2	-	2	-	uA	VDD = 3.0V, LCD OFF
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V
Audio Output Current	I_{OH}	-	-30	-	mA	VDD = 3.0V, V_{OH} = 2.4V
		-	-50	-		VDD = 3.0V, V_{OH} = 2.0V
	I_{OL}	-	15	-	mA	VDD = 3.0V, V_{OL} = 0.6V
		-	25	-		VDD = 3.0V, V_{OL} = 1.0V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I	I_{OH}	-	-2.0	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink I	I_{OL}	-	2.5	-	mA	VDD = 3.0V, V_{OL} = 0.8V

6.3. DC Characteristics (VDD = 4.5V, T_A = 25℃)

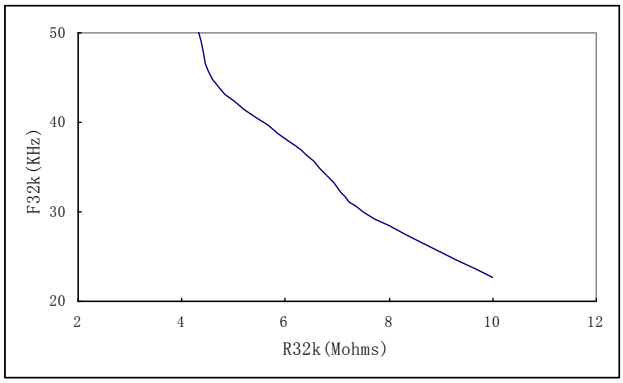
Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery application
Operating Current	I_{OP}	-	1100	-	uA	VDD = 4.5V, F_{CPU} = 1MHz
Halt Current	Ihalt1	-	30	-	uA	VDD = 3.0V, LCD ON, Maximum VLCD level
	Ihalt2	-	5	-	uA	VDD = 3.0V, LCD OFF
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 4.5V
Audio Output Current	I_{OH}	-	-50	-	mA	VDD = 4.5V, V_{OH} = 3.6V
	I_{OL}	-	25	-	mA	VDD = 4.5V, V_{OL} = 0.9V
Input High Level	V_{IH}	3.0	-	-	V	VDD = 4.5V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 4.5V
Output High I	I_{OH}	-	-4.5	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I	I_{OL}	-	3.5	-	mA	VDD = 4.5V, V_{OL} = 0.8V

6.4. The Relationships between the R_{32K} and the F_{32K}

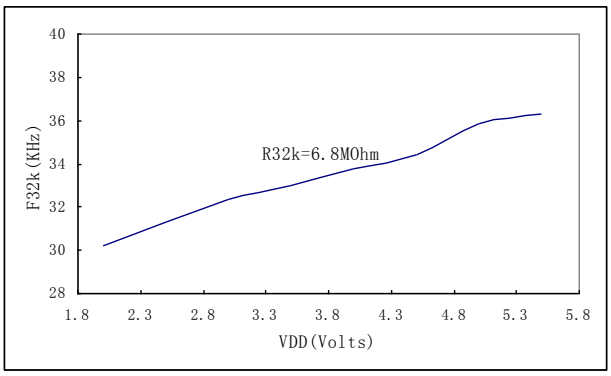
6.4.1. VDD = 3.0V, T_A = 25℃



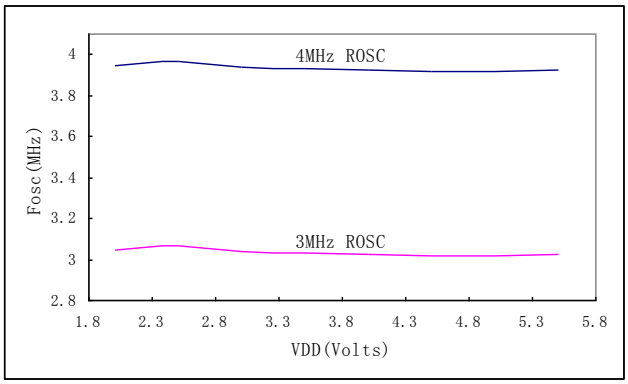
6.4.2. VDD = 4.5V, T_A = 25℃



6.5. The Relationships between the VDD and the F_{32k}

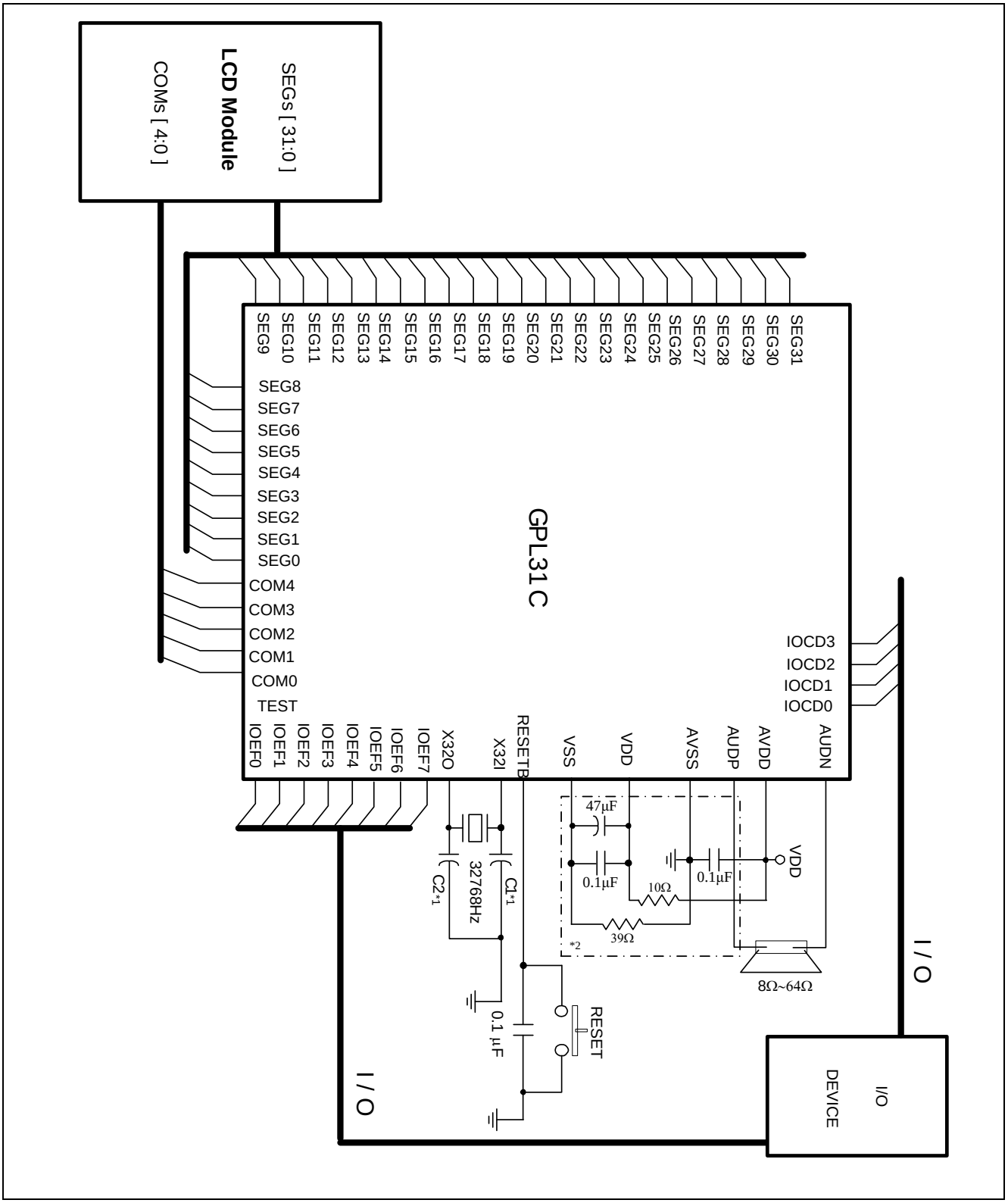


6.6. The Relationships between the VDD and the F_{OSC}



7. APPLICATION CIRCUITS

7.1. 160 dots LCD driver, 32 segments x 5 commons, 32kHz X'tal oscillator, with PWM audio- (1)

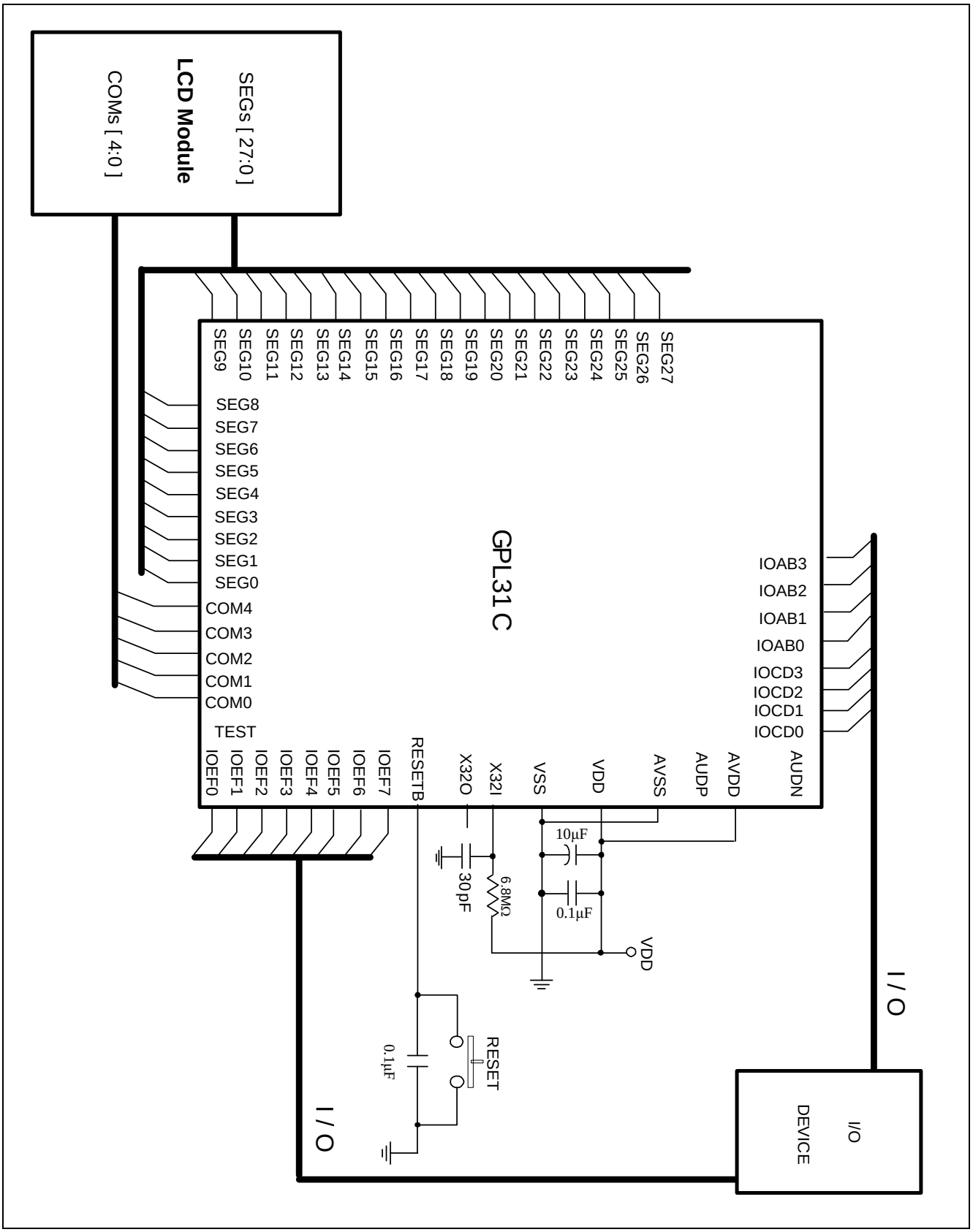


Note

***1:** C1/C2 values in above application circuit are for design guidance only. Different capacitor values may be required for different crystal used. Usually, the values of C1/C2 are in the range 12 ~ 20pF.

***2:** see 'GPL31C PWM side-effect APN' for details.

7.2. 145 dots LCD driver, 29 segments x 5 commons, 32kHz R-oscillator, SEG[31:28] as IOAB[0:3] , without PWM audio- (2)



8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL31C-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

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10. REVISION HISTORY

Date	Revision #	Description	Page
NOV. 30, 2016	2.0	1. Modified 3. Features : LCD duty description. 2. Modified 5.7 LCD controller/driver : LCD duty description. 3. Modified 6.2, 6.3 : Audio Output Current	3 7 8
MAR. 18, 2010	1.2	1. Modified 5.1. Map of Memory and I/Os. 2. Modified 7. APPLICATION CIRCUITS.	6 10-11
MAR. 27, 2009	1.1	1. Modified Data sheet name. 2. Add relationship waveform for frequency at section 6.4, 6.5 & 6.6. 3. Modified Application circuit at section 7.2, add “6.8MΩ“ resistor description.	1 9 11
NOV. 05, 2008	1.0	1.Modified Features 2.Modified Signal descriptions 3. Add “PAD Assignment” to section 4.1 4.Modified DC characteristics 5.Modified Application circuit, RESET -> RESETB	3 4 5 8 9
JUN. 07, 2007	0.1	Original	12