DATA SHEET

GPL811P08A
GPL811P04A

Low Power 660 Dots LCD Controller with 64KB/32KB OTP Rom

Sep. 11, 2013

Version 1.2

Table of Contents

PAGE

LOW POWER 660 DOTS LCD CONTROLLER WITH 64KB/32KB OTP ROM

1. GENERAL DESCRIPTION

GPL811P08A/GPL811P04A, a special designed CMOS 8-bit microprocessor by Generalplus, offers the best cost/performance ratio in the industry. It combines RAM, one-time programmable (OTP) ROM, I/Os, an interrupt controller, and an automatic display controller/driver in a small device. Its extraordinary features is the capability of operating in low voltage range from 2.2V ~ 3.6V and also operating under low power. This device is capable for many application fields such as low power watch and other LCD related products.

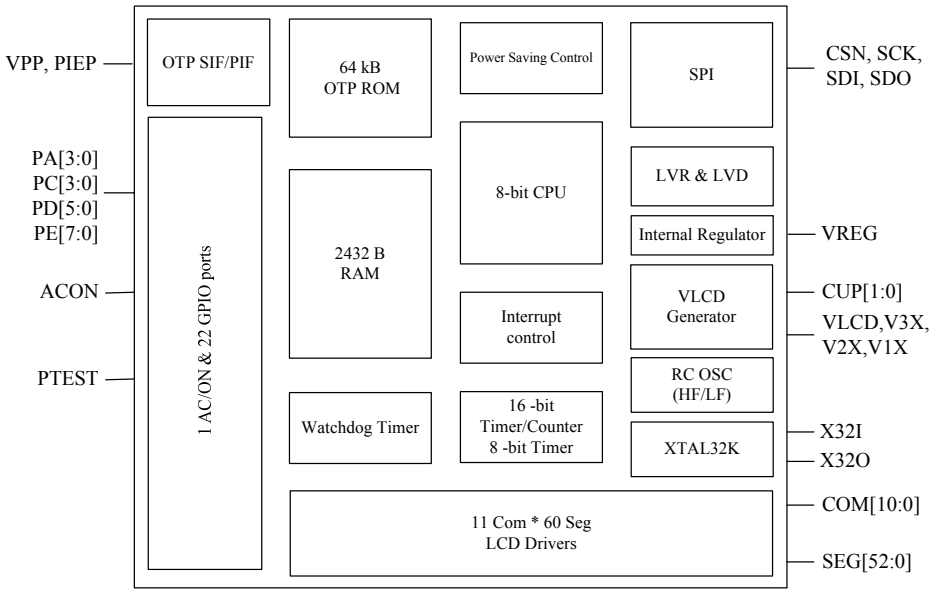
2. FEATURES

- Built-in 8-bit processor
- 2432-byte SRAM
- 64K-byte OTP ROM(GPL811P08A)
  32K-byte OTP ROM(GPL811P04A)
- 88 byte DPRAM
- Built-in 225k/500k/1000k/1800kHz RC oscillator for system operation
  - adjustable CPU clock speed : 1, 1/2, 1/4, 1/8, 1/16 for R_{OSC}
- Built-in 30.72kHz RC oscillator & 32768 Crystal oscillator circuit for timebase
- Low standby current, ISTBY < 1uA @3.6V, 25℃
- 22 general I/O pins.
  - PD[5:0](PD[5:3] shared with SEG[57:59]; PD[1:0] shared with 2 buzzers)
  - PC[3:0](shared with SEG[53:56])
  - PA[3:0](shared with SPI SDO/SDI/SCK/CSN pin
  - PE[7:0]
  - Built-in 2 x RFC function (PD2 used as input, PD[5:3] used as output)
- Serial Peripheral Interface(SPI)
  - CSN/SCK/SDI/SDO pin shared with PA[0:3]
- LCD configurations: 11 coms x 60 segs (MAX) , 3x60, 4x60, 5x60, 6x60, 8x60, 9x60, 10x60, 4x64
- LCD 1/3 ,1/4 bias; 1/3, 1/4, 1/5, 1/6, 1/8, 1/9, 1/10, 1/11 duty
- One 16-bit reloadable timer/counter(Timer0), one 8-bit reloadable timer/counter(Timer1)
- Watchdog mode (~2 sec)
- 9 interrupt sources
  (TMBB, TMBA, 128Hz, 2KHz, Timer0, Timer1, EXT(PD2), SPI, LVD(2.0V/2.2V/2.4V/2.6V))
- Power down mode
  (wake-up source: key input, TMBB, TMBA, 128Hz, Timer0)
- Low power consumption:
  - 200u @ 3.6V, F_{CPU} = 225KHz for operating mode
  - 3u@ 3.6V, F_{CPU} = 225KHz for halt mode
  - I stby < 1uA @ 3.0V
- Built_in internal regulator for LCD operation, 5-level contrast control
- Built_in Low voltage reset to avoid system runaway at low voltage

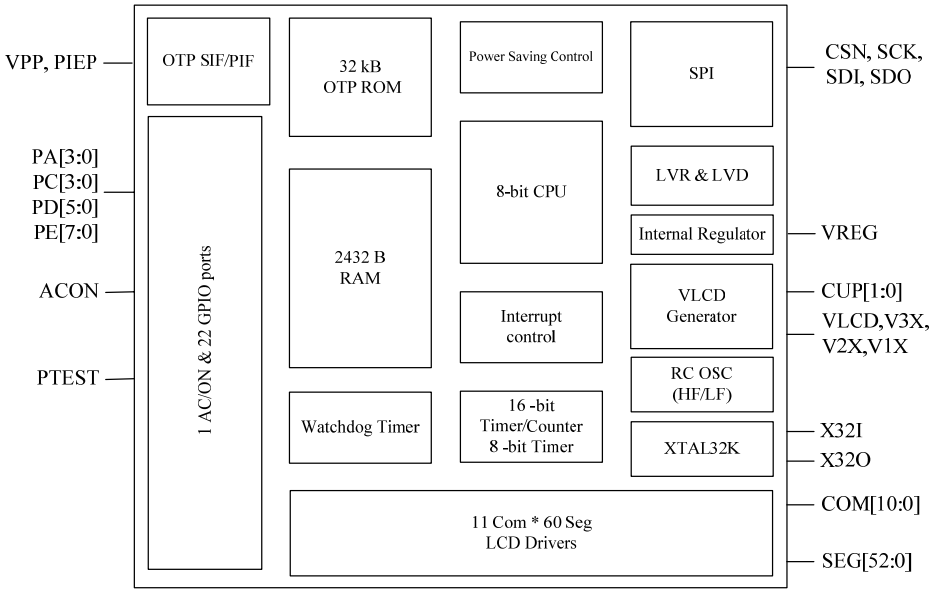
Note1: TMBB: 4KHz, 1KHz, 128Hz, 64Hz, 32Hz, 16Hz, 8Hz or 4Hz
Note2: TMBA: 2Hz or 1Hz

3. BLOCK DIAGRAM

3.1. GPL811P08A



3.2. GPL811P04A



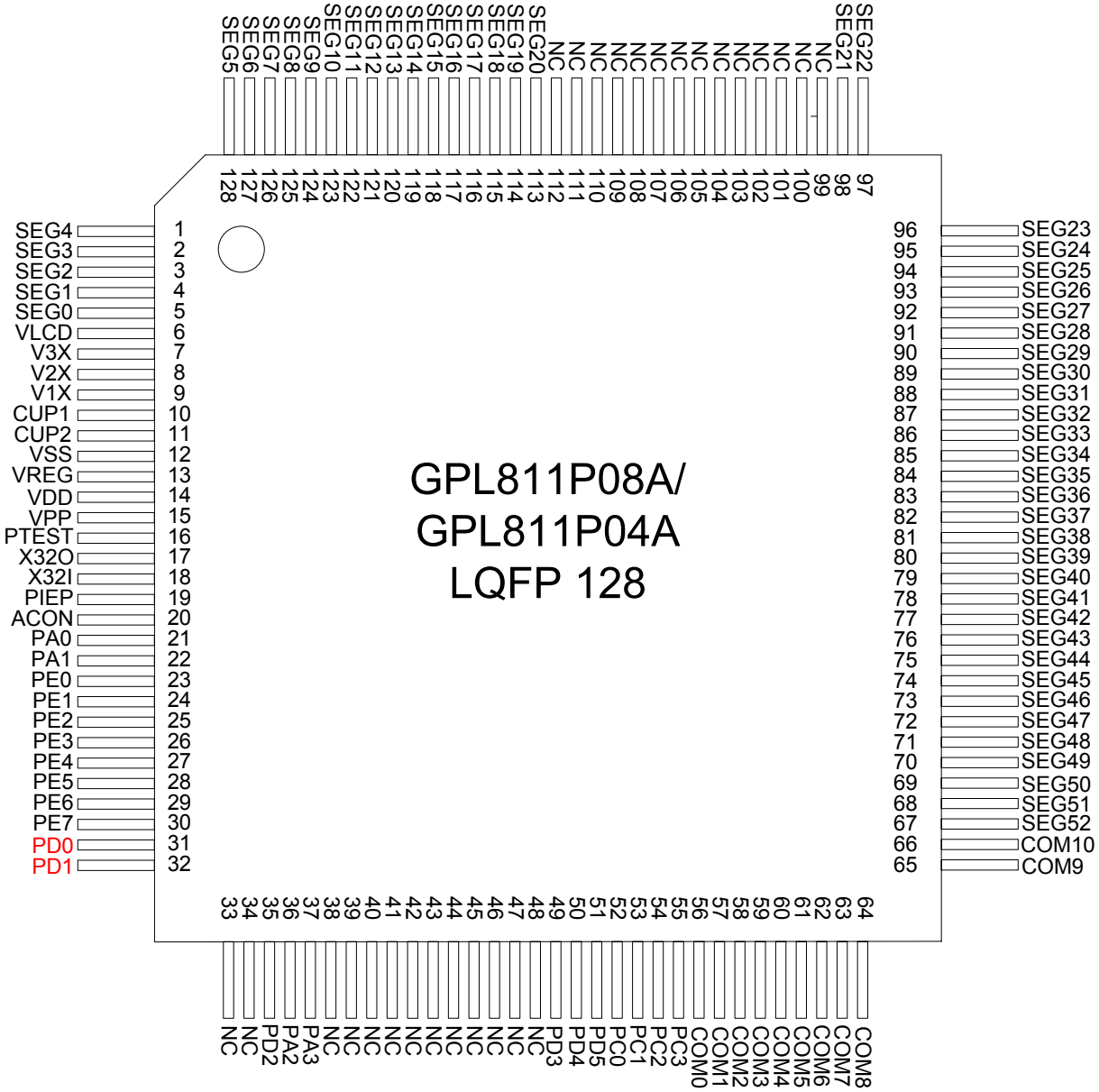
4. SIGNAL DESCRIPTIONS

4.1. PIN Description

Mnemonic	Type	Description
VDD	O	Power input
VSS	I	Ground input
VREG	O	Internal regulator output.
COM[2:0]	O	LCD driver common output
COM[10:3]	O	LCD driver common output. (COM[10:4] can be option to SEG[57:63];COM3 can be option to SEG56)
SEG[52:0]	O	LCD driver segment output
PD[5:0]	I/O	GPIO I/O port. (PD[5:3] shared with SEG[57:59]; PD[1:0] shared with 2 buzzers) In RFC application, PD[5:3]is used as pass-through (output) pin and connected to sensor. PD2 used as input-floating pin and connected to sensor & capacitor.
PC[3:0]	I/O	GPIO I/O port (shared with SEG[53:56])
PE[7:0]	I/O	GPIO I/O port
PA[3:0]	I/O	GPIO I/O port (PA[0:3] shared with SPI CSN/CLK/SDI/SDO pin)
PIEP	I	OTP programming interface enable
ACON	I	Clear or system power on pin (active low) and 4ms de-bounce circuit inside
VPP	P	OTP programming power. Should left floating or connect to VSS in normal operating mode
PTEST	I	Test mode input pin (active high)
X32I	I	32768Hz crystal input
X32O	O	32768Hz crystal output
V1X V2X V3X VLCD	O	VLCD generator output
CUP1 CUP2	I	Inputs for setting LCD bias

101pin

4.2. PIN Map(128 pin LQFP)



5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The 8-bit microprocessor in GPL811P08A/GPL811P04A is a high performance processor equipped with Accumulator, Program Counter, X Register, Y Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure).

5.2. Clock Source

The GPL811P08A/GPL811P04A equips with two groups of clock sources:

(1) High speed frequency (RCHF) to support the whole system operation. It offers four frequency options: 225k/ 500k/ 1000k/ 1800kHz and can be selected by register $18H that rely on user different application. GPL811P08A/GPL811P04A provides programmable CPU clock speed 1, 1/2, 1/4, 1/8, or 1/16 of RCHF for power saving.

(2) Low speed frequency to control LCD frame rate and time base timer. It comes from XTAL32K or IOSC30K selected by mask option.

5.3. ROM/RAM Area

The GPL811P08A/GPL811P04A features 64K-byte ROM that can be defined as the program area and its address located from $4000 to $FFFF. Its RAM consists of 2432 bytes (including Stack) at locations from $60 through $9DF.

5.4. Stop Clock Mode

The GPL811P08A/GPL811P04A provides a power saving mode for those applications required very low stand-by current. Users can simply enable the wake-up sources to stop the CPU clock by writing the STOP CLOCK Register ($09). By doing that, CPU will go to standby mode and the RAM and I/Os remain in their previous states until awake. There are five wake-up sources in the GPL811P08A/GPL811P04A: Port PortE wake-up, TMBB, TMBA, T128Hz or Timer0 wake-up. After the GPL811P08A/GPL811P04A wakes up, CPU will go to the next state where CPU enters sleep mode. Wake-up action will not influence RAM and I/Os.

Note1: TMBB: 4KHz, 1KHz, 128Hz, 64Hz, 32Hz, 16Hz, 8Hz or 4Hz
Note2: TMBA: 2Hz or 1Hz

5.5. I/O Ports

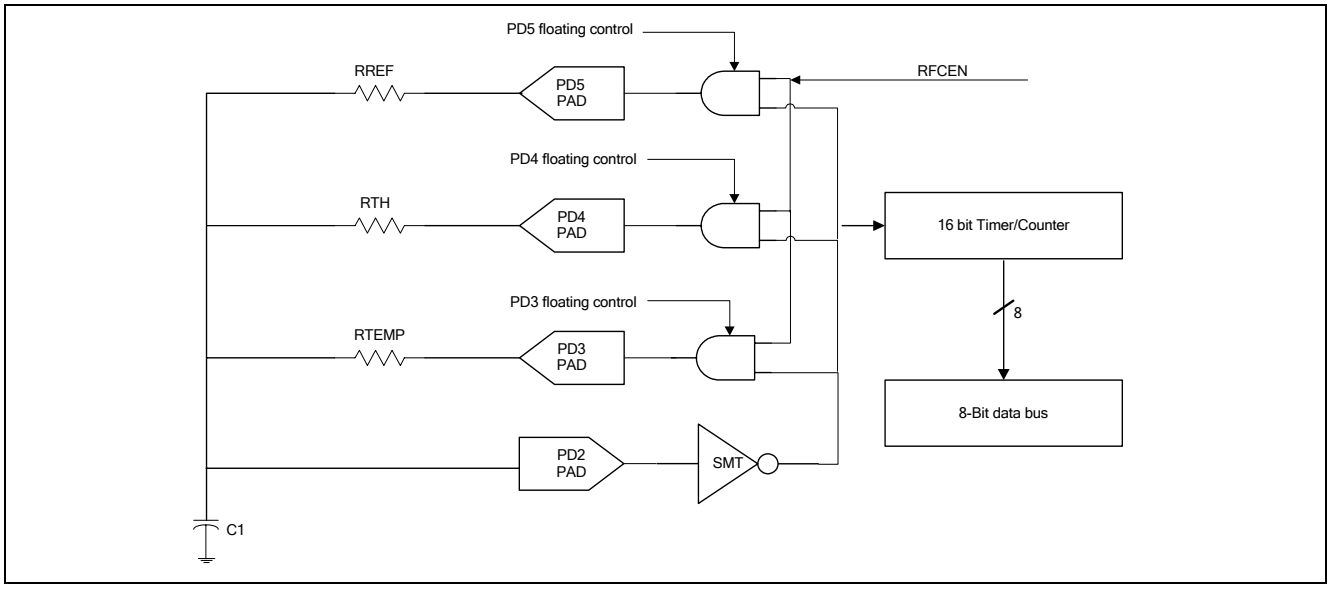
The GPL811P08A/GPL811P04A has four ports: PortA, PortC, PortD, and PortE. These port pins all equip with special features for key board scan. In general, when an initial reset starts, all ports are used as a general purpose input port. All PortA, PortC, PortD, and PortE contain three parts: data, direction and attribution registers. Programmer should follow the table below to define each I/O function with corresponding bit in each port.

PortA[3:0], PortC[3:0], PortD[5:0] , PortE[7:0]

Attribution	Direction	Data	Function	Description
0	0	0	Input with pull-low	General Purpose I/O function
0	0	1	Pure Input	
0	1	0	Output Low	
0	1	1	Output High	
1	1	0	Pad Floating	Special function

5.6. RFC Function

The RFC (Resistor to Frequency Converter) circuit contains a RC oscillation circuit and a 16-bit timer/counter to calculate the resistance of temperature or humidity sensor relative to referenced resistor. The circuit is shown below.



5.7. LCD Controller

GPL811P08A/GPL811P04A contains a LCD controller/driver that provides the capability to drive 11 commons and 60 segments LCD. To light the overhead of CPU, a display buffer is designed for mapping to LCD. A LCD dot/pattern is set ON or OFF by programming the corresponding bit of the display buffer. In addition, the LCD bias can be programmed as 1/3 or 1/4. The duty can be selected as 1/3, 1/4, 1/5, 1/6, 1/8, 1/9, 1/10 or 1/11. The frame rate is set to 71Hz at 1/9 duty, 77Hz at 1/10 or 1/5 duty, and 70Hz at 1/11 duty. When 1/3, 1/4, 1/6 or 1/8 duty is selected, its frame rate is set to 80Hz. The frame rate is measured when low speed frequency is 30.72KHz.

5.8. LCD Voltage Generation

The GPL811P08A/GPL811P04A offers a voltage regulator and a charge-pumping circuit. The voltage regulator provides a reference voltage V1X for the charge-pumping circuit to generate V2X, V3X and VLCD. Users can get the desired VLCD by changing the output reference voltage (writing to register) of the voltage regulator. Enabling the voltage regulator and charge-pumping circuit gets a stable VLCD that will not be affected by VDD. The VLCD is adjustable from 3V to 4.5V with 5 levels at 1/3bias, or 4.0V to 6.0V with 5 levels at 1/4bias.

5.9. Buzzer Driver

PD[1:0] can be used as buzzer output. When $16.b1 = b0 = '1', PD.1 and PD.0 are set for buzzer output. Or else when b1 = b0 = '0', PD.1 and PD.0 are set to normal I/O. When counter overflows, it will toggle PD.1 and PD.0 for driving buzzer.

5.10. Auxiliary Calculation Hardware

GPL811P08A/GPL811P04A contains auxiliary calculation hardware. This hardware allows some nibble operation to accomplish only at one store and load instruction. The original data content should be stored at the register ($50, $51) firstly and then many decimal operations, e.g. x10,/10 or nibble swap, can be gotten just by executing reading instruction at the relative register ($52~5F). It speeds up many decimal operations that originally need many instructions for one operation.

5.11. Analog Block

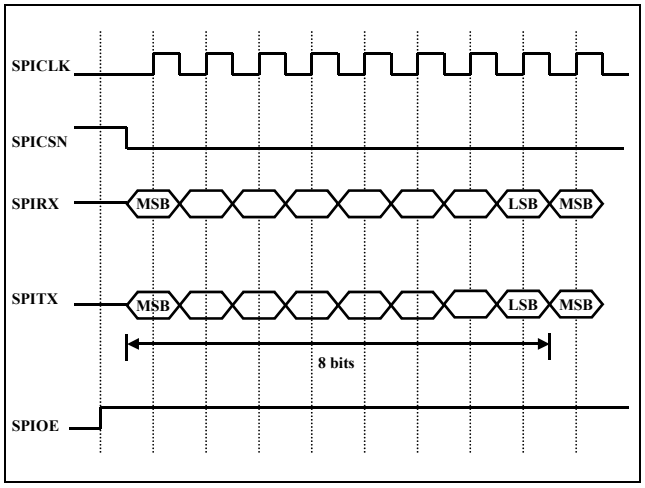
In addition to the LCD controller and clock source, GPL811P08A/GPL811P04A also provides many low power and useful analog blocks.

1.5V internal regulator by register provides whole system operation at low current environment.

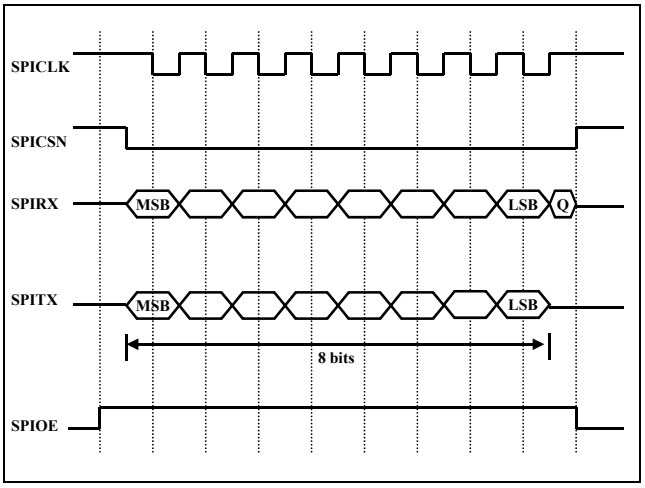
Internal low voltage reset analog block prevents system from abnormality at the voltage lower than the operation range.

5.12. SPI Controller

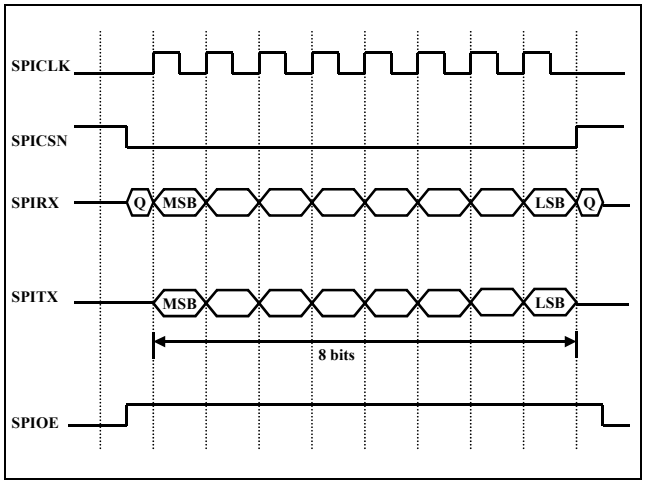
A Serial Peripheral Interface (SPI) controller is built in GPL811P08A/GPL811P04A to facilitate communicating with other devices and components. There are four control signals on SPI including SPICSN, SPICLK (SCK), SPIRX (SDI), and SPITX (SDO); the four signals are shared with PA0, PA1, PA2 and PA3. While SPI module is enabled by corresponding control bit. These four pins cannot be IO and any setting on corresponding GPIO control register will have no effect. Four types of timing are supported as follows:



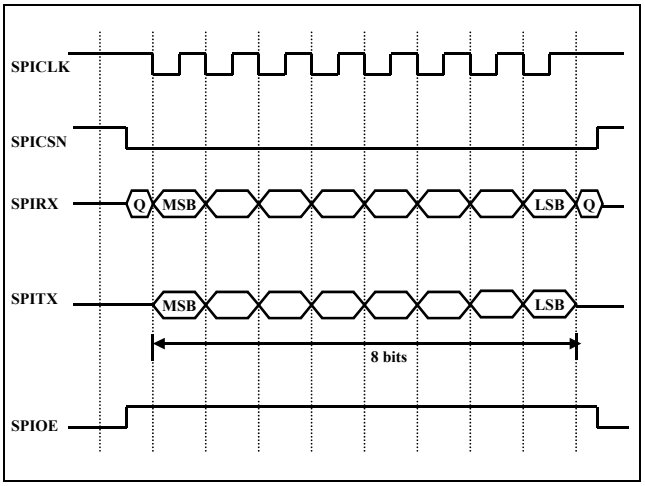
Master Mode, SPO = 0, SPH=0



Master Mode, SPO = 1, SPH=0



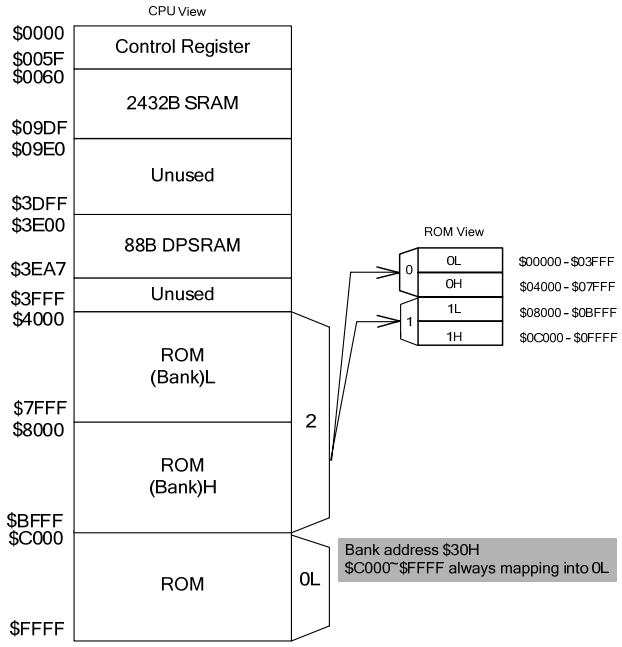
Master Mode, SPO = 0, SPH=1



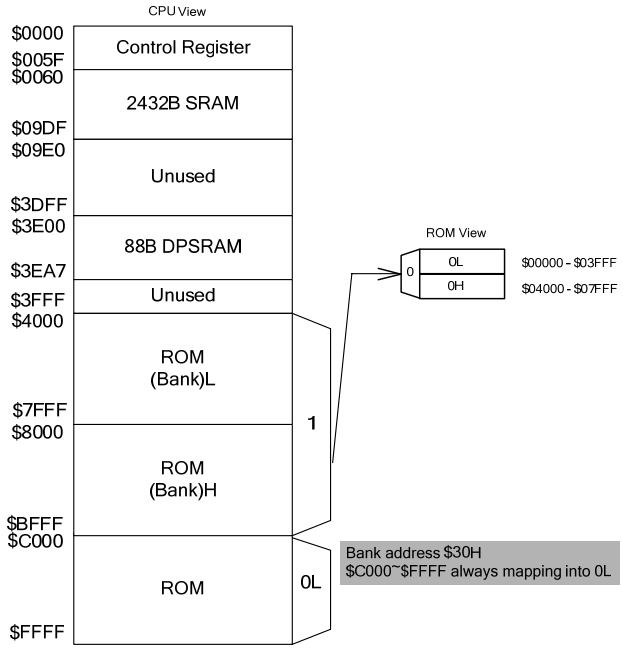
Master Mode, SPO = 1, SPH=1

5.13. Map of Memory

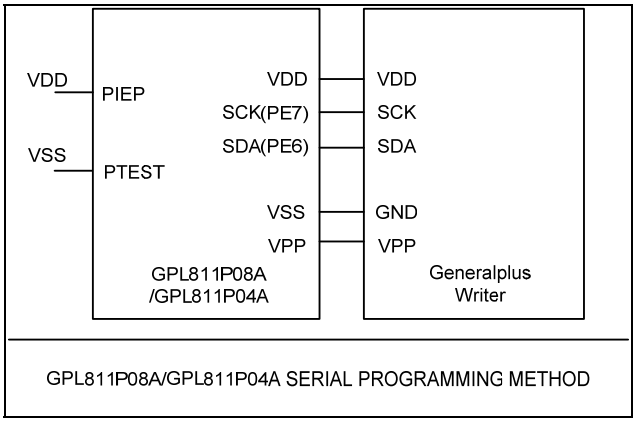
5.13.1. GPL811P08A



5.13.2. GPL811P04A



5.14. OTP Programming Circuit



Note1: Don't connect any component with PE7 and PE6 when programming.

Note2: Connect PIEP to VDD during OTP programming cycle, and keep it floating in normal run.

Note3: Connect VPP to Writer during OTP programming cycle, and keep it floating in normal run.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3~5 V
Input Voltage Range	V_{IN}	-0.3V to V_+ + 0.3V
Operating Temperature	T_{OPR}	-20℃ to +70℃
Storage Temperature	T_{STG}	-40℃ to +125℃

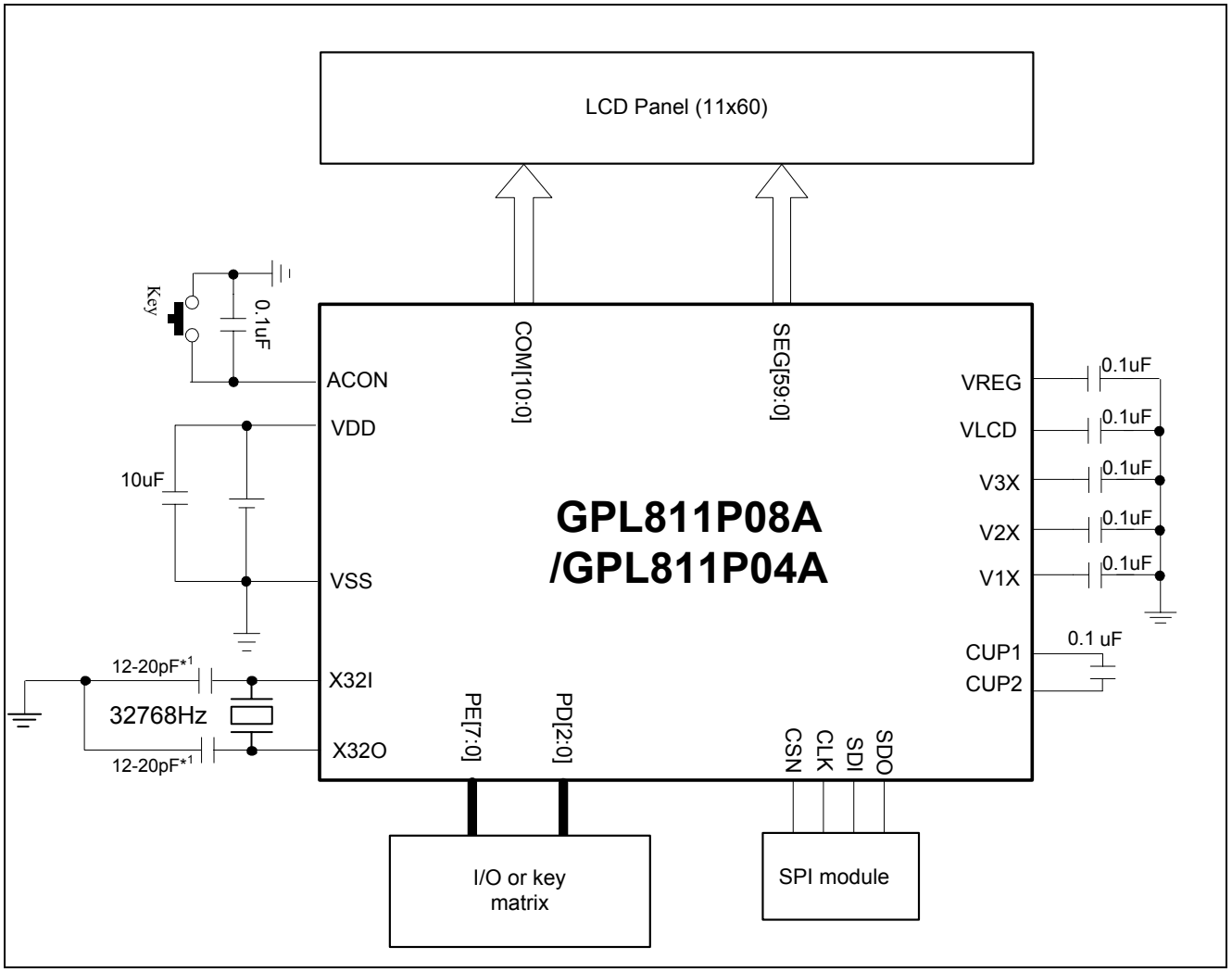
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics(T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Terminal	Test Condition
		Min.	Typ.	Max.			
Operating Voltage	VCC	2.2	-	3.6	V	VDDSW	
Input High Level	V_{IH}	Vdd*0.7	-	Vdd	V	PA,PC, PD,PE	
Input Low Level	V_{IL}	-	-	Vdd*0.3	V		
Output High Current (I/O)	I_{OH}	2	-	-	mA	PA,PC, PD,PE	Vdd = 3.0V, V_{OH} = 0.7*Vdd
Output Sink Current (I/O)	I_{OL}	4	-	-	mA		Vdd = 3.0V, V_{OL} = 0.3*Vdd
Output High Current (Buzzer)	I_{OH}	8	-	-	mA	PD[1:0]	Vdd = 3.0V, V_{OH} = 0.7*Vdd
Output Sink Current (Buzzer)	I_{OL}	12	-	-	mA		Vdd = 3.0V, V_{OL} = 0.3*Vdd
LCD Bias Voltage	VLCD	-5%	3.0~4.5	+5%	V	VLCD	1/3 bias At 25 deg
			4.0~6.0				1/4 bias At 25 deg
Pull low Resistance	R_{PL}	-	60	-	Kohm	PA, PC, PD,PE	VDD=2.2~3.6V
High Frequency	F_H	-20%	225	+20%	kHz		Clock select as 225kHz
		-	500	-			Clock select as 500kHz
			1000				Clock select as 1000kHz
			1800				Clock select as 1800kHz
Low Frequency	F_L	-20%	30.72	+20%	kHz		Low speed clock select as IOSC30K
		-	32768	-		X32I,X32O	Low speed clock select as XTAL32K
Operating Current	I_{OP}	-	200	-	uA		High Frequency =225kHz, CPU on, LCD on, no load (VDD=3.0V)
		-	350	-	uA		High Frequency =500kHz, CPU on, LCD on, no load (VDD=3.0V)
		-	600	-	uA		High Frequency =1000kHz, CPU on, LCD on, no load (VDD=3.0V)
		-	1000	-	uA		High Frequency =1800kHz, CPU on, LCD on, no load (VDD=3.0V)
Halt Current	I_{HALT}	-	3	-	uA		Low Frequency active, CPU off, LCD on, no load(VDD=3.0V) @50℃
Standby Current	I_{STBY}	-	-	1	uA		Clock is stopped, LCD off(VDD=3.0V) @25℃

Note: Vlcd should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

7. APPLICATION CIRCUITS



Note1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL811P08A -NnnV - C	Chip form
GPL811P04A -NnnV - C	Chip form
GPL811P08A -NnnV – QL09X	Halogen Free 128 pin LQFP Package
GPL811P04A -NnnV – QL09X	Halogen Free 128 pin LQFP Package

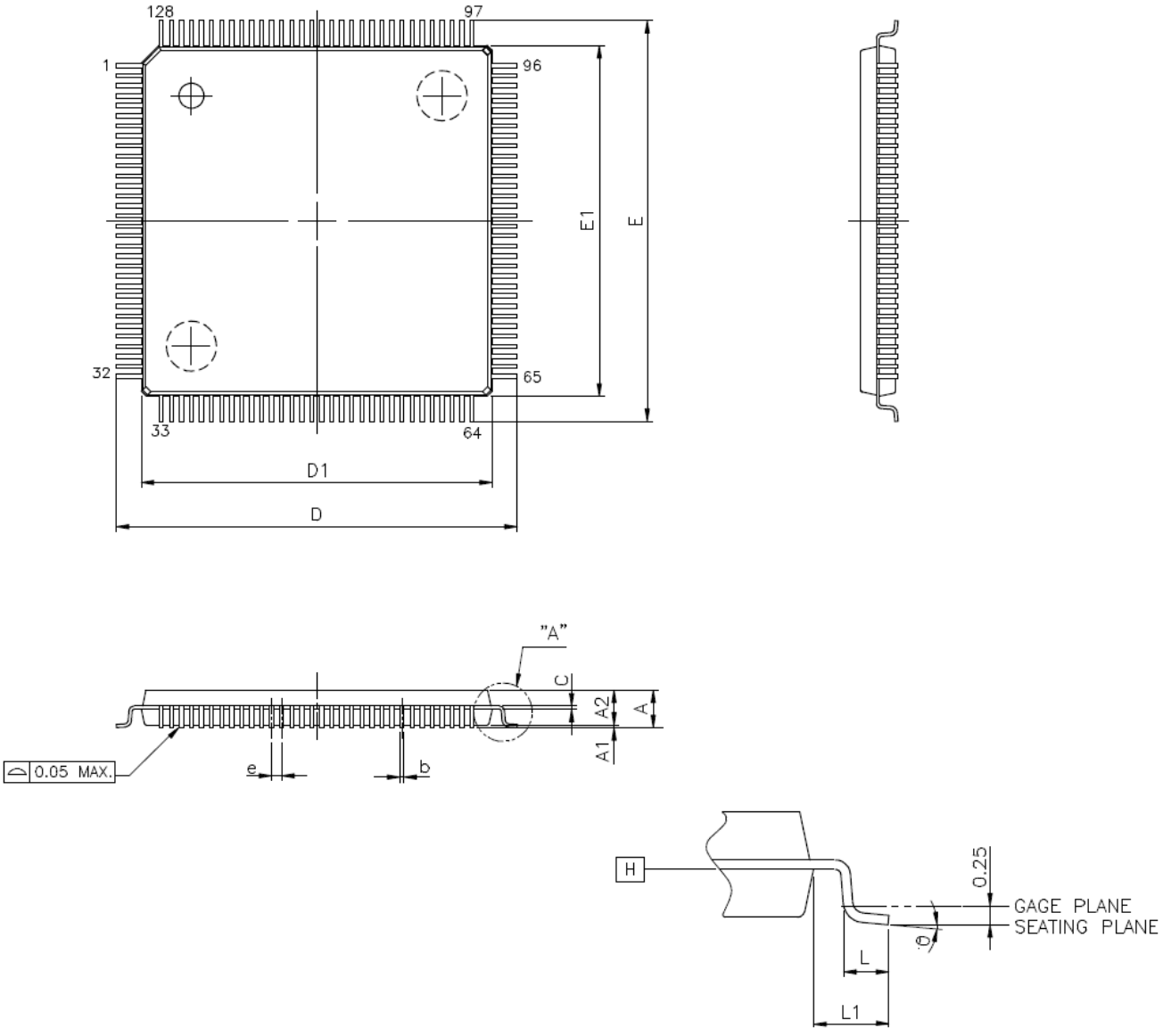
Note1: Code number (NnnV) is assigned for customer.

Note2: Code number (N = A-Z or 0-9, nn=00-99); version (V = A - Z)

Note3: Package form number (X = 0-9, serial number)

8.2. Package Information

8.2.1. LQFP 128L outline dimensions



Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	16.00 BSC.		
D1	14.00 BSC.		
E	16.00 BSC.		
E1	14.00 BSC.		
e	0.40 BSC.		
θ	0°	3.5°	7°
b	0.13	0.16	0.23
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF		

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10. REVISION HISTORY

Date	Revision #	Description	Page
Sep. 11, 2013	1.2	Modify Frame rate at 1/9 & 1/11 duty;	8
Jul. 10, 2013	1.1	Modify 4.2 PIN Map	6
Sep. 26, 2012	1.0	1. DC characteristics updated; 2. Package information added;	P4,P11 P6,P13
Feb. 6, 2012	0.1	Original	15