DATA SHEET

GPL812P02A

Low Power 128 Dots LCD Controller with 16KB OTP ROM

Oct. 02, 2014

Version 1.1

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LOW POWER 128 DOTS LCD CONTROLLER WITH 16KB OTP ROM

1. GENERAL DESCRIPTION

GPL812P02A, a special designed CMOS 8-bit microprocessor by Generalplus, features 256-byte RAM, 16KB one-time programmable (OTP) ROM, up to 25 software selectable general I/Os, an interrupt controller, and an automatic display controller/driver in a small device. It has a Clock Stop mode for power savings, which saves the RAM contents, but freezes the oscillator to make all other chip functions inoperative, and the stop mode can be released by using external wakeup sources. This device is applicable for many applications such as low power watch and other LCD relevant products.

2. FEATURES

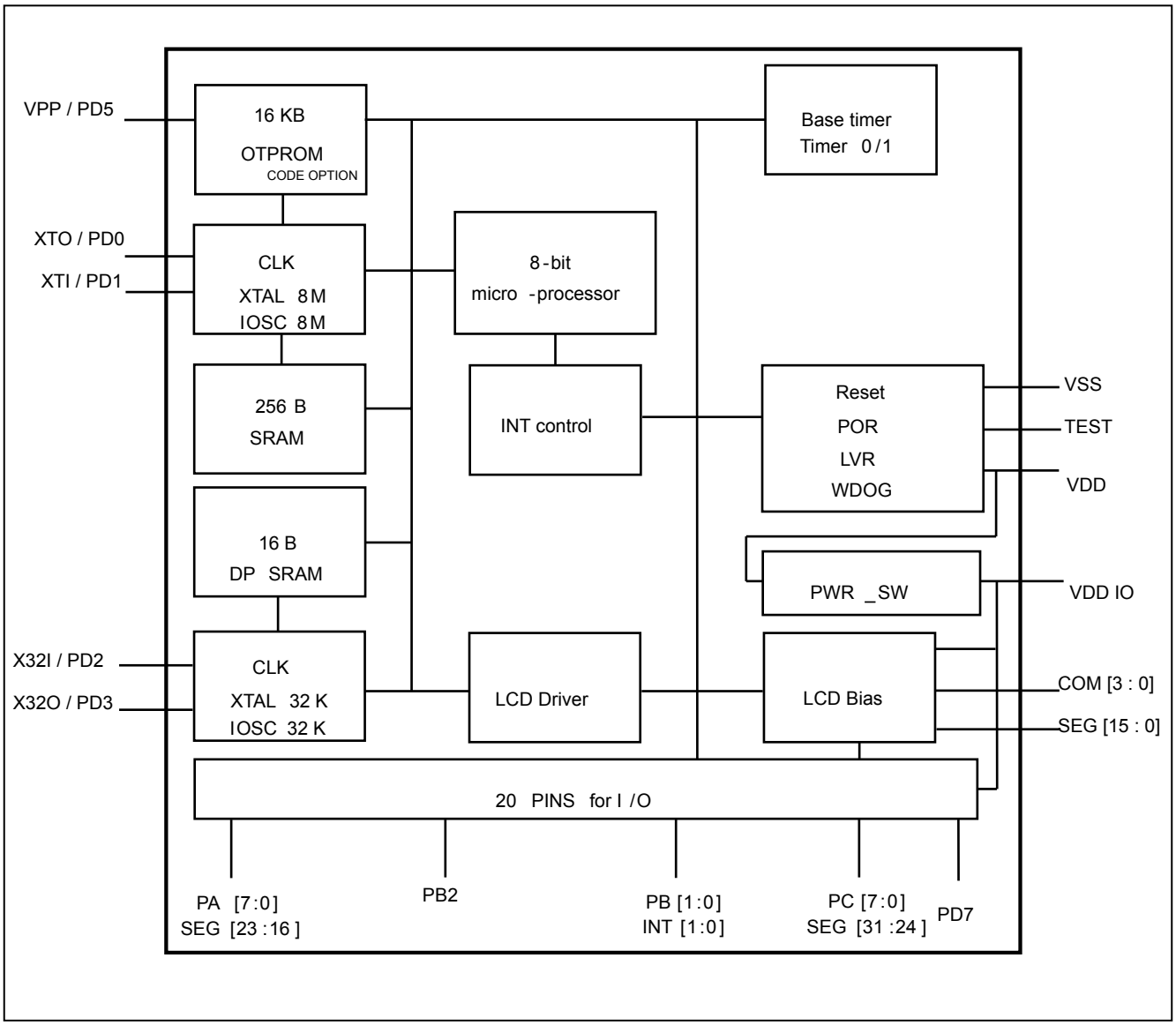
- Built-in 8-bit processor
- 256-byte SRAM
- 16K-byte OTP ROM
- 128 bit DPRAM
- Built-in 4M/8MHz Crystal or IOSC for system operation
  - internal oscillator with ±5% precision
- Built-in 32kHz IOSC or 32768Hz Crystal oscillator circuit for timebase.
- Operating voltage:
  - 4.0MHz@2.0V~3.6V or 8.0MHz@2.4V~3.6V selectable by code option
- Built-in Standby mode (Clock Stop mode) & Halt mode(with LCD and 32K timer on) for power saving
  - Low standby current, ISTBY < 1u @3.6V, 25℃
  - Low halt mode current, Ihalt < 8u @3.6V, 25℃
- Up to 25 bi-directional tri-state I/O ports
  - PA0~PA7 (SEG16~23),
  - PB0~1(INT0, INT1); PB2;
  - PC0~PC7 (SEG24~31)
  - PD7,VPP(PD5), X32O(PD3), X32I(PD2), XTI(PD1), XTO(PD0)
- RFC (Resister to Frequency Converter)
  - Uses 12-bit timer (Timer1) counter
  - PC7 as RFC input, PC6/5/4 as RFC output
- LCD configurations: 4 coms x 32 segs (MAX)
  - Frame rate is 85Hz.
  - LCD 1/2, 1/3 bias; 1/2, 1/3, 1/4 duty; VLCD = VDD
- Four timers
  - Basic timer provides Fosc/4194304 watch dog source
  - Timer0 is a general purpose 8-bit timer with input clock selectable
  - Timer1 is a general purpose 12-bit timer with input clock selectable
  - 32K timer is a time base wakeup source with frequency selectable
- 10 interrupt sources
  - TM0O, TM1O, CPUDiv1K, CPUDiv4K, CPUDiv32K, CPUDiv2M, TBHF, TBLF, EXTINT1 and EXTINT0 interrupts
- Wakeup source
  - Key (Port B/C/D) change wakeup
  - 32K time base wakeup(TBHF/TBLF)
- LVD (Low voltage detect)

  Sense VDD voltage@ 2.1V / 2.4V (register option)

Note1: TBHF: 128Hz, 256Hz, 512Hz or 1KHz

Note2: TBLF: 2Hz, 4Hz, 8Hz or 16Hz

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

4.1. Pin Description

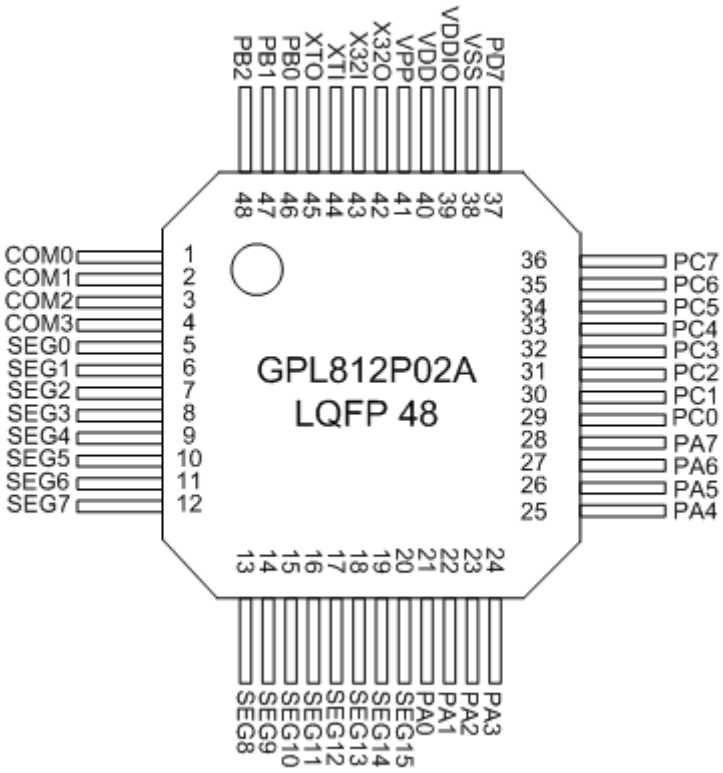
Type: I = Input, O = Output, S = Supply

Pin Name	Dice Pin No.	PKG Pin No.	Type	Main Function	Alternate Function
PA7/SEG23	28	28	I/O	**PortA[7:0]:** Bi-direction programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor, floating input or CMOS output. **SEG[23:16]:** LCD driver segment output	
PA6/SEG22	27	27	I/O		
PA5/SEG21	26	26	I/O		
PA4/SEG20	25	25	I/O		
PA3/SEG19	24	24	I/O		
PA2/SEG18	23	23	I/O		
PA1/SEG17	22	22	I/O		
PA0/SEG16	21	21	I/O		
NC	52	NC	I/O	**PortB[2:0]:** Bi-direction programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor, floating input or CMOS output. Normal wakeup; if a key status is changed, the chip can be awakened from sleep mode. **INT[1:0]:** external INT input.	
PB2	51	48	I/O		
PB1/INT1	50	47	I/O		
PB0/INT0	49	46	I/O		
PC7/SEG31	36	36	I/O	**PortC[7:0]:** Bi-direction programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor, floating input or CMOS output. Normal wakeup; if a key status is changed, the chip can be awakened from sleep mode. **SEG[31:24]:** LCD driver segment output	
PC6/SEG30	35	35	I/O		
PC5/SEG29	34	34	I/O		
PC4/SEG28	33	33	I/O		
PC3/SEG27	32	32	I/O		
PC2/SEG26	31	31	I/O		
PC1/SEG25	30	30	I/O		
PC0/SEG24	29	29	I/O		
PD7	37	37	I/O	**PortD[7]:** Bi-direction programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor, floating input or CMOS output.	
VPP/PD5	43	41	I/O	**PortD[5]:** Bi-direction programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor, floating input or CMOS output. Normal wakeup; if a key status is changed, the chip can be awakened from sleep mode. **VPP:** OTP Program power supply	
X32O/PD3	44	42	I/O	**PortD[3]:** Bi-direction programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor, floating input or CMOS output. Normal wakeup; if a key status is changed, the chip can be awakened from sleep mode. **Crystal Output:** It is connected with external crystal for 32KHz crystal oscillation circuitry in crystal mode.	
X32I/PD2	45	43	I/O	**PortD[2]:** Bi-direction programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor, floating input or CMOS output. Normal wakeup; if a key is changed, the chip can be awakened from sleep mode. **Crystal Input:** It is connected with external crystal for 32KHz crystal oscillation circuitry in crystal mode.	

Pin Name	Dice Pin No.	PKG Pin No.	Type	Main Function	Alternate Function
XTI/PD1	47	44	I/O	**PortD[1]:** Bi-direction programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor, floating input or CMOS output. Normal wakeup; if a key is changed, the chip can be awakened from sleep mode. **Crystal Input:** It is connected with external crystal for 4M/8M crystal oscillation circuitry in crystal mode.	
XTO/PD0	48	45	I/O	**PortD[0]:** Bi-direction programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor, floating input or CMOS output. Normal wakeup; if a key is changed, the chip can be awakened from sleep mode. **Crystal Output:** It is connected with external crystal for 4M/8M crystal oscillation circuitry in crystal mode.	
COM[3:0]	4~1	4~1	O	LCD driver common output	
SEG[15:0]	20~5	20~5	O	LCD driver segment output	
VDD	42	40	S	power supply	
VDDIO	40,41	39	S	power supply	
VSS	38,39	38	S	Ground	
TEST	46	NC	I	Test pin, high active.	

50pin

4.2. Pin Map(48 pin LQFP)



5. FUNCTION DESCRIPTIONS

5.1. CPU

The 8-bit microprocessor in GPL812P02A is a high performance processor equipped with Accumulator, Program Counter, X Register, Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure).

5.2. Clock Source

The GPL812P02A equips two types of clock sources:

(1) High speed frequency to support the whole system operation. There are two frequency options: 4MHz/8MHz and can be selected by register based on various user's application needs. It comes from IOSC8M or XTAL8M.

(2) Low speed frequency to control LCD frame rate and time base timer. It is derived from IOSC32K or XTAL32K.

5.3. ROM/RAM Area

The GPL812P02A features 16K-byte OTP-ROM that can be defined as the program area, address located from $C000H to $FFFFH. Its RAM consists of 256 bytes (including Stack) at locations $80H~$FFH & $180H~$1FFH.

5.4. Stop Clock Mode

The GPL812P02A equips a power saving mode for those applications requiring very low standby current. Users can simply enable the wakeup sources to stop CPU clock by writing the STOP CLOCK Register. By doing that, CPU will enter standby mode and the RAM and I/Os remain at their previous states until being awakened. There are two types of wakeup sources in the GPL812P02A, I/O PAD data transient (Port B/C/D Key change) and 32K timer base wake up source(TBHF/TBLF). After the GPL812P02A wakes up, CPU will go to the next state of where CPU enters sleep mode. Wake-up action will not influence RAM and I/Os.

Note1: TBHF: 128Hz, 256Hz, 512Hz or 1KHz

Note2: TBLF: 2Hz, 4Hz, 8Hz or 16Hz

5.5. I/O Ports

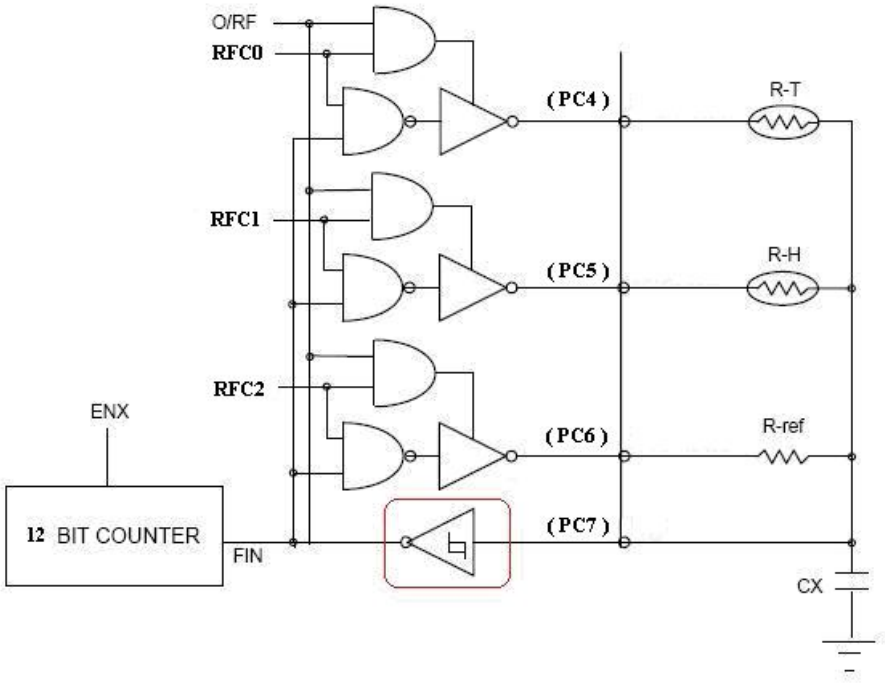
The GPL812P02A has four IO ports: PortA, PortB, PortC and PortD. These port pins may be multiplexed with an alternate function for the peripheral features on the device. In general, when an initial reset state occurs, all ports are used as a general purpose input port. There are three parts in IO structure: data, direction and attribution registers. Each corresponding bit in these ports should be given a value.

[Table] 5-1 I/O configurations

Attribution (P_IOX_ATT)	Direction (P_IOX_DIR)	Data (P_IOX_DAT)	Function	Description
0	0	0	Floating	Input with float
0	0	1	Pull low	Input with pull-low
0	1	0	Driving low	Output Data
0	1	1	Driving High	Output Data
1	0	0	Floating	Input with float
1	0	1	Pull high	Input with pull-high
1	1	0	Driving High	Output Data
1	1	1	Driving low	Output Data

5.6. RFC Function

The RFC (Resistor to Frequency Converter) circuit contains a RC oscillation circuit and a 12-bit timer/counter to calculate the resistance of temperature or humidity sensor related to reference resistor. The circuit is shown below.

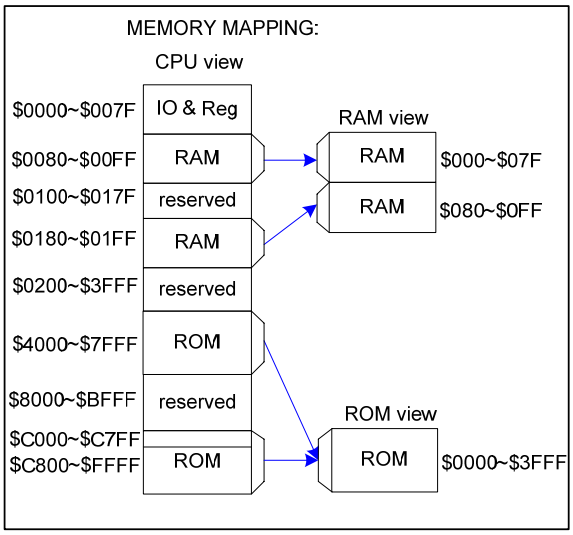


R-F CONVERTER

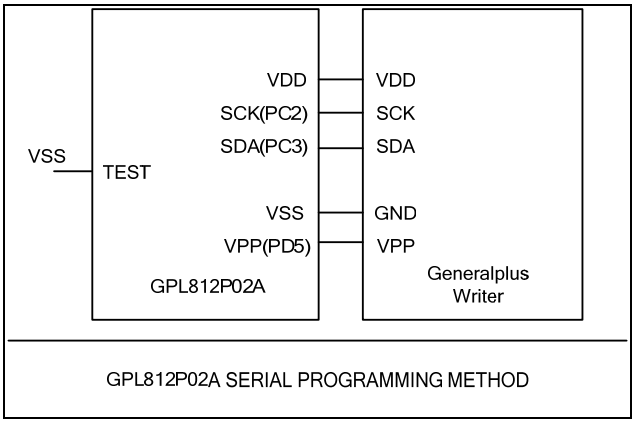
5.7. LCD Controller

GPL812P02A contains a LCD controller/driver that provides the capability to drive 4 commons and 32 segments LCD. To reduce CPU overhead, a display buffer is designed for LCD mappings. A LCD dot/pattern is set ON or OFF by programming the corresponding bit in the display buffer. In addition, the LCD can be programmed as 1/2duty with 1/2bias, 1/3duty with 1/2bias, 1/3duty with 1/3bias or 1/4duty with 1/3bias. The VLCD level is equal VDD. The LCD driver can also operate during sleep by keeping 32K oscillator running.

5.8. Map of Memory



5.9. OTP Programming Circuit



GPL812P02A SERIAL PROGRAMMING METHOD

Note1: Don't connect any component with PC3 and PC2 when programming.

Note2: Connect VPP to Writer during OTP programming cycle, and keep it floating in normal run.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

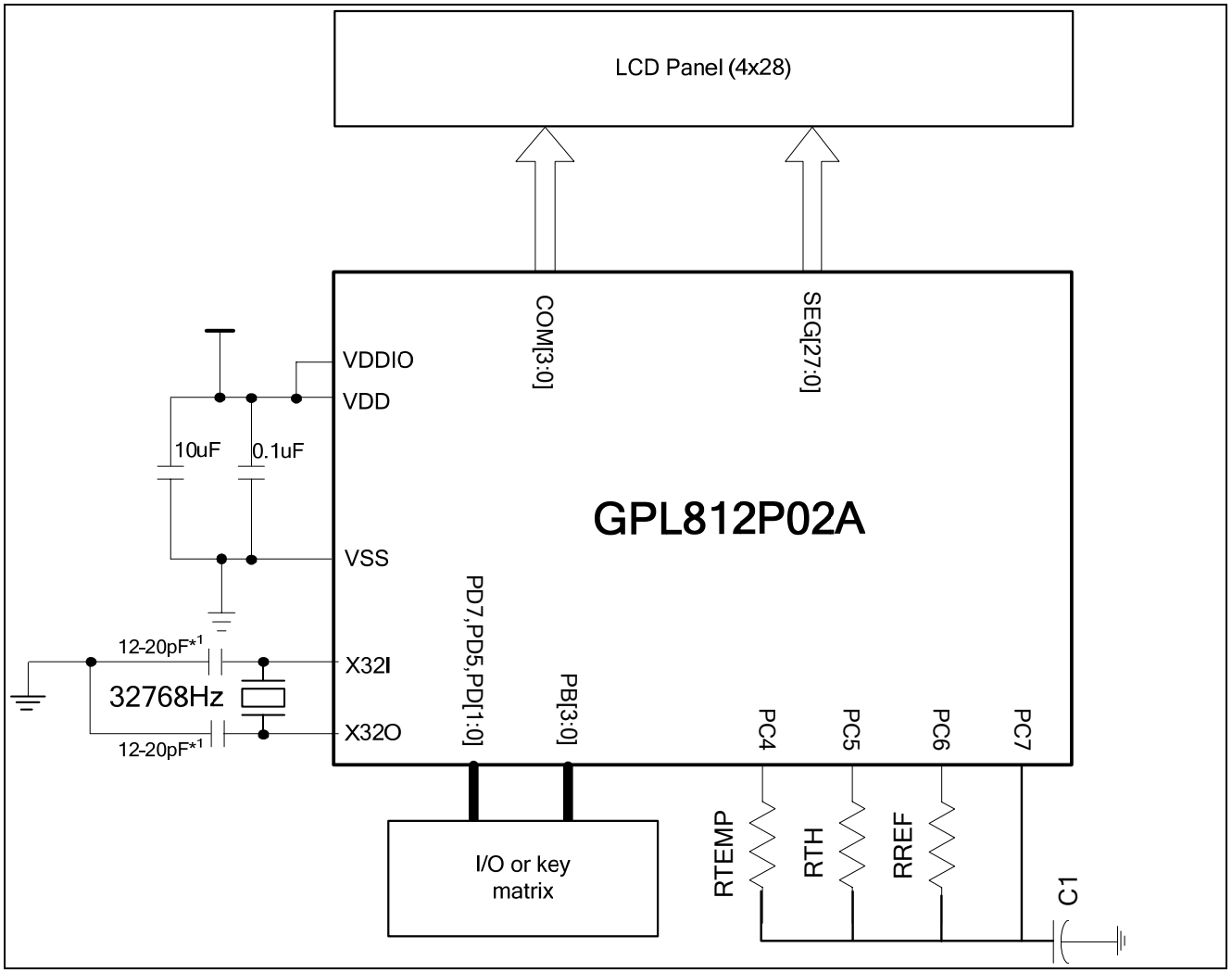
Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3~5 V
Input Voltage Range	V_{IN}	-0.3V to V_+ + 0.3V
Operating Temperature	T_{OPR}	0℃ to +70℃
Storage Temperature	T_{STG}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

6.2. DC Characteristics(T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage1	VDD	2.4	-	3.6	V	F_{CPU} = 8.0MHz
		2.0	-	3.6		F_{CPU} = 4.0MHz
Operating Current	I_{OP}	-	1.5	2	mA	F_{CPU} = 8.0MHz @ 3.0V, no load
Halt Current	I_{HALT}	-	6	8	uA	Low Frequency active, CPU off, LCD on, no load(VDD=3.6V)
Standby Current	I_{STBY}	-	0.5	1	uA	VDD = 3.6V
Input High Level	V_{IH}	0.7VDD	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.3VDD	V	VDD = 3.0V
Output High Level PB, PC, PD	V_{OH}	0.8VDD	-	-	V	VDD = 3.0V I_{OH} = -8mA
Output Low Level PB, PC, PD	V_{OL}	-	-	0.2VDD	V	VDD = 3.0V I_{OL} = 20mA
Input Pull High Resistor PA, PB, PC, PD	R_H	40	50	100	Kohm	Pull High Typ@VDD = 3.0V
Input Pull Low Resistor PA, PB, PC, PD	R_L	40	50	100	Kohm	Pull Low Typ@VDD = 3.0V

7. APPLICATION CIRCUITS



Note1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL812P02A -NnnV - C	Chip form
GPL812P02A -NnnV – QL23X	Halogen Free 48 pin LQFP Package

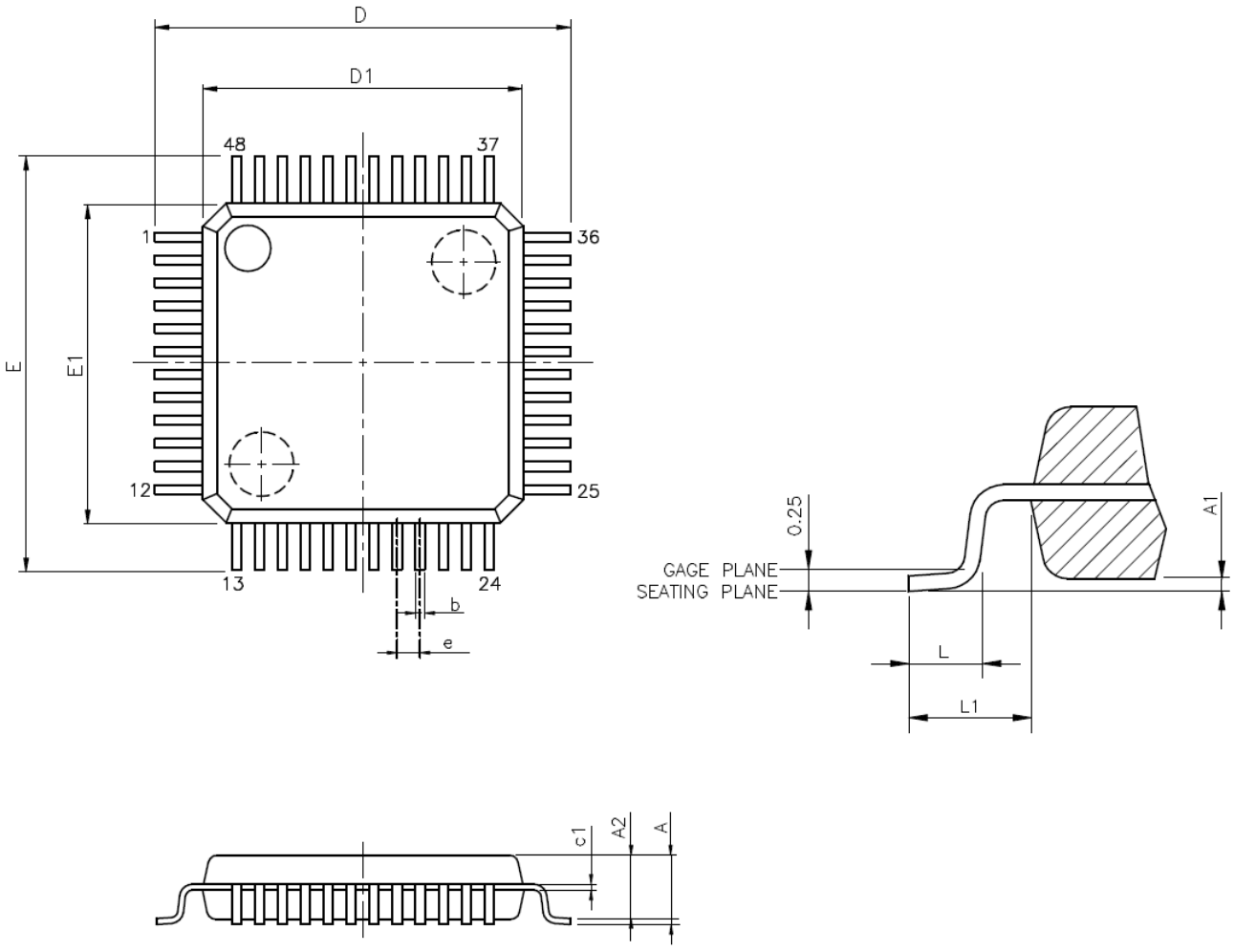
Note1: Code number (NnnV) is assigned for customer.

Note2: Code number (N = A-Z or 0-9, nn=00-99); version (V = A - Z)

Note3: Package form number (X = 0-9, serial number)

8.2. Package Information

8.2.1. LQFP 48L outline dimensions



Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	9.00 BSC.		
D1	7.00 BSC.		
E	9.00 BSC.		

Symbol	Millimeter		
	Min.	Nom.	Max.
E1	7.00 BSC.		
e	0.5 BSC.		
b	0.17	0.22	0.27
C1	0.09	-	0.16
L	0.45	0.60	0.75
L1	1.00 REF		

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10. REVISION HISTORY

Date	Revision #	Description	Page
Oct. 02, 2014	1.1	1. Add LVD function 2. Modify BLOCK DIAGRAM 3. Remove PB3	3, 4, 5.
Apr. 01, 2013	1.0	1. DC Characteristics modified. 2. Package information added.	9 6, 11
Jun. 28, 2012	0.1	Original	13