DATA SHEET

GPL85110A

2048-Dot Mono LCD Controller/ Driver with 1M-Byte ROM

Jul 22, 2016

Version 1.3

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2048-Dot Mono LCD Controller/ Driver with 1M-Byte ROM

1. GENERAL DESCRIPTION

The GPL85110A, an 8-bit microprocessor, features 1M bytes Mask ROM, 1.5K bytes working RAM, 512 bytes LCD RAM, 22 I/Os, interrupt/ wakeup controller, two 16-bit timers, two SPI interfaces, a 14-bit DAC with push-pull amplifier for driving speaker directly and automatic display controller/ driver for mono LCD.

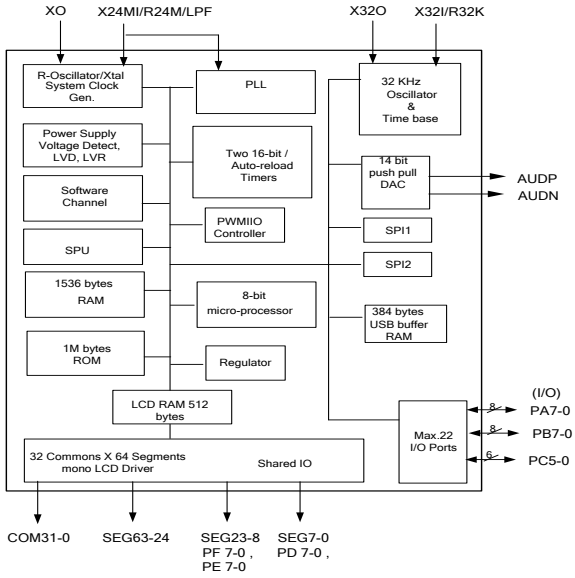
The GPL85110A contains 64 segments and 32 commons, forming a maximum of 2048 dots LCD resolution. The GPL85110A operates over a wide voltage ranged from 2.3V through 5.5V. The Low Voltage Reset function assures system still functions properly when power drops below certain level. The microprocessor can implement software for audio processing, functional control and others.

The GPL85110A carries a high performance SPU voice engine to achieve 8-channel voice with ADPCM/PCM data. It can produce attractive and high resolution sound easily. Plus, it features one 14-bit DAC with push-pull amplifier for driving speaker directly. Its large memory area can be used to store both program and audio data. There is a Serial Peripheral Interface (SPI) controller built-in to facilitate communicating with other devices. Furthermore, a SLEEP (power-down) function is also built-in to extend battery life.

The GPL85110A is designed with state-of-the-art technology to fulfill LCD application needs, especially for hand-held products.

2. BLOCK DIAGRAM

2.1. GPL85110A



3. FEATURES

- 8-bit micro-processor
- 1M bytes Mask ROM
- 1.5K bytes SRAM
- 512 bytes LCD RAM
- Operating voltage: 2.3V – 5.5V
- Max. CPU operating speed:
  - 12.0MHz @ 2.7V – 5.5V
  - 8.0MHz @ 2.3V – 3.6V
- Programmable CPU clock: /2, /4, /8, /16, /32, /64 and /128 clock frequency
- Six wake-up sources
- 23 IRQs & 4 NMI Interrupts
- Internal built-in regulator to supply core power (3.3V, for 3-battery application). Also internal built-in regulator can be turned off and external power is used to supply core power (for 2-battery application).
- SPU(Sound Processing Unit) engine with 8 voice channels
  - Supports 4/5 bit ADPCM and 8/16 bit PCM data format
  - Transforms 4/5 bit ADPCM data to 14 bit data to play high quality sound
  - Supports special tag such as Silence Tag, Event tag

- One software channel with noise filter to play high quality sound.
- Programmable LCD driver
  - Up to 64 segments and 32 commons, forming a maximum of 2048 dots LCD resolution; User can select different segment/common combination including 16 x 64, 24 x 56 and 32 x 48 etc. by code option.
  - Supports from 1/2 duty up to 1/32 duty
  - Supports 1/3, 1/4, 1/5, 1/6, 1/6.5, 1/7 bias
  - 512 bytes dedicated LCD RAM
  - Supports normal type-B and type-C LCD waveform with or without key scan
  - Built-in voltage regulator to generate VLCD for LCD driver
  - 46-level contrast control (VLCD=3.5V~8V)
  - Power saving SLEEP mode
- Low Voltage Detector
  8-level (2.3V/ 2.4V/2 .6V/ 2.9V/ 3.0V/ 3.3V/ 3.6V/ 4.0V) voltage detector
- Low Voltage Reset
- Peripherals
  - Dedicated I/Os: PA[7:0], PB[7:0], PC[5:0]
  - Shared I/Os: PD[7:0]/SEG[7:0], PE[7:0]/SEG[15:8], PF[7:0]/SEG[23:16]
  - Eight I/Os with high sink current for LED application
  - Key wakeup/interrupt function
  - Built-in 32.768KHz oscillator circuit for real time clock function (X'tal or R-osc)
  - Built-in R-oscillator (external resistor is needed) l or PLL for system operating clock
  - Internal time base generator
  - Two 16-bit reloadable timer/counters
  - Watchdog timer
  - 14-bit DAC with push-pull amplifier for driving speaker directly
  - IR output
  - Hardware PWMIO
  - Two SPI serial interface I/Os
- Powerful 8-ch Sound Processing Unit (SPU)
  - Variable tone-color sampling rate: max = 96KHz @ SPU_clock = 24MHz
  - 8-voice polyphony
  - Supports PCM/ADPCM tone-color table

4. APPICATION FIELD

- Handheld LCD game
- Educational toys (Electronic Learning Aids)
- Data bank
- Dictionary
- Translator

5. SIGNAL DESCRIPTIONS

5.1. Main Function PIN

Mnemonic	PIN No.	Type	Description
SEG7-0/PD7-0	60-53	O	LCD driver segment output. SEG7-0 shared pin with PD7-0
SEG15 - 8 /PE7-0	45-52	O	LCD driver segment output. SEG15 - 8 shared pin with PE7-0
SEG23 - 16/PF7-0	37-44	O	LCD driver segment output. SEG23 - 16 shared pin with PF7-0
SEG47 - 24	12-30,32-36	O	LCD driver segment output.
SEG63 - 48	149-153,1-3,4-11	O	LCD driver segment output.
COM31 - 16	147-132	O	LCD driver common output.
COM15 - 0	76-61	O	LCD driver common output.
PA0/IRO/EXT1	95	I/O	PA0 is a bi-directional I/O port, which can be software programmed as wakeup I/O and is shared with IRO (IR output) and external interrupt 1.
PA1/EXT2	94	I/O	PA1 is a bi-directional I/O port, which can be software programmed as wakeup I/O and is shared with external interrupt 2.
PA3 - 2	92,93	I/O	PA3-2 is a bi-directional I/O port, which can be software programmed as wakeup I/O.
PA4/ PWMIO0	91	I/O	PA4 is a bi-directional I/O port, which can be software programmed as wakeup I/O and is shared with PWMIO0.
PA5/ PWMIO1	90	I/O	PA5 is a bi-directional I/O port, which can be software programmed as wakeup I/O and is shared with PWMIO1.
PA6/ PWMIO2	89	I/O	PA6 is a bi-directional I/O port, which can be software programmed as wake up I/O and is shared with PWMIO2.
PA7/PWMIO3	88	I/O	PA7 is a bi-directional I/O port, which can be software programmed as wakeup I/O and is shared with PWMIO3.
PB0/SPI2_CSN/IISCKO	86	I/O	PB0 is shared with SPI2_CSN and IISCKO
PB1/ SPI2_SCK//IISDAO	85	I/O	PB1 is shared with SPI2_SCK and IISDAO
PB2/ SPI2_SDO/IISWSO	84	I/O	PB2 is shared with SPI2_SDO and IISWSO
PB3/ SPI2_SDI	83	I/O	PB3 is shared with SPI2_SDI.
PB4/SPI1_CSN/ PWMIO0	81	I/O	PB4 is shared with SPI1_CSN and shared with PWMIO0and is a high drive IO.
PB5/SPI1_SCK/ PWMIO1/IISCKI	80	I/O	PB5 is shared with SPI1_SCK and IISCKI and shared with PWMIO1 and is a high drive IO.
PB6/SPI1_SDO/ PWMIO2/IISDAI	79	I/O	PB[6:5] is shared with SPI1_SDO and IISDAI and shared with PWMIO2 and is a high drive IO.
PB7/ SPI1_SDI/ PWMIO3/IISWSI	78	I/O	PB7 is shared with SPI1_SDI and IISWSI and shared with PWMIO3 and is a high drive IO.
PC5 -0	96-101	I/O	PC[5:0] is a bi-directional I/O port
R24MI/LPF	104	I	ROSC input connected to VDD33V_REGOUT through a resistor, or RC low pass filter connection for PLL(Mask option).
RESETB	110	I	System reset input, low active, internal pull high.
AUDP, AUDN	115,113	O	Audio output of push pull DAC
NC	119	I	Unused pin for user
X32I/R32K	105	I	32.768KHz crystal input or connects to VDD33V_REGOUT through a resistor (option).
X32O	106	O	32.768KHz crystal output
TEST	111	I	Test input, internal pull low

Mnemonic	PIN No.	Type	Description
CAP1P, CAP1N	122,123	P	LCD voltage generation. Charge pump capacitor interconnection pins.
CAP2P, CAP2N	124,125	P	LCD voltage generation. Charge pump capacitor interconnection pins.
LCDVPP	126	P	LCD voltage generation. Voltage generated by charge pump.
V4	128	P	LCD voltage generation
V3	129	P	LCD voltage generation
V2	130	P	LCD voltage generation
V1	131	P	LCD voltage generation
VLCD	127	P	LCD voltage generation. The highest Voltage for LCD display.
VDD_REGIN	109	P	Power for Regulator
VSS_REG	108	P	Ground for Regulator
VDD33V_REGOUT	107	P	3.3V power output from regulator (regulator can be off when external 3V is supplied).
VDD_LCD	120	P	Power for LCD driver
VSS_LCD	121	P	Ground for LCD driver
VDD_IO	87	P	Power for PA, PC, PD, PE, PF
VSS_IO	82	P	Ground for PA, PB, PC, PD, PE, PF
VDD_PB	77	P	Power for PB
VDD_DAC	114	P	Power for push pull DAC driver
VSS_DAC	116	P	Ground for push pull DAC driver
AVDD_DAC	118	P	Analog ground for push pull DAC
AVSS_DAC	117	P	Analog power for push pull DAC

6. FUNCTIONAL DESCRIPTIONS

6.1. Memories

GPL85110A contains 2048 bytes SRAM, 512 bytes LCD RAM and 1M bytes ROM.

6.2. Operating States

There are three operation modes in GPL85110A: standby, halt and operating. The following table shows the differences among these modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz Oscillator	ON	ON	OFF
LCD Driver	ON	ON/OFF	OFF

6.2.1. Operating Mode

In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated.

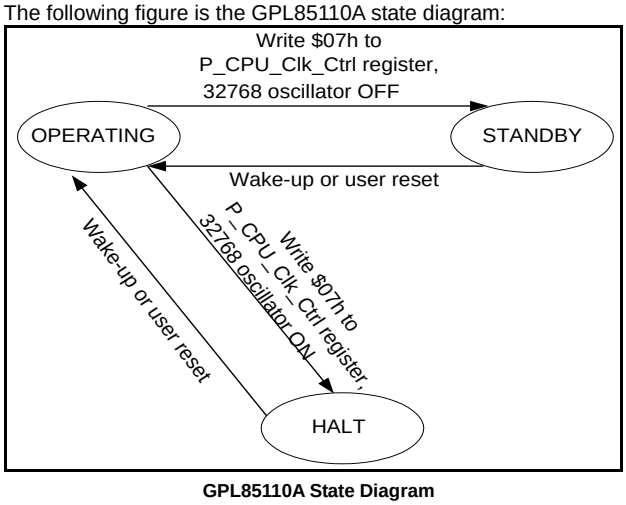
6.2.2. Standby Mode

Turn off 32768Hz oscillator and write "07H" to P_CLK_CPU_Ctrl Register ($3006) to activate standby mode. The standby mode is a mode that the device is placed in its lowest current consumption state. In standby mode, all functions are turned off; in addition, RAM and I/Os will remain in their previous states.

6.2.3. Halt Mode

Write "07H" to P_CLK_CPU_Ctrl Register ($3006) but still keeps 32768Hz oscillator running to enter halt mode. In halt mode, CPU clock halts and waits for an event (e.g. key press, timer overflow) to wake up. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode.

The following figure is the GPL85110A state diagram:



GPL85110A State Diagram

6.3. Speech and Melody, and DAC

The GPL85110A uses a high performance SPU voice engine to archive 8-channel voice with ADPCM/PCM code. The SPU also supports automatic zero-crossing concatenating function. A hardware multiplier is also embedded in this SPU for software use. The fixed addresses of RAM area $0000 - $009F is designed as address pointers and a data buffer for the 8-channel speech/melody generation. Moreover, one 14-bit software channel with noise filter is also supported. There is one 14-bit DAC with push-pull amplifier for direct audio output.

6.4. Hardware PWMIO

Hardware PWMIO supports four LED outputs with brightness control of 256 levels. The clock source of PWMIO can be selected by user's request.

6.5. LCD Controller/Driver

GPL85110A has a built-in LCD driver and supports monochrome LCD control. The LCD driver can support up to 32COM * 64SEG. Programmers are able to define the LCD configuration by setting up the LCD Control Register. Once the LCD configuration is completed, the desired pattern can be displayed by filling the LCD buffer with proper data. The LCD driver can also operate in halt mode by keeping 32768Hz oscillator running. The LCD driver in GPL85110A supports 1/2 – 1/32 duty and 1/3 - 1/7 bias.

6.6. LCD Voltage Generator

To achieve highly integrated circuit and save external components, GPL85110A has built-in charge-pump circuit to generate LCD's bias voltages VLCD, V4, V3, V2 and V1. The level of VLCD can be adjusted by software. It is suggested that VLCD must be higher than VDD_IO or abnormal operation will occur.

6.7. Low Voltage Detection

The GPL85110A equips an 8-level (Software programmable) low voltage detector to detect low voltage events. Users can turn on the low voltage detection that monitors VDD_REGIN periodically to check whether it is lower than the given value. In addition, if LV NMI is enabled, a NMI will be issued to notify CPU if power voltage drops below the given value. Also, the voltage detector will generate a system reset if power supply voltage drops too low.

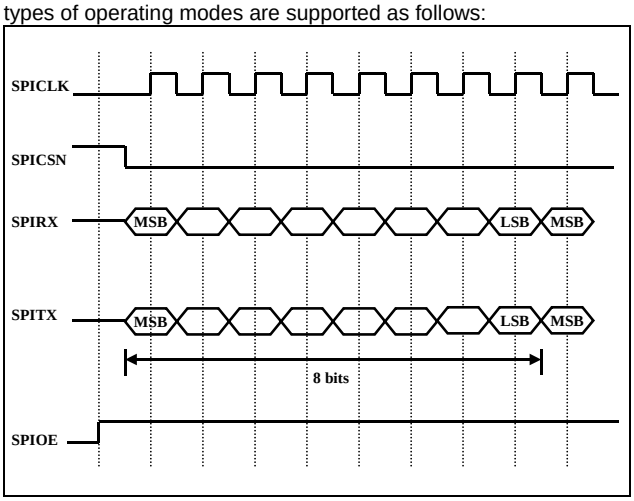
6.8. Watchdog Timer (WDT)

An on-chip watchdog timer is also available in the GPL85110A. The WDT is designed to recover the system from unexpected operations. In some cases, if WDT is not cleared within one

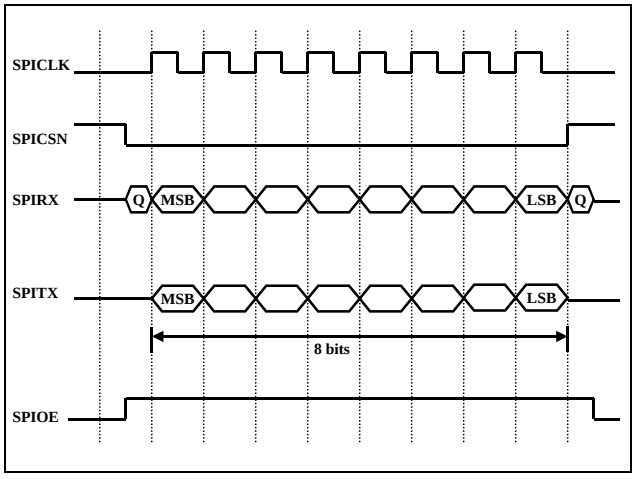
second, the WDT will generate a system reset to restart system. If WDT is enabled, the WDT should be cleared periodically to avoid accidental reset. The WDT can be cleared through software programming. Note that the WDT only works when 32768Hz clock is activated.

6.9. SPI Controller

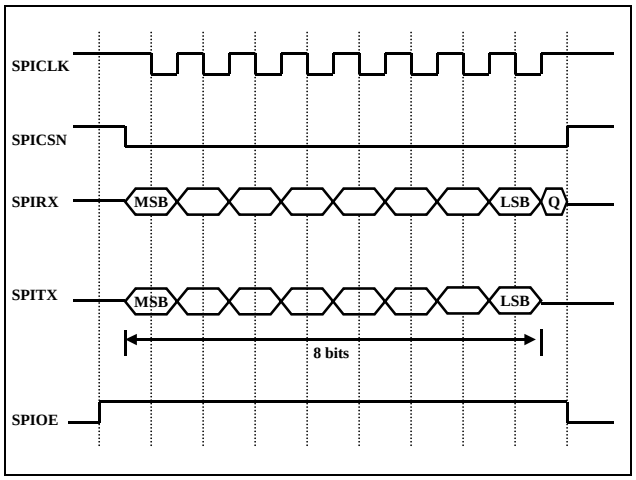
Two Serial Peripheral Interface (SPI) controllers are built-in to enable synchronous serial communication with master/slave peripherals. There are four control signals on SPI including SPICSN, SPICLK (SCK), SPIRX (SDI), and SPITX (SDO). The four signals of SPI1 are shared with PB4, PB5, PB6 and PB7. The four signals of SPI2 are shared with PB0, PB1, PB2 and PB3. While SPI module is enabled by corresponding control bit, these four pins cannot be used as GPIOs and any setting on corresponding GPIO control register will have no effect. Four types of operating modes are supported as follows:



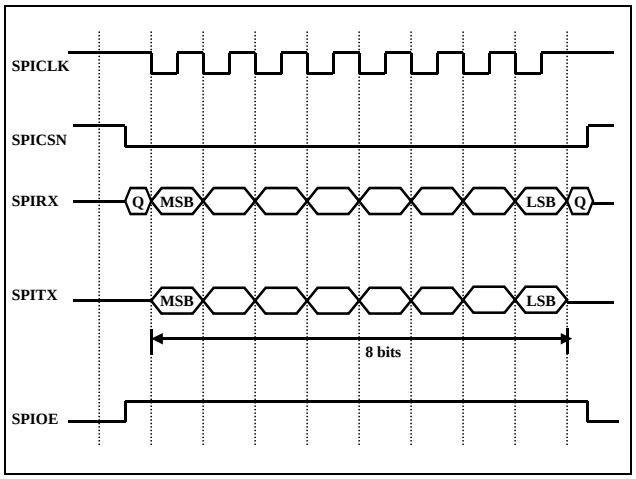
Master Mode, Polarity = 0, Phase=0



Master Mode, Polarity = 0, Phase=1



Master Mode, Polarity = 1, Phase=0



Master Mode, Polarity = 1, Phase=1

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD_REGIN=4.5V, for 3-battery Application, Internal Regulator Enabled Output, T_A=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REGIN	2.7	-	5.5	V	For 3-battery
Operating Current	I_{OP1}	-	6	9	mA	F_{CPU} = 8.0MHz @ 5.0V F_{XTAL} = 16.0MHz, without loading, DAC disabled. PLL2 OFF/USB OFF
	I_{OP2}	-	8	12	mA	F_{CPU} = 12.0MHz @ 5.0V F_{ROSC} = 24.0MHz, no load, DAC disabled. PLL2 OFF/USB OFF
Halt Current	I_{HALT}	-	55	110	μA	VDD_REGIN = 4.5V, 32K X'tal ON, Strobe off, LCD ON, 1/7 Bias, VLCD=TBD V, no LCD panel
Standby Current (Regulator on)	I_{STBYR}	-	5	10	μA	VDD_REGIN = 4.5V, internal regulator on, all off.
Input High Level	V_{IH}	0.7VDD_IO	-	VDD_IO	V	VDD_ IO = 4.5V
Input Low Level(PA/PB/PC) (PD/PE/PF)	V_{IL1} V_{IL2}	0	-	0.3VDD_IO	V	VDD_ IO = 4.5V
Output High Current (I/O) PA/PB4~PB7 PB0~PB3/PC PD/PE/PF	 I_{OH1} I_{OH2} I_{OH3}	 9.8 7 3.5	 14 10 5	 18.2 13 6.5	mA	VDD_ IO = 4.5V, V_{OH} = 3.15V
Output Sink Current (I/O) PA4~PA7 PB4~PB7 PA0~PA3/PB0~PB3/PC PD/PE/PF	 I_{OL1} I_{OL2} I_{OL3} I_{OL4}	 25 18 6.3 3.5	 50 36 9 5	 75 54 11.7 6.5	mA	VDD_ IO = 4.5V, V_{OL} = 1.35V
Input Pull-Low Resistor PA(weak pull) PA(strong pull) PB~PF	 R_{PL}	 100 35 35	 150 50 50	 200 65 65	KΩ	V_{IN} = 4.5V
Input Pull-High Resistor PA(weak pull) PA(strong pull) PB,PC	 R_{PH}	 100 35 35	 150 50 50	 200 65 65	KΩ	V_{IN} = 0V

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	3.5	-	8	V	VDD_REGIN = 4.5V, no load
OSC Resistor	R_{OSC}	-	23	-	KΩ	F_{OSC} = 24MHz @ 4.5V
OSC32K Resistor	R_{OSC32k}	-	3.1	-	MΩ	F_{OSC32} = 32768Hz @ 4.5V
CPU Clock	F_{CPU}	-	-	12	MHz	F_{CPU} = F_{OSC}/2 @ 2.7V

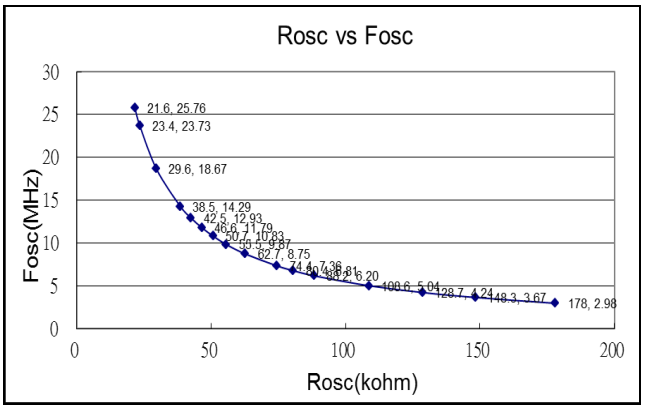
Note: V_{LCD} should be higher than VDD_IO to prevent abnormal functions.

7.3. DC Characteristics (VDD_REGIN= 3.0V, for 2-battery Application, Internal Regulator Output Disabled, T_A=25℃)

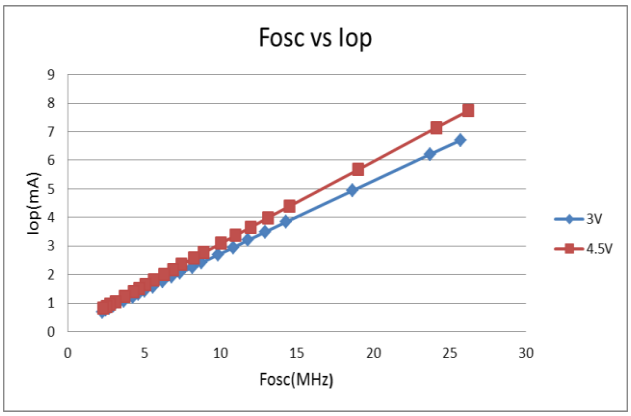
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REGIN	2.3	-	3.6	V	For 2-battery
Operating Current	I_{OP1}	-	5	8	mA	F_{CPU} = 8.0MHz @ 3.0V F_{XTAL} = 16.0MHz, no load, DAC disabled. PLL2 OFF/USB OFF
	I_{OP2}	-	7	10	mA	F_{CPU} = 12.0MHz @ 3.0V F_{ROSC} = 24.0MHz, no load, DAC disabled. PLL2 OFF/USB OFF
Halt Current	I_{HALT}	-	50	100	μA	VDD_REGIN = 3.3V, 32K X'tal ON, Strobe off, LCD ON, 1/7 Bias, VLCD=TBD V, no LCD panel
Standby Current (Regulator off)	I_{STBY}	-	1	5	μA	VDD_REGIN = 3.0V, all off
Input High Level(PA/PB/PC) (PD/PE/PF)	V_{IH1} V_{IH2}	0.7VDD_IO	-	VDD_IO	V	VDD_IO = 3.0V
Input Low Level(PA/PB/PC) (PD/PE/PF)	V_{IL1} V_{IL2}	0	-	0.3VDD_IO	V	VDD_ IO = 3.0V
Output High Current (I/O) PA/PB4~PB7 PB0~PB3/PC PD/PE/PF	 I_{OH1} I_{OH2} I_{OH3}	 4.9 3.5 1.75	 7 5 2.5	 9.1 6.5 3.25	mA	VDD_ IO = 3.0V, V_{OH} = 2.1V
Output Sink Current (I/O) PA4~PA7 PB4~PB7 PA0~PA3/PB0~PB3/PC PD/PE/PF	 I_{OL1} I_{OL2} I_{OL3} I_{OL4}	 13 10 3.5 2.1	 26 20 5 3	 39 30 6.5 3.9	mA	VDD_ IO = 3.0V, V_{OL} = 0.9V
Input Pull-Low Resistor PA(weak pull) PA(strong pull) PB~PF	R_{PL}	 100 35 35	 150 50 50	 200 65 65	KΩ	V_{IN} = 3.0V
Input Pull-High Resistor PA(weak pull) PA(strong pull) PB,PC	R_{PH}	 100 35 35	 150 50 50	 200 65 65	KΩ	V_{IN} = 0V
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	3.5	-	8	V	VDD_ IO = 3.0V
OSC Resistor	R_{OSC}	-	34	-	KΩ	F_{OSC} = 16MHz @ 3.0V
OSC32K Resistor	R_{OSC32k}	-	3.1	-	MΩ	F_{OSC32} = 32768Hz @ 3.0V
CPU Clock	F_{CPU}	-	-	8	MHz	F_{CPU} = F_{OSC}/2 @ 2.3V

Note: V_{LCD} should be higher than VDD to prevent abnormal functions.

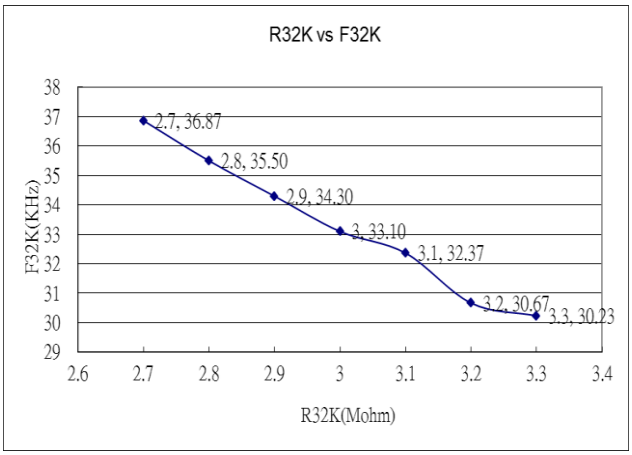
7.4. The Relationship between the R_{OSC} and the F_{OSC}



7.6. The Relationship between the F_{CPU} and the I_{OP}



7.5. The Relationship between the R32K and the F32K



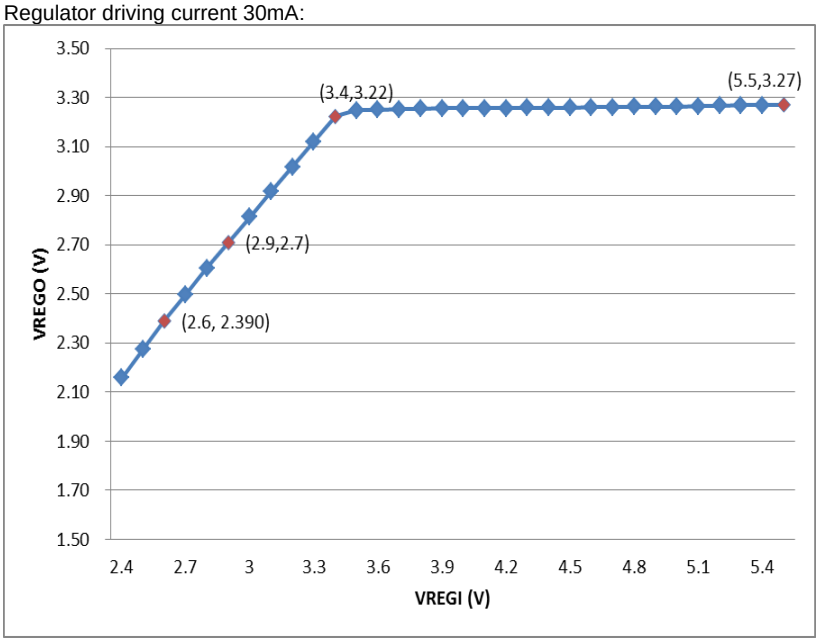
7.7. DAC Characteristics (VDD_REGIN = 5.0V, TA = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	bit
THD+n (5V@0.45W)	-	-	0.1	-	%
Noise at No Signal	-	-	-65	-	dBr A
Dynamic Range(-60dB)	-	-	-65	-	dBr A

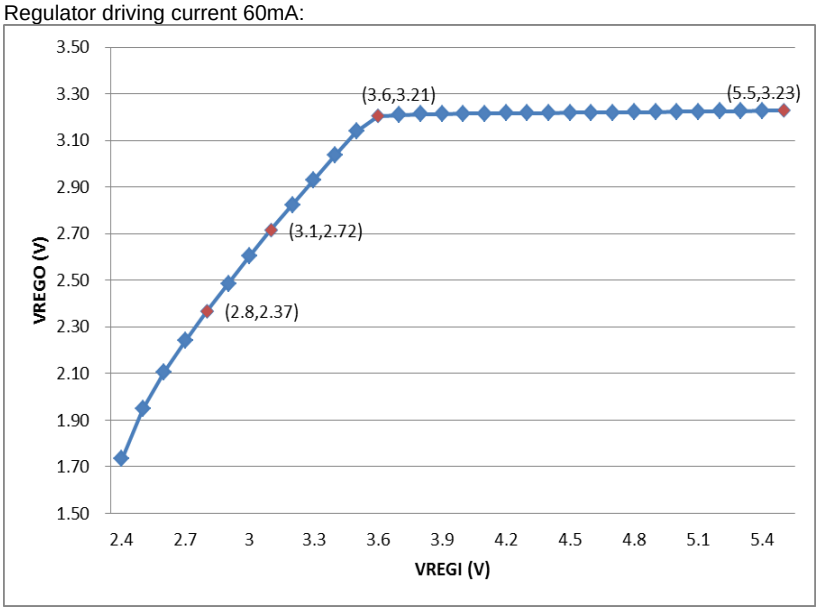
7.8. Regulator Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage	VREGI	2.3	-	5.5	V	
Maximum Current Output	$IREGO_{45}$	-	-	60	mA	VDD5V (Regulator in)= 4.5V, △VDD (Regulator out) <100mV
Maximum Current Output	$IREGO_{30}$	-	-	60	mA	VDD5V (Regulator in)= 3.0V, △VDD (Regulator out) <300mV
Output Voltage	VREGO	3.135	3.3	3.465	V	VREGI > 3.5V
Standby Current	IRGES	-	2.5	-	uA	No load

Regulator driving current 30mA:

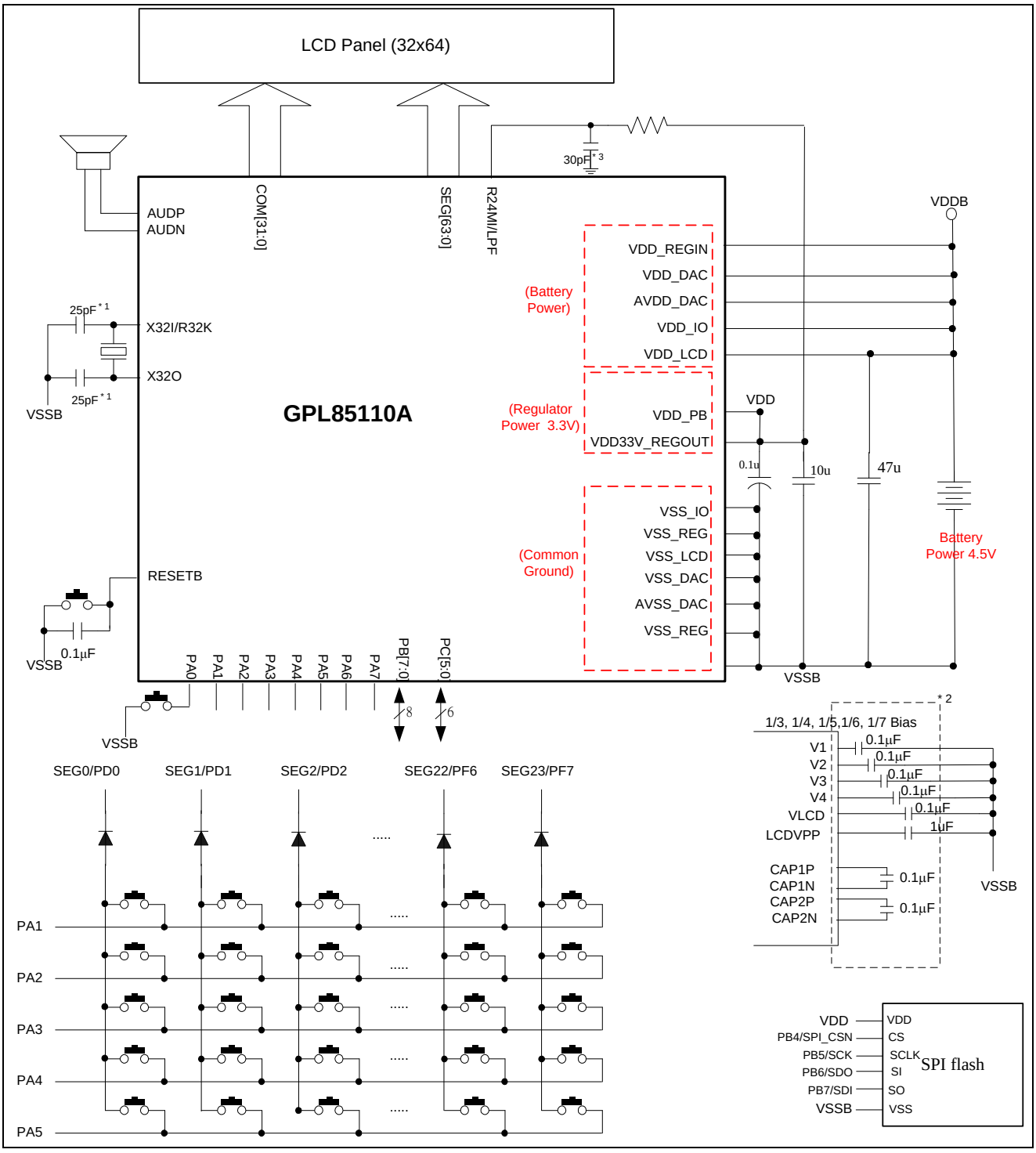


Regulator driving current 60mA:



8. APPLICATION CIRCUITS

8.1. 2048 Dots LCD Driver, 64 Segments × 32 Commons, for 3-battery Application, Internal 3.3V Regulator Enabled, ROSC24M XTAL32K Selected, PB[4:7] Connected to 3.3V SPI Flash using Internal 3.3V Regulator Power - (1)

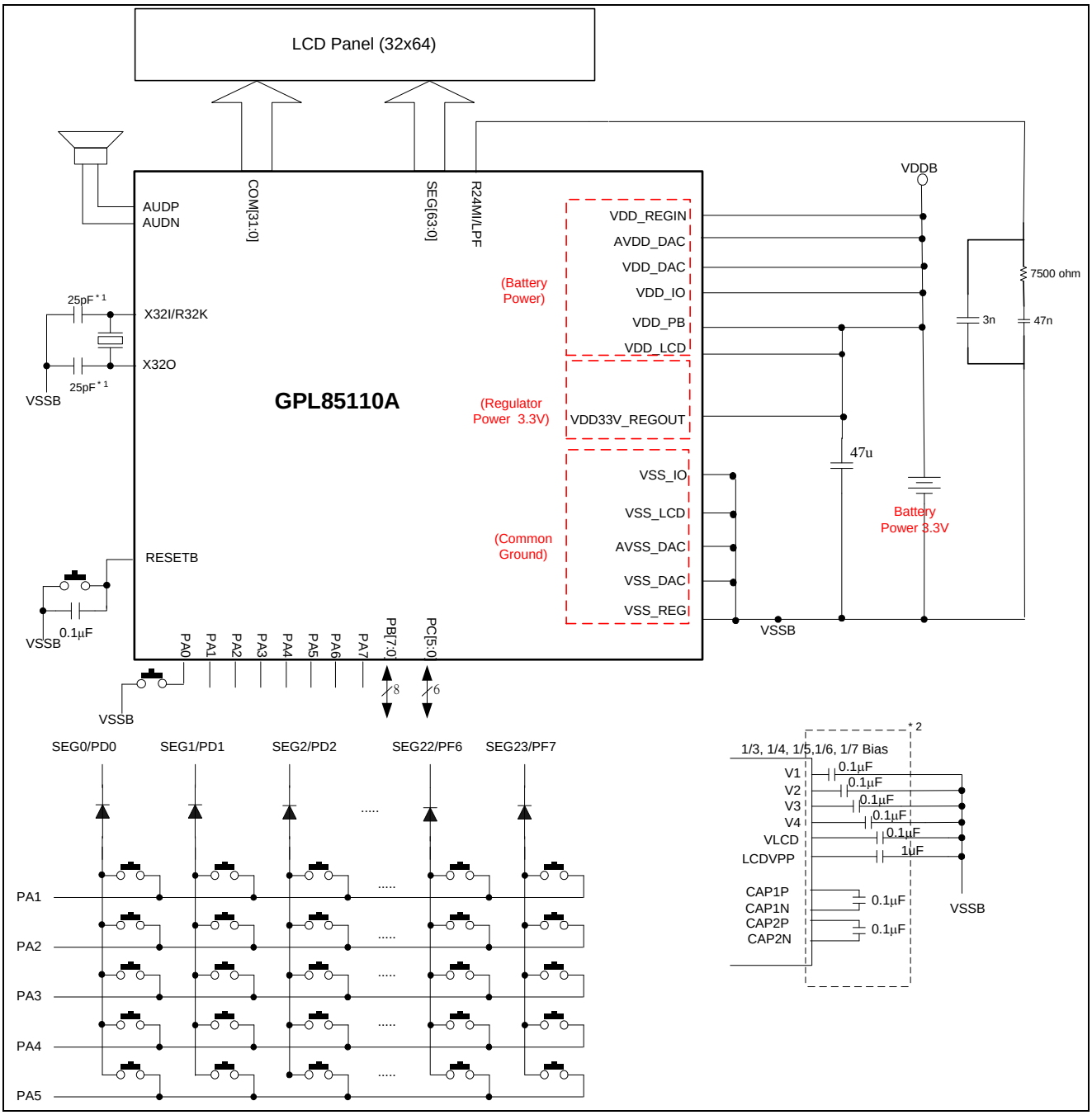


Note*1: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and CL1=CL2 =26~36pF (including PCB parasitic loading, for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF).

Note*2: These capacitor values are for design guidance only. The ratio of capacitance of LCDVPP to the capacitance of CAP1N/CAP1P/CAP2N/CAP2P is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and cannot be larger than capacitance of LCDVPP. However, for larger LCD panel, we recommend the following: 1uF capacitance for VLCD, V1~V4, 2.2uF capacitance for LCDVPP, and 0.22uF capacitance for CAP1P/ CAP1N/ CAP2P/ CAP2N.

Note*3: This capacitor can be removed if this node is immune from noise.

8.2. 2048 Dots LCD Driver, 64 Segments × 32 Commons, Internal 3.3V Regulator Disabled, for 2-battery Application, System PLL XTAL32K Selected - (2)



Note*1: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and CL1=CL2 =26~36pF (including PCB parasitic loading, for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF).

Note*2: These capacitor values are for design guidance only. The ratio of capacitance of LCDVPP to the capacitance of CAP1N/ CAP1P/ CAP2N/ AP2P is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and cannot be larger than capacitance of LCDVPP. However, for larger LCD panel, we recommend the following: 1uF capacitance for VLCD, V1~V4, 2.2uF capacitance for LCDVPP, and 0.22uF capacitance for CAP1P/ CAP1N/ CAP2P/ CAP2N.

9. ORDERING INFORMATION

Product Number	Package Type
GPL85110A -NnnV-C	Chip form

Note1: Code number (NnnV) is assigned for customer.

Note2: Code number (N = A-Z or 0-9, nn=00-99); version (V = A - Z)

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
Jul 22, 2016	1.3	update IOH/IOL range	9-11
Jul 16, 2014	1.2	update description of regulator	12
Aug 13, 2013	1.1	update VDD_IO/VSS_IO description, update application circuit for 32K xtal	6,14-15
Nov 07, 2012	1.0	Release to 1.0	4,9-14
Aug 20, 2012	0.2	1. Modify some items of section 5.1 SIGNAL DESCRIPTIONS. 2. Add section 7 and section 8.	5-6 9-13
Jun. 05, 2012	0.1	Original	10