DATA SHEET

GPL87103A

Low Power 432 Dots LCD Controller with 24KB ROM

Mar. 15, 2016

Version 1.1

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LOW POWER 432 DOTS LCD CONTROLLER WITH 24KB ROM

1. GENERAL DESCRIPTION

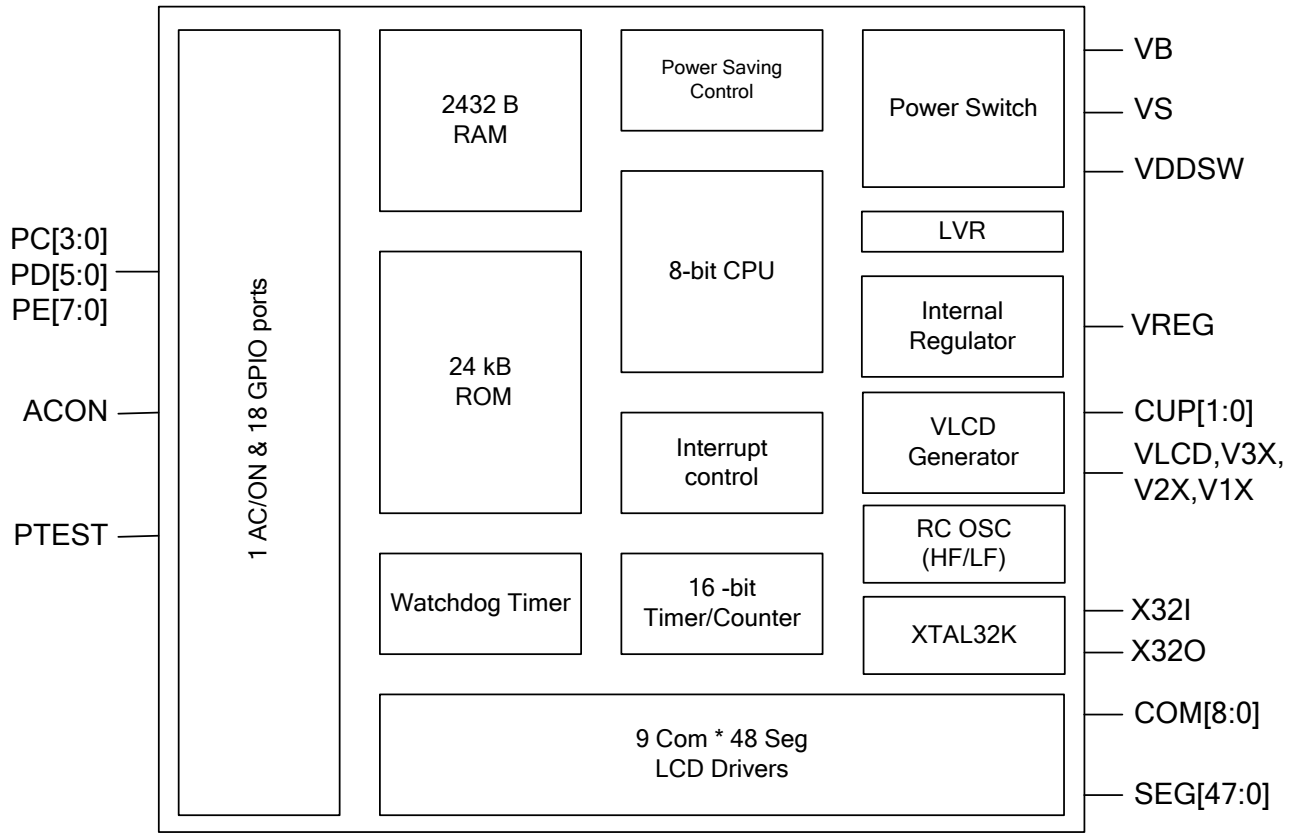
GPL87103A, a special designed CMOS 8-bit microprocessor by Generalplus, offers the best cost/performance ratio in the industry for LCD application, equipping RAM, ROM, I/Os, an interrupt controller, and an automatic display controller/driver in a small device. Its extraordinary features is the capability of operating in low voltage range from 1.2V ~ 3.6V and also operating under low power that is suitable for solar cell environment. It also builds in an internal power switch to select two-way power source automatically and facilitates user applying for solar cell and battery co-operation application. This device is suitable for many application fields such as low power calculator and other LCD related products required either only one solar cell or battery application, or even two way power source.

2. FEATURES

- Built-in 8-bit processor
- 2432-byte SRAM
- 24K-byte ROM(include 2KB test code ROM size)
- 54 byte DPRAM
- Built-in 225k/500k/1000k/1800kHz RC oscillator for system operation
  - adjustable CPU clock speed : 1, 1/2, 1/4, 1/8, 1/16 for R_{OSC}
  - 1000k/1800kHz CPU clock speed only can be used at operation voltage 1.8V~3.6V
- Built-in 30.72kHz RC oscillator & 32768Hz Crystal oscillator circuit for timebase
- Low operating voltage: 1.2 V – 1.8 V@0 ~ 70℃
  1.8 V – 3.6 V@-20～70℃
- Low standby current, I_{STBY} < 1uA @3.6V, 25℃
- 18 general I/O pins.
  - PD[5:0](PD[1:0] share with 2 Buzzer)
  - PC[3:0]
  - PE[7:0]
  - Built-in 2 x RFC function (PD2 used as input, PD[5:3] used as output)
- LCD configurations: 9 coms x 48 segs (MAX) , 3x48, 4x48, 5x48, 6x48, 8x48
- LCD 1/3 ,1/4 bias; 1/3, 1/4, 1/5, 1/6, 1/8, 1/9 duty
- One 16-bit reloadable timer/counter
- Watchdog mode (~2 seconds)
- 6 interrupt sources
  (TMBB, TMBA, 128Hz, 2KHz, Timer, EXT(PD2))
- Power down mode
  (wake-up source: key input, TMBB, TMBA,128Hz, Timer)
- Built_in power switch for two-way power source
  - 15uA @ 3.6V, F_{CPU} = 225KHz for operating mode
  - 3 uA @ 3.6V, F_{CPU} = 225KHz for halt mode
  - I stby < 1uA @ 1.5V
- Built_in internal regulator for LCD operation, 5-level contrast control
- Built_in internal regulator for system operation
- Built_in Low voltage reset to avoid system away from abnormal operation at low voltage

Note1: TMBB: 4KHz, 1KHz, 128Hz, 64Hz, 32Hz, 16Hz, 8Hz or 4Hz
Note2: TMBA: 2Hz or 1Hz

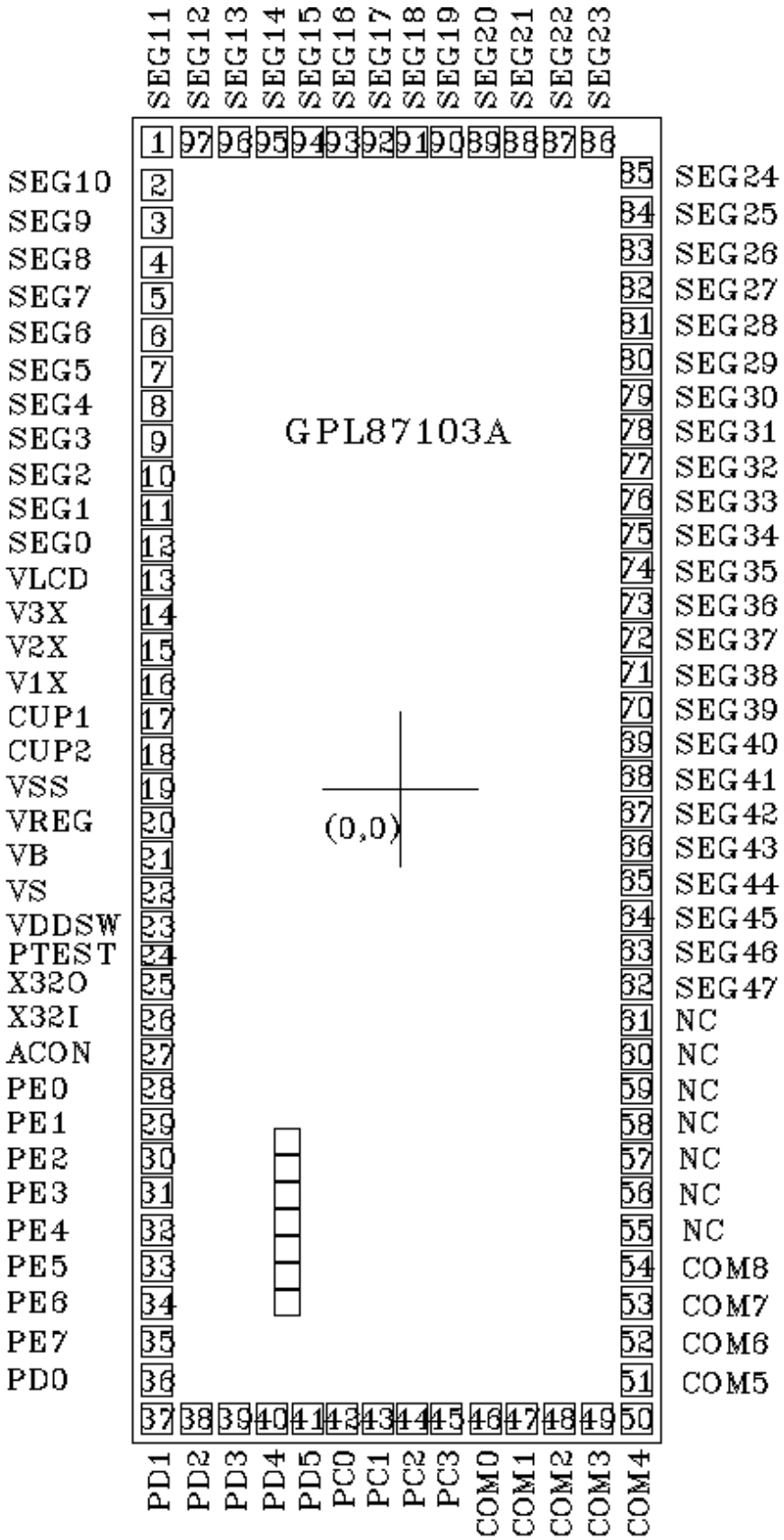
3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	Type	Description
VS	I	Solar cell power input
VB	I	Battery power input
VDDSW	O	Power switch output
VREG	O	Internal regulator output
VSS	I	Ground input
COM[8:0]	O	LCD driver common output
SEG[47:0]	O	LCD driver segment output
PD[5:0]	I/O	GPIO I/O port. (PD[1:0] share with 2 Buzzer) In RFC application, PD[5:3]used as pass-through (output) pin and connected to sensor. PD2 used as input-floating pin and connected to sensor & capacitor.
PC[3:0]	I/O	GPIO I/O port
PE[7:0]	I/O	GPIO I/O port
ACON	I	Clear or system power on pin (active low) and 4ms de-bounce circuit inside
PTEST	I	Test mode input pin (active high)
X32I	I	32768Hz crystal input
X32O	O	32768Hz crystal output
V1X V2X V3X VLCD	O	VLCD generator output
CUP1 CUP2	I	Inputs for setting LCD bias

4.1. PAD Assignment



Note1: This IC substrate should be connected to VSS or floated.

Note2: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as closed as possible.

5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The 8-bit microprocessor in GPL87103A is a high performance processor equipped with Accumulator, Program Counter, X Register, Y Register, Stack pointer and Processor Status Register (this is the same as the CPU6502 instruction structure).

5.2. Clock Source

The GPL87103A equips with two groups of clock sources:

(1) High speed frequency(RCHF) supports the entire system operation. It provides four frequency options, 225K /500K/ 1000K/ 1800KHz and can be selected by Register $18H for different application requirements. GPL87103A provides programmable CPU clock speeds, 1, 1/2, 1/4, 1/8, or 1/16 of RCHF for power saving.

(2) Low speed frequency controls LCD frame rate and time base timer. It comes from XTAL32K or IOSC30K selected by mask option.

5.3. ROM/RAM Area

The GPL87103A provides 24K-byte ROM that can be defined as the program area and its address locates from $4000 to $FFFF. Its RAM consists of 2432 bytes (including Stack) at locations from $60 through $9DF.

5.4. Stop Clock Mode

The GPL87103A provides a power saving mode for those applications required very low stand-by current. Users can simply enable the wake-up sources to stop the CPU clock by writing the STOP CLOCK Register ($09). By doing that, CPU will enter standby mode and the RAM and I/Os remain in their previous states until being awakened. There are five wake-up sources in the GPL87103A, Port PortE wake-up, TMBA, TMBB, T128Hz or Timer wake-up. After the GPL87103A is awakened, CPU will go to the next state of Sleep. Wake-up action will not affect RAM and I/Os.

Note1: TMBB: 4KHz, 1KHz, 128Hz, 64Hz, 32Hz, 16Hz, 8Hz or 4Hz

Note2: TMBA: 2Hz or 1Hz

5.5. I/O Ports

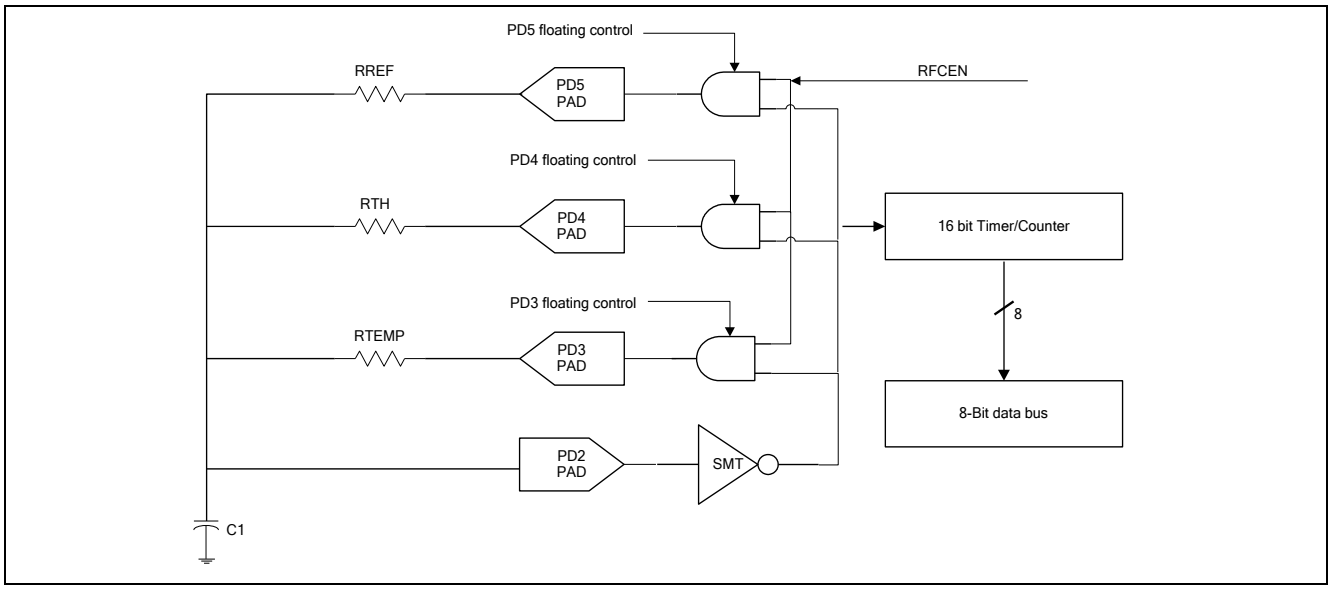
The GPL87103A has three ports: PortC, PortD and PortE. These port pins all equip some special features for key board scan. In general, when an initial reset starts, all ports are used as a general purpose input port. PortC, PortD, and PortE contain three parts: data, direction and attribution registers. Programmer should follow the following table to set each I/O function with corresponding bit in each ports.

PortC[3:0], PortD[5:0] , PortE[7:0]

Attribution	Direction	Data	Function	Description
0	0	0	Input with pull-low	General Purpose I/O function
0	0	1	Pure Input	
0	1	0	Output Low	
0	1	1	Output High	
1	1	0	Pad Floating	Special function

5.6. RFC Function

The RFC (Resistor to Frequency Converter) circuit contains a RC oscillation circuit and a 16-bit timer/counter to calculate the resistance of temperature or humidity sensor related to reference resistor. The circuit is shown below.



5.7. LCD Controller

GPL87103A contains a LCD controller/driver that provides the capability of driving 9 commons and 48 segments LCD. To reduce CPU loading, a display buffer is designed for mapping to LCD. A LCD dot/pattern is set ON or OFF by programming the corresponding bit of the display buffer. In addition, the LCD bias can be programmed as 1/3 or 1/4. The duty can be selected as 1/3, 1/4, 1/5, 1/6, 1/8 or 1/9. The frame rate is set to 85Hz at 1/9 duty and 77Hz at 1/5 duty. When the 1/3, 1/4, 1/6 or 1/8 duty selected, its frame rate is set to 80Hz. The frame rate is measured when low speed frequency equals to 30.72KHz.

5.8. LCD Voltage Generation

The GPL87104A offers a voltage regulator and a charge-pumping circuit. Users can get the desired VLCD by changing the output reference voltage (writing to register) of the voltage regulator. Enabling the voltage regulator and charge-pumping circuit gets a stable VLCD that will not be affected by VDD. The VLCD is adjustable from 3V to 4.5V with 5 levels at 1/3bias, or 4.0V to 6.0V with 5 levels at 1/4bias. It is suggested that VLCD must be higher than VDD or abnormal operation will occur.

5.9. Buzzer Driver

PD[1:0] can be used as buzzer output. When $16.b1 = b0 = '1', PD.1 and PD.0 are set for buzzer output. Or else when b1 = b0 = '0', PD.1 and PD.0 are set to normal I/O. When counter overflows, it will toggle PD.1 and PD.0 for driving buzzer.

5.10. Auxiliary Calculation Hardware

GPL87103A contains auxiliary calculation hardware. This hardware allows some nibble operations to accomplish only at one store and load instruction. The original data content should first be stored at the register ($50, $51) and then, many decimal operations, e. g. x10, /10 or nibble swap, can be gotten just by executing reading instruction at the relative register ($52~5F). It speeds up many decimal operations that originally need many instructions for one operation.

5.11. Analog Block

In addition to the LCD controller and clock source, GPL87103A also provides many low power and useful analog blocks. The built-in power switch changes the power source automatically between battery and solar cell source and it is helpful for two-way source that is a common solution for many low power system. 1.2V/1.5V internal regulator provides whole system operation at low current environment. Internal low voltage reset analog block prevents the system from abnormal operation at the voltage that is lower than the operation range.

5.12. Mask Options

5.12.1. Low speed clock source selection

1). Rosc30K

2). X'TAL32K

5.12.2. Watchdog timer

1). Enable

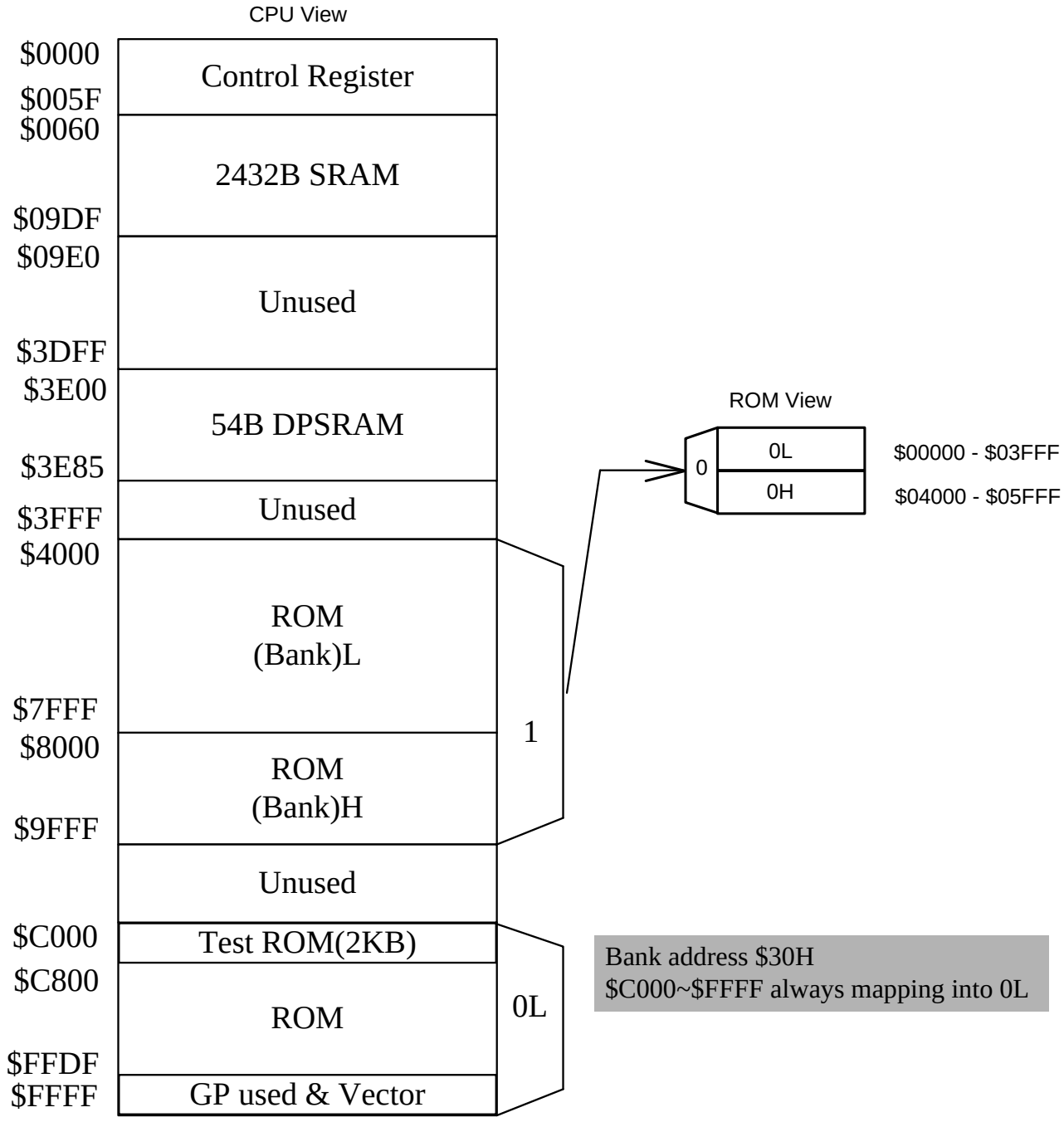
2). Disable

5.12.3. Operation voltage selection

1). 1.2V~1.8V

2). 1.8V~3.6V

5.13. Map of Memory



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3~5 V
Input Voltage Range	V_{IN}	-0.3V to V_+ + 0.3V
Operating Temperature	T_{OPR}	-20℃ to +70℃@1.8V~3.6V
		0℃ to +70℃@1.2V~1.8V
Storage Temperature	T_{STG}	-40℃ to +125℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics(T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Terminal	Test Condition
		Min.	Typ.	Max.			
Operating Voltage	VCC	1.2	-	1.8	V	VDDSW	Operation voltage select 1.2~1.8V
		1.8	-	3.6			Operation voltage select 1.8~3.6V
Hysteresis voltage of power switch	V_{HS}	0.09	0.1	0.13	V	VB, VS	
Internal regulator output for logic	VREG	1.1	1.2	1.4	V	VREG	Operation voltage select 1.2~1.8V
		1.3	1.5	1.7			Operation voltage select 1.8~3.6V
Input High Level	V_{IH}	Vddsw*0.7	-	Vddsw	V	PC, PD, PE	
Input Low Level	V_{IL}	-	-	Vddsw*0.3	V	PC, PD, PE	
Output High Current (I/O)	I_{OH}	2.0	-	-	mA	PC, PD, PE	Vddsw = 3.0V, V_{OH} = 0.7*Vddsw
		0.4	-	-			Vddsw = 1.5V, V_{OH} = 0.7*Vddsw
Output Sink Current (I/O)	I_{OL}	4.0	-	-	mA		Vddsw = 3.0V, V_{OL} = 0.3*Vddsw
		1.0	-	-			Vddsw = 1.5V, V_{OL} = 0.3*Vddsw
Output High Current (Buzzer)	I_{OH}	8	-	-	mA	PD[1:0]	Vddsw = 3.0V, V_{OH} = 0.7*Vddsw
		2	-	-			Vddsw = 1.5V, V_{OH} = 0.7*Vddsw
Output Sink Current (Buzzer)	I_{OL}	10	-	-	mA		Vddsw = 3.0V, V_{OL} = 0.3*Vddsw
		3	-	-			Vddsw = 1.5V, V_{OL} = 0.3*Vddsw
LCD Bias Voltage	Vlcd	-5%	3.0~4.5	+5%	V	Vlcd	1/3 bias, At 25 deg and -8.1mv/℃
			4.0~6.0				1/4 bias,At 25 deg and -10.8mv/℃
Pull low Resistance	R_{PL}	50	140	210	K	PC, PD, PE	VDD=1.2~3.6V
High Frequency	F_H	-20%	225	+20%	kHz		Clock selected as 225kHz *2
		-	500	-			Clock selected as 500kHz *2
			1000				Clock selected as 1000kHz *2
			1800				Clock selected as 1800kHz *2
Low Frequency	F_L	-20%	30.72	+20%	kHz		Low speed clock select as IOSC30K
		-	32.768	-		X32I, X32O	Low speed clock select as XTAL32K
Operating Current	I_{OP}	-	15	20	μA		High Frequency =225kHz, CPU on, LCD on, no load (VDD=3.6V)
		-	35	-	μA		High Frequency =500kHz, CPU on, LCD on, no load (VDD=3.6V)
		-	65	-	μA		High Frequency =1000kHz, CPU on, LCD on, no load (VDD=3.6V)
		-	100	-	μA		High Frequency =1800kHz, CPU on, LCD on, no load (VDD=3.6V)

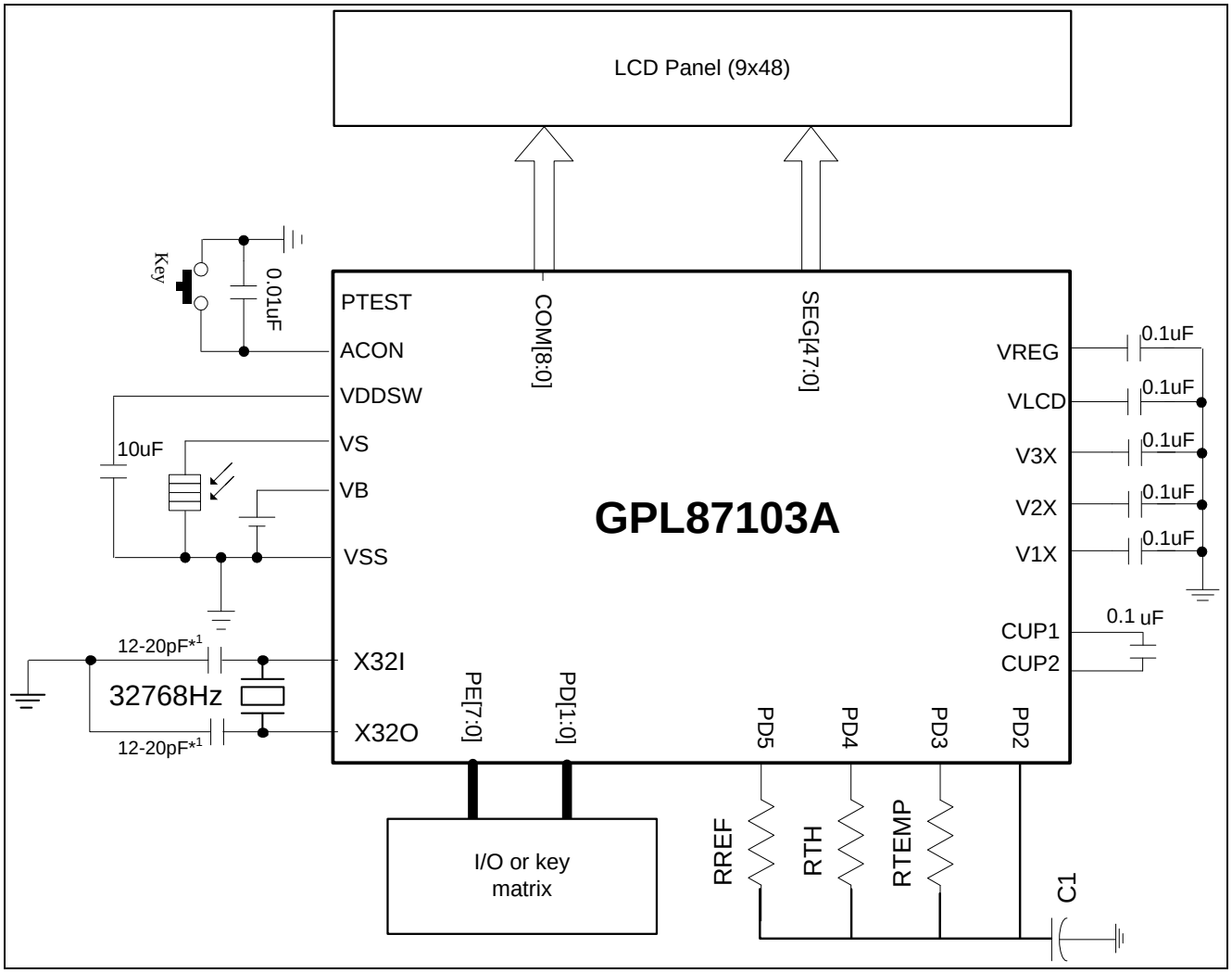
Characteristics	Symbol	Limit			Unit	Terminal	Test Condition
		Min.	Typ.	Max.			
Halt Current	I_{HALT}	-	3.2	4	μA		Low Frequency active, CPU off, LCD on, no load(VDD=3.6V) @50℃
Standby Current	I_{STBY}	-	-	1.0	μA		Clock is stopped, LCD off(VDD=3.6V) @25℃
		-	-	1.5	μA		Clock is stopped, LCD off(VDD=3.6V) @50℃

Note1: Vlcd should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

Note2: Only the main CPU frequency selected in confirm sheet is guaranteed in thee range of +/-20% variation, and the other frequencies may be beyond the range of +/-20% variation.

For example, if 1800KHZ is selected as CPU frequency in confirm sheet, 1800KHZ is varied in the range of +/-20%. The other frequencies such as 225KHZ, 500KHZ, or 1000KHZ may beyond the range of +/-20% variation.

7. APPLICATION CIRCUITS



Note1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL87103A -NnnV-C	Chip form

Note1: Code number (NnnV) is assigned for customer.

Note2: Code number (N = A-Z or 0-9, nn=00-99); version (V = A - Z)

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
Mar. 15, 2016	1.1	modified section 6.2	10-11
Aug. 01, 2011	1.0	1. modified features; 2. modified V4X to Vlcd in block diagram, signal description & PAD assignment; 3. modified section 5.7; 4. removed control register description at section 5.12; 5. modified section 6.1 & 6.2;	15
Nov. 25, 2010	0.1	Original	14