DATA SHEET

GPL87220A
GPL87216A
GPL87208A

Low Power 3072/2048/1536 dots LCD Controller with 160KB/128KB/64KB ROM

Jul. 30, 2013

Version 1.0

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LOW POWER 3072/2048/1536 DOTS LCD CONTROLLER WITH 160KB/128KB/64KB ROM

1. GENERAL DESCRIPTION

GPL87220A/GPL87216A/GPL87208A, a special designed 8-bit CMOS microprocessor, offers one of the best cost/performance ratio LCD controllers in the industry. It embeds RAM, ROM, I/Os, an interrupt controller, and an automatic display controller/driver in a small device. Its extraordinary features is the capability of operating in low voltage range from 1.1V ~ 3.6V and also operating under low power. This device is applicable for many application fields such as low power watch and other LCD related products.

2. FEATURES

■ Built-in 8-bit processor

■ 6048/2464/2464 -byte SRAM

■ 160K/128K/64K -byte ROM(include 2KB test code ROM size)

■ 384/256/192 -byte DPRAM

■ Built-in 225k/500k/1000k/1800k/4000KHz RC oscillator for system operation

- adjustable CPU clock speed : 1, 1/2, 1/4, 1/8, 1/16 for Rosc

- 1000k/1800k/4000kHz CPU clock speed only can be used at operation voltage 1.8V~3.6V

■ Built-in 30.72kHz RC oscillator & 32768 Crystal oscillator circuit for timebase.

■ Low operating voltage: 1.1 V – 3.6 V

■ Low standby current, I_{STBY} < 1uA @3.6V@25℃

■ 36 general I/O pins.

PA[3:0] (PA[3:2]shared with SEG[94:95] @GPL87220A)

PB[7:0] (shared with COM[16:23])

PC[7:0] (shared with COM[24:31] @GPL87220A/GPL87216A)

PD[7:0] (PD6 can be used as EXT2INT, PD2 can be used as EXTINT, PD[1:0] shared with 2 Buzzer)

PE[7:0]

- Built-in 2x RFC function (PD2 or PE3 as input, PD[5:3] or PE[2:0] as output)

■ LCD configurations:

- 32 coms x 96 segs (MAX), 24X94, 16X94, 11X64, 10X64, 9X64, 8X64, 6X64, 5X64, 4X64, 3X64, 2X64 @GPL87220A;

- 32 coms x 64 segs (MAX), 24X64, 16X64, 11X64, 10X64, 9X64, 8X64, 6X64, 5X64, 4X64, 3X64, 2X64 @GPL87216A;

- 24 coms x 64 segs (MAX), 16X64, 11X64, 10X64, 9X64, 8X64, 6X64, 5X64, 4X64, 3X64, 2X64 @GPL87208A;

■ LCD 1/2, 1/3, 1/4, 1/5 bias; 1/2, 1/3, 1/4, 1/5, 1/6, 1/8, 1/9, 1/10, 1/11, 1/16, 1/24, 1/32 duty

■ One 16-bit reloadable timer/counter(Timer0), Two 8-bit reloadable timer/counter（Timer1,Timer2）

■ Serial Peripheral Interface(SPI)

- SPI CSN/SCK/SDI/SDO pin shared with SEG[93:90]

■ 4-channel PWMIO output

- PWM output pin shared with PA[3:0]

■ EL light driver

- ELC, ELP pin share with PA[1:0]

■ Watchdog mode (~2 sec)

■ 12 interrupt sources

IRQ controller

- 2Khz for RTC
- 128Hz
- TMBB（4Hz/8Hz/16Hz/32Hz/64Hz/128Hz/1KHz/4KHz）
- TMBA（1Hz/2Hz）
- EXTINT(PD2)
- EXT2INT(PD6)
- Timer0 overflow
- Timer1 overflow
- Timer2 overflow
- Low battery voltage detection (1.2V/2.0V/2.2V/2.5V)
- DMA
- SPI

■ Power down mode

(wake-up source: key input, TMBB, TMBA, 128Hz, Timer0, Timer1, Timer2)

■ Low power consumption:

- 30uA @ 1.5V, Fcpu = 225KHz for operating mode
- 8 uA @ 1.5V, Fcpu = 225KHz for halt mode
- I stby < 1uA @ 1.5V

■ Built_in internal regulator for LCD operation, 16 level contrast control

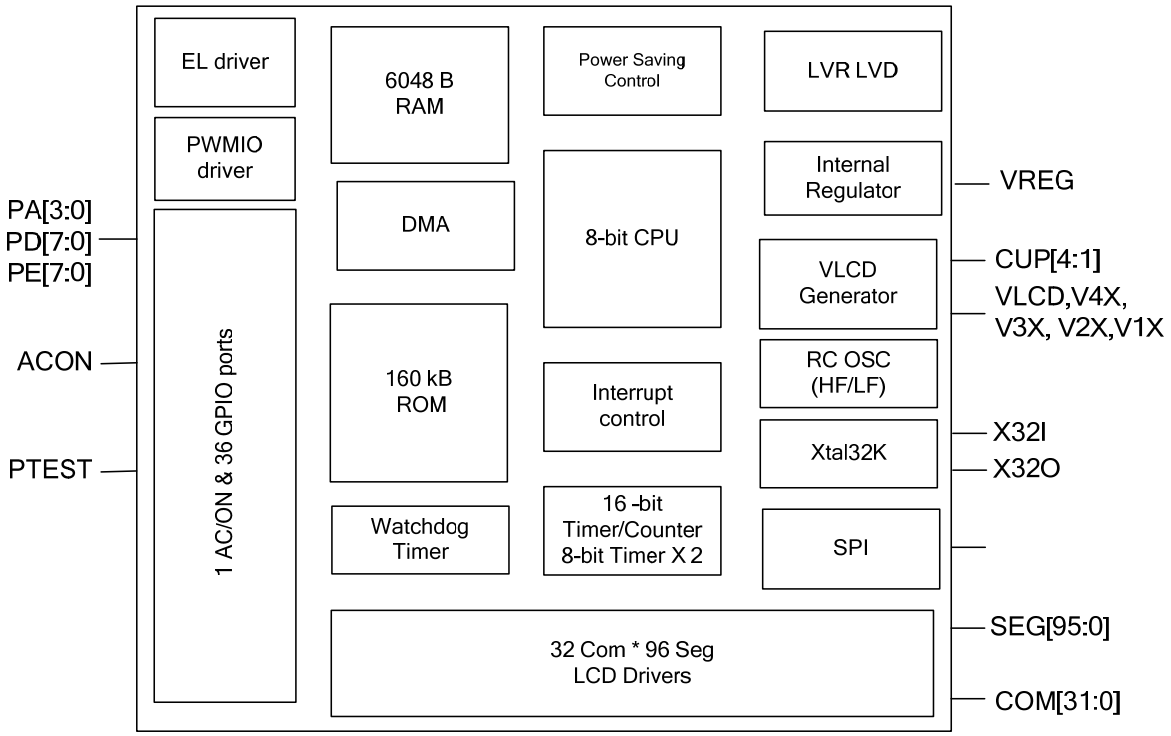
■ Built_in internal regulator for system operation

■ Built_in 1.2V/2.0V/2.2V/2.5V low voltage detector

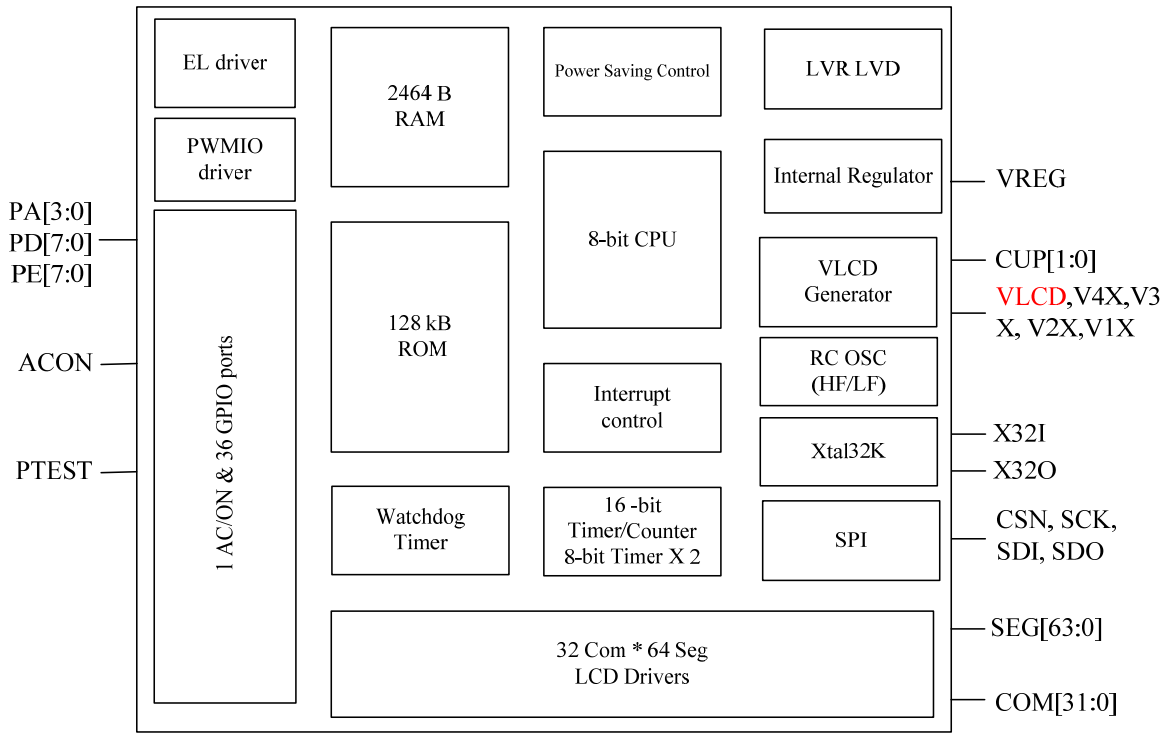
■ Built_in Low voltage reset to avoid system runaway at low voltage.

3. BLOCK DIAGRAM

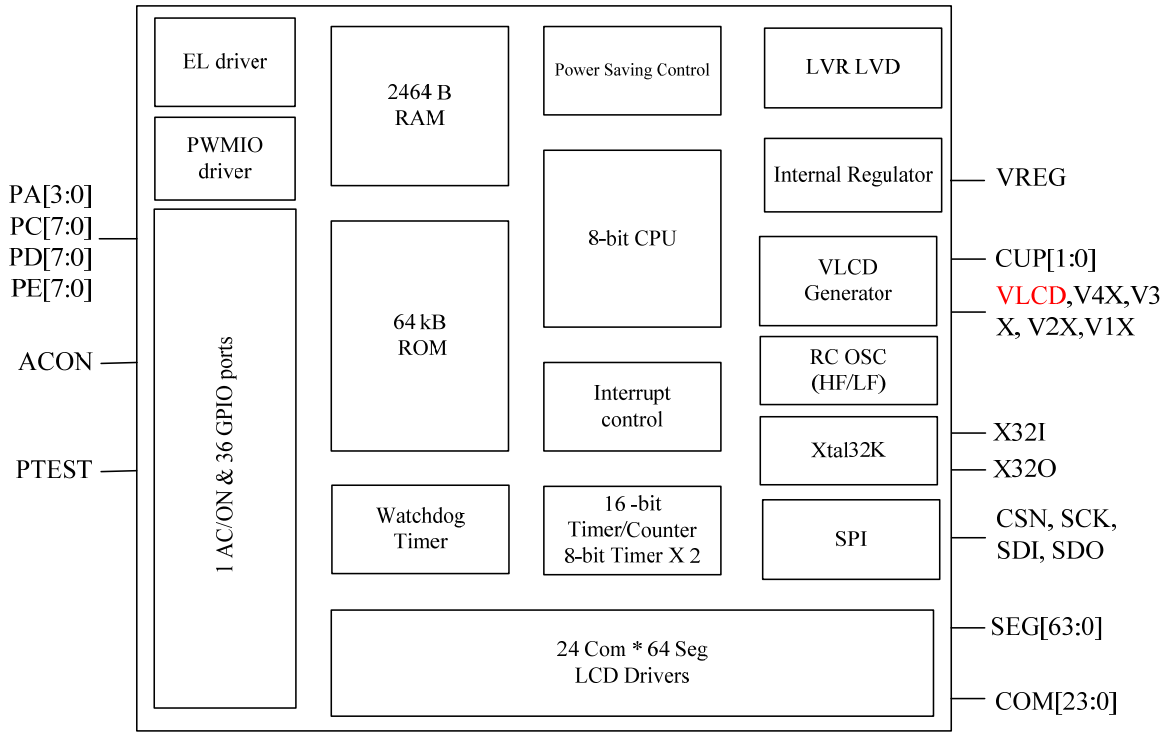
3.1. GPL87220A



3.2. GPL87216A



3.3. GPL87208A



4. SIGNAL DESCRIPTIONS

4.1. GPL87220A

Mnemonic	Type	Description
VDD	I	Power supply voltage input
VREG	O	Internal regulator output.
VSS	I	Ground input.
COM[15:0]	O	LCD driver common output.
COM[23:16]	I/O	LCD driver common output. (COM[23:16] shared with PB[0:7])
COM[31:24]	I/O	LCD driver common output. (COM[31:24] shared with PC[0:7] , COM[31:26] can be option to SEG[93:88]
SEG[87:0]	O	LCD driver segment output.
SEG[89:88]	I/O	LCD driver segment output. (SEG[89:88] shared with X32I/X32O)
SEG[93:90]	I/O	LCD driver segment output. (SEG[93:90] shared with SPI CSN/CLK/SDI/SDO)
SEG[95:94]	I/O	LCD driver segment output. (SEG[95:94] shared with PA[3:2])
PA[1:0]	I/O	GPIO I/O port. (PA[3:0] can be option to PWMIO, PA[1:0] can be option to ELP & ELC)
PE[7:0]	I/O	GPIO I/O port. In RFC2 application, PE[2:0] can be used as pass-through (output) pin and connected to sensor. PE3 can be used as input-floating pin and connected to sensor & capacitor.
PD[7:0]	I/O	GPIO I/O port. (PD7 can be used as clk32K output; PD[1:0] shared with 2 Buzzer) In RFC1 application, PD[5:3] can be used as pass-through (output) pin and connected to sensor. PD2 can be used as input-floating pin and connected to sensor & capacitor.
ACON	I	Clear or system power on pin (active low) and 4ms debounce ckt inside.
PTEST	I	Test mode input pin. (active high)
V1X V2X V3X V4X VLCD	O	VLCD generator output.
CUP1 CUP2 CUP3 CUP4	I	Inputs for setting LCD bias.

Total 160 pads

4.2. GPL87216A

Mnemonic	Type	Description
VDD	I	Power supply voltage input.
VREG	O	Internal regulator output.
VSS	I	Ground input.
COM[15:0]	O	LCD driver common output.
COM[23:16]	I/O	LCD driver common output. (COM[23:16] shared with PB[0:7])
COM[31:24]	I/O	LCD driver common output. (COM[31:24] shared with PC[0:7])
SEG[63:0]	O	LCD driver segment output.
CSN/SCK/SDI/SDO	I/O	SPI interface signal, CSN/SCK/SDI/SDO
PA[3:0]	I/O	GPIO I/O port. (PA[3:0] can be option to PWMIO, PA[1:0] can be option to ELP & ELC)
PE[7:0]	I/O	GPIO I/O port.

Mnemonic	Type	Description
		In RFC2 application, PE[7:5] can be used as pass-through (output) pin and connected to sensor. PE4 can be used as input-floating pin and connected to sensor & capacitor.
PD[7:0]	I/O	GPIO I/O port. (PD7 can be used as clk32K output; PD[1:0] shared with 2 Buzzer) In RFC1 application, PD[5:3] can be used as pass-through (output) pin and connected to sensor. PD2 can be used as input-floating pin and connected to sensor & capacitor.
ACON	I	Clear or system power on pin (active low) and 4ms debounce ckt inside.
PTEST	I	Test mode input pin. (active high)
X32I	I	32768Hz crystal input
X32O	O	32768Hz crystal output
V1X V2X V3X V4X VLCD	O	VLCD generator output.
CUP1 CUP2 CUP3 CUP4	I	Inputs for setting LCD bias.

Total 136 pads

4.3. GPL87208A

Mnemonic	Type	Description
VDD	I	Power supply voltage input.
VREG	O	Internal regulator output.
VSS	I	Ground input.
COM[15:0]	O	LCD driver common output.
COM[23:16]	I/O	LCD driver common output. (COM[23:16] shared with PB[0:7])
PC[7:0]	I/O	GPIO I/O port.
SEG[63:0]	O	LCD driver segment output.
CSN/SCK/SDI/SDO	I/O	SPI interface signal, CSN/SCK/SDI/SDO
PA[3:0]	I/O	GPIO I/O port. (PA[3:0] can be option to PWMIO, PA[1:0] can be option to ELP & ELC)
PE[7:0]	I/O	GPIO I/O port. In RFC2 application, PE[7:5] can be used as pass-through (output) pin and connected to sensor. PE4 can be used as input-floating pin and connected to sensor & capacitor.
PD[7:0]	I/O	GPIO I/O port. (PD7 can be used as clk32K output; PD[1:0] shared with 2 Buzzer) In RFC1 application, PD[5:3] can be used as pass-through (output) pin and connected to sensor. PD2 can be used as input-floating pin and connected to sensor & capacitor.
ACON	I	Clear or system power on pin (active low) and 4ms debounce ckt inside.
PTEST	I	Test mode input pin. (active high)
X32I	I	32768Hz crystal input
X32O	O	32768Hz crystal output
V1X V2X V3X V4X VLCD	O	VLCD generator output.

Mnemonic	Type	Description
CUP1 CUP2 CUP3 CUP4	I	Inputs for setting LCD bias.

Total 136 pads

5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The 8-bit microprocessor in GPL87220A/GPL87216A/GPL87208A is a high performance processor equipped with Accumulator, Program Counter, X Register, Y Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure).

5.2. Clock Source

The GPL87220A/GPL87216A/GPL87208A equips with two groups of clock sources:

(1) High speed frequency (RCHF) to support the whole system operation. It provides five frequency 225k /500k/ 1000k/ 1800k/ 4000kHz and can be selected by register $18H that rely on user different application. GPL87220A/ GPL87216A/ GPL87208A provides programmable CPU clock speed 1, 1/2, 1/4, 1/8, or 1/16 of RCHF for power saving.

(2) Low speed frequency to control LCD frame rate and time base timer. It comes from XTAL32K or IOSC30K selected by mask option.

5.3. ROM/RAM Area

The GPL87220A/GPL87216A/GPL87208A provides 160K/ 128K/ 64K-byte ROM that can be defined as the program area and its address locates from $4000 to $FFFF. Its RAM consists of 6048/ 2464/2464 bytes (including Stack) at locations from $60 through $17FF/$9FF/$9FF.

5.4. Stop Clock Mode

The GPL87220A/GPL87216A/GPL87208A provides a power saving mode for those applications required very low stand-by current. Users can simply enable the wake-up sources to stop the CPU clock by writing the STOP CLOCK Register ($09). By doing that, CPU will enter standby mode and the RAM and I/Os remain in their previous states until being awakened. There are seven wake-up sources in the GPL87220A/GPL87216A/ GPL87208A: Port PortE wake-up, TMBA, TMBB, T128Hz, Timer0, Timer1 or Timer2 wake-up. After the GPL87220A/GPL87216A/ GPL87208A wakes up, CPU will execute the next instruction right after where the sleep took place. Wake-up action will not affect RAM and I/Os.

Note1: TMBB: 4KHz, 1KHz, 128Hz, 64Hz, 32Hz, 16Hz, 8Hz or 4Hz
Note2: TMBA: 2Hz or 1Hz

5.5. I/O Ports

The GPL87220A/GPL87216A/GPL87208A has five ports: PortA, PortB, PortC, PortD and PortE. These port pins all equip with special features for key board scan. In general, when an initial reset start, all ports are used as a general purpose input port. PortA, PortB, PortC, PortD and PortE contain three parts: data, direction and attribution registers. Programmer should follow the table below to set each I/O function with corresponding bit in each port.

PortA[3:0], PortB[7:0], PortC[7:0], PortD[7:0] , PortE[7:0]

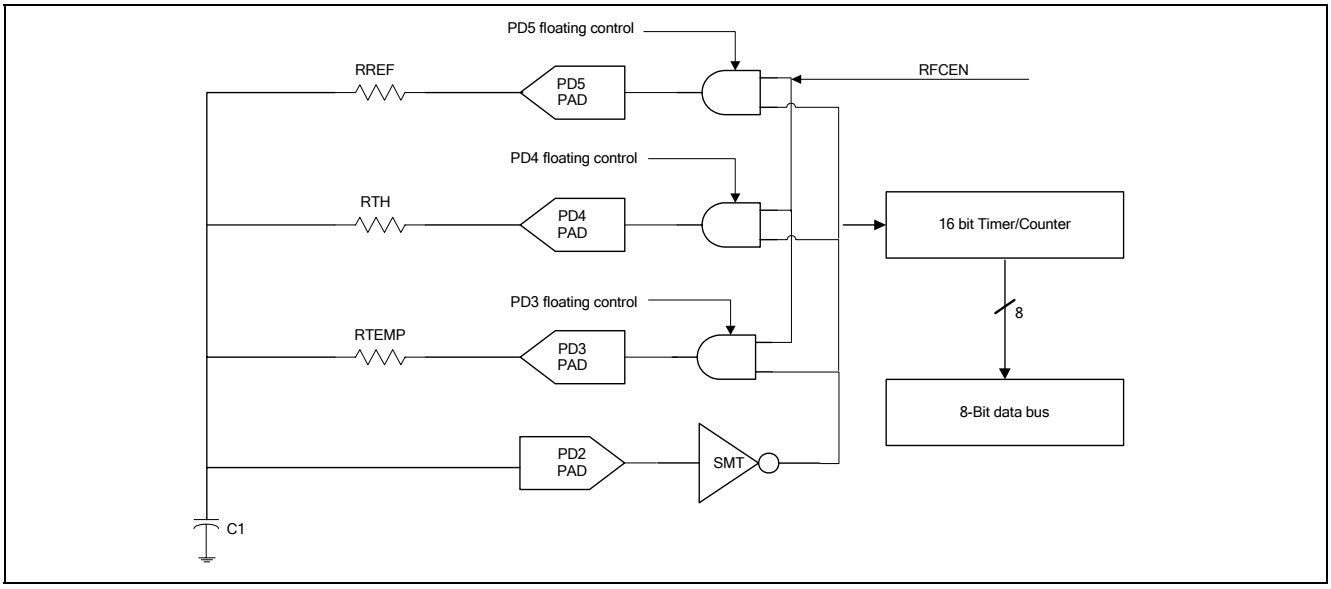
Attribution	Direction	Data	Function	Description
0	0	0	Input with pull-low	General Purpose I/O function
0	0	1	Pure Input	
0	1	0	Output Low	
0	1	1	Output High	
1	1	0	Pad Floating	Special function

5.6. RFC Function

The RFC (Resistor to Frequency Converter) circuit contains a RC oscillation circuit and a 16-bit timer/counter to calculate the resistance of temperature or humidity sensor relative to reference resistor.

PD[5:2] or PE[7:4] used as RFC pin selected by mask option RFCSHEN.

The circuit is shown below.



5.7. LCD Controller

GPL87220A/GPL87216A/GPL87208A contains a LCD controller/driver that provides the capability of driving 32/32/24 commons and 96/64/64 segments LCD. To light the overhead of CPU, a display buffer is designed for mapping to LCD. A LCD dot/pattern is set ON or OFF by programming the corresponding bit of the display buffer. In addition, the LCD bias can be programmed as 1/3, 1/4 or 1/5. The duty can be selected as 1/2, 1/3,1/4, 1/5, 1/6, 1/8, 1/9, 1/10, 1/11, 1/16, 1/24 or 1/32. The frame rate is set to 85Hz at 1/9 duty; 77Hz at 1/5 or 1/10 duty; and 87Hz at 1/11 duty. When the other duty selected, its frame rate is set to 80Hz. The frame rate is measured when low speed frequency equal 30.72KHz.

5.8. LCD Voltage Generation

The GPL87220A/GPL87216A/GPL87208A offers a voltage regulator and a charge-pumping circuit. Users can get the desired VLCD by changing the output reference voltage (writing to register) of the voltage regulator. Enabling the voltage regulator and charge-pumping circuit gets a stable VLCD that will not be affected by VDD. The VLCD is adjustable from 3V to 4.5V with 16 levels at 1/3bias, 4.0V to 6.0V with 16 level at 1/4bias, 5.0V to 6.5V with 10 level at 1/5 bias, 3.0V at 1/2bias.

5.9. Buzzer Driver

PD[1:0] can be used as buzzer output. When $16.b1 = b0 = '1', PD.1 and PD.0 are set for buzzer output. Or else when b1 = b0 = '0', PD.1 and PD.0 are set to normal I/O. When Timer0 overflows, it will toggle PD.1 and PD.0 for driving buzzer.

5.10. Auxiliary Calculation Hardware

GPL87220A/GPL87216A/GPL87208A contains auxiliary calculation hardware. This hardware allows some nibble operation to accomplish only at one store and load instruction. The original data content should be stored at the register ($50, $51) firstly, then many decimal operation, ex: x10,/10 or nibble swap, can be gotten just by executing reading instruction at the relative register ($52~5F). It speeds up many decimal operations that originally need many instructions for one operation.

5.11. Hardware PWMIO

Hardware PWMIO supports 4 LED outputs from PA0~3 with brightness control of 256 levels. The clock source of PWMIO can be selected by user's request.

5.12. DMA function

GPL87220A/GPL87216A/GPL87208A contains DMA for direct access from ROM/RAM to RAM/DPRAM. User can select access mode by control register including ROM to DPRAM, ROM to RAM, RAM to DPRAM and DPRAM to RAM. Status flag will go high when DMA action is done. User can choose to generate DMA endflag interrupt or not.

5.13. Analog Block

In addition of the LCD controller and clock source, GPL87220A/GPL87216A/GPL87208A also provides many low power and useful analog block.

1.2V or 1.5V internal regulator by mask option provides whole system operation at low current environment.

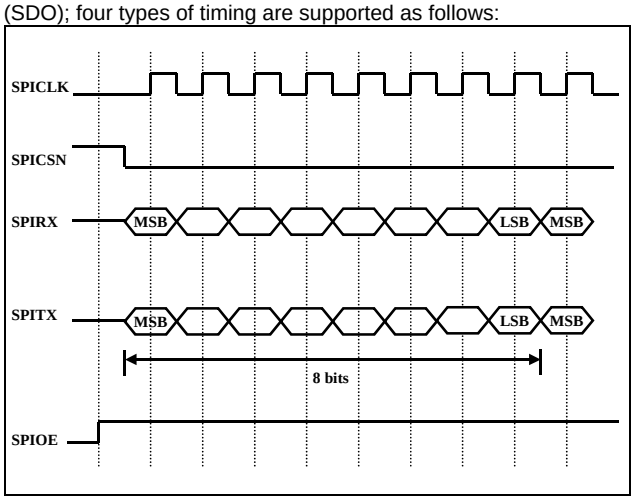
It also provides a 1.2V/2.0V/2.2V/2.5V voltage detector to detect the voltage of the VDD pin, User can read the state of VDD from port $1B. If the VDD is higher than LVD level (1.2V/ 2.0V/ 2.2V/ 2.5V), $1B.bit0 will be '0', else will be '1'.

Internal low voltage reset analog block prevents the system from

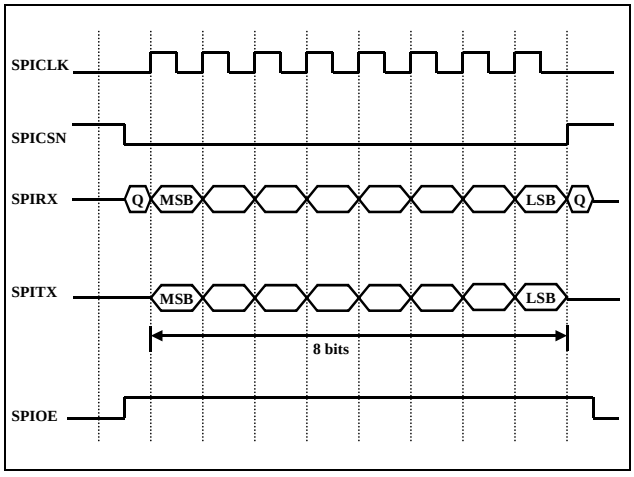
runaway at the voltage that is lower than the operation range.

5.14. SPI Controller

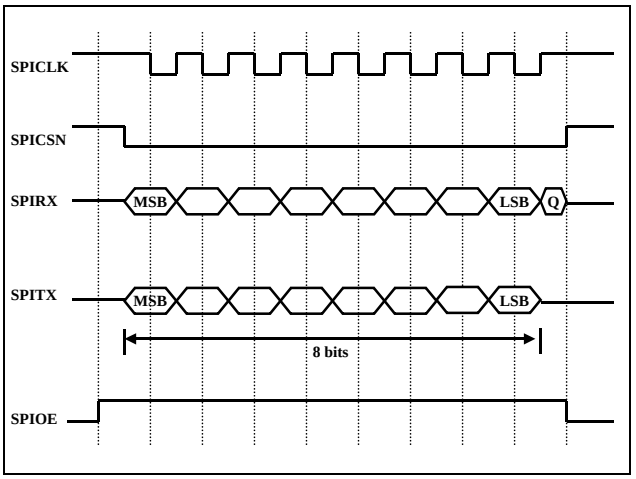
A Serial Peripheral Interface (SPI) controller is built in GPL87220A/GPL87216A/GPL87208A to facilitate communicating with other devices and components. There are four control signals on SPI including SPICSN, SPICLK (SCK), SPIRX (SDI), and SPITX (SDO); four types of timing are supported as follows:



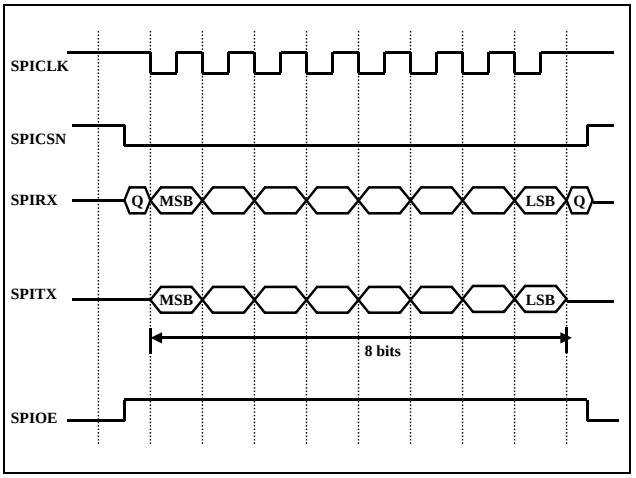
Master Mode, SPO = 0, SPH=0



Master Mode, SPO = 0, SPH=1



Master Mode, SPO = 1, SPH=0



Master Mode, SPO = 1, SPH=1

5.15. Mask Options

5.15.1. Low speed clock source select

1). Rosc30K

2). X'TAL32K

5.15.2. Watchdog timer

1). Enable

2). Disable

5.15.3. Internal 1Mohm reset pull high resistor

1). Enable

2). Disable

5.15.4. Low voltage detect function select

1). Disable

2). Enable

5.15.5. COM/PC pin share select

1). Pin used as PC[7:0]

2). Pin used as COM[24:31]

5.15.6. COM/PB pin share select

1). Pin used as PB[7:0]

2). Pin used as COM[16:23]

5.15.7. SEG/PA pin shared selection

1). Pin used as PA[3:2]

2). Pin used as SEG[94:95]

5.15.8. RFC function control

1). Disable

2). Enable

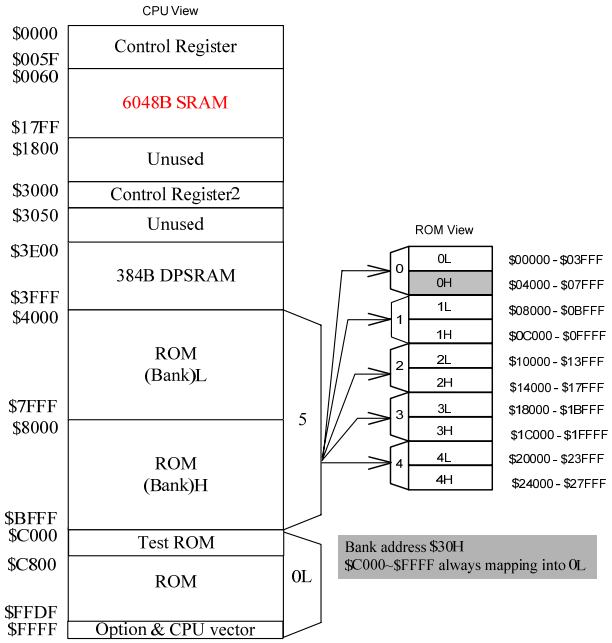
5.15.9. RFC function shift control

1). PD[5:2] used as RFC function

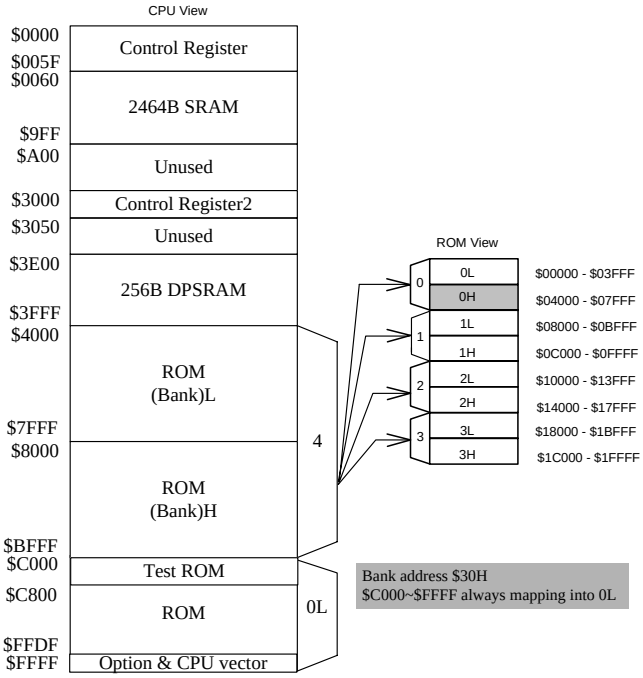
2). PE[7:4] used as RFC function

5.16. Map of Memory

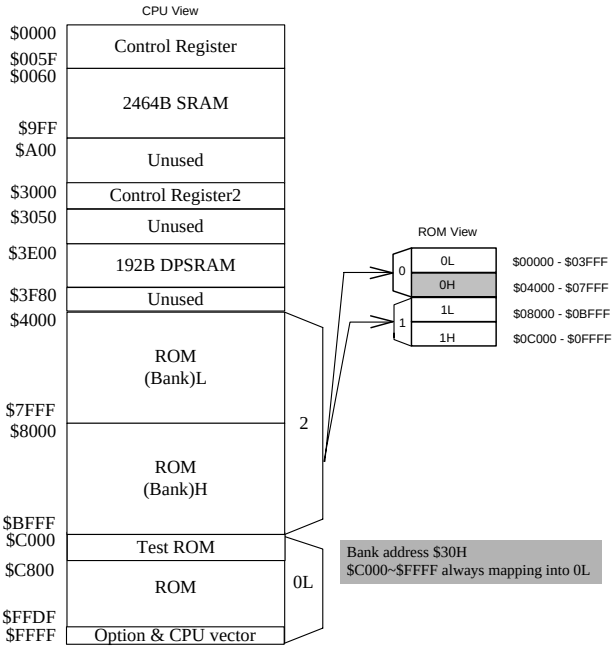
5.16.1. GPL87220A



5.16.2. GPL87216A



5.16.3. GPL87208A



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3~5 V
Input Voltage Range	V_{IN}	-0.3V to V_+ + 0.3V
Operating Temperature	T_{OPR}	-20℃ to +70℃
Storage Temperature	T_{STG}	-40℃ to +125℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

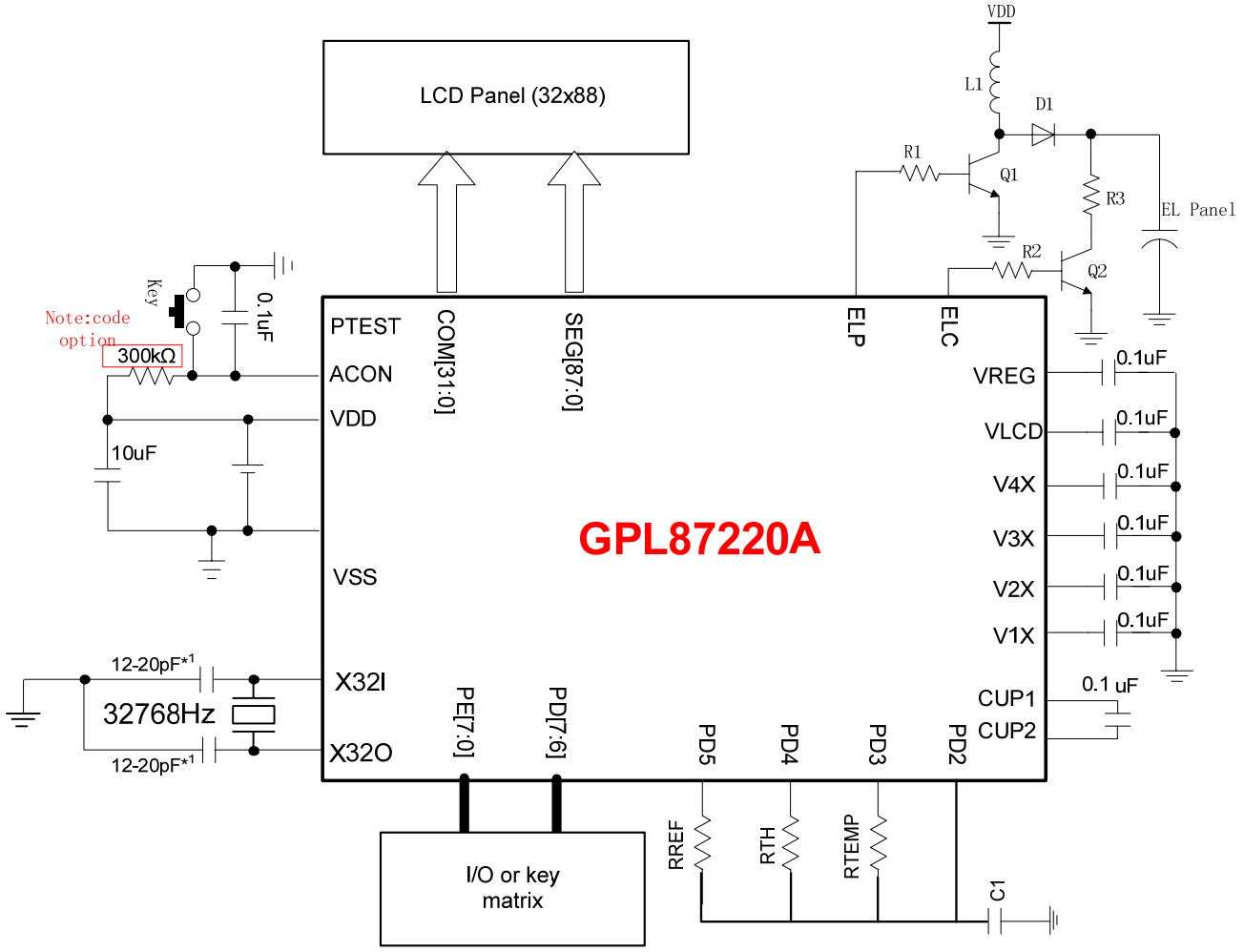
6.2. DC Characteristics

Characteristics	Symbol	Limit			Unit	Terminal	Test Condition
		Min.	Typ.	Max.			
Operating Voltage	VCC	1.1	-	1.8	V	VDD	Operation voltage select 1.1~1.8V
		1.8	-	3.6			Operation voltage select 1.8~3.6V
Internal regulator output for logic	VREG	1.0	1.2	1.3	V	VREG	Operation voltage select 1.1~1.8V
		1.3	1.5	1.7	V	VREG	Operation voltage select 1.8~3.6V
Input High Level	V_{IH}	Vdd*0.7	-	Vdd	V	PA,PB,PC, PD,PE	
Input Low Level	V_{IL}	-	-	Vdd*0.3	V		
Output High Current (I/O)	I_{OH}	2.0	-	-	mA	PA,PB, PC,PD,PE	Vdd = 3.0V, V_{OH} = 0.7*Vdd
		0.4	-	-			Vdd = 1.5V, V_{OH} = 0.7*Vdd
Output Sink Current (I/O)	I_{OL}	4.0	-	-	mA		Vdd = 3.0V, V_{OL} = 0.3*Vdd
		1.0	-	-			Vdd = 1.5V, V_{OL} = 0.3*Vdd
Output High Current (Buzzer)	I_{OH}	8.0	-	-	mA	PD[1:0]	Vdd = 3.0V, V_{OH} = 0.7*Vdd
		2.0	-	-			Vdd = 1.5V, V_{OH} = 0.7*Vdd
Output Sink Current (Buzzer)	I_{OL}	10.0	-	-	mA		Vdd = 3.0V, V_{OL} = 0.3*Vdd
		3.0	-	-			Vdd = 1.5V, V_{OL} = 0.3*Vdd
LCD Bias Voltage	VLCD	-5%	3.0	+5%	V	VLCD	1/2 bias At 25 deg and -5.4mv/℃
			3.0~4.5				1/3 bias At 25 deg and -8.1mv/℃
			4.0~6.0				1/4 bias At 25 deg and -10.8mv/℃
			5.0~6.25				1/5 bias At 25 deg and -13.5mv/℃
Pull low Resistance	R_{PL}	-	150	-	Kohm	PA,PB,PC, PD,PE	VDD=1.5V
		-	60	-			VDD=3.0V
High Frequency	F_H	-20%	225	+20%	kHz		Clock select as 225kHz
		-	500	-			Clock select as 500kHz
			1000				Clock select as 1000kHz
			1800				Clock select as 1800kHz
			4000				Clock select as 4000kHz
Low Frequency	F_L	-20%	30.72	+20%	kHz		Low speed clock select as IOSC30K
		-	32.768	-		X32I,X32O	Low speed clock select as XTAL32K
Operating Current	I_{OP}	-	30	-	uA		High Frequency =225kHz, CPU on, LCD on, no load (VDD=3.6V)
		-	600	-	uA		High Frequency =4000kHz, CPU on, LCD on, no load (VDD=3.6V)
Halt Current	I_{HALT}	-	8	-	uA		Low Frequency active, CPU off, LCD on, no load(VDD=3.6V) @50℃

Characteristics	Symbol	Limit			Unit	Terminal	Test Condition
		Min.	Typ.	Max.			
Standby Current	I_{STBY}	-	-	1	uA		Clock is stopped, LCD off(VDD=3.6V) @25℃
		-	-	2	uA		Clock is stopped, LCD off(VDD=3.6V) @50℃

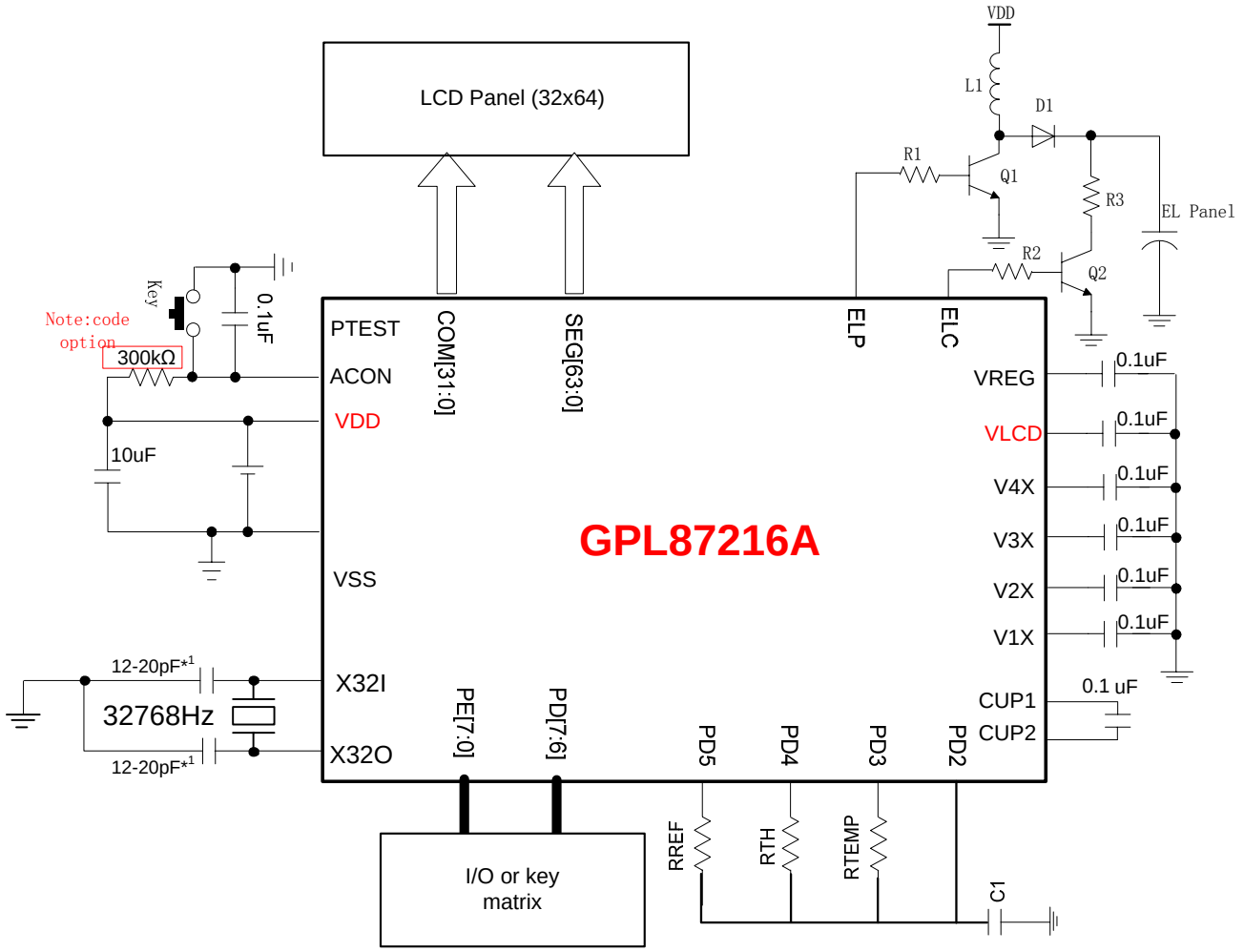
7. APPLICATION CIRCUITS

7.1. GPL87220A



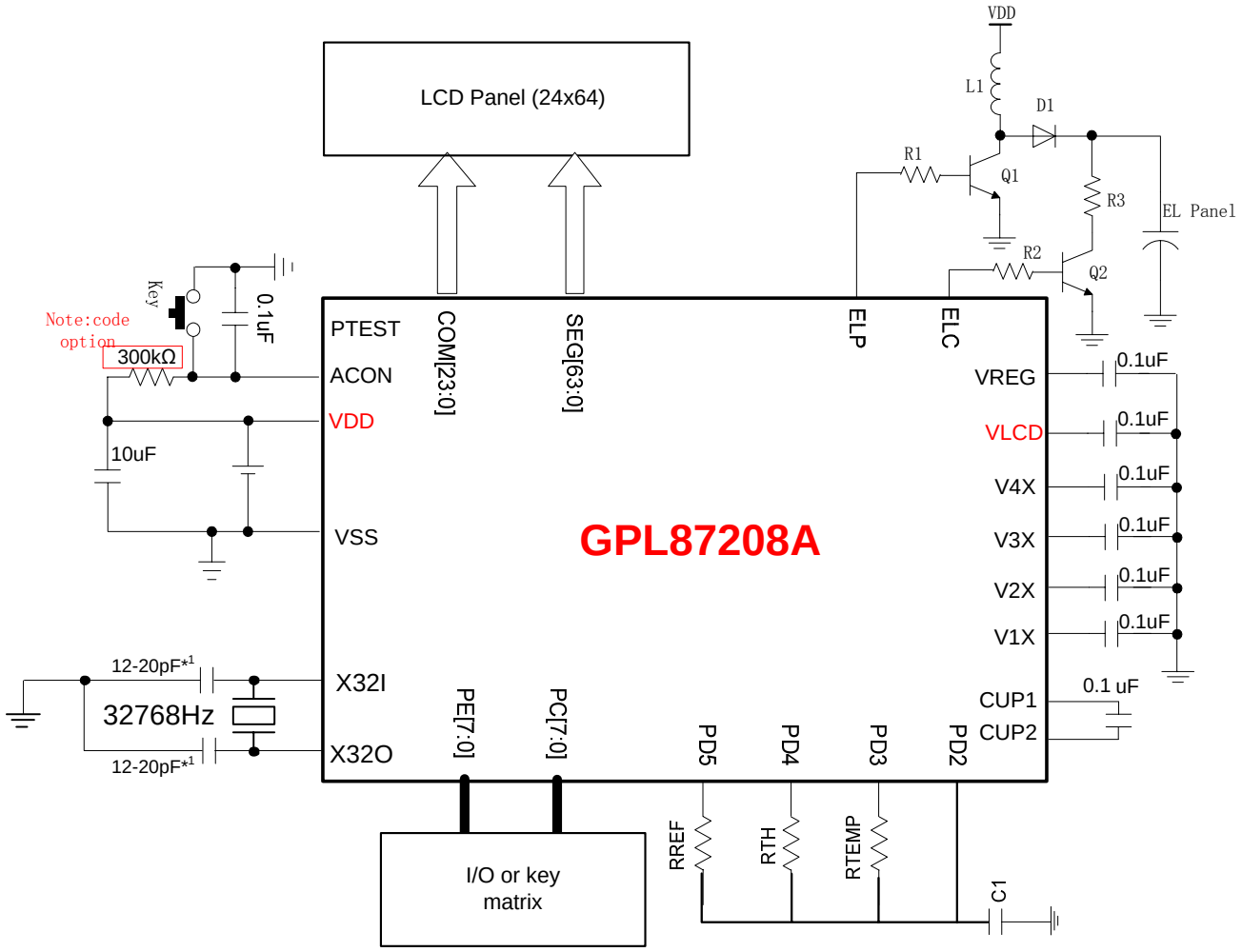
Note1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

7.2. GPL87216A



Note1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

7.3. GPL87208A



Note1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL87220A -NnnV - C	Chip form
GPL87216A -NnnV - C	Chip form
GPL87208A -NnnV - C	Chip form

Note1: Code number (NnnV) is assigned for customer.

Note2: Code number (N = A-Z or 0-9, nn=00-99); version (V = A - Z)

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
JUL. 30, 2013	1.0	Feature modified; DC characteristics modified;	3 12
SEP. 27, 2010	0.1	Original	14