DATA SHEET

GPLB13A

660 DOTS DATA BANK

FEB. 01, 2007

Version 1.2

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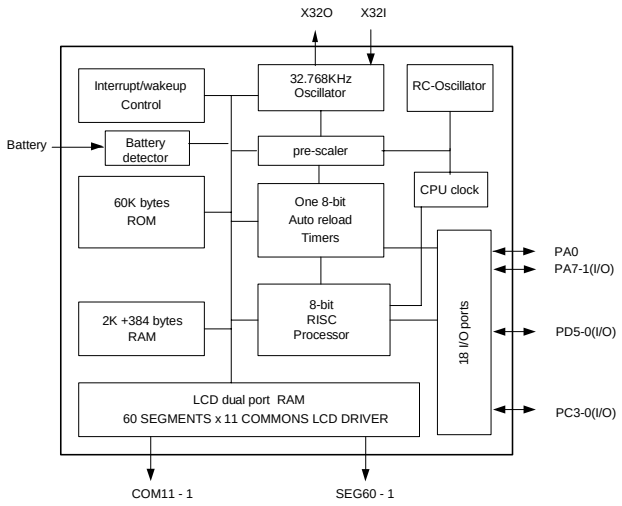
660 DOTS DATA BANK

1. GENERAL DESCRIPTION

GPLB13A, a low power 8-bit CMOS microcontroller with advanced processing technology and mechanism by Generalplus, contains tons of functionality in a compact package such as SRAM, ROM, I/Os, an interrupt controller, a timer and a LCD controller/driver. The amount of 60K bytes of ROM is capable to provide sufficient space for LCD graphical data. The 2432 bytes of SRAM are totally free to users. In addition, 18 I/Os, timer, LCD driver, NMI controller, Watch Dog Timer and other features increase the capability of driving sophisticated functions and displaying fantastic LCD graphics. The GPLB13A is a high-end microcontroller that filled with modern technology and strong backup from Generalplus. Obviously, it is the most suitable product to accomplish the demanded functions for you.

2. BLOCK DIAGRAM



3. FEATURES

- Built-in 8-bit CPU
  - 60K bytes ROM
  - 2432 bytes SRAM
  - Max. operating speed: 1.5MHz @ 1.2V
- NMI controller
  - 2Hz for Real Time Clock (RTC)
  - 128Hz
  - Key(PA6 - 0)
  - Counter overflow
  - Low Battery Voltage Detect (PA7 is an IRQ source)
- Programmable LCD driver
  - Up to 60 segments, up to 11 commons, maximum 660 dots
    In 1/4 duty, COM[5:11] are optioned to SEG[60:54]
    53*11, 54*10, 56*8, 60*4 LCD configurations (by soft)
    In 1/11duty, PortC[3:0] and PortD[5:3] can be optioned to SEG[54:60] (by mask option)
  - 1/3, 1/4 bias, 1/4, 1/8, 1/10 or 1/11 duty
  - Adjustable LCD voltage (16 level)
    1/4 bias: 2.65V - 3.4V
    1/3 bias: 2.4V - 3.3V
  - 88 bytes dedicated LCD RAM
- Operating voltage:
  - 1.1V - 1.7V
- Adjustable CPU clock speed
  - 5 speed : 1, 1/2, 1/4, 1/8, 1/16 of RC-oscillator frequency are available
- Low-power consumption:
  - 30μA operating current @1.5V, F_{CPU} = 260KHz
  - 9μA halt mode current @ 1.5V, F_{CPU} = 260KHz
  - <1.0μA typical standby current @ 1.5V
- 0.9V low voltage reset
- Power saving SLEEP mode
- 1.2V battery low voltage detector
- Peripherals
  - 18 I/O ports (PA7 - 0, PD5 - 0, PC3 - 0)
  - Built-in RC-oscillator
  - Built-in 32.768KHz crystal oscillator for real time clock Function
  - 8-bit reloadable timer/counter with prescaler
  - Watchdog Timer for reliable operation
- 4 options for RC-oscillator
  - 260KHz, 470KHz, 850KHz and 1800KHz @ 1.5V

4. SIGNAL DESCRIPTIONS

Mnemonic	Type	Description
VDD	P	Power supply input
VSS	P	Ground reference
RESET	I	System reset input (internal pull-high), low active
TEST	I	Test input (internal pull-low), high active
X32I	I	32.768KHz crystal input
X32O	O	32.768KHz crystal output
PA7 - 0	I/O	Bi-directional I/O port
PD2 – 0	I/O	Bi-directional I/O port
PD3/SEG60		Bi-directional I/O port / LCD Segment 60 (Decided by Mask Option)
PD4/SEG59		Bi-directional I/O port / LCD Segment 59 (Decided by Mask Option)
PD5/SEG58		Bi-directional I/O port / LCD Segment 58 (Decided by Mask Option)
PC0/SEG57	I/O	Bi-directional I/O port / LCD Segment 57 (Decided by Mask Option)
PC1/SEG56		Bi-directional I/O port / LCD Segment 56 (Decided by Mask Option)
PC2/SEG55		Bi-directional I/O port / LCD Segment 55 (Decided by Mask Option)
PC3/SEG54		Bi-directional I/O port / LCD Segment 54 (Decided by Mask Option)
BATTERY	I	Battery voltage detect pin
VLCD	O	LCD drive voltage output pin
V1	O	LCD drive voltage output pins
V2		
V3		
CUP1	I	Capacitor connection pins for LCD bias circuit
CUP2		
CUP3	I	Capacitor connection pins for generate analog VDD (AVDD)
CUP4		
AVDD	O	Analog power output
COM4 - 1	O	LCD common outputs
COM5/SEG60	O	LCD Common 5/Segment 60 (Decided by software programming)
COM6/SEG59	O	LCD Common 6/Segment 59 (Decided by software programming)
COM7/SEG58	O	LCD Common 7/Segment 58 (Decided by software programming)
COM8/SEG57	O	LCD Common 8/Segment 57 (Decided by software programming)
COM9/SEG56	O	LCD Common 9/Segment 56 (Decided by software programming)
COM10/SEG55	O	LCD Common 10/Segment 55 (Decided by software programming)
COM11/SEG54	O	LCD Common 11/Segment 54 (Decided by software programming)
SEG16 - 1	O	LCD segment outputs
SEG53 - 17	O	LCD segment outputs

Legend: I = Input, O = Output, P = Power

Total 98 pins

Note: When ROSC mode is selected, pin X32I should be floating or connected to VSS and X32O should be floating.

5. FUNCTIONAL DESCRIPTIONS

5.1. Map of Memory and I/Os

*I/O PORT:

- PORT A_DATA $0073
  PORT A_DIR $0071
  PORT A_Buzzer output $0072

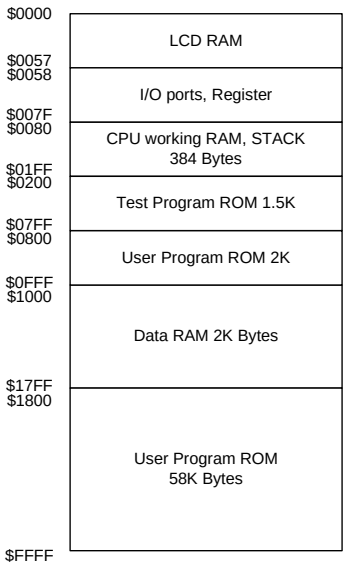
- PORT B_DATA $006F
  PORT B_DIR $006E
  PORT B_CFG $006D

- PORT C_DATA $005F
  PORT C_DIR $005E
  PORT C_CFG $005D

*NMI SOURCE:

- 2Hz
- 128Hz
- Power key (PA0)
- Normal key (PA6-1)
- Counter overflow
- Low Battery

*MEMORY MAP



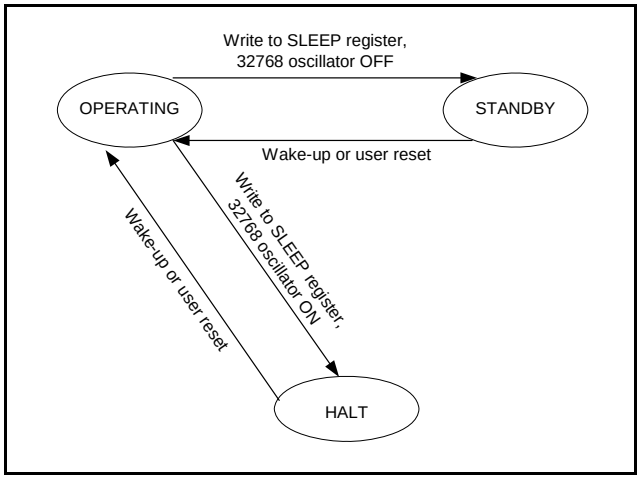
5.2. Operating States

The GPLB13A supports three operating states: standby, halt, and operating. Following table shows the differences between the three operating states.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768 oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

In operating state, all modules (CPU, 32768 oscillator, timer/counter, LCD driver…) are activated. The halt/standby state is entered by writing to SLEEP register ($7A). There are four wake-up sources in GPLB13A: port A wake-up, counter overflow wake-up, 128Hz wake-up and 2Hz wake-up. If any wake-up event occurs, CPU will go to the RESET state.

When in standby, all modules will be shut down, and RAM and I/Os remain in their previous states. The current consumption is minimized in standby. By writing to SLEEP register but keeps 32768 oscillator running, the system is in halt state. In halt state, CPU clock is halted while it waits for an event (key press, timer overflow) to generate a wake-up. The 32768 related modules (timer/counter, LCD driver…) may remain active in the halt state. Following figure is a state diagram for the GPLB13A.



State Diagram of GPLB13A

5.3. CPU Clock

GPLB13A provides programmable CPU clock speed 1, 1/2, 1/4, 1/8, or 1/16 of RC-oscillator frequency for power saving mode. When the system is under heavy load or the voltage of battery is low, user can reduce power consumption by slowing down the speed of CPU clock.

5.4. Low Battery Voltage Detector

The GPLB13A provides a 1.2V battery voltage detector to detect the voltage of the BATTERY pin. User can read the state of battery from port $6B. If the battery is higher than 1.2V, $6B.bit5 will be '0', else will be '1'.

5.5. Buzzer Driver

Port A can be used as buzzer output. When $72.b6 = b7 = '1', PortA.6 and PortA.7 are set for buzzer output. Or else when b6 = b7 = '0', PortA.6 and PortA.7 are set to normal I/O. When down counter overflows, it will toggle PA.6 and PA.7 for driving buzzer.

5.6. LCD Controller/Driver

GPLB13A contains total of 660 dots LCD controller and driver. Once the LCD configuration is initialized, the desired pattern can be displayed by filling the LCD buffer with appropriate data. The LCD driver can also operate during sleep by keeping 32768 oscillator running. The LCD driver in GPLB13A is designed to fit most LCD specifications. The duty is programmable as 1/4, 1/8, 1/10 or 1/11. The following table shows the mapping between LCD and display buffer.

5.6.1. LCD RAM mapping

	SEG8 - 1 (b7 - 0)	SEG16 - 9 (b7 - 0)	SEG24 - 17 (b7 - 0)	SEG32 - 25 (b7 - 0)	SEG40 - 33 (b7 - 0)	SEG48 - 41 (b7 - 0)	SEG56 - 49 (b7 - 0)	SEG60 - 57 (b3 - 0)
COM1	07H	06H	05H	04H	03H	02H	01H	00H
COM2	0FH	0EH	0DH	0CH	0BH	0AH	09H	08H
COM3	17H	16H	15H	14H	13H	12H	11H	10H
COM4	1FH	1EH	1DH	1CH	1BH	1AH	19H	18H
COM5	27H	26H	25H	24H	23H	22H	21H	20H
COM6	2FH	2EH	2DH	2CH	2BH	2AH	29H	28H
COM7	37H	36H	35H	34H	33H	32H	31H	30H
COM8	3FH	3EH	3DH	3CH	3BH	3AH	39H	38H
COM9	47H	46H	45H	44H	43H	42H	41H	40H
COM10	4FH	4EH	4DH	4CH	4BH	4AH	49H	48H
COM11	57H	56H	55H	54H	53H	52H	51H	50H

Note: Bit 7-4 of $00H, $08H, $10H, $18H, $20H, $28H, $30H, $38H, $40H, $48H, $50H, Users can not access these ram contents, and do not use these rams as data storage.

5.7. LCD Voltage Doubler/Regulator

To get the best LCD quality, the LCD supply voltage should not change with the system power. The GPLB13A provides a robust and adjustable (16-level) LCD supply voltage. Users can get desired VLCD to fit specific LCD panels by changing the output reference voltage (program $5A). The available VLCD voltage range is summarized as the following table. The default value of LCD voltage is 2.82V(1/3 Bias), 3.0V(1/4 Bias).

$5A		07	06	05	04	03	02	01	00
LCD Voltage	**1/3 Bias**	2.82V	2.76V	2.7V	2.64V	2.58V	2.52V	2.46V	2.4V
	1/4 Bias	3.0V	2.95V	2.9V	2.85V	2.8V	2.75V	2.7V	2.65V
$5A		0F	0E	0D	0C	0B	0A	09	08
LCD Voltage	**1/3 Bias**	3.3V	3.24V	3.18V	3.12V	3.06V	3.0V	2.94V	2.88V
	1/4 Bias	3.4V	3.35V	3.3V	3.25V	3.2V	3.15V	3.1V	3.05V

Note: In 1/3 Bias Mode, LCD voltage ($5A is 0F) is not 3.3V, when VDD is smaller than 1.1V. LCD Voltage will decease with VDD (VLCD is about 3*VDD).

5.8. Reset Function

GPLB13A can be reset by setting the RESET pin to ground voltage and its operation starts when this pin is set to power voltage. The RESET pin is internally pulled high. Beside, an automatic reset function (internal reset function) operates when power is turned on.

Low voltage reset function is a mask option. When the low voltage reset option is set to enable. The chip will generate a reset signal to reset the system when the system voltage is below 0.9V.

Watchdog timer is available on GPLB13A. The WDT is designed for the system to recover from abnormal operation. When the system is hanged, WDT will generate a system reset to restart the system after 1 second. The WDT should be cleared every 0.5 seconds to avoid accidental reset. Writing to port $7F can clear the WDT. Note that the WDT works only when 32768 Hz clock or pre-scalar clock is active.

5.9. Mask Options

5.9.1. 32768 oscillator

1). X'TAL

2). R-oscillator

5.9.2. Watchdog timer

1). Enable

2). Disable

5.9.3. PA3, PA4, PA5 input mode selection mode

1). Pull-high

2). Floating

5.9.4. System low voltage reset detector

1). Enable

2). Disable

5.9.5. Battery low voltage detector

1). Enable

2). Disable

5.9.6. SEGMENT/IO

1). PC[3:0] / SEG[54:57]

2). PD[5:3] / SEG[58:60]

Note1: When P_70H_LCD_Configuration is set to 1/4 duty, pin COM[5:11] is always optioned as SEG[60:54] which means the display is 4 (COM) x 60 (SEG). Those pins shared with SEG[54:60] can also be used as their original functions, not necessary to the SEG function only. For example, in 1/4 duty mode, the PortC[3:0] can also be used as ordinary I/O and similarity applies for other pins as well. This identity also applies to the 1/8 duty and 1/10 duty modes.

Note2: In 1/8 duty mode, pin COM[9:11] is always optioned as SEG[56:54]. A display of 8(COM) x 56 (SEG) is formed, see note #1 for more information. To achieve a 8 (COM) x 60 (SEG) in 1/8 duty mode, the PortC[0] and PortD[5:3] must be configured as SEGs via mask option and cannot be used as I/O any more.

Note3: In 1/10 duty setup, pin COM11 is used as the SEG54, which forms 10 (COM) In 1/10 duty setup, 10 (COM) x 54 (SEG) dots, see note #1 for more information. To achieve higher number of LCD dot, see note #2 for details.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

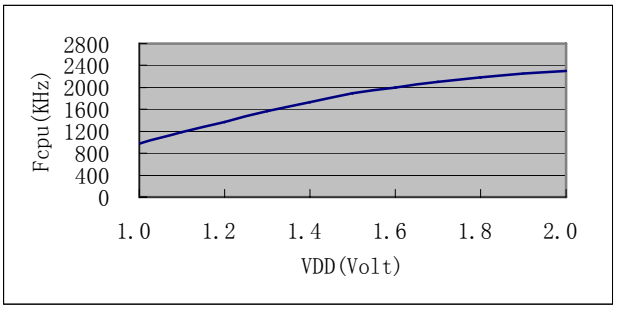
Characteristics	Symbol	Ratings
DC Supply Voltage	VDD	< 3.0V
Input Voltage Range	V_{IN}	-0.5V to VDD + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (VDD = 1.5V, T_A = 25℃)

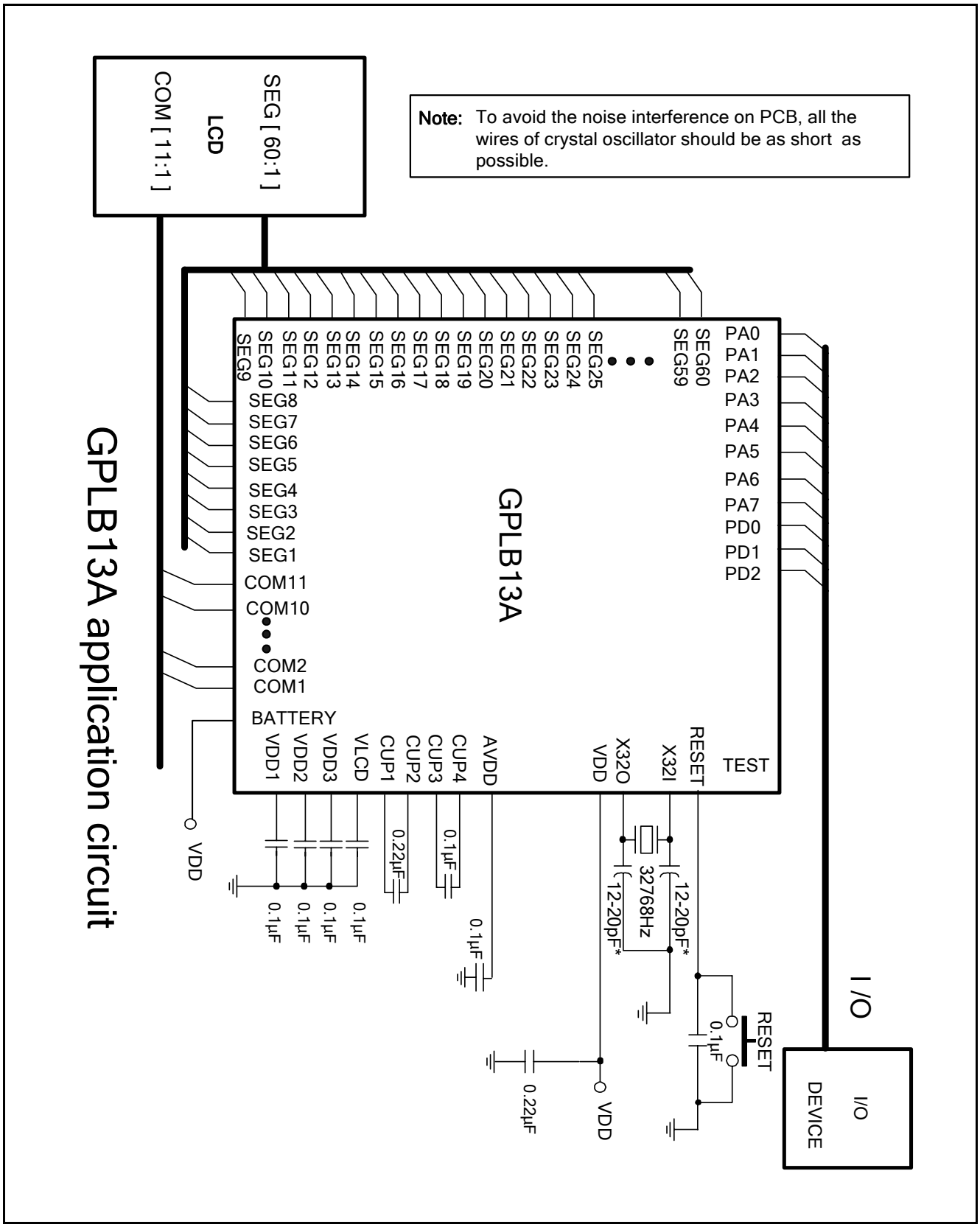
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	1.1	1.5	1.7	V	-
Operating Current1	I_{OP1}	-	130	-	μA	F_{CPU} = 1800KHz @ VDD = 1.5V, no load
Operating Current2	I_{OP2}	-	25	-	μA	F_{CPU} = 260KHz @ VDD = 1.5V, no load
Halt Mode Current	I_{halt}	-	9.0	-	μA	F_{CPU} = 260KHz @ VDD = 1.5V, no load
CPU Clock	F_{CPU}	-	-	1500K	Hz	VDD = 1.2V
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 1.5V, 32768 Hz OFF
Input High Level	V_{IH}	1.0	-	-	V	VDD = 1.5V
Input Low Level	V_{IL}	-	-	0.5	V	VDD = 1.5V
Input Current	I_{IL}	-	-	5.0	μA	VDD = 1.5V, V_{IN} = 0V (input internal pull high)
Output High Current (BZ)	I_{OH}	-	-2.5	-	mA	VDD = 1.5V, V_{OH} = 1.0V
Output Sink Current (BZ)	I_{OL}	-	2.5	-	mA	VDD = 1.5V, V_{OL} = 0.5V
Output High Current (I/O)	I_{OH}	-	-250	-	μA	VDD = 1.5V, V_{OH} = 1.0V
Output Sink Current (I/O)	I_{OL}	-	450	-	μA	VDD = 1.5V, V_{OL} = 0.5V

6.3. The Relationships between the VDD and the F_{cpu}



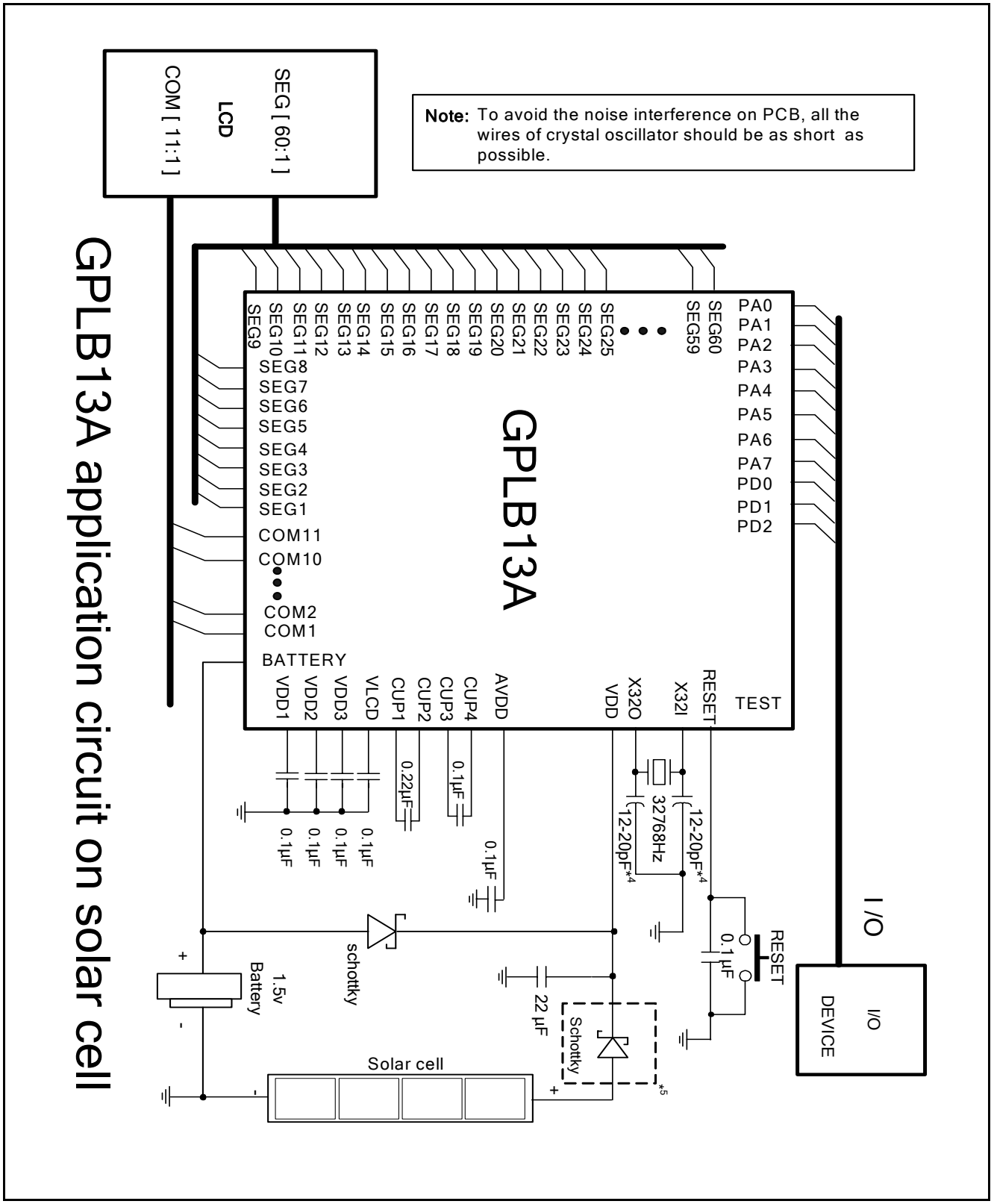
7. APPLICATION CIRCUITS

7.1. Application Circuit - (1)



Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

7.2. Application Circuit - (2)



Note1: In CRYSTAL mode, an accurate time base is generated from the 32768Hz crystal oscillator. The 32768Hz crystal should be installed.

Note2: In ROSC mode, a suitable time base is generated from the RC-Oscillator. The 32768Hz crystal is not necessary to be installed.

Note3: To avoid the noise interference on PCB around crystal circuit, following rules are recommended:

Capacitors between the crystals should be placed as close as possible to X32I and X32O. A shielding by ground is suggested.

Note4: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note5: This schottky diode may be omitted if the leakage current of solar cell is small.

8. DISCLAIMER

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9. REVISION HISTORY

Date	Revision #	Description	Page
FEB. 01, 2007	1.2	Delete ‘’Low voltage power down’ in 1.GENERAL DESCRIPTION.	3
JUL. 18, 2006	1.1	1. Add the Rosc diagram to section 6.3. 2. Modify the 7. APPLICATION CIRCUITS.	8 9,10
MAR. 30, 2006	1.0	Release.	12
AUG. 30, 2005	0.3	Change the sharing of IO and LCD segments.	1, 2, 5, 7, 8
AUG. 17, 2005	0.2	Add the information about 5. FUNCTIONAL DESCRIPTIONS, 6.ELECTRICAL SPECIFICATIONS and 7.APPLICATION CIRCUITS.	3~8
JUL. 28, 2005	0.1	Original	4