DATA SHEET

GPLB20D3

480 Dots Data Bank

Jul 26, 2015

Version 1.2

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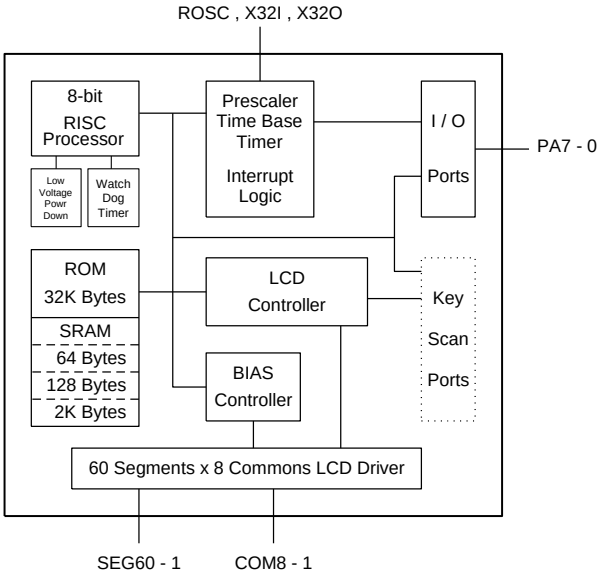
480 DOTS DATA BANK

1. GENERAL DESCRIPTION

GPLB20D3, an 8-bit CMOS microcontroller with advanced processing technology and mechanism by Generalplus, contains tons of functions in a compact package such as SRAM, ROM, I/Os, an interrupt controller, a timer and an LCD controller/driver. The amount of 30K bytes of ROM is able to provide proper space for LCD graphical data. The 2176 bytes of SRAM are totally free to users. In addition, 8 I/Os, timer, LCD driver, NMI controller, Watchdog Timer, Low Voltage Power Down and other features strengthen the capability of driving sophisticated functions and displaying remarkable LCD graphics.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit CPU
- 30K bytes of ROM
- 60 * 8 dual port SRAM for LCD display buffer
- 128 bytes of SRAM for CPU working space
- 2K bytes of SRAM for data
- 8 I/O ports
- LCD controller/driver (1/4 bias, V_{OP} = VDD, Type-B)
  - . 60 * 8 (480 dots)
  - . 60 * 6 (360 dots)
  - . 48 * 8 (384 dots)
  - . 48 * 6 (288 dots)
- Built-in R-oscillator and 32.768KHz crystal oscillator
- 8-bit Reloadable timer/counter with pre-scaler
- NMI controller with following sources
  - . 2Hz for RTC
  - . 128Hz
  - . Key (PA7 - 0)
  - . Counter overflow
- Halt and Standby mode
- Watchdog Timer (WDT)
- Low Voltage Power Down (LVPD)
- Wide operating range: 2.4V - 3.6V @ 1.0MHz

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	25	I	Power supply input
VSS	52	I	Ground input
RESET	27	I	System reset input (internal pull-high), low active
TEST	21	I	Test input (internal pull-low), high active
X32I	29	I	32.768KHz crystal input
X32O	28	O	32.768KHz crystal output
ROSC	26	I	R-oscillator input, connect a resistor to VDD through a resistor
PA7 - 0	37 - 30	I/O	Input /output port
COM8 - 6 COM5 - 3 COM2 - 1	38 - 40 24 - 22 20 - 19	O	LCD common output
SEG60 - 50 SEG49 - 19 SEG18 - 1	41 - 51 53 - 83 1 - 18	O	LCD segment output.

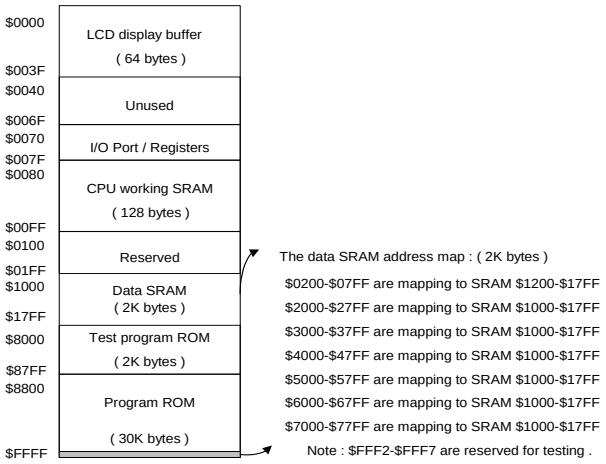
Note1: All of SEG16 - 1 can be used as key strobe output pins by software programming register ($007E). There are two kinds of combinations for key scan option.

Note2: When ROSC is selected, it is at R-oscillator mode. Then, pin X32I should be connected to VSS and pin X32O should be left floating.

Number of key scan port selected	The option for key scan port	($ 007E) bit 2, bit 1, bit 0
Number ≦8	SEG8 - 1 or SEG16 - 9	1, 0, 1 1, 1, 0
9≦ Number ≦16	SEG16 - 1	1, 1, 1

5. FUNCTIONAL DESCRIPTIONS

5.1. ROM Area



5.2. Mask Options

5.2.1. 32K from Crystal / R-osc with prescaler

The system time base, LCD timing and auto-strobe signals are generated from 32.768KHz crystal oscillator. To support those systems without 32.768KHz crystal, this option is provided. When non-crystal mode is selected, the signals and timing listed above will be generated from prescaler. By programming register $007C, user can get a suitable clock to replace 32.768KHz clock. Register $007A:B5 can be used to turn off this clock.

5.2.2. Dogen (WDT enable) / Dogdis (WDT disable)

There is an on-chip WDT available on GPLB20D3. The WDT is designed to recover system when it crashes. If the system is in halt or does not response, WDT will generate a system reset to restart system after 1 second. If WDT is enabled, the WDT should be cleared every 0.5 seconds to avoid accidental reset. The WDT can be cleared by writing to $007F. Note that the WDT only works when 32768Hz crystal is available.

5.2.3. Low voltage power down (LVPD) enable / disable

Low Voltage Power Down circuit will be enabled only when 32768Hz signal is available. If LVPD circuit sensed VDD <= 2.2V, the system will enter Low Voltage (standby) mode after R-osc stops. In Low Voltage mode current consumption will be minimized. This feature can be used to avoid possible data loss during battery replacement.

5.3. LCD Mapping and Specification

$00H - $3F SRAM space is allocated for LCD display buffer. To display a pattern on LCD, users just write the corresponding bits of display buffer. The following table shows the mapping between LCD and display buffer.

	SEG8 - 1 (b7 - 0)	SEG16 - 9 (b7 - 0)	SEG24 - 17 (b7 - 0)	SEG32 - 25 (b7 - 0)	SEG40 - 33 (b7 - 0)	SEG48 - 41 (b7 - 0)	SEG56 - 49 (b7 - 0)	SEG60 - 57 (b7 - 0)
COM1	07H	06H	05H	04H	03H	02H	01H	00H
COM2	0FH	0EH	0DH	0CH	0BH	0AH	09H	08H
COM3	17H	16H	15H	14H	13H	12H	11H	10H
COM4	1FH	1EH	1DH	1CH	1BH	1AH	19H	18H
COM5	27H	26H	25H	24H	23H	22H	21H	20H
COM6	2FH	2EH	2DH	2CH	2BH	2AH	29H	28H
COM7	37H	36H	35H	34H	33H	32H	31H	30H
COM8	3FH	3EH	3DH	3CH	3BH	3AH	39H	38H

The GPLB20D3 supports LCD's with following characteristics:

Duty: 1/6 or 1/8

Bias: 1/4; V_{LCD} = VDD

V1 = VDD * 3/4

V2 = VDD * 2/4

V3 = VDD * 1/4

VEE = GND

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	VDD	< 6.0V
Input Voltage Range	V_{IN}	-0.5V to VDD + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

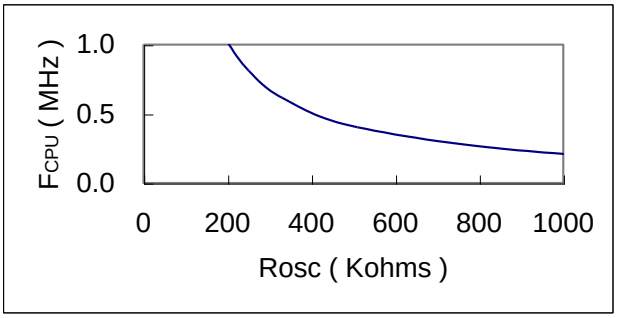
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (VDD = 3.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	160	-	μA	F_{CPU} = 500kHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, 32768Hz OFF
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (PA7, PA6)	I_{OH}	-	-2.5	-	mA	VDD = 3.0V V_{OH} = 2.0V
Output Sink Current (PA7, PA6)	I_{OL}	-	2.5	-	mA	VDD = 3.0V V_{OL} = 1.0V
Output High Current (PA5 - 0, PC, PD)	I_{OH}	-	-1.0	-	mA	VDD = 3.0V V_{OH} = 2.0V
Output Sink Current (PA5 - 0, PC, PD)	I_{OL}	-	1.0	-	mA	VDD = 3.0V V_{OL} = 1.0V
CPU Clock	F_{CPU}	-15%	580	+15%	KHz	VDD = 3.0V, R_{OSC} = 330KΩ

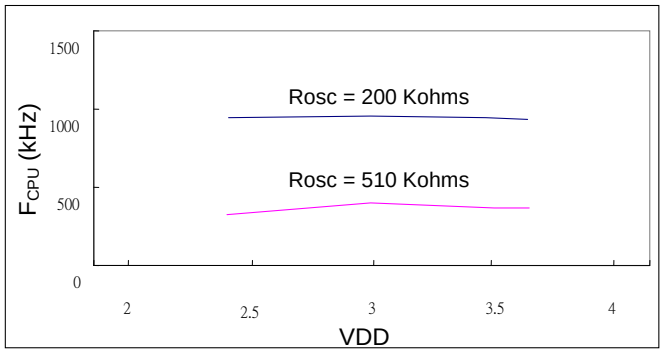
6.3. The relationships between the F_{CPU} and the VDD

6.3.1. VDD = 3.0V, T_A = 25℃

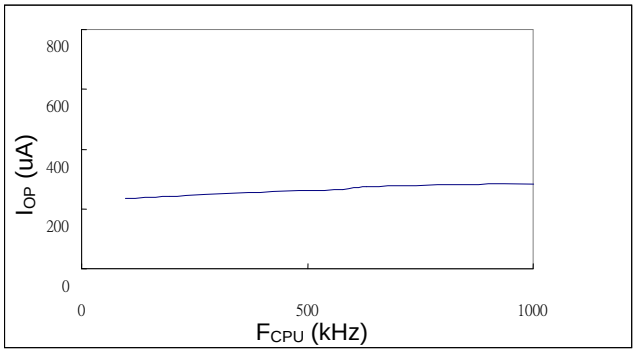


$R_{OSC\ (Kohm)}$	200	240	330	510	1000
$F_{CPU\ (KHZ)}$	950	630	580	370	195

6.4. The relationships between the F_{CPU} and the VDD

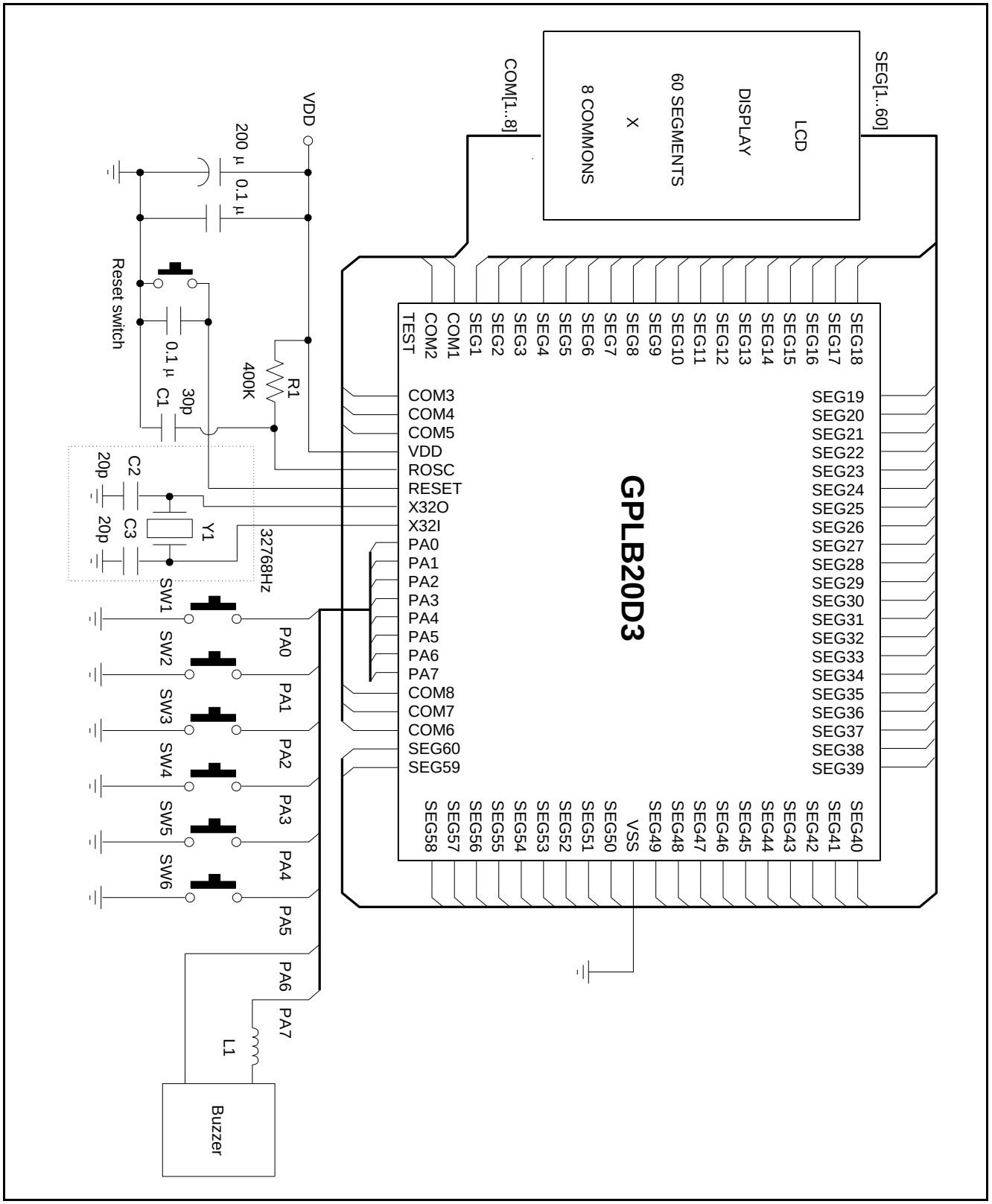


6.5. The relationships between the F_{CPU} and the I_{OP}

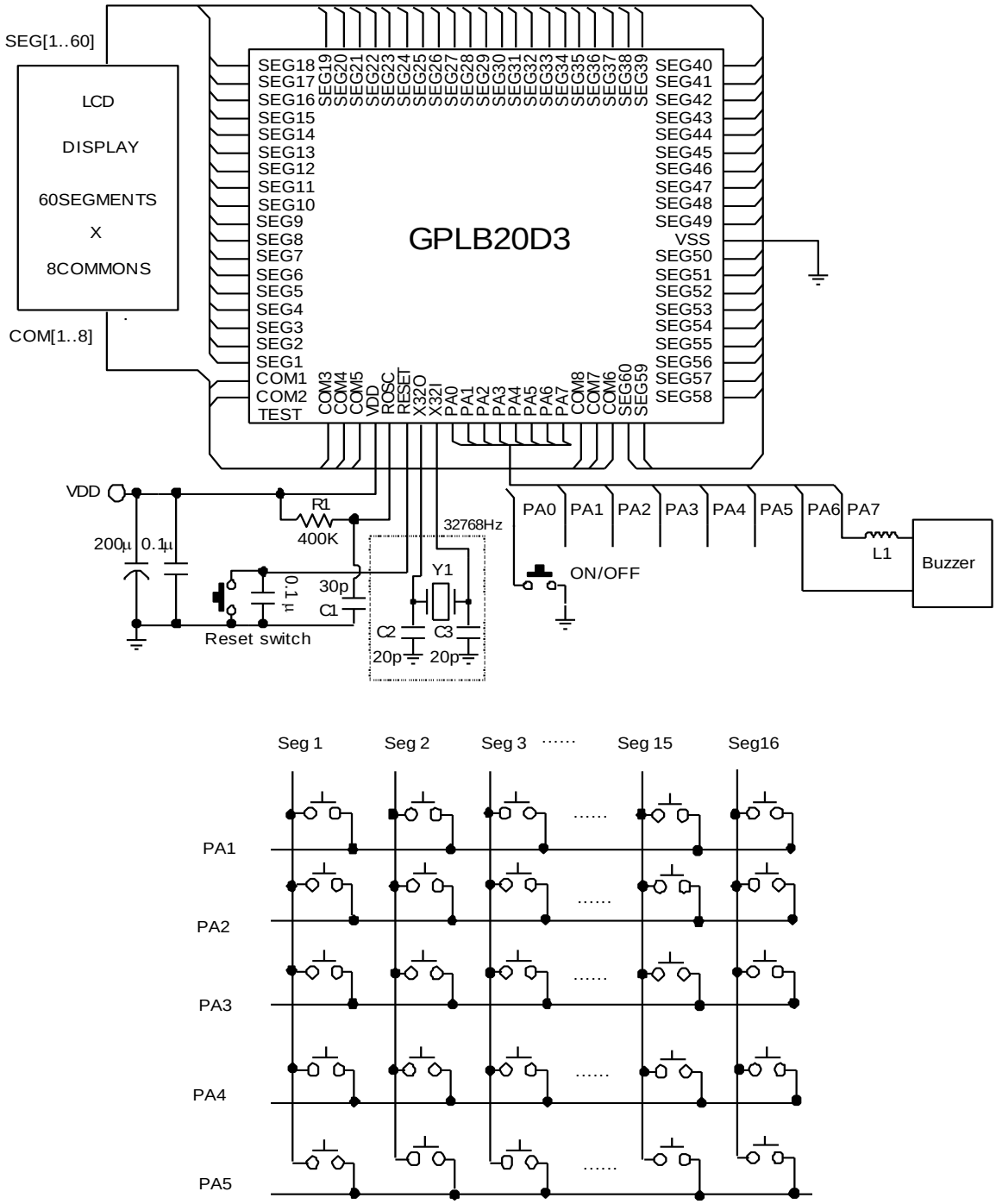


7. APPLICATION CIRCUITS

7.1. Application Circuit - (1)



7.2. Application Circuit - (2)



Note1: In the CRYSTAL mode, the accurate time base is generated from the 32768Hz crystal oscillator; the 32768Hz crystal oscillator should be installed.

Note2: In the ROSC mode, a suitable time base is generated from the R-Oscillator. The 32768Hz crystal oscillator is unnecessary to be installed.

Note3: To avoid the noise interference on PCB around R-Oscillator and crystal circuit, following rules are suggested:

1). R1 and C1 should be placed as close as possible to ROSC pin.

2). C2, C3 and crystal should be placed as close as possible to X32I and X32O. A shielding by ground is suggested.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPLB20D3-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
JUL. 27, 2016	1.2	Modify 6.2, 6.3.	6
JUN. 23, 2005	1.1	Modify wide operating range. Modify 6.4, 6.5.	1 4, 5
APR. 22, 2005	1.0	Original Note: The GPLB20D3 data sheet v1.0 is a continued version of SPLB20D2 data sheet v0.2.	11