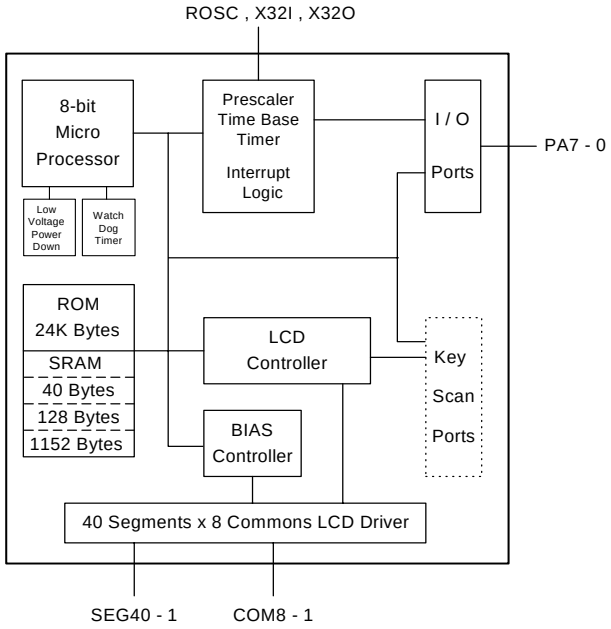
320 DOTS DATA BANK

1. GENERAL DESCRIPTION

GPLB24A is an 8-bit CMOS microprocessor with advanced processing technology and mechanisms by Generalplus. It includes 1280-bytes working RAM, 22K-bytes ROM, 8 I/Os, an interrupt controller, a timer and a LCD controller/driver. The 22K-byte ROM provides proper space for LCD graphic data. The 1280-bytes of CPU working SRAM is available to users for programming and data storage. The GPLB24A is capable of driving sophisticated functions and displaying remarkable LCD graphics. A Sleep (power-down) feature is also built-in to reduce power consumption. The GPLB24A is a high-end micro-controller that includes, not only the latest technology, but also the full commitment and support of Generalplus. Clearly the most suitable solution for your product needs.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 22K bytes ROM
- 40 dual port SRAM for 40 x 8 LCD display buffer
- 128 bytes SRAM for CPU working space
- 1152 bytes SRAM for data
- 8 I/O ports
- LCD controller/driver (1/4 bias, V_{OP} = VDD, Type-B)
  - . 40 x 8 (320 dots)
  - . 40 x 6 (240 dots)
- Built-in R-oscillator and 32.768KHz crystal oscillator
- 8-bit reloadable timer/counter with prescaler
- NMI controller with following sources
  - . 2Hz for Real Time Counter (RTC)
  - . 128Hz
  - . Key (PA7 - 0)
  - . Counter overflow
- Halt and Standby mode
- Watchdog Timer (WDT)
- Power saving sleep mode
- Low Voltage Power Down
- Wide operating range: 2.4V - 3.6V @ 1.0MHz
  3.6V - 5.5V @ 1.0MHz

4. APPLICATION FIELD

- Hand held games
- Pet games
- Educational games, etc.

5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	9	I	Power supply input
VSS	22	I	GND
RESET	11	I	System reset input (internal pull-high), low active
TEST	63	I	Test input (internal pull-low), high active
X32I	13	I	32.768 KHz crystal input
X32O	12	O	32.768 KHz crystal output
ROSC	10	I	R-oscillator input, connect a resistor to VDD through a resistor
PA7 - 0	21 - 14	I/O	Input / output port
COM8 - 1	8 - 1	O	LCD common output. COM7, COM8 can be reassigned as IOZ6, IOZ7
SEG40 - 1	23 - 62	O	LCD segment output. See note 1 below.

Note1: SEG16 - 1 can be used as keyboard scan output pins by programming register ($007E).

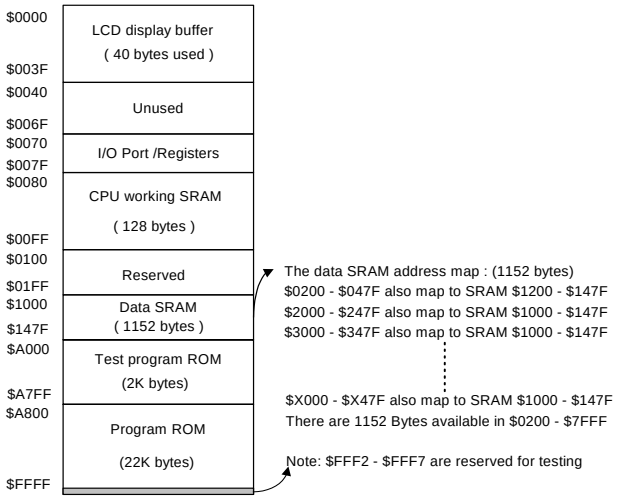
Note2: When the ROSC mode is selected, pin X32I should be connected to VSS and X32O should be floating.

Key scan options are as follows:

Key scan port No.	Key scan assignment options	($ 007E) bit 2, bit 1, bit 0
1 - 8	SEG1 - 8 or	1, 0, 1
	SEG9 - 16	1, 1, 0
9 - 16	SEG1 - 16	1, 1, 1

6. FUNCTIONAL DESCRIPTIONS

6.1. ROM Area



6.2. Mask Options

6.2.1. 32K from Crystal / R-osc with prescaler

When the crystal mode is selected, the system time base, LCD timing, and auto-strobe signal is generated form the 32.768KHz crystal oscillator. The R-osc option is provided to support system timebase, LCD timing, and auto-strobe signal without 32.768KHz crystal oscillator. When the R-osc mode is selected, the signals and timings will be generated from pre-scaler. By programming register ($007C), users can get a suitable clock (R-osc) to replace the 32.768 KHz clock. Bit-5 of register ($007A) can also turn off this clock.

6.2.2. Watchdog enable / Watchdog disable

There is an on-chip WDT (Watchdog Timer) available in the GPLB24A. The WDT is designed for recovering from a system crash. If the system is stalled, the WDT will generate a system reset to restart system after 1 second. If the WDT is enabled, the WDT is cleared every 0.5 seconds to avoid accidental reset. The WDT can be cleared by writing to address ($007F). Note that the WDT only works when 32768 crystal is available.

6.2.3. Low voltage power down (LVPD) enable/disable

The Low Voltage Power Down circuit is enabled only when 32768 signal is available. If the LVPD circuit senses VDD < 2.2V, the system will enter the Low Voltage (standby) mode after the R-osc stops. In the Low Voltage mode current consumption is minimized. This feature can be used to avoid possible data loss during battery replacement.

6.3. LCD Mapping and Specification

SRAM space ($00H - $3F) is allocated for LCD display buffer. To display a pattern on the LCD, the user simply writes the corresponding bits as display buffer. The following table shows the mapping between LCD and display buffer.

	SEG8 - 1 (b7 - 0)	SEG16 - 9 (b7 - 0)	SEG24 - 17 (b7 - 0)	SEG32 - 25 (b7 - 0)	SEG40 - 33 (b7 - 0)
COM1	07H	06H	05H	04H	03H
COM2	0FH	0EH	0DH	0CH	0BH
COM3	17H	16H	15H	14H	13H
COM4	1FH	1EH	1DH	1CH	1BH
COM5	27H	26H	25H	24H	23H
COM6	2FH	2EH	2DH	2CH	2BH
COM7	37H	36H	35H	34H	33H
COM8	3FH	3EH	3DH	3CH	3BH

The GPLB24A supports LCD's with the following characteristics:

Duty: 1/6 or 1/8

Bias: 1/4; V_{LCD} = VDD

V_1 = VDD * 3/4

V_2 = VDD * 2/4

V_3 = VDD * 1/4

VEE = GND

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	VDD	< 6.0V
Input Voltage Range	V_{IN}	-0.5V to VDD + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 3.0V, T_A = 25℃)

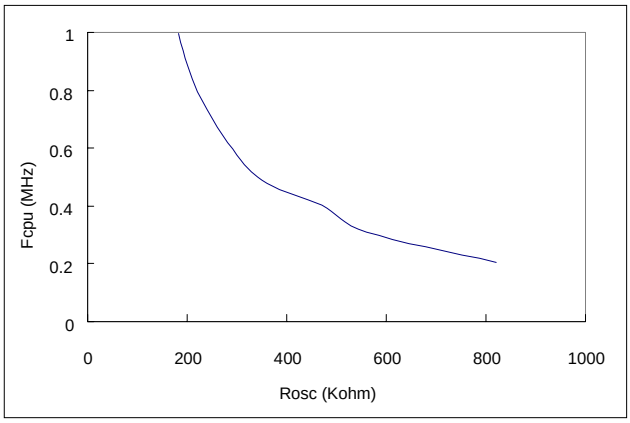
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	5.5	V	For 2-battery
Operating Current	I_{OP}	-	160	-	μA	F_{CPU} = 500KHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, 32768Hz OFF
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output high I (PA5 - 0)	I_{OH}	-	-1.0	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output sink I (PA5 - 0)	I_{OL}	-	1.0	-	mA	VDD = 3.0V, V_{OL} = 1.0V
Output high I (PA7 - 6)	I_{OH}	-	-2.5	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output sink I (PA7 - 6)	I_{OL}	-	2.5	-	mA	VDD = 3.0V, V_{OL} = 1.0V

7.3. DC Characteristics (VDD = 4.5V, T_A = 25℃)

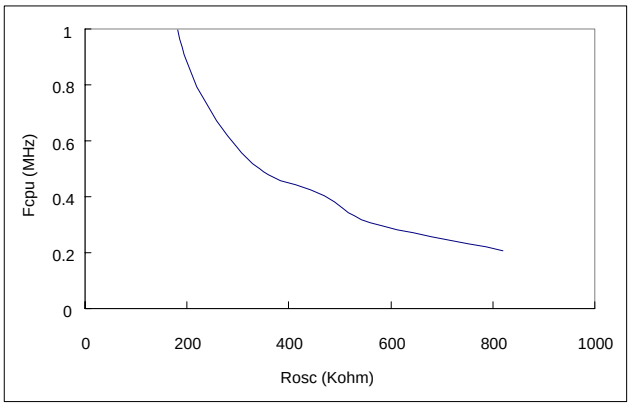
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	400	-	μA	F_{CPU} = 500KHz @ 4.5V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 4.5V, 32768Hz OFF
Input High Level	V_{IH}	3.0	-	-	V	VDD = 4.5V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 4.5V
Output high I (PA5 - 0)	I_{OH}	-	-1.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output sink I (PA5 - 0)	I_{OL}	-	1.0	-	mA	VDD = 4.5V, V_{OL} = 0.8V
Output high I (PA7 - 6)	I_{OH}	-	-3.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output sink I (PA7 - 6)	I_{OL}	-	3.0	-	mA	VDD = 4.5V, V_{OL} = 0.8V

7.4. The Relationship between the R_{OSC} and the F_{CPU}

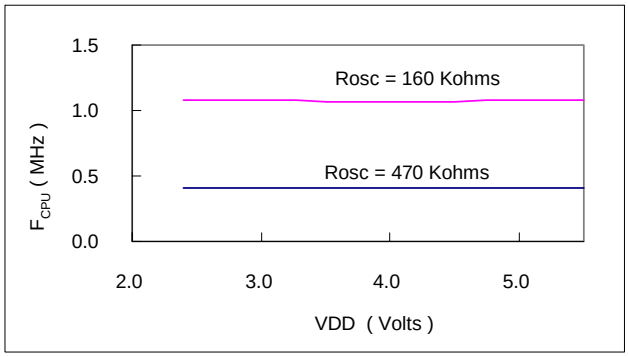
7.4.1. VDD = 3.0V, T_A = 25℃



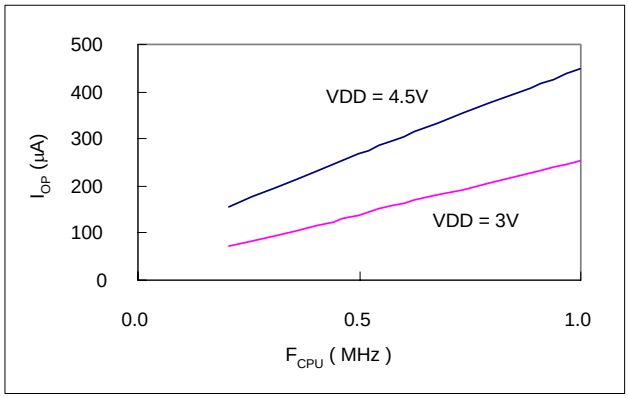
7.4.2. VDD = 4.5V, T_A = 25℃



7.5. The Relationships between the VDD and the F_{CPU}

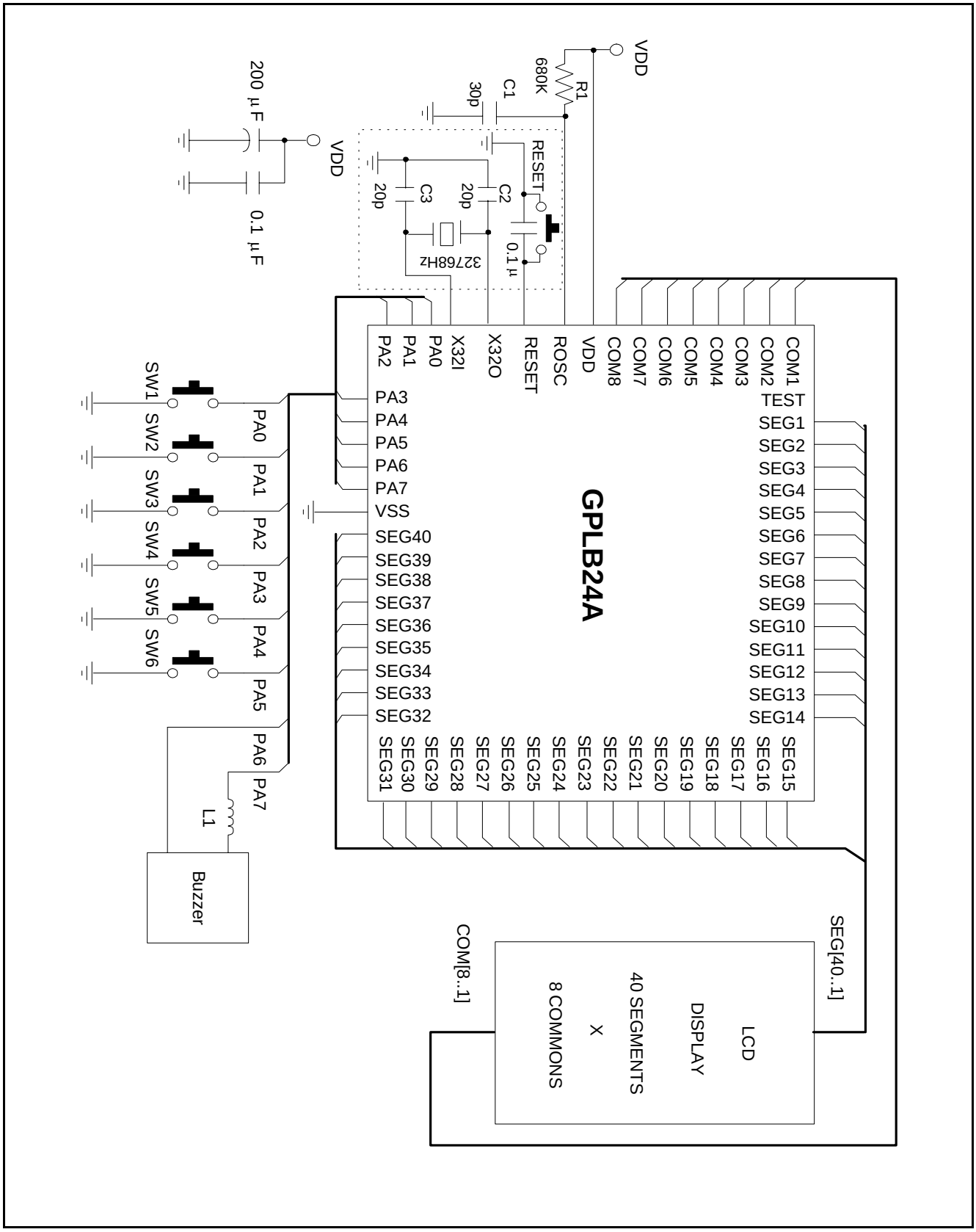


7.6. The Relationships between the F_{CPU} and the I_{OP}

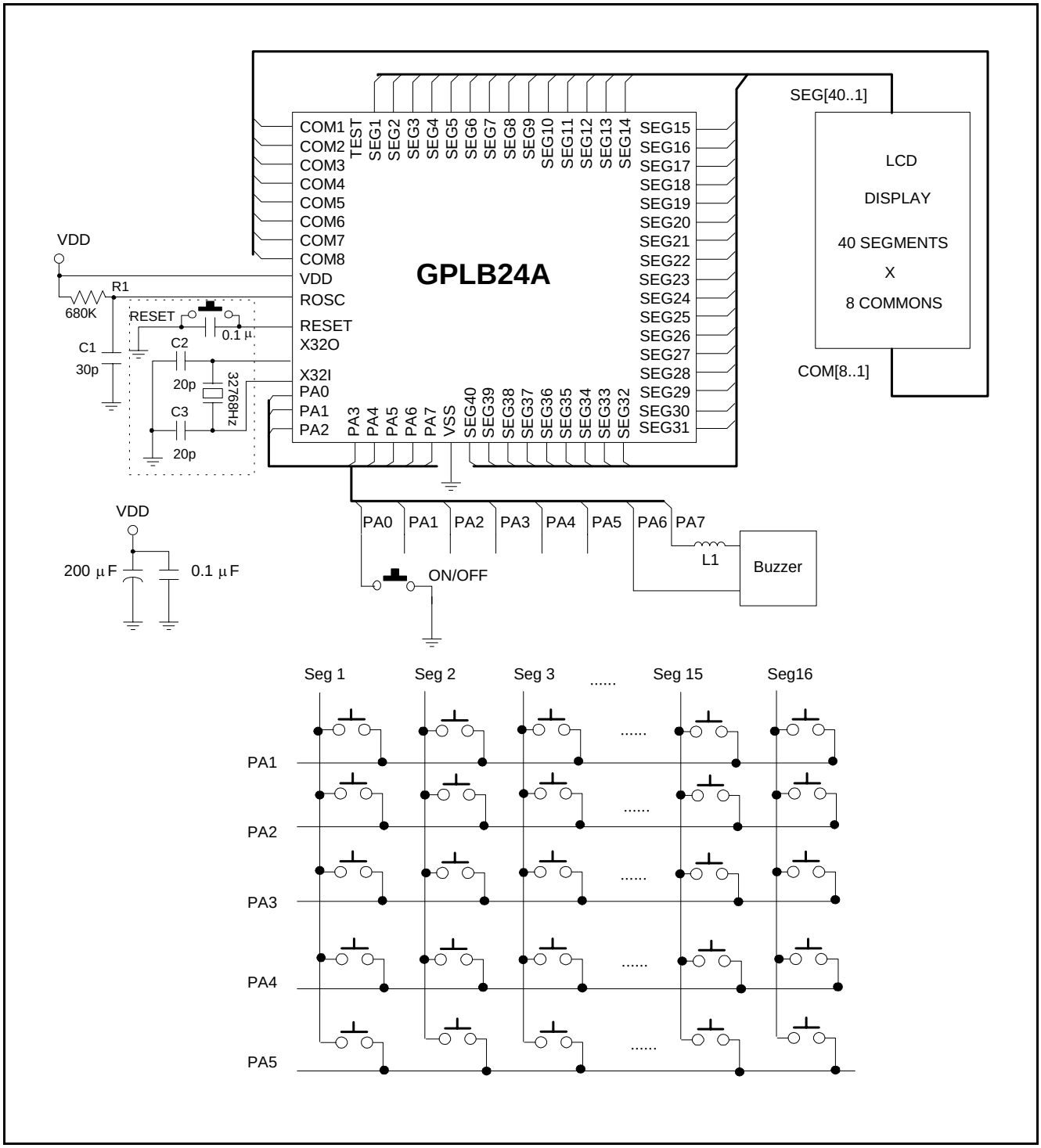


7.7. APPLICATION CIRCUITS

7.8. Application Circuit - (1)



7.9. Application Circuit - (2)



Note1: In the CRYSTAL mode, the 32768Hz crystal oscillator generates an accurate time base. The Crystal mode requires the installation of a 32768Hz crystal oscillator.

Note2: In the ROSC mode, a suitable time base is generated from the R-Oscillator. A 32768Hz crystal oscillator does not need to be installed.

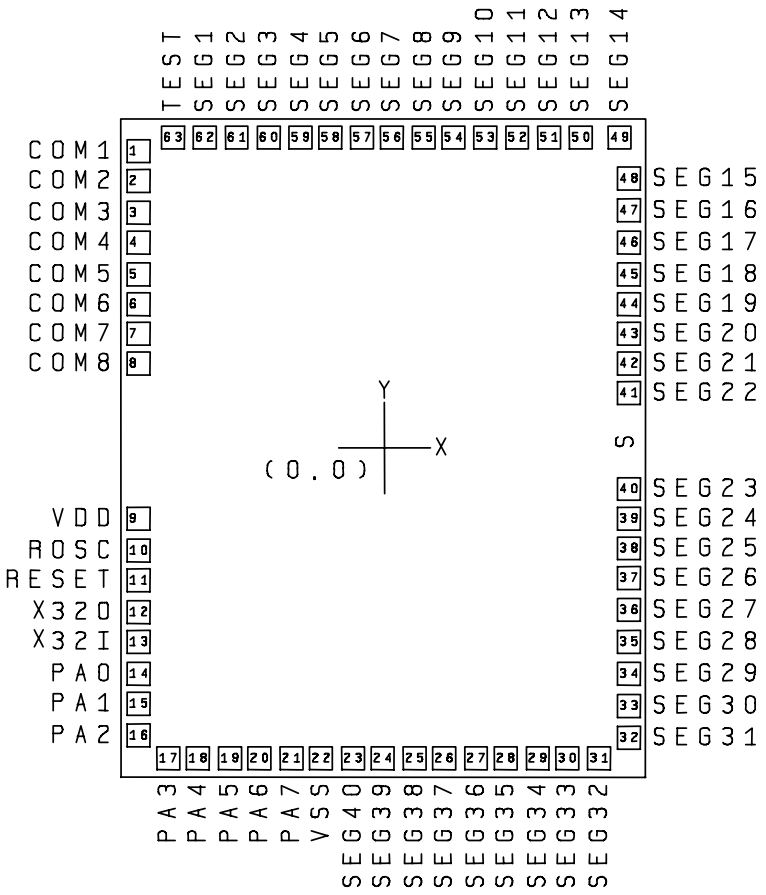
Note 3: To avoid noise interference on the PCB around R-Oscillator and crystal circuit, the following installation guidelines are suggested:

1). R1 and C1 should be placed as near as possible to the ROSC pin.

2). C2, C3 and the Crystal should be placed as near as possible to X32I and X32O. A shielding by ground is suggested.

8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

8.2. Ordering Information

Product Number	Package Type
GPLB24A-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

8.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	COM1	-1075	1301	33	SEG30	1071	-1125
2	COM2	-1075	1166	34	SEG29	1071	-985
3	COM3	-1075	1031	35	SEG28	1071	-845
4	COM4	-1075	896	36	SEG27	1071	-705
5	COM5	-1075	761	37	SEG26	1071	-570
6	COM6	-1075	631	38	SEG25	1071	-440
7	COM7	-1075	501	39	SEG24	1071	-310
8	COM8	-1075	371	40	SEG23	1071	-180
9	VDD	-1075	-313	41	SEG22	1071	244
10	ROSC	-1075	-448	42	SEG21	1071	374
11	RESET	-1075	-583	43	SEG20	1071	504
12	X32O	-1075	-718	44	SEG19	1071	634
13	X32I	-1075	-853	45	SEG18	1071	764
14	PA0	-1075	-988	46	SEG17	1071	904
15	PA1	-1075	-1123	47	SEG16	1071	1044
16	PA2	-1075	-1258	48	SEG15	1071	1184
17	PA3	-954	-1357	49	SEG14	1026	1357
18	PA4	-819	-1357	50	SEG13	862	1357
19	PA5	-684	-1357	51	SEG12	722	1357
20	PA6	-549	-1357	52	SEG11	582	1357
21	PA7	-414	-1357	53	SEG10	442	1357
22	VSS	-279	-1357	54	SEG9	302	1357
23	SEG40	-144	-1357	55	SEG8	167	1357
24	SEG39	-9	-1357	56	SEG7	32	1357
25	SEG38	126	-1357	57	SEG6	-103	1357
26	SEG37	261	-1357	58	SEG5	-238	1357
27	SEG36	396	-1357	59	SEG4	-373	1357
28	SEG35	531	-1357	60	SEG3	-513	1357
29	SEG34	666	-1357	61	SEG2	-653	1357
30	SEG33	801	-1357	62	SEG1	-793	1357
31	SEG32	936	-1357	63	TEST	-933	1357
32	SEG31	1071	-1265				

9. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Generalplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. GENERALPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, GENERALPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. GENERALPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by GENERALPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

10. REVISION HISTORY

Date	Revision #	Description	Page
MAR. 08, 2005	1.0	Original Note: The GPLB24A data sheet v1.0 is a continued version of SPLB24A data sheet v1.4.	11