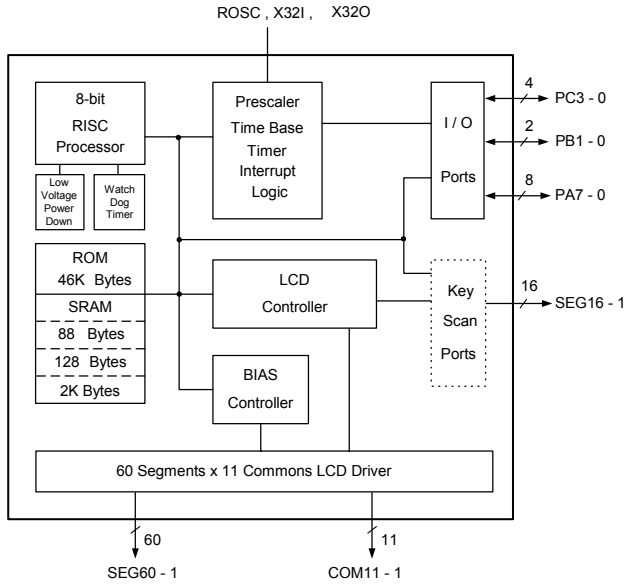
660 DOTS DATA BANK

1. GENERAL DESCRIPTION

GPLB25A, an 8-bit CMOS microcontroller with advanced processing technology and mechanism by Generalplus, contains tons of functionalities in a compact package such as SRAM, ROM, I/Os, an interrupt controller, a timer and a LCD controller/driver. The amount of 46K bytes of ROM is capable to provide sufficient space for LCD graphical data. The 2176-bytes of SRAM are totally free to users. In addition, 14 I/Os, timer, LCD driver, NMI controller, Watch Dog Timer, Low Voltage Power Down and other features increase the capability of driving sophisticated functions and displaying fantastic LCD graphics. The GPLB25A is a high-end microcontroller that filled with modern technology and strong backup from Generalplus. Obviously, it is the most suitable product to accomplish the demanded functions for you.

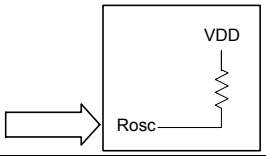
2. BLOCK DIAGRAM



3. FEATURES

- Built-in 8-bit CPU (CPU14B)
  - 46K bytes ROM
  - 128 bytes SRAM for CPU working space
  - 2K bytes SRAM for data
  - Max. operating speed: 1.0MHz @ 2.4V
- NMI controller
  - 2Hz for Real Time Clock (RTC)
  - 128Hz
  - Key(PA7 - 0)
  - Counter overflow
- Programmable LCD driver
  - Up to 60 segments, up to 11 commons, maximum 660 dots
  - 1/4 or 1/5 bias capability
  - 1/10 or 1/11 duty
  - 88 bytes dedicated LCD RAM
  - LCD com/seg driving strength can be adjusted to compromise the display quality and current consumption
  - 16-level VLCD adjustable
- Low Voltage Power Down
- Wide operating voltage:
  - 2.4V - 3.6V @ 1.0MHz
  - 3.6V - 5.5V @ 1.0MHz
- Power saving SLEEP mode
- Serial SRAM interface
- Low-power consumption:
  - 200μA typical @ 3.0V, F_{CPU} = 500KHz
  - <1μA typical standby current @ 3.0V
- Peripherals
  - 14 I/O ports (PA7 - 0, PB1 - 0, PC3 - 0)
  - Built-in RC-oscillator (only one resistor is needed)
  - Built-in 32.768KHz crystal oscillator for real time clock function
  - 8-bit reloadable timer/counter with prescaler
  - Watchdog Timer for reliable operation

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	34	P	Power supply input
VSS	61	P	Ground reference
RESET	36	I	System reset input (internal pull-high), low active
TEST	31	I	Test input (internal pull-low), high active
X32I	38	I	32.768KHz crystal input
X32O	37	O	32.768KHz crystal output
ROSC	35	I	ROSC input, connect to VDD through a resistor 
PA7 - 0	46 - 39	I/O	Bi-directional I/O port
PC3 - 0	30 - 27	I/O	Bi-directional I/O port
COM11 - 1	26 - 16	O	LCD common output
SEG15 - 1 SEG46 - 16 SEG60 - 47	15 - 1 62 - 92 47 - 60	O	LCD segment output
PB1 - 0	32 - 33	I/O	Port B is a bi-directional I/O port, can be software programmed as serial SRAM port.

Legend: I = Input, O = Output, P = Power

Note1: All of the SEG16 - 1 can be used as key strobe output pins by programming the Register ($007E). There are two kinds of combinations for key scan.

Note2: When ROSC-mode is selected, pin X32I should be floating or connected to VSS and X32O should be floating.

No. of selected key scan port	The option for key scan port	($ 007E) bit 2, bit 1, bit 0
No. ≦8	SEG8 - 1 or SEG16 - 9	1, 0, 1 1, 1, 0
9≦No. ≦16	SEG16 - 1	1, 1, 1

5. FUNCTIONAL DESCRIPTIONS

5.1. Map of Memory and I/Os

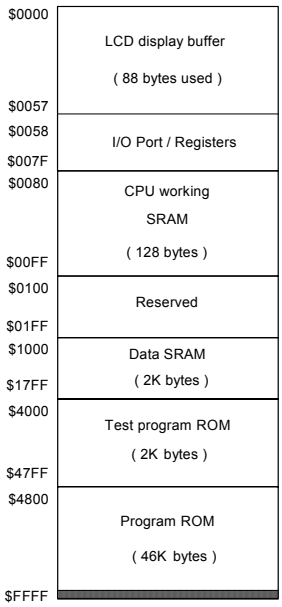
*I/O PORT:

- PORT A_DATA $0073
  PORT A_DIR $0071
  PORT A_CFG $0072
- PORT B_DATA $0067
  PORT B_CFG $0068
- PORT C_DATA $005F
  PORT C_DIR $005E
  PORT C_CFG $005D
- SERIAL SRAM INTERFACE
  $0060 - $0066

*NMI SOURCE:

- 2Hz
- 128Hz
- Power key (PA0)
- Normal key (PA7 - 1)
- Counter overflow

*MEMORY MAP



Note: $FFF2 - $FFF7 are reserved for GENERALPLUS testing.

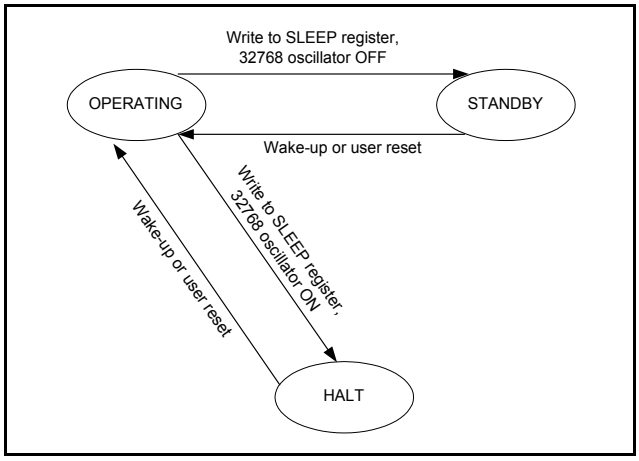
5.2. Operating States

The GPLB25A supports three operating states: standby, halt, and operating. Following table shows the differences between the three operating states.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768 oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

In operating state, all modules (CPU, 32768 oscillator, timer/counter, LCD driver…) are activated. The halt/standby state is entered by writing to SLEEP register ($7A). There are four wake-up sources in GPLB25A: port A wake-up, counter overflow wake-up, 128Hz wake-up and 2Hz wake-up. If any wake-up event occurs, CPU will go to the RESET state.

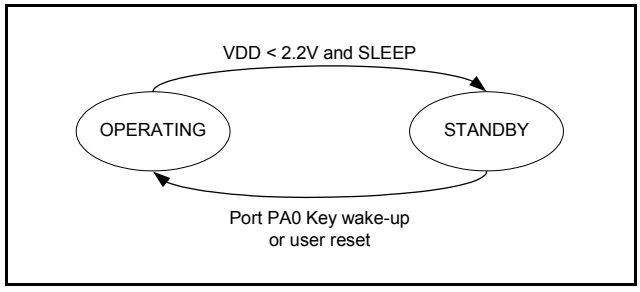
When in standby, all modules will be shut down, and RAM and I/Os remain in their previous states. The current consumption is minimized in standby. By writing to SLEEP register but keeps 32768 oscillator running, the system is in halt state. In halt state, CPU clock is halted while it waits for an event (key press, timer overflow) to generate a wake-up. The 32768 related modules (timer/counter, LCD driver…) may remain active in the halt state. Following figure is a state diagram for the GPLB25A.



State Diagram of GPLB25A

5.3. Low Voltage Power Down

The GPLB25A provides a 2.2V voltage detector to detect a low voltage event. If VDD drops below 2.2V, after a SLEEP command is issued, system will shut down all activities (LCD bias, LCD display, 32768 oscillator) and enters standby to reduce current consumption. This low voltage power down can be awakened by a PA0 key wake-up or RESET. Users can use this feature to implement battery change function. The average current consumption of the Low Voltage Detector is about 0.07μA (VDD = 3.0V).



State Diagram of Low Voltage Power Down

5.4. LCD Controller/Driver

GPLB25A contains total of 660 dots LCD controller and driver. Programmers can set the LCD configuration (bias, duty) by writing to LCD control register ($70). Once the LCD configuration is initialized, the desired pattern can be displayed by filling the LCD buffer with appropriate data. The LCD driver can also operate during sleep by keeping 32768 oscillator running. The LCD driver in GPLB25A is designed to fit most LCD specifications. It can either be programmed as 1/4 or 1/5 bias and the duty is also programmable as 1/10 or 1/11. The following table shows the mapping between LCD and display buffer.

LCD RAM mapping:

	SEG8 - 1 (b7 - 0)	SEG16 - 9 (b7 - 0)	SEG24 - 17 (b7 - 0)	SEG32 - 25 (b7 - 0)	SEG40 - 33 (b7 - 0)	SEG48 - 41 (b7 - 0)	SEG56 - 49 (b7 - 0)	SEG60 - 57 (b3 - 0)
COM1	07H	06H	05H	04H	03H	02H	01H	00H
COM2	0FH	0EH	0DH	0CH	0BH	0AH	09H	08H
COM3	17H	16H	15H	14H	13H	12H	11H	10H
COM4	1FH	1EH	1DH	1CH	1BH	1AH	19H	18H
COM5	27H	26H	25H	24H	23H	22H	21H	20H
COM6	2FH	2EH	2DH	2CH	2BH	2AH	29H	28H
COM7	37H	36H	35H	34H	33H	32H	31H	30H
COM8	3FH	3EH	3DH	3CH	3BH	3AH	39H	38H
COM9	47H	46H	45H	44H	43H	42H	41H	40H
COM10	4FH	4EH	4DH	4CH	4BH	4AH	39H	48H
COM11	57H	56H	55H	54H	53H	52H	51H	50H

5.5. Watchdog Timer (WDT)

An on chip watchdog timer is available on GPLB25A. The WDT is designed for recovering from system abnormal operation. If the system is hanged, WDT will generate a system reset to restart system after 1 second. If WDT is enabled, the WDT should be cleared every 0.5 seconds to avoid accidental reset. The WDT can be cleared by writing to $7F. Note that the WDT only works when 32768 Hz crystal is available.

5.6. Mask Options

5.6.1. 32768 oscillator

1). X'TAL

2). R-oscillator with prescaler

5.6.2. Watchdog timer

1). Enable

2). Disable

5.6.3. PA3, PA4, PA5 input mode selection mode

1). Pull-high

2). Floating

5.6.4. Low voltage power down

1). Enable

2). Disable

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	VDD	< 6.0V
Input Voltage Range	V_{IN}	-0.5V to VDD + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (VDD = 3.0V, T_A = 25℃)

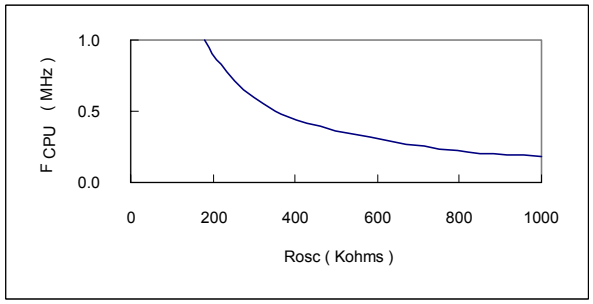
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I_{OP}	-	200	-	μA	F_{OSC2} = 500KHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, 32768Hz off
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I (PA5 - 0)	I_{OH}	-	-0.8	-	mA	VDD = 3.0V, V_OH = 2.0V
Output Sink I (PA5 - 0)	I_{OL}	-	1.0	-	mA	VDD = 3.0V, V_{OL} = 1.0V
Output High I (PA7, 6)	I_{OH}	-	-2.0	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output Sink I (PA7, 6)	I_{OL}	-	2.0	-	mA	VDD = 3.0V, V_{OL} = 1.0V
Output High I (PB1, 0)	I_{OH}	-	-1.7	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output Sink I (PB1, 0)	I_{OL}	-	1.7	-	mA	VDD = 3.0V, V_{OL} = 1.0V
Output High I (PC3, 0)	I_{OH}	-	-0.8	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output Sink I (PC3, 0)	I_{OL}	-	1.0	-	mA	VDD = 3.0V, V_{OL} = 1.0V
Operating Current	I_{OP}	-	200	-	μA	F_{OSC2} = 500kHz @ 3.0V, no load

6.3. DC Characteristics (VDD = 4.5V, T_A = 25℃)

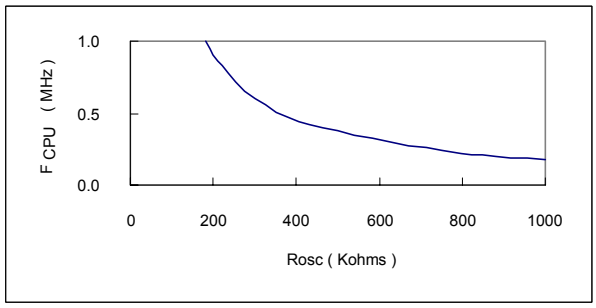
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	430	-	μA	F_{OSC2} = 500kHz @ 4.5V, no load
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 4.5V, 32768Hz off
Input High Level	V_{IH}	2.0	-	-	V	VDD = 4.5V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 4.5V
Output High I (PA5 - 0)	I_{OH}	-	-1.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I (PA5 - 0)	I_{OL}	-	1.0	-	mA	VDD = 4.5V, V_{OL} = 1.0V
Output High I (PA7, 6)	I_{OH}	-	-2.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I (PA7, 6)	I_{OL}	-	2.0	-	mA	VDD = 4.5V, V_{OL} = 1.0V
Output High I (PB1, 0)	I_{OH}	-	-2.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I (PB1, 0)	I_{OL}	-	2.0	-	mA	VDD = 4.5V, V_{OL} = 1.0V
Output High I (PC3, 0)	I_{OH}	-	-1.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I (PC3, 0)	I_{OL}	-	1.0	-	mA	VDD = 4.5V, V_{OL} = 1.0V

6.4. The Relationship between the R_{OSC} and the F_{CPU}

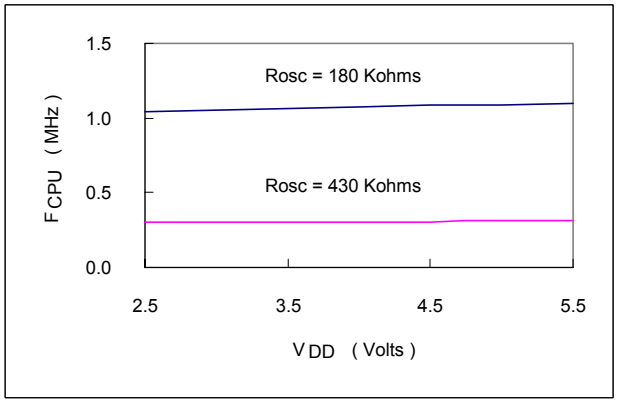
6.4.1. VDD = 3.0V, T_A = 25℃



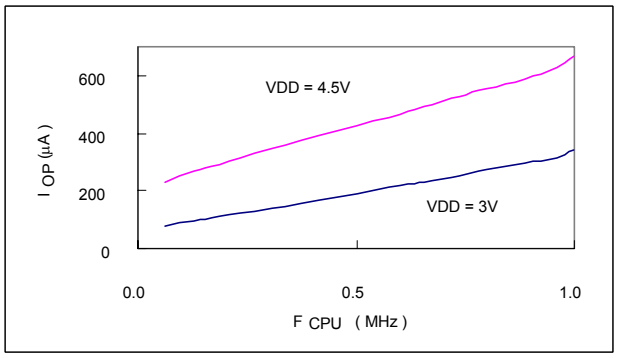
6.4.2. VDD = 4.5V, T_A = 25℃



6.4.3. Frequency vs. VDD

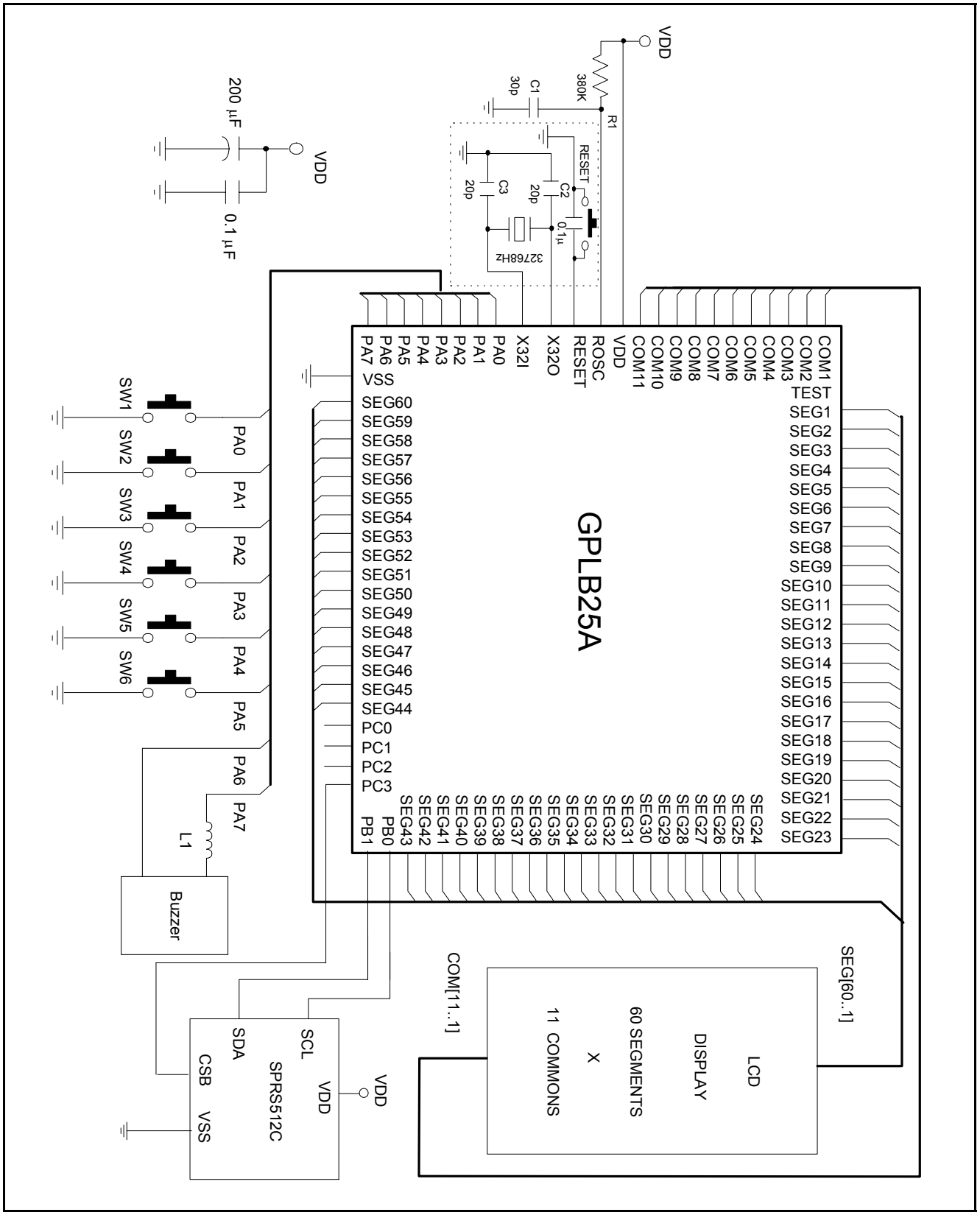


6.4.4. Operating current vs. frequency vs. VDD



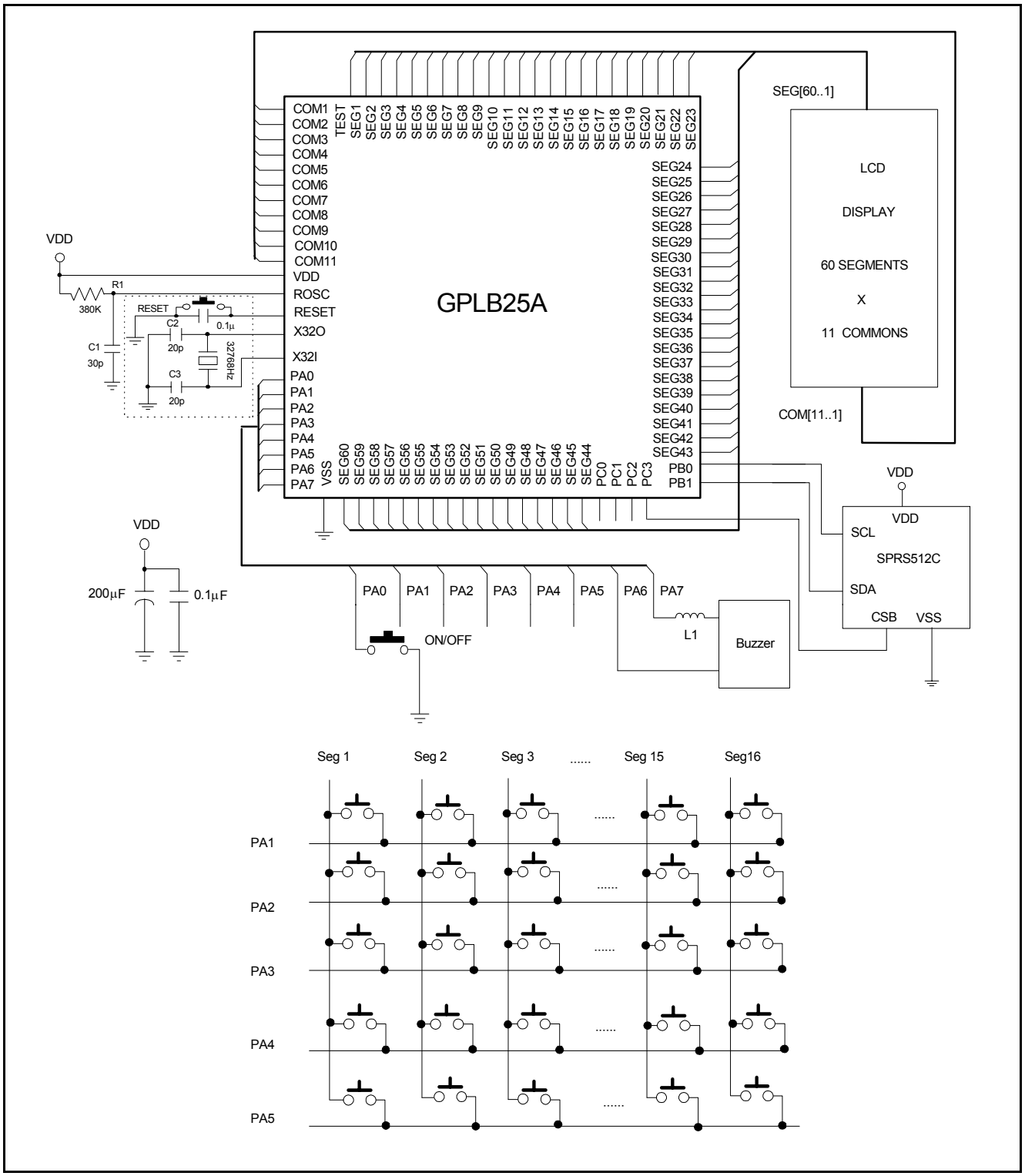
7. APPLICATION CIRCUITS

7.1. Application Circuit - (1)



* Using segments for LCD display only.

7.2. Application Circuit - (2)



* Using segments for both LCD display and key scan.

Note1: In CRYSTAL mode, an accurate time base is generated from the 32768Hz crystal oscillator. The 32768Hz crystal should be installed.

Note2: In ROSC mode, a suitable time base is generated from the R-Oscillator. The 32768Hz crystal is not necessary to be installed.

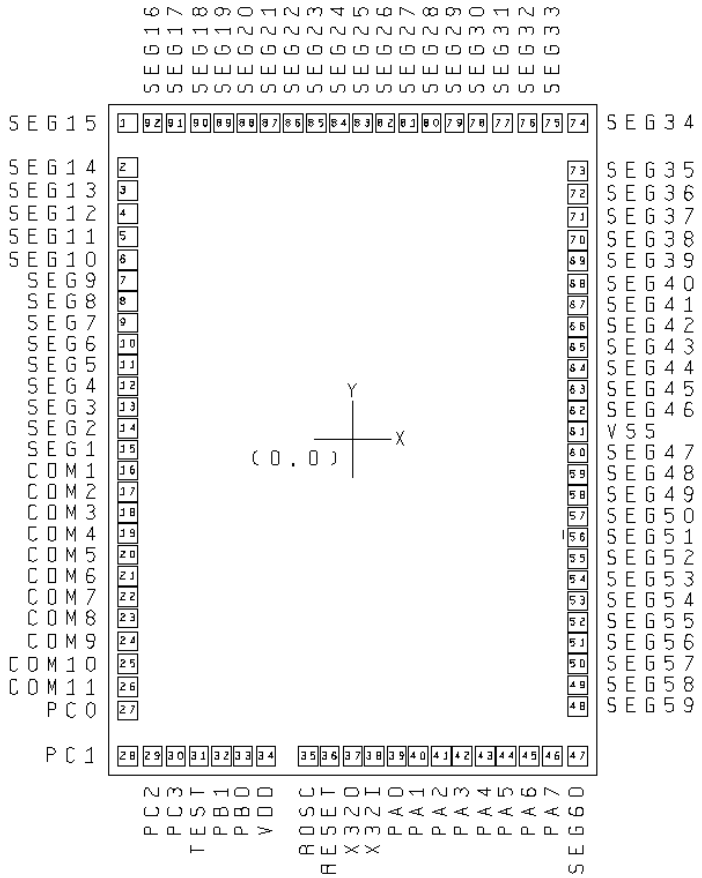
Note3: To avoid the noise interference on PCB around R-Oscillator and crystal circuit, following rules are recommended:

1). R1 and C1 should be placed as close as possible to ROSC pin.

2). C2, C3 and crystal should be placed as close as possible to X32I and X32O. A shielding by ground is suggested.

8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

8.2. Ordering Information

Product Number	Package Type
GPLB25A -NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

8.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	SEG15	-1169	1649	45	PA6	920	-1650
2	SEG14	-1169	1419	46	PA7	1045	-1650
3	SEG13	-1169	1299	47	SEG60	1170	-1650
4	SEG12	-1169	1179	48	SEG59	1170	-1391
5	SEG11	-1169	1059	49	SEG58	1170	-1281
6	SEG10	-1169	944	50	SEG57	1170	-1171
7	SEG9	-1169	829	51	SEG56	1170	-1061
8	SEG8	-1169	719	52	SEG55	1170	-951
9	SEG7	-1169	609	53	SEG54	1170	-841
10	SEG6	-1169	499	54	SEG53	1170	-731
11	SEG5	-1169	389	55	SEG52	1170	-621
12	SEG4	-1169	279	56	SEG51	1170	-511
13	SEG3	-1169	169	57	SEG50	1170	-401
14	SEG2	-1169	59	58	SEG49	1170	-291
15	SEG1	-1169	-51	59	SEG48	1170	-181
16	COM1	-1169	-161	60	SEG47	1170	-67
17	COM2	-1169	-271	61	VSS	1170	43
18	COM3	-1169	-381	62	SEG46	1170	153
19	COM4	-1169	-491	63	SEG45	1170	263
20	COM5	-1169	-601	64	SEG44	1170	373
21	COM6	-1169	-711	65	SEG43	1170	483
22	COM7	-1169	-821	66	SEG42	1170	593
23	COM8	-1169	-931	67	SEG41	1170	703
24	COM9	-1169	-1051	68	SEG40	1170	813
25	COM10	-1169	-1171	69	SEG39	1170	928
26	COM11	-1169	-1291	70	SEG38	1170	1043
27	PC0	-1169	-1411	71	SEG37	1170	1163
28	PC1	-1169	-1650	72	SEG36	1170	1283
29	PC2	-1044	-1650	73	SEG35	1170	1403
30	PC3	-919	-1650	74	SEG34	1170	1649
31	TEST	-795	-1650	75	SEG33	1040	1649
32	PB1	-680	-1650	76	SEG32	910	1649
33	PB0	-565	-1650	77	SEG31	780	1649
34	VDD	-450	-1650	78	SEG30	655	1649
35	ROSC	-231	-1650	79	SEG29	535	1649
36	RESET	-116	-1650	80	SEG28	415	1649
37	X32O	-1	-1650	81	SEG27	295	1649
38	X32I	114	-1650	82	SEG26	175	1649
39	PA0	229	-1650	83	SEG25	55	1649
40	PA1	344	-1650	84	SEG24	-65	1649
41	PA2	459	-1650	85	SEG23	-185	1649
42	PA3	574	-1650	86	SEG22	-305	1649
43	PA4	689	-1650	87	SEG21	-425	1649
44	PA5	804	-1650	88	SEG20	-545	1649

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
89	SEG19	-665	1649	91	SEG17	-915	1649
90	SEG18	-785	1649	92	SEG16	-1042	1649

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
MAR. 10, 2005	1.0	Original Note: The GPLB25A data sheet v1.0 is a continued version of SPLB25A data sheet v1.2.	13