DATA SHEET

GPLB27A

LCD Controller with 46K Bytes OTP

Oct 19, 2012

Version 1.7

Table of Contents

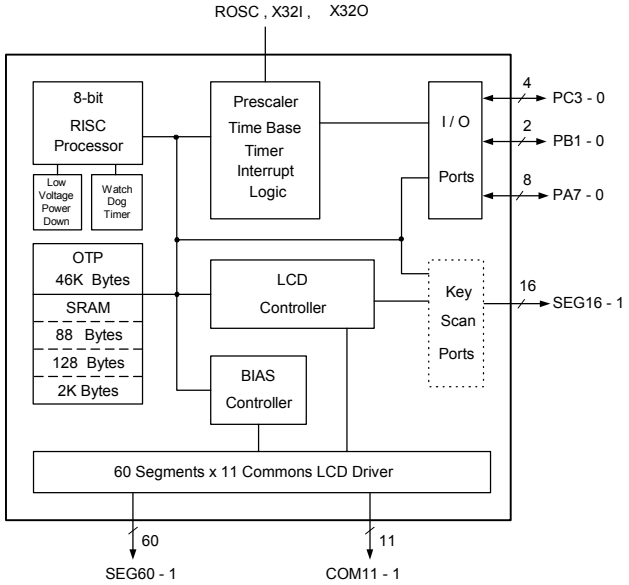
PAGE

LCD CONTROLLER WITH 46K BYTES OTP

1. GENERAL DESCRIPTION

GPLB27A, an 8-bit CMOS microcontroller with advanced processing technology and mechanism by Generalplus, integrates many features in a compact package, including SRAM, One-Time-Programmable (OTP) ROM, I/Os, an interrupt controller, a timer and a LCD controller/driver. The amount of 46K bytes of OTP ROM is able to deliver sufficient space for LCD graphical data. The 2176-bytes of SRAM are all opened to users. In addition, 14 I/Os, timer, LCD driver, NMI controller, Watchdog Timer, Low Voltage Power Down and other features increase the capability of driving sophisticated functions and displaying fantastic LCD graphics. The GPLB27A is a high-end microcontroller that filled with modern technology and strong backup from Generalplus. Obviously, it is one of the most suitable products for LCD applications. The GPLB27A can also fully emulate the GPLB25B. For more information about how to program GPLB27A OTP chip, please refer to ***Generalplus OTP/MTP Writer User's Manual.***

2. BLOCK DIAGRAM



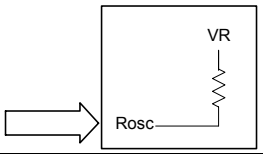
3. FEATURES

- Built-in 8-bit CPU (CPU15)
  - 46K bytes OTP ROM
  - 128 bytes SRAM for CPU working space
  - 2K bytes SRAM for data
  - Max. operating speed:4.0MHz @ 2.6V
- NMI controller
  - 2Hz for Real Time Clock (RTC)
  - 128Hz
  - Key(PA7 - 0)
  - Counter overflow
- Programmable LCD driver
  - Up to 60 segments, up to 11 commons, maximum 660 dots
  - 1/4, 1/5 bias capability
  - 1/4, 1/5, 1/6, 1/8, 1/9, 1/10, 1/11 duty
  - 88 bytes dedicated LCD RAM
  - Fixed LCD COM/SEG driving strength
  - 16-level VLCD adjustable
- Low Voltage Reset Level is 2.4V and can be disabled by mask Option
- Low Voltage Detect Level is 2.6V and can be disabled by mask option
- Low Voltage Power Down and is controlled by register
- Wide operating voltage:
  - 2.6V - 3.6V @ 4.0MHz
  - 3.6V - 5.5V @ 4.0MHz
- Power saving SLEEP mode
- Serial SRAM interface
- Low-power consumption:
  - 500μA typical @ 3.0V, F_{CPU} = 500KHz
  - <20μA typical halt current @ 3.0V
  - <1.0μA typical standby current @ 3.0V
- Peripherals
  - 14 I/O ports (PA7 - 0, PB1 - 0, PC3 - 0)
  - Built-in RC-oscillator (only one resistor is needed)
  - Built-in 32.768KHz crystal oscillator for real time clock function
  - 8-bit reloadable timer/counter with prescaler
  - Watchdog Timer for reliable operation

4. APPLICATION FIELD

- Handheld Game
- Watch, Clock
- Scientific Calculator
- Translator
- Data Bank

5. SIGNAL DESCRIPTIONS

Mnemonic	PAD No.	QFP 100 Pin No.	Type	Description
VDD	33, 90	36, 95	P	Power supply input
VSS	15, 62	17, 66	P	Ground reference
RESET	36	39	I	System reset input (internal pull-high), low active
TEST	39	42	I	Test input (internal pull-low), high active
X32I	37	40	I	32.768KHz crystal input
X32O	38	41	O	32.768KHz crystal output
VR	34	37	O	1.8V Regulator out, for ROSC used only
ROSC	35	38	I	ROSC input, connect to VR pin through a resistor 
PA7 – 0	47 - 40	43 - 50	I/O	Bi-directional I/O port
PC3 – 0	30 - 27	29, 31 - 33	I/O	Bi-directional I/O port
COM11 – 1	26 - 16	18 - 28	O	LCD common output
SEG14 - 1 SEG18 - 15 SEG19 SEG46 - 20 SEG60 - 47	1 - 14 94 - 97 92 63-89 48-61	3 - 16 2, 98 - 100 96 67-79, 81-94 52 - 65	O	LCD segment output
PB1 - 0	31 - 32	34 - 35	I/O	Port B is a bi-directional I/O port, can be software programmed as serial SRAM port.
VPP	93	97	P	High voltage input for OTP programming
VDDT	91	-	P	Double-bonding with VDD(PAD No. 90)

Legend: I = Input, O = Output, P = Power

Note1: All of the SEG16 - 1 can be used as key strobe output pins via programming the Register ($007E). There are two kinds of combinations for key scan.

Note2: When ROSC-mode is selected, pin X32I should be floating or connected to VSS and X32O should be floating.

No. of selected key scan port	The option for key scan port	($ 007E) bit 2, bit 1, bit 0
No. ≦8	SEG8 - 1 or SEG16 - 9	1, 0, 1 1, 1, 0
9≦No. ≦16	SEG16 - 1	1, 1, 1

6. FUNCTIONAL DESCRIPTIONS

6.1. Map of Memory and I/Os

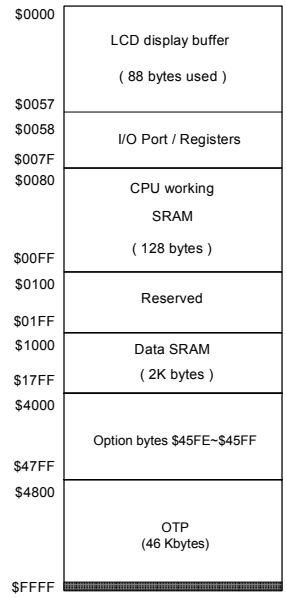
*I/O PORT:

- PORT A_DATA $0073
  PORT A_DIR $0071
  PORT A_CFG $0072
- PORT B_DATA $0067
  PORT B_CFG $0068
- PORT C_DATA $005F
  PORT C_DIR $005E
  PORT C_CFG $005D
- SERIAL SRAM INTERFACE
  $0060 - $0066

*NMI SOURCE:

- 2Hz
- 128Hz
- Power key (PA0)
- Normal key (PA7 - 1)
- Counter overflow

*MEMORY MAP



Note: $FFF2 - $FFF7 are reserved for GENERALPLUS testing.

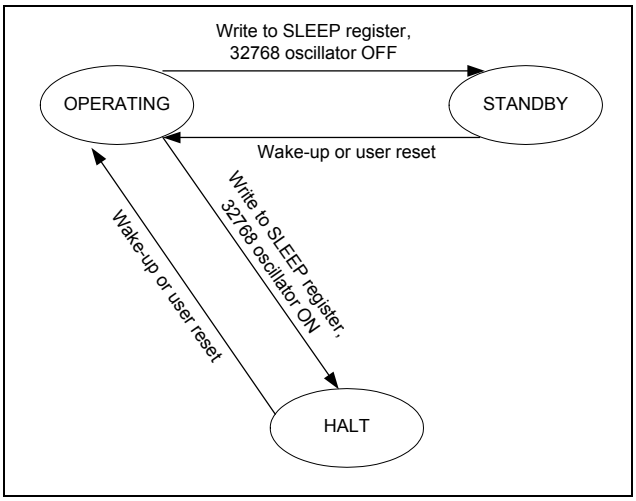
6.2. Operating States

The GPLB27A supports three operating states: standby, halt, and operating. Following table shows the differences among these three operating states.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768 oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

In operating state, all modules (CPU, 32768Hz oscillator, timer/counter, LCD driver…etc.) are activated. The halt/standby state is entered by writing to SLEEP register ($7A). There are four wake-up sources in GPLB27A: PortA wake-up, counter overflow wake-up, 128Hz wake-up and 2Hz wake-up. If any wake-up event occurs, CPU will go to the RESET state.

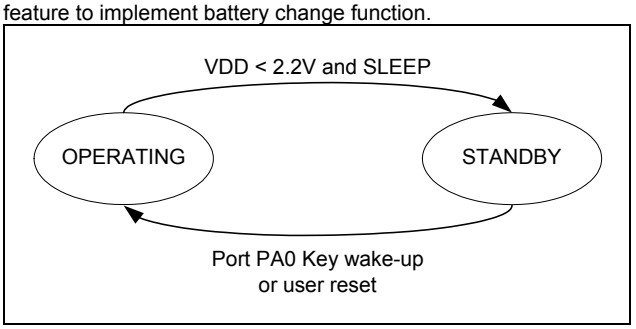
When in standby, all modules will be shut down, and RAM and I/Os remain in their previous states. The current consumption is minimized in standby. The system is in halt state if writing to SLEEP register but keeps 32768Hz oscillator running. In halt state, CPU clock is halted while it waits for an event (key press, timer overflow) to generate a wake-up. The 32768 related modules (timer/counter, LCD driver…) may remain active in halt state. Following figure is a state diagram of GPLB27A.



State Diagram of GPLB27A

6.3. Low Voltage Power Down

The GPLB27A provides a 2.6V voltage detector to detect a low voltage event. If VDD drops below 2.6V, after a SLEEP command is issued, system will shut down all activities (LCD bias, LCD display, 32768Hz oscillator) and enters standby to reduce current consumption. This low voltage power down can be awakened by a PA0 key wake-up or RESET. Users can use this feature to implement battery change function.



State Diagram of Low Voltage Power Down

6.4. LCD Controller/Driver

GPLB27A contains total of 660 dots LCD controller and driver. Programmers can set the LCD configuration (bias, duty) by writing to LCD control register ($70). Once the LCD configuration is initialized, preferred pattern can be displayed by filling appropriate data into LCD buffer. The LCD driver can also operate during sleep by keeping 32768Hz oscillator running. The LCD driver in GPLB27A is designed to fit most LCD specifications. It can either be programmed as 1/4 or 1/5 bias and the duty is also programmable as 1/4, 1/5, 1/6, 1/8, 1/9, 1/10 or 1/11. The following table shows the mapping between LCD and display buffer.

LCD RAM mapping:

	SEG8 - 1 (b7 - 0)	SEG16 - 9 (b7 - 0)	SEG24 - 17 (b7 - 0)	SEG32 - 25 (b7 - 0)	SEG40 - 33 (b7 - 0)	SEG48 - 41 (b7 - 0)	SEG56 - 49 (b7 - 0)	SEG60 - 57 (b3 - 0)
COM1	07H	06H	05H	04H	03H	02H	01H	00H
COM2	0FH	0EH	0DH	0CH	0BH	0AH	09H	08H
COM3	17H	16H	15H	14H	13H	12H	11H	10H
COM4	1FH	1EH	1DH	1CH	1BH	1AH	19H	18H
COM5	27H	26H	25H	24H	23H	22H	21H	20H
COM6	2FH	2EH	2DH	2CH	2BH	2AH	29H	28H
COM7	37H	36H	35H	34H	33H	32H	31H	30H
COM8	3FH	3EH	3DH	3CH	3BH	3AH	39H	38H
COM9	47H	46H	45H	44H	43H	42H	41H	40H
COM10	4FH	4EH	4DH	4CH	4BH	4AH	39H	48H
COM11	57H	56H	55H	54H	53H	52H	51H	50H

6.5. Watchdog Timer (WDT)

An on-chip watchdog timer is available on GPLB27A. The WDT is designed to recover system from abnormal operation. If the system is hanged, WDT will generate a system reset to restart system after 1 second. If WDT is enabled, the WDT should be cleared every 0.5 seconds to avoid accidental reset. The WDT can be cleared by writing to $7F. Note that the WDT works in both with/without 32768Hz crystal modes, but WDT with 32768 Hz crystal mode is recommended.

6.6. Programmable Options ($45FE~$45FF)

6.6.1. 32768 oscillator ($45FE, bit0)

1: X'TAL

6.6.2. Watchdog timer ($45FE, bit1)

1: Enable

0: Disable

6.6.3. PA3, PA4, PA5 input mode selection mode ($45FE, bit2)

1: Pull-high

0: Floating

6.6.4. Low voltage reset ($45FE, bit3)

1: Enable

0: Disable

6.6.5. Low voltage detect ($45FE, bit4)

1: Enable

0: Disable

6.6.6. OTP Security ($45FF, bit7)

1: No security (OTP is readable by writer)

0: Security (OTP is not readable by writer)

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	VDD	< 6.0V
Input Voltage Range	VIN	-0.5V to VDD + 0.5V
Operating Temperature	TA	0℃ to +60℃
Storage Temperature	TSTO	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 3.0V, T_A = 25℃)

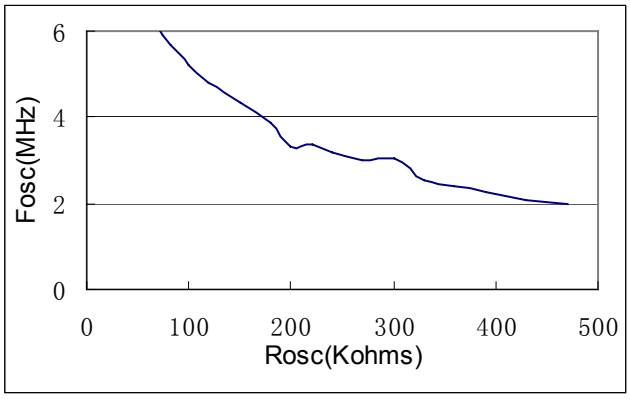
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.6	-	3.6	V	For 2-battery
Operating Current	IOP	-	500	-	μA	FOSC2 = 500KHz @ 3.0V, no load
Standby Current	ISTBY	-	-	2.0	μA	VDD = 3.0V, 32768Hz off
Halt Current	IHALT	-	20	-	μA	VDD = 3.0V, CPU off, LCD on, 32kHz xtal on, no load
Input High Level	VIH	2.0	-	-	V	VDD = 3.0V
Input Low Level	VIL	-	-	0.8	V	VDD = 3.0V
Output High I (PA5 - 0)	IOH	-	-0.8	-	mA	VDD = 3.0V, VOH = 2.0V
Output Sink I (PA5 - 0)	IOL	-	1.0	-	mA	VDD = 3.0V, VOL = 1.0V
Output High I (PA7, 6)	IOH	-	-2.0	-	mA	VDD = 3.0V, VOH = 2.0V
Output Sink I (PA7, 6)	IOL	-	2.0	-	mA	VDD = 3.0V, VOL = 1.0V
Output High I (PB1, 0)	IOH	-	-1.7	-	mA	VDD = 3.0V, VOH = 2.0V
Output Sink I (PB1, 0)	IOL	-	1.7	-	mA	VDD = 3.0V, VOL = 1.0V
Output High I (PC3, 0)	IOH	-	-0.8	-	mA	VDD = 3.0V, VOH = 2.0V
Output Sink I (PC3, 0)	IOL	-	1.0	-	mA	VDD = 3.0V, VOL = 1.0V

7.3. DC Characteristics (VDD = 4.5V, T_A = 25℃)

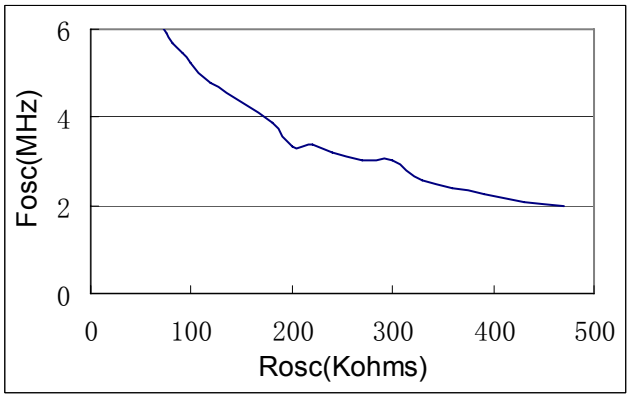
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	1000	-	μA	F_{OSC2} = 500kHz @ 4.5V, no load
Standby Current	I_{STBY}	-	-	3.0	μA	VDD = 4.5V, 32768Hz off
Halt Current	I_{HALT}	-	40	-	μA	VDD = 4.5V, CPU off, LCD on, 32kHz xtal on, no load
Input High Level	V_{IH}	3.0	-	-	V	VDD = 4.5V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 4.5V
Output High I (PA5 - 0)	I_{OH}	-	-1.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I (PA5 - 0)	I_{OL}	-	1.0	-	mA	VDD = 4.5V, V_{OL} = 1.0V
Output High I (PA7, 6)	I_{OH}	-	-2.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I (PA7, 6)	I_{OL}	-	2.0	-	mA	VDD = 4.5V, V_{OL} = 1.0V
Output High I (PB1, 0)	I_{OH}	-	-2.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I (PB1, 0)	I_{OL}	-	2.0	-	mA	VDD = 4.5V, V_{OL} = 1.0V
Output High I (PC3, 0)	I_{OH}	-	-1.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I (PC3, 0)	I_{OL}	-	1.0	-	mA	VDD = 4.5V, V_{OL} = 1.0V

7.4. The Relationships between the R_{OSC} and the F_{CPU}

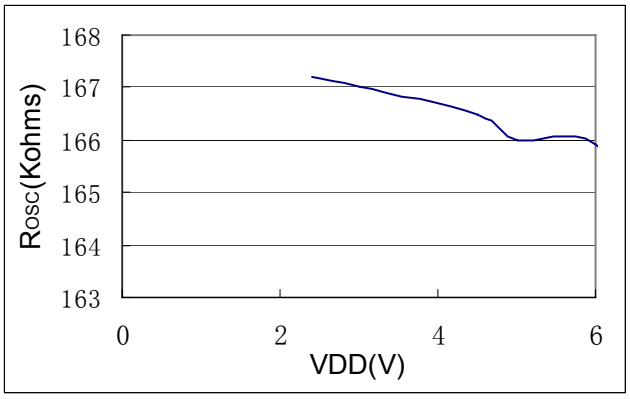
7.4.1. VDD=3V , 25℃



7.4.2. VDD=4.5V , 25℃

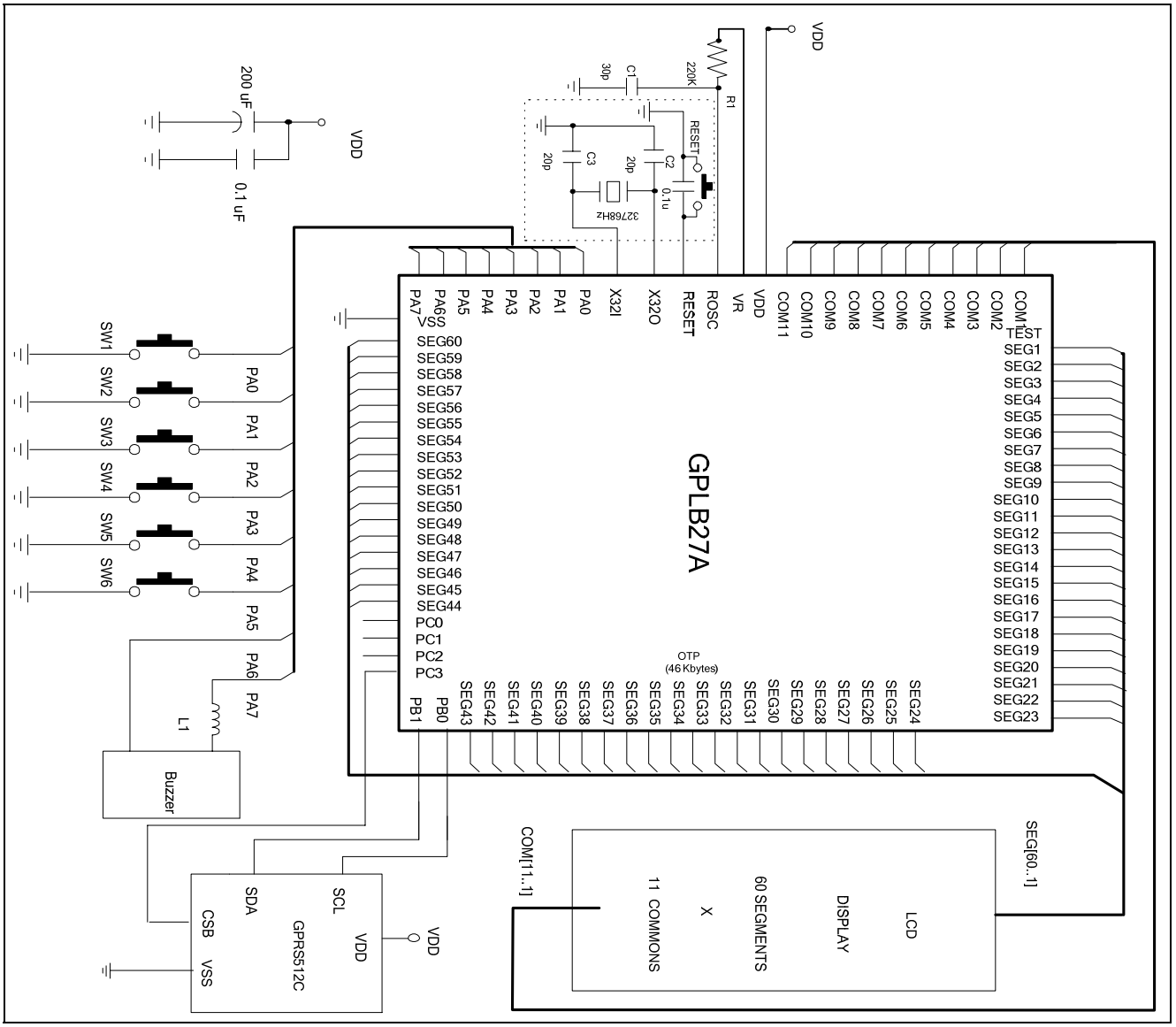


7.5. The Relationships between the VDD and the R_{OSC} @ 4.0M Hz



8. APPLICATION CIRCUITS

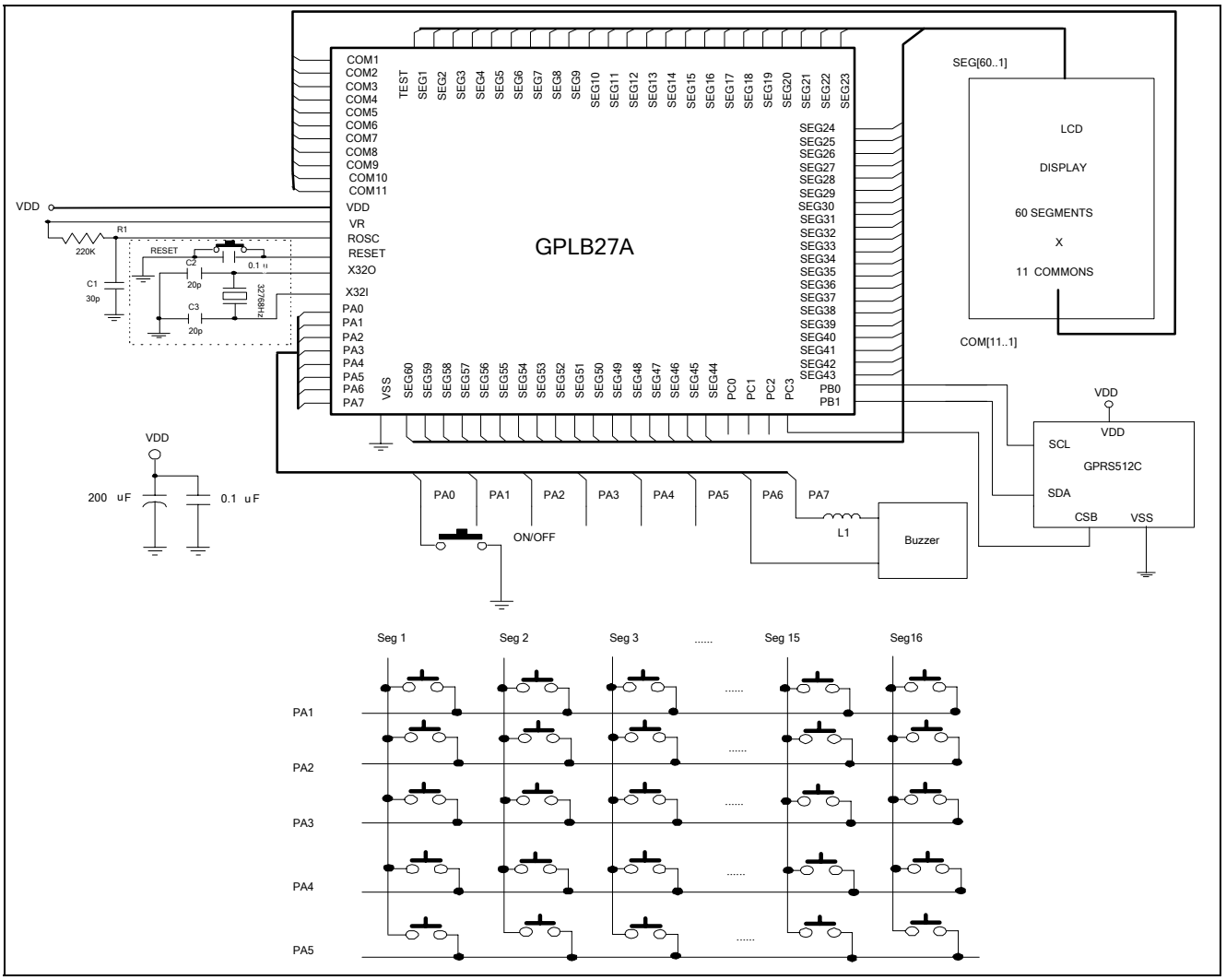
8.1. Application Circuit - (1)



* Using segments for LCD display only.

Note1: The capacitor values of C2/C3 shown in above figures are for design guidance only. Different capacitor values may be needed for different crystals used.

8.2. Application Circuit - (2)



* Using segments for both LCD display and key scan.

Note1: In CRYSTAL mode, an accurate time base is generated from the 32768Hz crystal oscillator. The 32768Hz crystal should be installed.

Note2: The capacitor values of C2/C3 shown in above figures are for design guidance only. Different capacitor values may be needed for different crystal used.

Note3: In ROSC mode, a suitable time base is generated from the R-Oscillator. The 32768Hz crystal is not necessary to be installed.

Note4: To avoid the noise interference on PCB around R-Oscillator and crystal circuit, following rules are recommended:

1). R1 and C1 should be placed as close as possible to ROSC pin.

2). C2, C3 and crystal should be placed as close as possible to X32I and X32O. A shielding by ground is suggested.

9. ORDERING INFORMATION

Product Number	Package Type
GPLB27A-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
OCT 19, 2012	1.7	Package information removed.	5,11
FEB. 11, 2010	1.6	Modify 7.2 DC Characteristics.	9
APR. 20, 2009	1.5	1. Add description about emulation of GPLB25B. 2. Remove 1/3 bias description.	3 3, 6
FEB. 27, 2007	1.4	Delete 5.6.1. “0: R-oscillator divided to about 32KHz”.	7
DEC. 22, 2006	1.3	1. Add halt current and revise operating current information. 2. Add pin description for VPP. 3. Add R_{OSC} vs. F_{CPU} information. 4. Add footnote for capacitor values used with 32kHz crystal.	3, 8, 9 4 9 11
SEP. 21, 2005	1.2	Modified the “6.2.DC Characteristics: Standby Current’s Max.”, “6.3.DC Characteristics: Standby Current’s Max.” and “Input High Level’s Min.”.	6
APR. 29, 2005	1.1	Add QFP 100 package information.	2, 3, 12
APR. 12, 2005	1.0	Original Note: The GPLB27A data sheet v1.0 is a continued version of SPLB27A data sheet v1.0.	12