DATA SHEET

GPLB301A

2368 Dots LCD Controller with 512KB OTP

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Version 1.5

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2368 DOTS LCD CONTROLLER WITH 512KB OTP

1. GENERAL DESCRIPTION

The GPLB301A, an 8-bit CMOS microprocessor, contains 4288 bytes working RAM, 512K bytes OTP memory, 30 I/Os, interrupt/wakeup controller, UART for serial communication, Serial SRAM interface and Bus memory interface for memory expansion, and automatic display controller/driver for LCD. It is an OTP (one-time-programming) version for GPLB30/ GPLB32 /GPLB33 /GPLB37 /GPLB38B. The embedded OTP memory enables users to customize application programs fast and conveniently. Users may use GPLB301A for prototyping and then use GPLB30/ GPLB32/ GPLB33/ GPLB37/ GPLB38B for mass production.

The pin sequence of GPLB301A is compatible with GPLB32 and GPLB37. It also features one PWM driver with two audio channels to produce attractive sound effects easily. Its large OTP area can be used to store both program and audio data (speech duration approx. 138 seconds at 7KHz sampling rate using a 4-bit ADPCM). The built-in UART speeds up data transmission between two devices. Furthermore, a SLEEP (power-down) function is also built in to extend power life. The GPLB301A is designed with state-of-the-art technology to fulfill LCD application needs, especially for hand-held products.

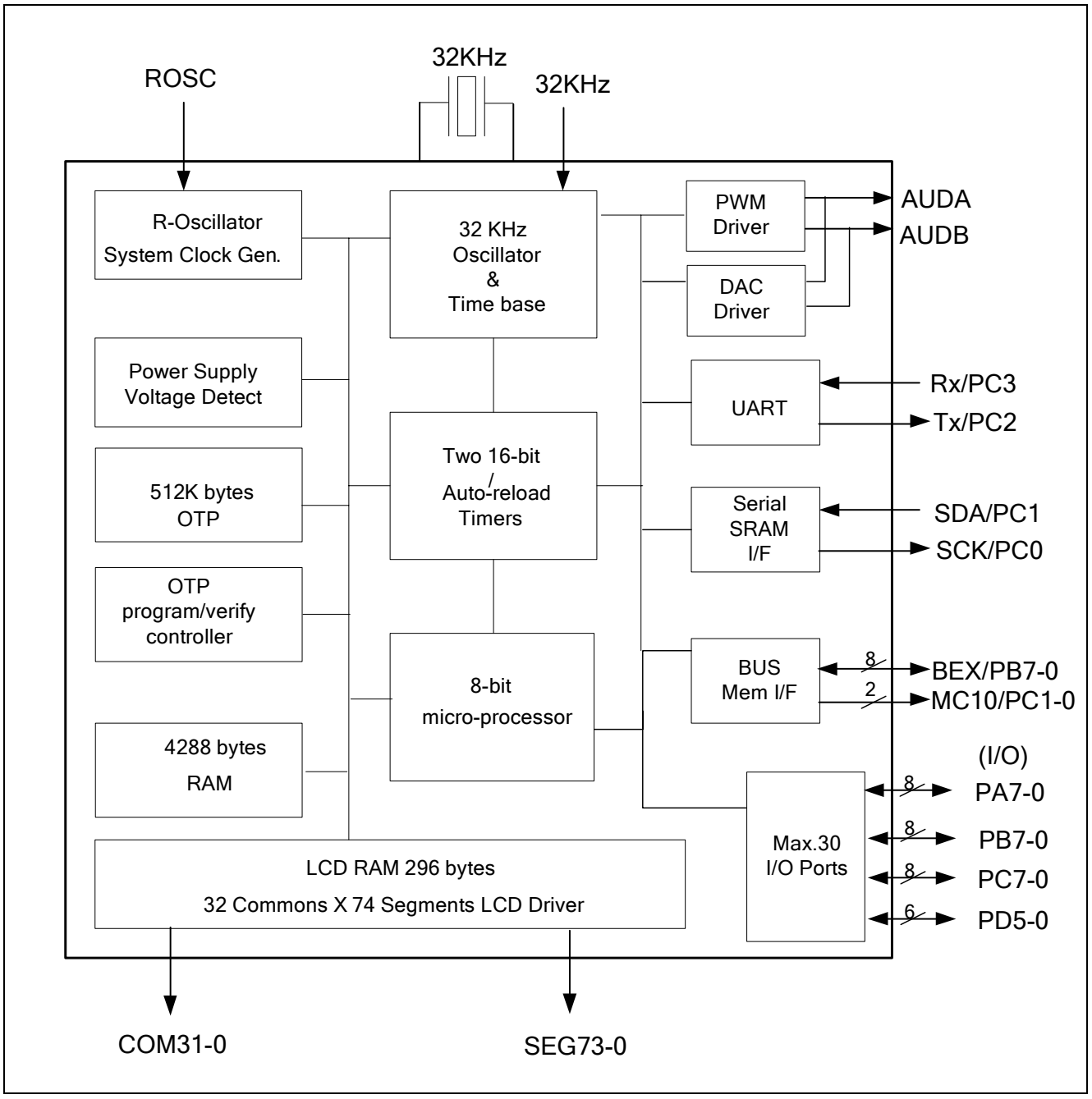
2. FEATURES

GPLB301 can emulate varieties of GPLB3X series, The GPLB301 is able to emulate the following series via options.

Body selected	**ALL**	**GPLB30A**	**GPLB32A**	**GPLB33A**	**GPLB33B**	**GPLB37A**	**GPLB38B**
RAM Size	4288 Bytes	2752 Bytes	1216 Bytes	1216 Bytes	1024 Bytes	1216 Bytes	1216 Bytes
OTP Size	512K Bytes	96K Bytes	512K Bytes	64K Bytes	96K Bytes	256K Bytes	512K Bytes
Wake-up Sources	6	6	6	6	5	6	5
Interrupt Sources	7	7	7	7	5	7	5
UART	Yes	Yes	Yes	Yes	-	Yes	-
Serial SRAM Interface	Yes	Yes	Yes	Yes	-	Yes	-
BUS Memory Interface	Yes	Yes	-	-	-	-	-
Voltage Regulator for External Memory Devices	Yes	Yes	-	-	-	-	-
Segment	74	70	74	52	48	74	64
Common	32	16	32	16	16	32	16
LCD Dots	2368	1120	2368	832	768	2368	1024
Bias	1/5, 1/6	1/5	1/5, 1/6	1/5	1/3,1/4,1/5	1/5, 1/6	1/5
Duty	1/16, 1/32	1/16	1/16, 1/32	1/16	1/4,1/8,1/16	1/16, 1/32	1/16
LCD RAM	296 Bytes	140 Bytes	296 Bytes	104 Bytes	96 Bytes	296 Bytes	128 Bytes
Max. I/O Pins	30	29	28	24	24	28	12
PA	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]
PB	[7:0]	[7:0]	[5:0]	[7:0]	[7:0]	[5:0]	-
PC	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]	[7:4]
PD	[5:0]	[4:0]	[5:0]	-	-	[5:0]	-
Dedicated I/Os:	PA[0:7], PB[0:7], PC[0:7]	PA[0:4]	PA[0:5]	PA[0:6]	PA[0:7], PC[0:1]	PA[0:5]	PA[0:7] PC[7:4]
Shared Pin I/Os: PA	-	PA[5:7] / SEG[69:67]	PA[6:7] / SEG[63:62]	PA[7] / SEG[51]	PB[0:7] / SEG[41:34]	PA[6:7] / SEG[63:62]	-
Shared Pin I/Os: PB	-	PB[0:7] / BMI AD BUS[0:7] / SEG[64:57]	PB[0:5] / SEG[69:64] / COM[21:16]	PB[0:7] / SEG[46:39]	PC[2:7] / SEG[47:42]	PB[0:5] / SEG[69:64] / COM[21:16]	-

Body selected	ALL	GPLB30A	GPLB32A	GPLB33A	GPLB33B	GPLB37A	GPLB38B
Shared Pin I/Os: PC[0:1]	-	PC[0:1] / BMI MC[0:1] / SSRAM SDA, SCK	PC[0:1] / SSRAM SCK, SDA / SEG[61:60]	PC[0:1] / SSRAM SCK, SDA	-	PC[0:1] / SSRAM SCK, SDA / SEG[61:60]	-
Shared Pin I/Os: PC[2:3]	-	PC[2:3] / UART Tx / Rx / SEG[66:65]	PC[2:3] / UART Tx / Rx	PC[2:3] / UART Tx / Rx	-	PC[2:3] / UART Tx / Rx	-
Shared Pin I/Os: PC[4:5]	-	PC[4:5] / SEG[56:55] / Ext_I , Ext_CK	PC[4:5] / SEG[73:72] / COM[25:24] / Ext_I, Ext_ck	PC[4:5] / SEG[50:49] / Ext_I , xt_ck	-	PC[4:5] / SEG[73:72] / COM[25:24] / Ext_I, Ext_ck	-
Shared Pin I/Os: PC[6:7]	-	PC[6:7] / SEG[54:53]	PC[6:7] / SEG[71:70] / COM[23:22]	PC[6:7] / SEG[48:47]	-	PC[6:7] / SEG[71:70] / COM[23:22]	-
Shared Pin I/Os: PD	PD[0:5] / COM[31:26]	PD[0:4] / SEG[52:48]	PD[0:5] / COM[31:26]	-	-	PD[0:5] / COM[31:26]	-

3. BLOCK DIAGRAM



4. APPICATION FIELD

- Handheld games
- Scientific calculator
- Talking calculator, Talking clock
- Talking instrument controller
- General speech synthesizer
- Data Bank

5. SIGNAL DESCRIPTIONS

5.1. GPLB30/GPLB33A/GPLB33B/GPLB38B is Selected

Mnemonic	PIN No.	LQFP 216 PIN No.	Type	Description
SEG73 - 47 SEG46 - 19 SEG18 - 0	63~89 98~125 129~147	73-99 126-153 175-193	O	LCD driver segment output. SEG15 - 0 share pin with key scan port.
COM15 - 0, COM25 - 16, COM31 - 26 / PD0 - 5	148~162,1 53~62 47~52	194-208,5 63-72 57-62	O	LCD driver common output. COM31 - 26 optioned to PD0 - 5.
PA7 - 0	46~39	56-55,48-43	I/O	Port A is a bi-directional I/O port, which can be software programmed as wake up I/O.
PB7 - 0	38~31	42-35	I/O	Port B is a bi-directional I/O port. Share pin with Bus Memory Interface Addr/Data.
PC7 - 4	30~27	34-31	I/O	Port C is a bi-directional I/O port.
PC1 / MC1 / SDA PC0 / MC0 / SCK	24~23	29-28	I/O	Port C is a bi-directional I/O port. Share pin with Bus Memory MC1 - 0. Also share pin with SDA/SCK.
PC3 / Rx	26	30	I/O	UART input. Share pin with PC3.
PC2 / Tx	25	29	I/O	UART output. Share pin with PC2.
ROSC	7	11	I	ROSC input, connect to VDD through a resistor.
RESETB	6	10	I	System reset input, low active.
AUDA, AUDB	5,3	9,7	O	PWM audio output.
X32I	10	14	I	32.768KHz crystal input or connect to VDD through a resistor (option).
X32O	9	13	O	32.768KHz crystal output.
TESTP	8	12	I	Test input.
CUP4 - 1	15~12	19-16	P	LCD voltage generation. Charge pump capacitor interconnection pins.
VLCD	22	26	P	LCD voltage generation.
V4 - 1	19~16	23-20	P	LCD voltage generation.
VROUT	20	24	P	Internal regulator output. Enable or disable via bonding option. Should be connected to VDD if internal Regulator is disabled.
VDD	90,126	118,154	P	Positive supply for logic and IO pins.
VDD	21	25	P	Positive supply for analog pins.
VSS	11,91,127	15,119,155	P	Ground reference for logic and IO pins.
PVDD	4	8	P	Positive supply for PWM driver.
PVSS	2	6	P	Ground reference for PWM driver.

Legend: I = Input, O = Output, P = Power, B = Bonding option

Note: *See body option section for details. If GPLB33A is selected, SEG[73:52] are disabled and COM[31:16] are disabled. GPLB30's PA7 can be optioned to SEG67. If GPLB30 is selected and PA7/S67 option is set as 1, PA7 is enabled and SEG67 is disabled.

5.2. GPLB32/GPLB37 is Selected

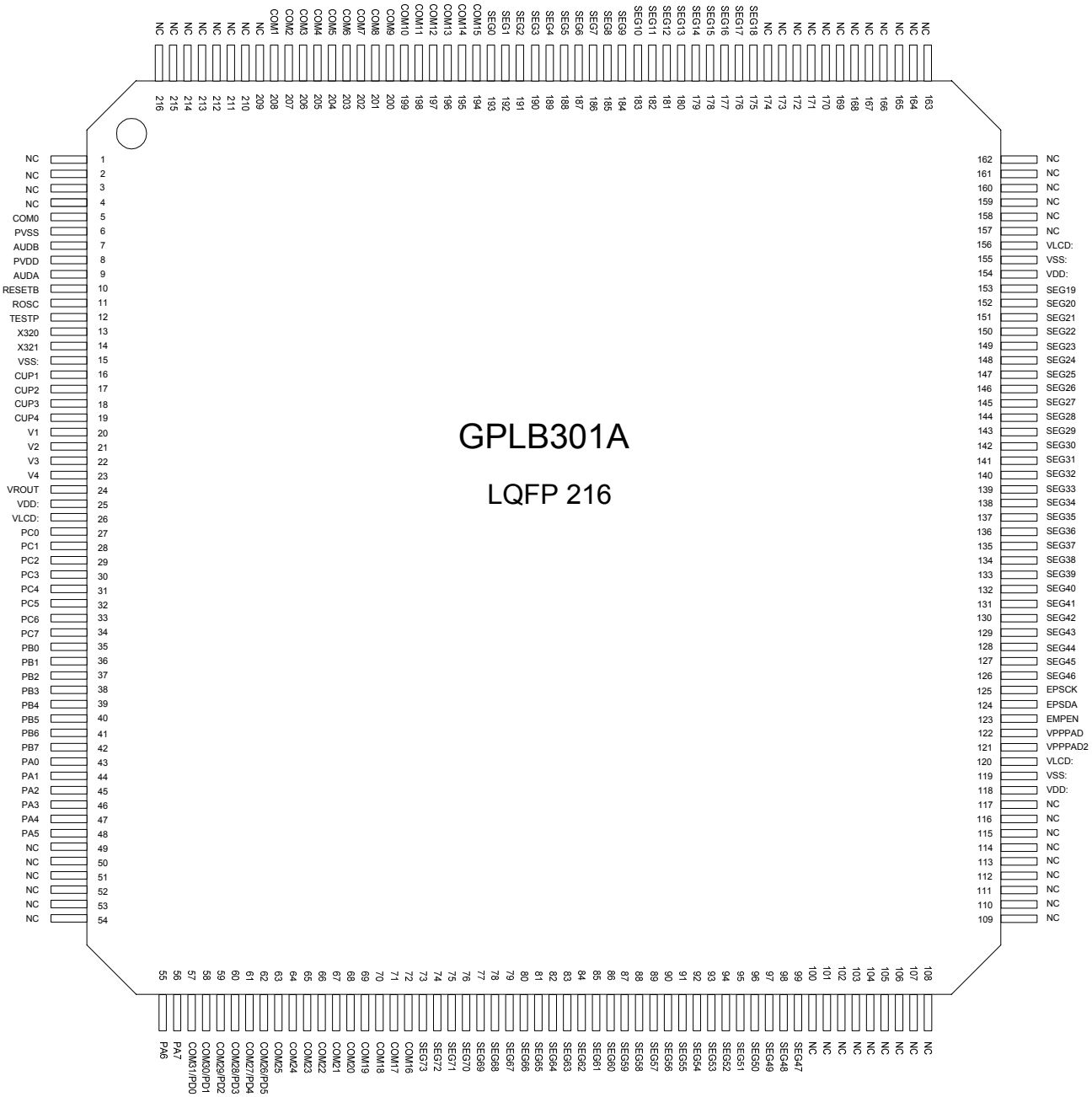
Mnemonic	PIN No.	LQFP 216 PIN No.	Type	Description
SEG59 - 47	77~89	73-99	O	LCD driver segment output. SEG15 - 0 share pin with key scan port.
SEG46 - 19	98~125	126-153		
SEG18 - 0	129~147	175-208		
SEG63 - 62 / PA6 - 7	73~74	83-84		SEG63 - 62 optioned to PA6 - 7.
SEG61 - 60/PC0-1/SCK, SDA	75~76	85-86		SEG61 - 60 optioned to PC0 - 1 / SCK, SDA.
SEG73 - 70/COM25-22/ PC4 - 7	63~66	73-76		SEG73 - 70 optioned to COM25 - 22 or PC4 - 7.
SEG69 - 64 / COM21-16 / PB0-5	67~72	77-82		SEG69 - 64 optioned to COM21 - 16 or PB0 - 5.
COM15 - 0	148~162,1	194-208,5	O	LCD driver common output.
COM31 - 26 / PD0 - 5	47~52	57-62		COM31 - 26 optioned to PD0 - 5.
PA5 - 0	44~39	48-43	I/O	Port A is a bi-directional I/O port, which can be software programmed as wake up I/O.
PC3 / Rx	26	30	I/O	UART input. Share pin with PC3.
PC2 / Tx	25	29	I/O	UART output. Share pin with PC2.
ROSC	7	11	I	R-oscillator input, connect to VDD through a resistor.
RESETB	6	10	I	System reset input, low active.
AUDA, AUDB	5,3	9,7	O	PWM/DAC audio output.
X32I	10	14	I	32.768KHz crystal input or connect to VDD through a resistor (option)
X32O	9	13	O	32.768KHz crystal output.
TESTP	8	12	I	Test input
CUP4 - 1	15~12	19-16	P	LCD voltage generation. Charge pump capacitor inter-connection pins.
VLCD	22	26	P	LCD voltage generation.
V4 - 1	19~16	23-20	P	LCD voltage generation.
VDD	90,126	118,154	P	Positive supply for logic and IO pins.
VDD	21	25	P	Positive supply for analog pins.
VSS	11,91,127	15,119,155	P	Ground reference.
PVDD	4	8	P	PWM driver power.
PVSS	2	6	P	PWM driver ground reference.

5.3. OTP Program/Verify Pin

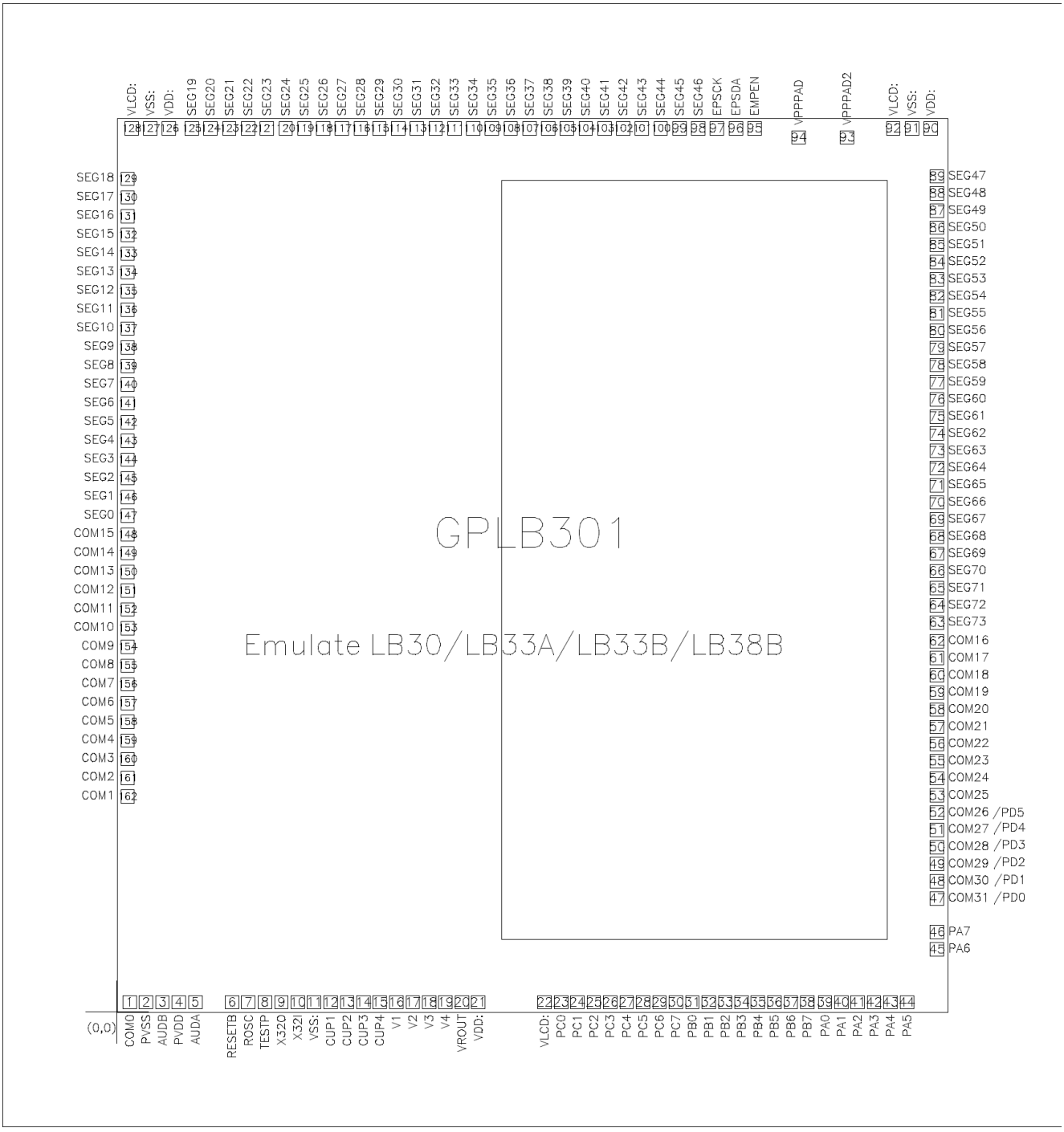
Mnemonic	PIN No.	LQFP 216 PIN No.	Type	Description
VPPPAD, VPPPAD2	94-93	122-121	P	High voltage input for OTP program
EMPEN	95	123	I	OTP program/verify enable (high active)
EPSDA	96	124	I/O	OTP program/verify serial data
EPSCK	97	125	I	OTP program/verify serial clock

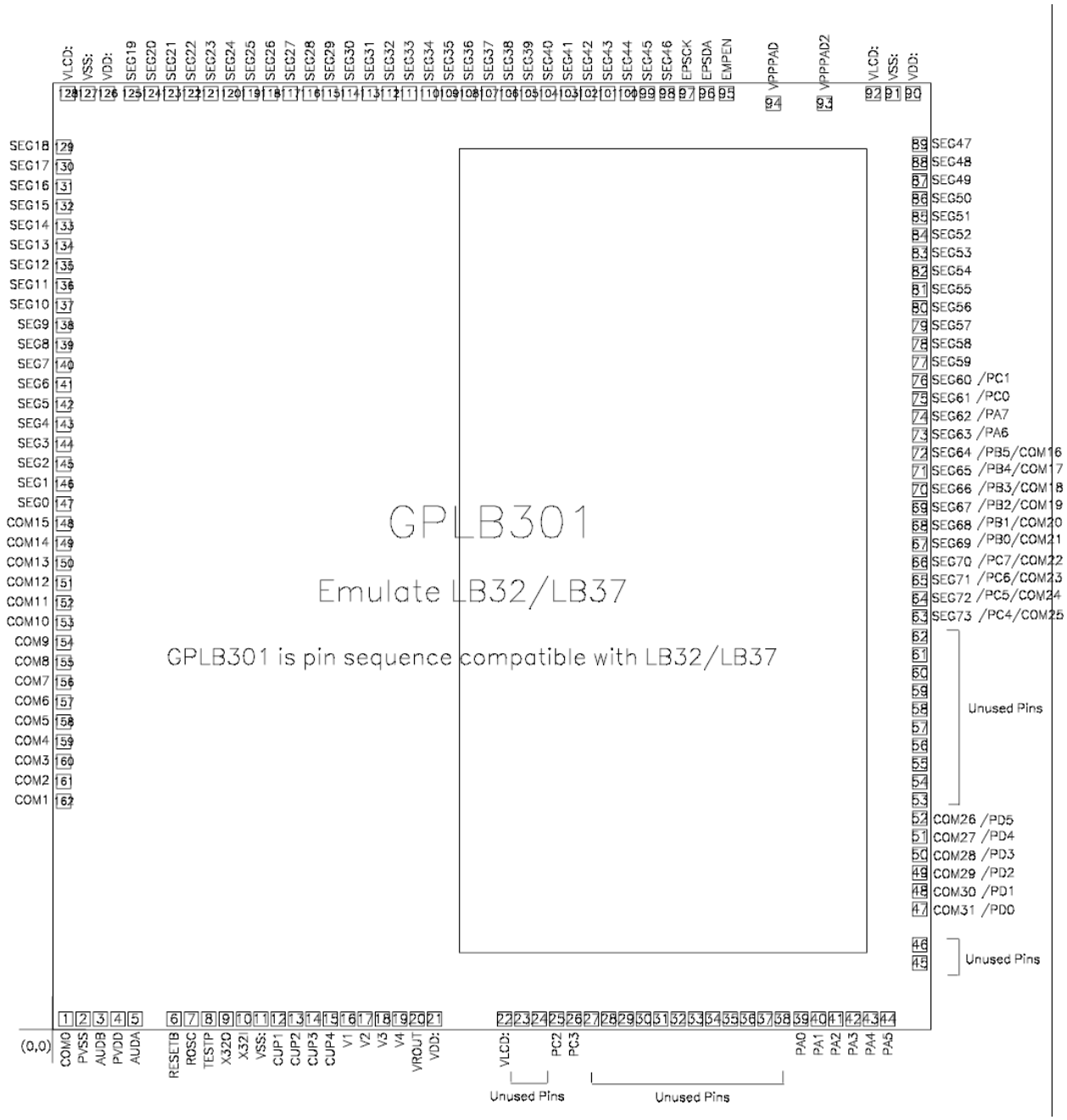
5.4. PIN Map

LQFP 216 Package Top View



5.5. PAD Assignment





This IC substrate should be connected to VSS or floated

Note1: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

Note2: Pin VROUT should be connected to VDD if internal Regulator is disabled.

6. FUNCTIONAL DESCRIPTIONS

6.1. Memories

The GPLB301A contains 512K-byte OTP and 4288-byte SRAM. Cooperating with Generalplus bus extender, GPBA01B, the external memory, either RAM or OTP, can be extended up to 4MB. Serial SRAM interface is also provided in GPLB301A, thus SRAM space can be extended with Generalplus Serial SRAM, GPRS512C or SPRS1024C.

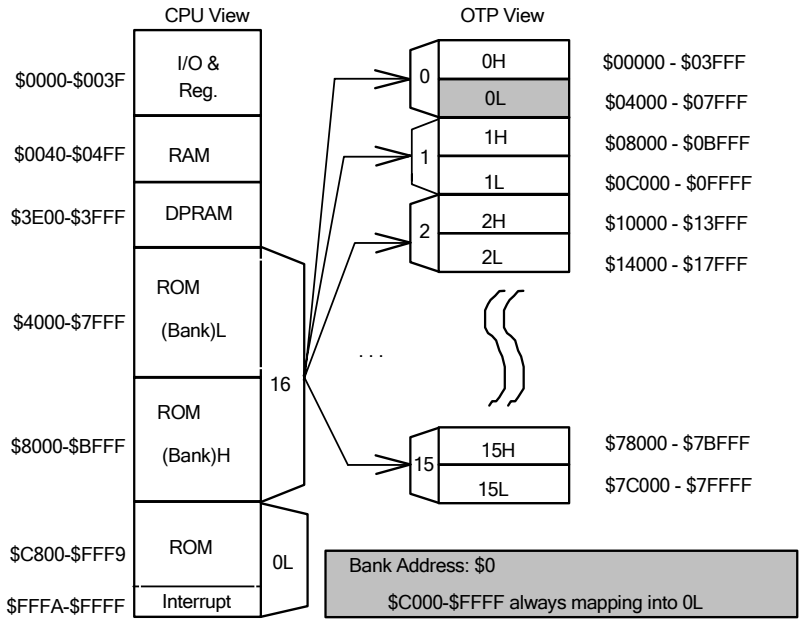
6.2. Map of Memory and I/Os

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



1. $4000-$BFFF can be external memory if MEXT ($07.7) = 1 and Bank port ($00.7) = 1.
2. $C000-$FFFF can be external memory if MEXT ($07.7) = 1 and EXC ($0b.1) = 1.
3. User program should start from $C800. $C000-$C7FF is the test program area.
4. User program interrupt vector: $FFFA ~ $FFFF.
5. Test Program interrupt vector: $FFF2~$FFF7.

6.3. Operating States

There are three operation modes involved in GPLB301A: standby, halt and operating. The following table describes the differences between these modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

6.3.1. Operating mode

In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated. Generally speaking, this mode consumes the highest power.

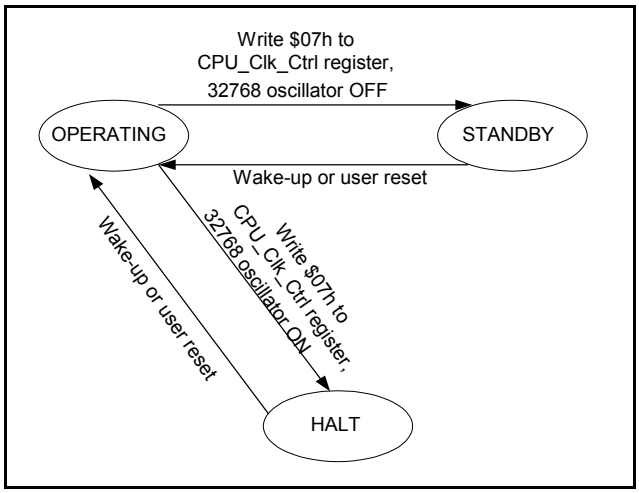
6.3.2. Standby mode

Write “07H” to P_04H_CPU_Clk_Ctrl Register ($04) and turn off 32768Hz oscillator to activate standby mode. The standby mode is a mode where the device is placed in its lowest power consumption state. In standby mode, all functions are turned off; in addition, RAM and I/Os remain in their previous states.

6.3.3. Halt mode

Write “07H” to P_04H_CPU_Clk_Ctrl Register ($04) but still keeps 32768Hz oscillator running to enter halt mode. In halt mode, CPU clock halts and waits for an event (e.g. key press, timer overflow) to wake up. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode.

The following figure is the GPLB301A state diagram:



GPLB301A State Diagram

6.4. Speech and Melody

For speech synthesis, the GPLB301A provides several timer interrupts for a precise sampling frequency. The sound data can be stored into OTP and be played back. Several algorithms are recommended for high fidelity and good compression of sound such as PCM and ADPCM. For melody synthesis, the GPLB301A provides a dual tone mode. Once in the dual tone mode, users only need to program the tone frequency for each channel by writing to the timer/counter TM0 and TM1, and set the envelope of each channel. The hardware will toggle the tone wave automatically.

6.5. LCD Controller/Driver

The GPLB301A contains a 2368-dot LCD controller/driver. Programmers are able to define the LCD configuration by setting up the LCD Control Register. Once the LCD configuration is completed, the desired pattern can be displayed by filling the LCD buffer with proper data. The LCD driver can also operate during sleep by keeping 32768Hz oscillator running. The LCD driver in GPLB301A supports 1/4, 1/8, 1/16, 1/32 duty and 1/3, 1/4, 1/5, 1/6 bias.

6.6. LCD Voltage Generation

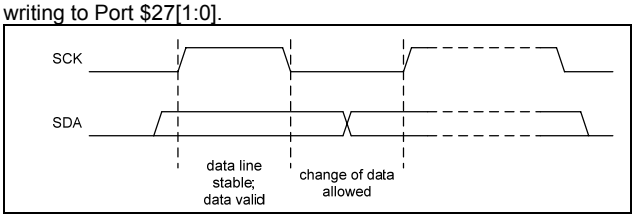
The GPLB301A offers a voltage regulator and a charge-pumping circuit. The voltage regulator provides a reference voltage (V2) for the charge-pumping circuit to generate VLCD. Users can get the desired VLCD by changing the output reference voltage (writing to register) of the voltage regulator. Enabling the voltage regulator and charge-pumping circuit gets a stable VLCD that will not be affected by VDD. The VLCD is adjustable from 2.45V to 5.75V (in 1/5 LCD bias) or 2.95V to 6.85V (in 1/6 LCD bias) with 32 levels.

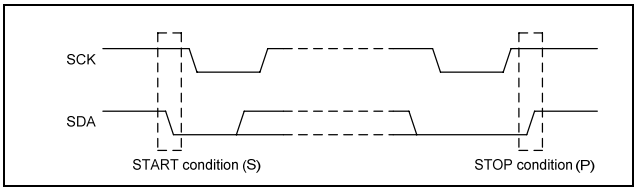
6.7. PWM Output

Internally, the GPLB301A has a pair of PWM drivers, supporting two sound channels. Each channel is able to play speech or tone individually. The PWM drivers can directly drive speaker or buzzer without buffer or amplification circuit.

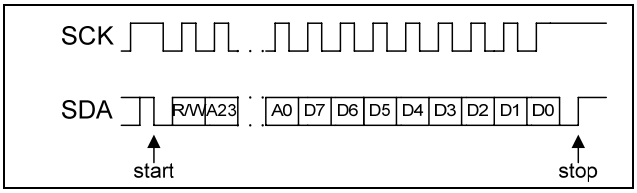
6.8. Serial SRAM Interface

The Serial SRAM interface is able to expand the data storage SRAM. The Control Registers are ranged from $30-$36. Note that the pins of SDA and SCK are shared with PC [1:0] and therefore, users should set PC[1:0] as Serial SRAM interface by writing to Port $27[1:0].

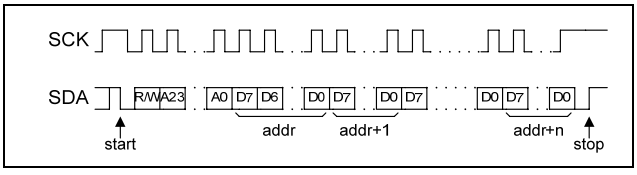




6.8.1. Read/Write timing



6.8.2. Continuous Read/Write timing



6.9. Bus Memory Interface

A built-in Bus memory interface is available on GPLB301A. Through the use of Bus memory interface, user can expand the memory space by using an external Bus memory (SRAM, mask ROM or Flash). The Bus memory interface includes 10 signal pins: MC1, MC0 and AD BUS[7:0] which shared pad with port B. Before using the Bus memory interface, users should set MEXT=1 ($03.7) and BANK register ($0), then access address $4000-BFFF to read or write data from external bus memory. Note that when using Bus memory interface, CPU clock setting can not be set as

Fosc/1, should be /2 or slower.

MC1	MC0	AD BUS [7:0]
L	L	Data for Write
L	H	Data for Read
H	L	AL (Address Low byte)
H	H	AH (Address High byte)

6.10. Voltage Regulator

The GPLB301A offers a voltage regulator, which supplies power source for external memory devices. The voltage regulator can output four voltage levels, 2.5V/2.6V/2.7V/3.0V via bonding option. The output voltage level should be properly selected based on the electrical characteristics of external memory devices involved.

6.11. Asynchronous Serial Interface (UART)

The GPLB301A supports a 1-channel UART for serial communications. The bit-rate is up to 115.2kbps. UART operation is controlled by UART command registers. Configurations such as Tx/Rx interrupt, parity check, parity even/odd and clock source can be configured in the command registers. Two interrupts are generated by Rx and Tx. The Rx or Tx interrupt activates when a byte is received or transmitted. Reading the status register informs whether the interrupt is generated by Rx or Tx. Frame, overrun and parity errors are detected as each byte is received and all error status can be read from status register. The UART supports clock auto calibration. If auto calibration is selected, standard baud rate from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to the baud rate control registers. The supported baud rates and their minimum R-oscillator clock frequency requirements are shown in the table below.

Baud Rate(bps)	Min. Frosc(Hz)
1200	24000
2400	48000
4800	96000
9600	192000
19200	384000
38400	768000
51200	1024000
57600	1152000
102400	2048000
115200	2304000

If the auto calibration is not selected, users can get desired baud rates by writing appropriate values to pre-scalar registers. Non-standard baud rates can be obtained by this method. In the non-calibration mode, users should understand that the R-oscillator frequency may alter due to manufacturing process variations, supply voltage, operating temperature and tolerance of external R components used.

6.12. Low Voltage Detection

The GPLB301A provides an 8-level (Software programmable) low voltage detector to detect low voltage events. Users can turn on the low detection to monitor VDD periodically to check if it is lower than the given value. In addition, if LV NMI is enabled, a NMI will be issued to notify CPU if power voltage drops below the given value. Also, the voltage detector will generate a system reset if power supply voltage drops below 2.2V.

6.13. Watchdog Timer (WDT)

An on chip watchdog timer is also available in the GPLB301A. The WDT is designed to recover the system from abnormal operation. In some cases, if WDT is not cleared within one second, the WDT will generate a system reset to restart system. If WDT is enabled, the WDT should be cleared periodically to avoid accidental reset. The WDT can be cleared through software programming. Note that the WDT only works when 32768Hz clock is activated.

6.14. Code Options

6.14.1. Body option

1). GPLB30
2). GPLB32
3). GPLB33A
4). GPLB33B
5). GPLB37

GPLB301A OTP code options include body option. Body option is the body selection to emulate. It prevents from using the nonexistent resource of that body. For example, GPLB32 is selected as body option of GPLB301. If RAM OTP DPRAM IO resources are used that don't exist in GPLB32, it won't work well.

6.14.2. 32768 oscillator

1). X'TAL
2). R-oscillator

6.14.3. Watchdog timer

3). Enable
4). Disable

6.14.4. LVR

5). Enable

6). Disable

6.14.5. Voltage regulator

7). Enable

8). Disable

6.14.6. Regulator output selection

9). 2.5V

10). 2.6V

11). 2.7V

12). 3V

6.14.7. PWM/DAC (only for GPLB32/GPLB37 selected)

13). Enable

14). Disable

6.14.8. Security

15). Enable

16). Disable

6.15. Code Options (I/O LCD shared pin) for GPLB30 Selected

6.15.1. PA[5:7]/SEG[69:67]

Each port/segment can be optioned as I/O or LCD output individually.

6.15.2. PB[0:7]/SEG[64:57]

Each port/segment can be optioned as I/O or LCD output individually.

6.15.3. PC[2:3]/SEG[66:65]

Each port/segment can be optioned as I/O or LCD output individually.

6.15.4. PC[4:7]/SEG[56:53]

Each port/segment can be optioned as I/O or LCD output individually.

6.15.5. PD[0:4]/ SEG[52:48]

Each port/segment can be optioned as I/O or LCD output individually.

6.16. Code Options (I/O LCD shared pin) for GPLB32/GPLB37 Selected

6.16.1. PA[6:7]/SEG[63:62]

Each port/segment can be optioned as I/O or LCD output individually.

6.16.2. PB[0:5]/SEG[69:64]/COM[21:16]

Each port/segment can be optioned as I/O or LCD output individually.

6.16.3. PC[0:1]/SEG[61:60]

Each port/segment can be optioned as I/O or LCD output individually.

6.16.4. PC[4:7]/SEG[73:70]/COM[25:22]

Each port/segment can be optioned as I/O or LCD output individually.

6.16.5. PD[0:5]/COM[31:26]

Each port/segment can be optioned as I/O or LCD output individually.

6.17. Code Options (I/O LCD shared pin) for GPLB33A Selected

6.17.1. PA7/SEG51

Each port/segment can be optioned as I/O or LCD output individually.

6.17.2. PB[0:7]/SEG[46:39]

Each port/segment can be optioned as I/O or LCD output individually.

6.17.3. PC[4:7] / SEG[50:47]

Each port/segment can be optioned as I/O or LCD output individually.

6.18. Code Options (I/O LCD shared pin) for GPLB33B Selected

6.18.1. PB[0:7] / SEG[41:34]

Each port/segment can be optioned as I/O or LCD output individually.

6.18.2. PC[2:7] / SEG[47:42]

Each port/segment can be optioned as I/O or LCD output individually.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V+	< 7.0V
Input Voltage Range	VIN	-0.5V to V+ + 0.5V
Operating Temperature	TA	0℃ to +60℃
Storage Temperature	TSTO	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

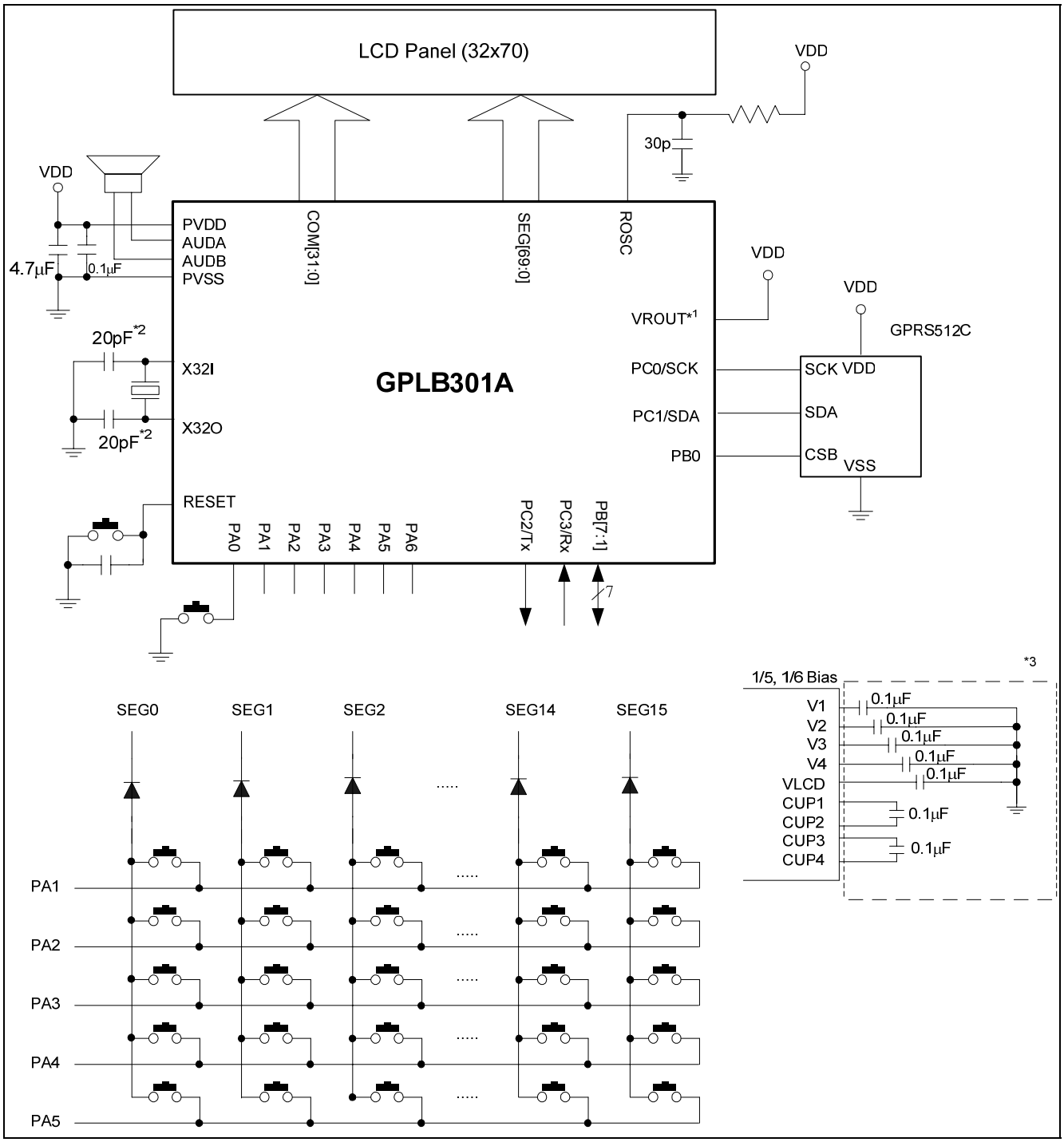
7.2. DC Characteristics

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
		3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	1400	-	μA	F_{CPU} = 1.0MHz @ 3.0V F_{ROSC} = 4.0MHz, no load
Halt Current	I_{HALT0}	-	20	-	μA	VDD = 3.0V, 32K X'tal ON, emulating GPLB30A/GPLB31A/GPLB32A/GPLB33A/GPLB37A, LCD ON, 1/5 bias, no LCD panel
	I_{HALT1}	-	40	-	μA	VDD = 3.0V, 32K X'tal ON, emulating GPLB33B/GPLB38B, LCD ON, 1/5 bias, no LCD panel
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, all off
Audio Output Current	I_{OH}	-	-20	-	mA	VDD = 3.0V, V_{OH} = 2.5V
		-	-40	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Audio Output Current	I_{OL}	-	20	-	mA	VDD = 3.0V, V_{OL} = 0.5V
		-	40	-	mA	VDD = 3.0V, V_{OL} = 1.0V
Input High Level	V_{IH}	2.2	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (I/O)	I_{OH}	-1.0	-	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (I/O)	I_{OL}	1.0	-	-	mA	VDD = 3.0V, V_{OL} = 0.8V
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	2.45	-	5.75	V	VDD = 3.0V, 1/5 bias, no load
		2.95	-	6.85	V	VDD = 3.0V, 1/6 bias, no load
Regulator Output Voltage	V_{REG}	-	2.5	-	V	Output voltage is selected by bonding option
		-	2.6	-		
		-	2.7	-		
		-	3.0	-		
Regulator Output Voltage Drop	V_{RDROP}	-	-	100	mV	I_L = 1.0mA, VDD = 3.6V
OSC Resistor	R_{OSC}	-	160	-	KΩ	F_{OSC} = 2.0MHz @ 3.0V
CPU Clock	F_{CPU}	-	-	6.0	MHz	F_{CPU} = F_{OSC}/1 @ 2.4V
		-	-	10.0	MHz	F_{CPU} = F_{OSC}/1 @ 3.6V

Note: V_{LCD} should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

8. APPLICATION CIRCUITS

8.1. 2240 Dots LCD Driver, Emulating GPLB30/GPLB32/GPLB33/GPLB37, 70Segments × 32 commons with External Serial SRAM, Regulator Disabled - (1)

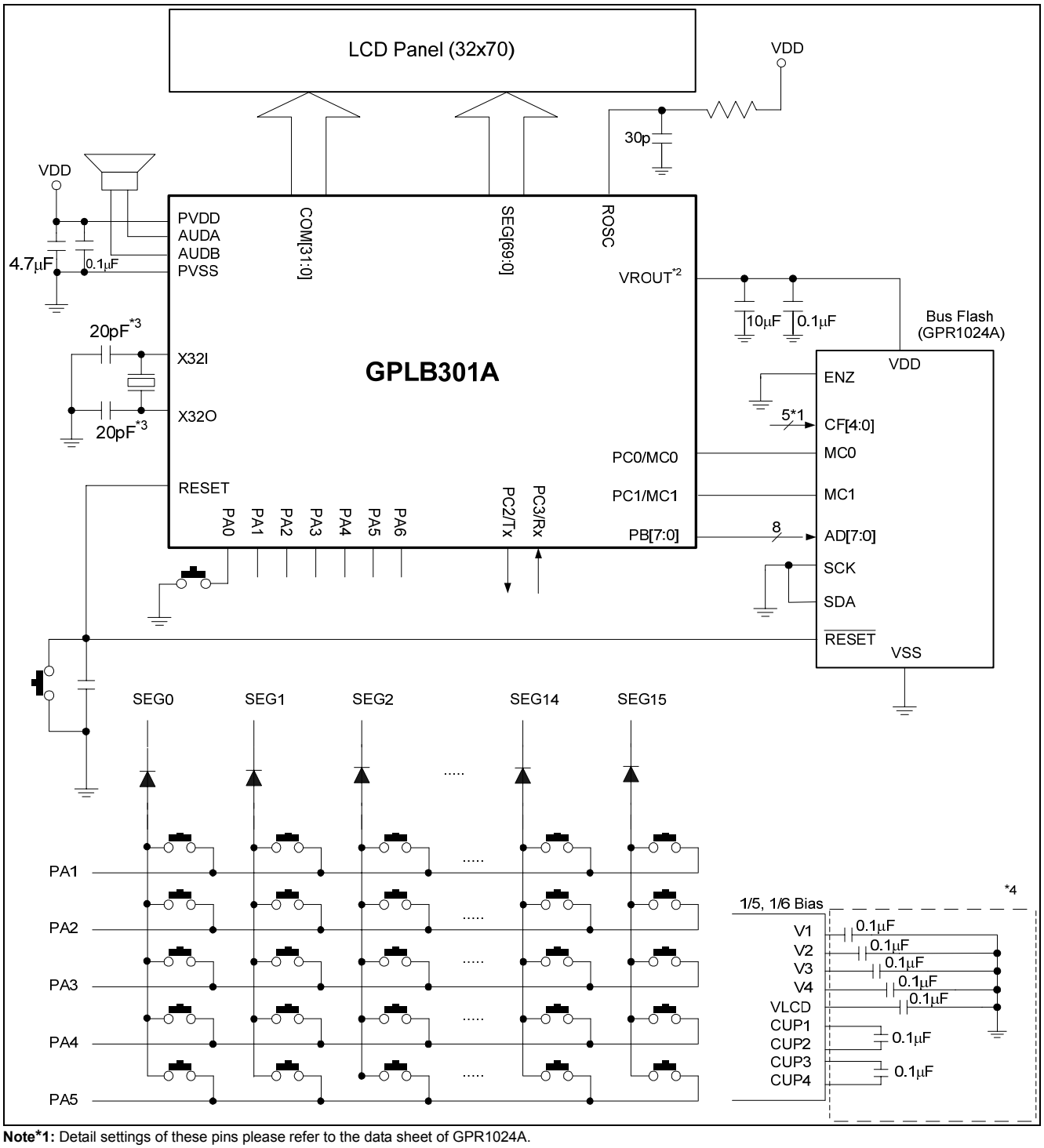


Note*1: Pin VROUT should be connected to VDD if internal Regulator is disabled.

Note*2: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*3: These capacitor values are for design guidance only. Different capacitor values may be required for different LCD panel connected.

8.2. 2240 Dots LCD Driver, emulating GPLB30/GPLB32/GPLB33/GPLB37, 70 Segments × 32 Commons with External Bus Flash, Regulator Enabled - (2)



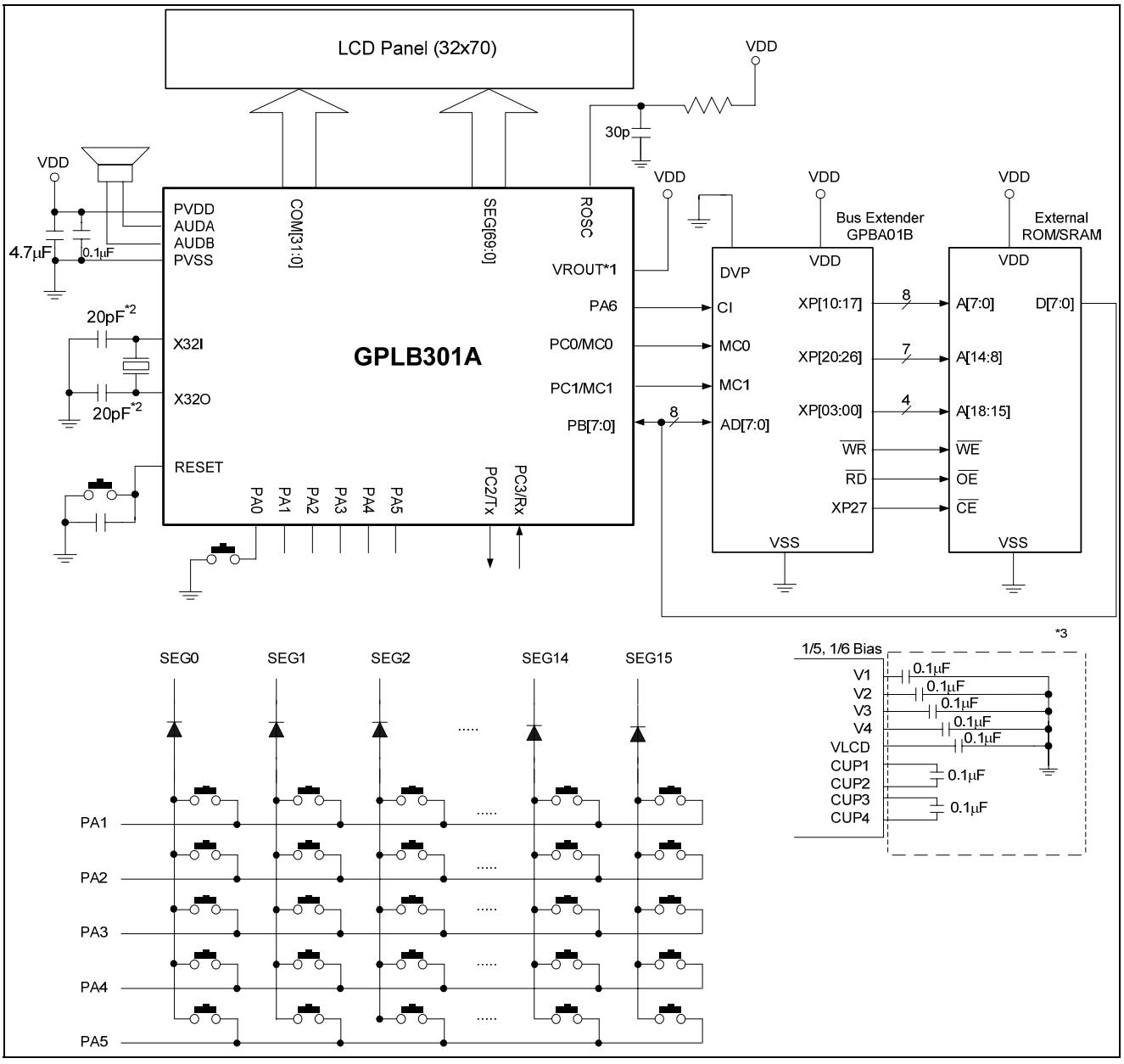
Note*1: Detail settings of these pins please refer to the data sheet of GPR1024A.

Note*2: Pin VROUT should be connected to VDD if internal Regulator is disabled.

Note*3: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*4: These capacitor values are for design guidance only. Different capacitor values may be required for different LCD panel connected.

8.3. 2240 Dots LCD Driver, emulating GPLB30/GPLB32/GPLB33/GPLB37, 70 Segments × 32 Commons with Bus Extender, Regulator Disabled - (3)

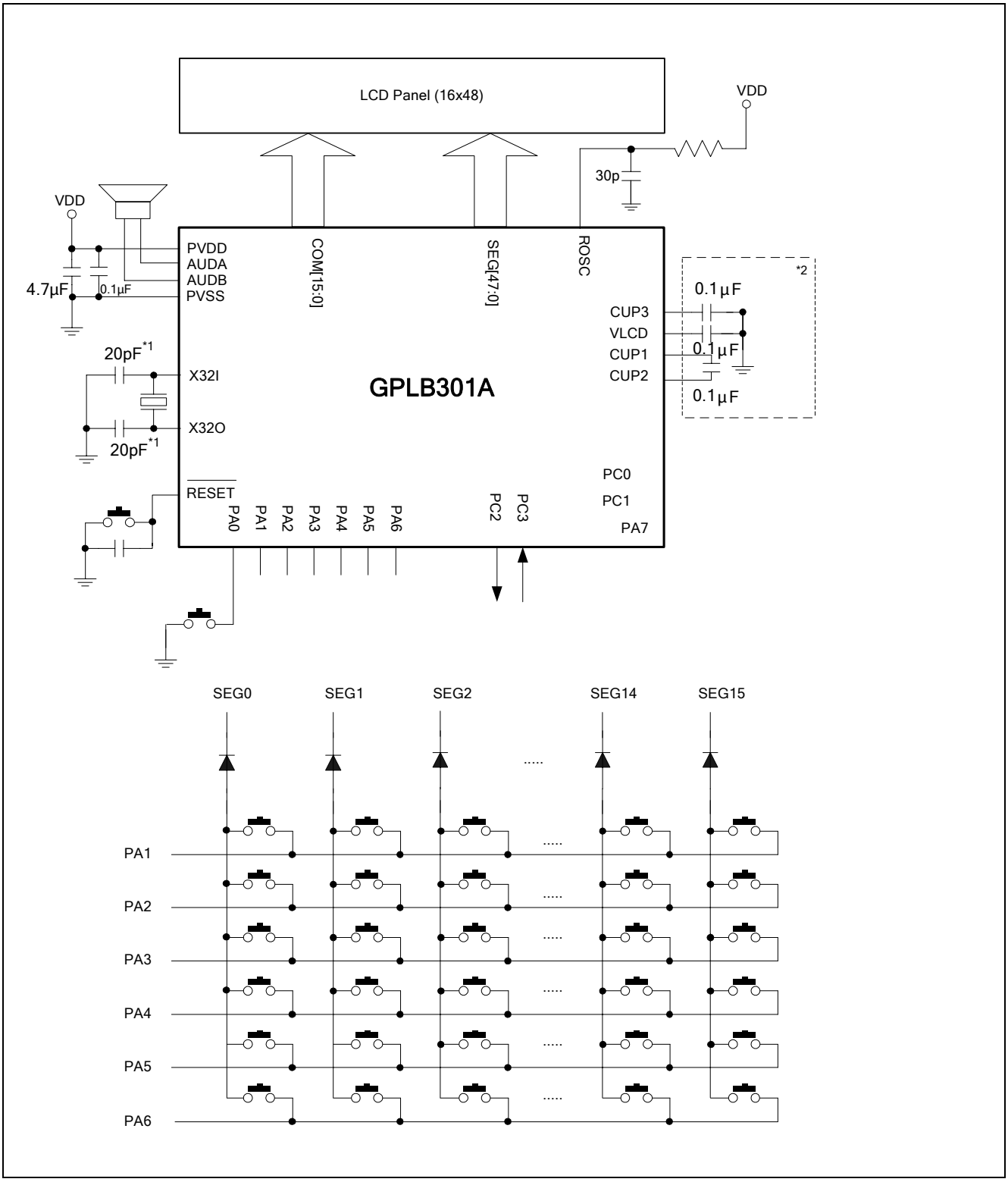


Note*1: *Pin VROUT should be connected to VDD if internal Regulator is disabled.

Note*2: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*3: These capacitor values are for design guidance only. Different capacitor values may be required for different LCD panel connected.

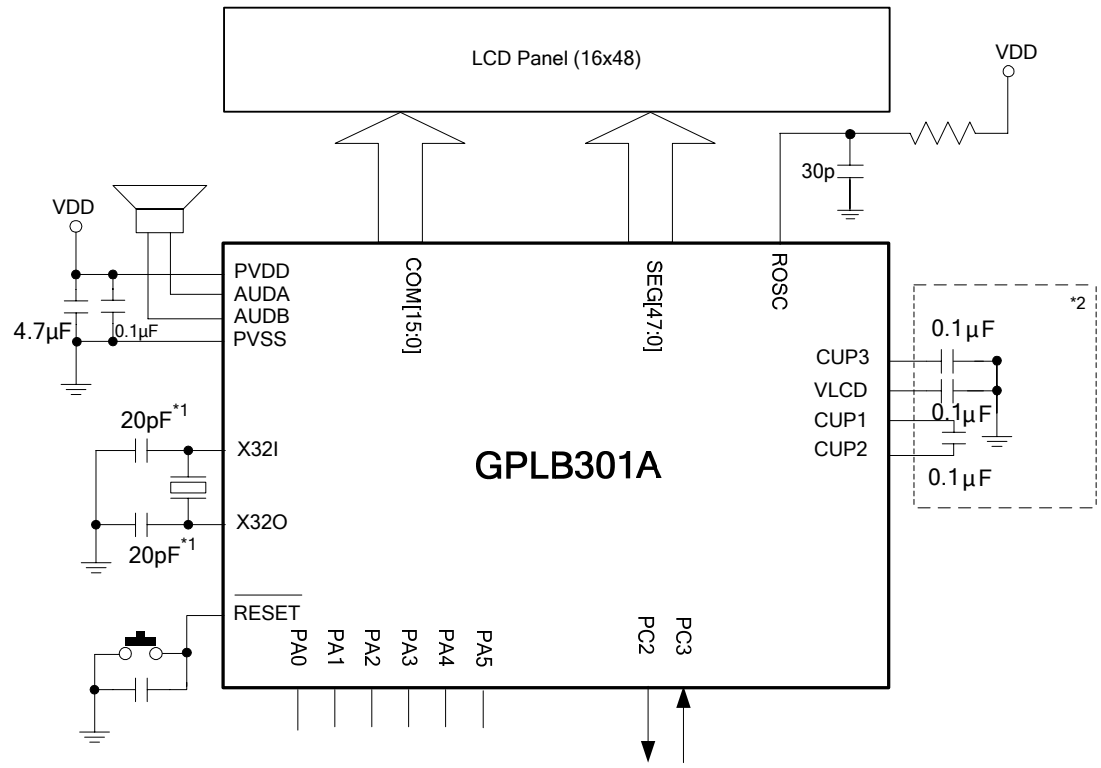
8.4. 768 Dots LCD Driver, emulating GPLB33B, 48 Segments × 16 Commons, 1/5 Bias, 96 Keys + On/Off Key - (4)

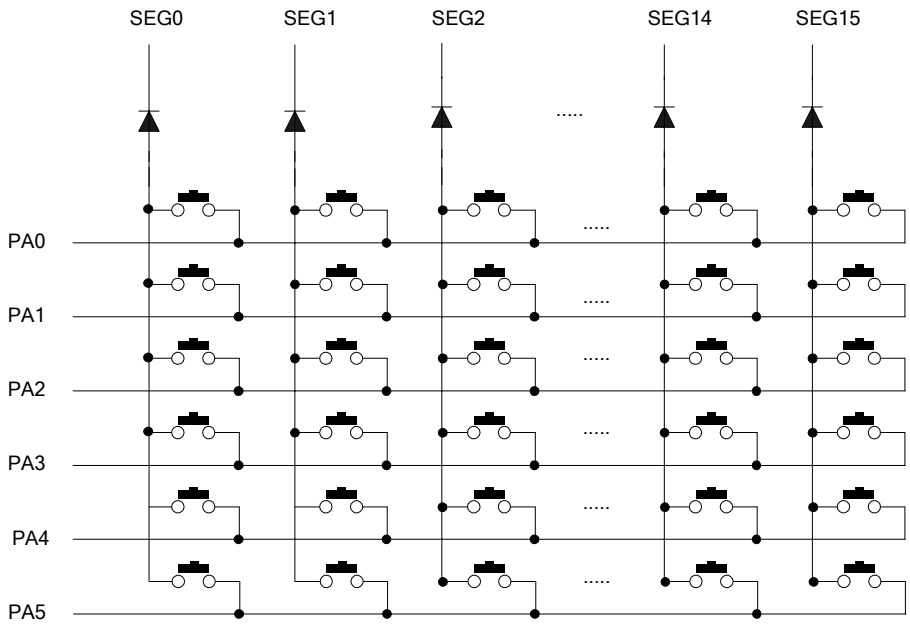


Note*1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*2: These capacitor values are for design guidance only. Different capacitor values may be required for different LCD panel connected.

8.5. 768 Dots LCD Driver, emulating GPLB33B, 48 Segments × 16 Commons, 1/5 Bias, 96 Keys - (5)

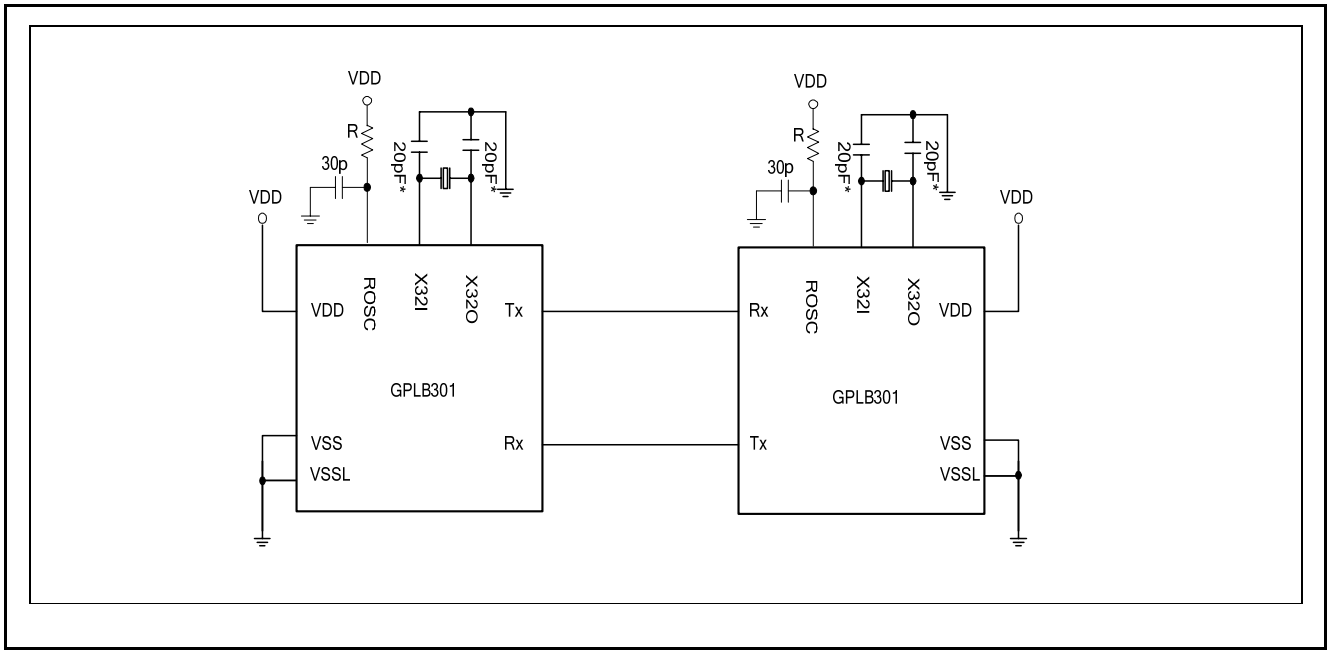




Note*1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*2: These capacitor values are for design guidance only. Different capacitor values may be required for different LCD panel connected.

8.6. Serial Communications between two GPLB301As - (6)



9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPLB301A-NnnV-C	Chip form
GPLB301A-NnnV-QL17x	Halogen Free Package

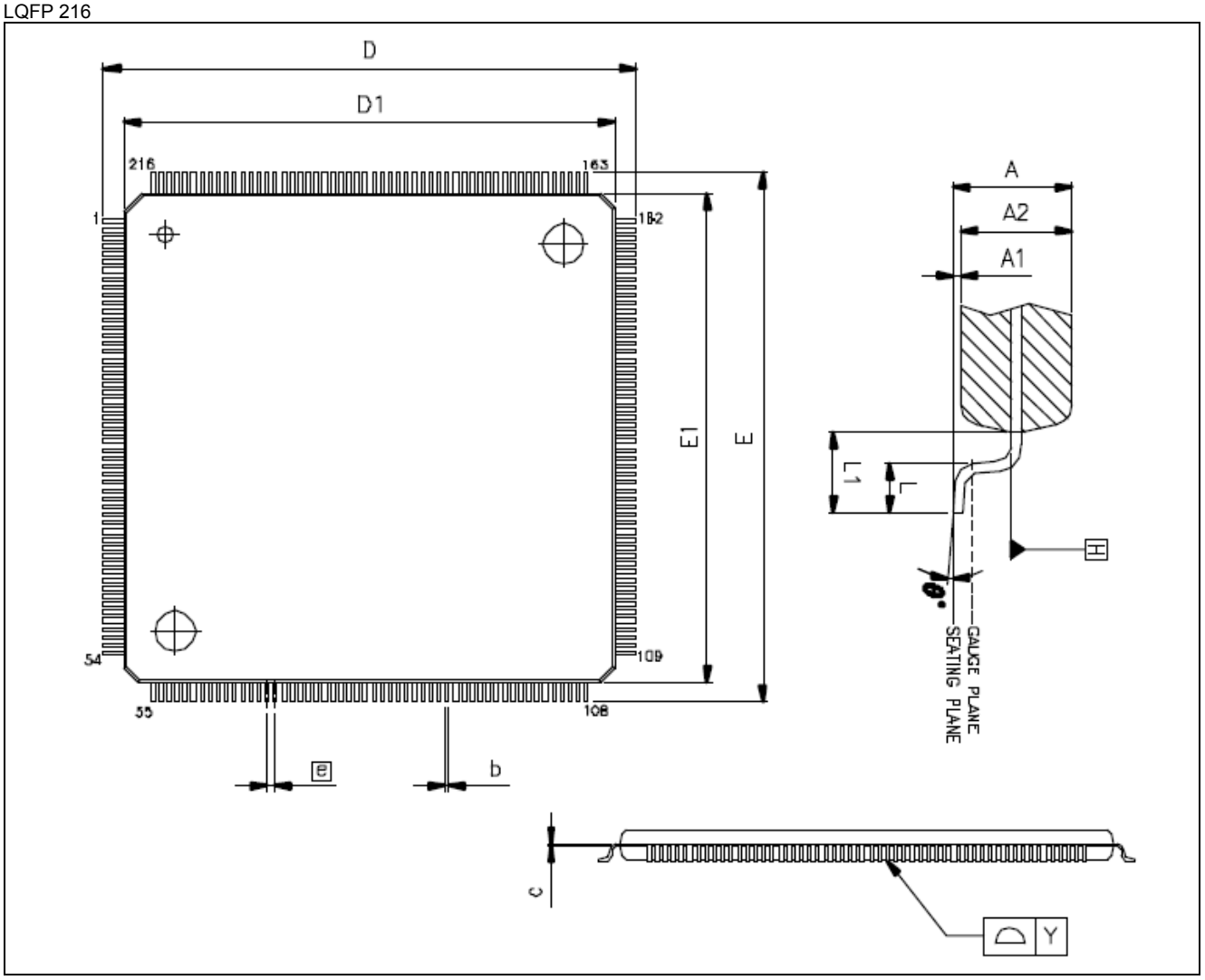
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 0 - 9, serial number).

9.2. Package Information

LQFP 216



Symbol	Min.	Nom.	Max.	Unit
A	-	-	1.60	Millimeter
A1	0.05	-	0.15	Millimeter
A2	1.35	1.40	1.45	Millimeter
b	0.13	0.18	0.23	Millimeter
c	0.09	-	0.20	Millimeter
D	26.00 BSC			Millimeter

Symbol	Min.	Nom.	Max.	Unit
D1		24.00 BSC		Millimeter
E		26.00 BSC		Millimeter
E1		24.00 BSC		Millimeter
e		0.40 BSC		Millimeter
L	0.45	0.60	0.75	Millimeter
L1		1.00 REF		Millimeter
Y		0.08		Millimeter
θ°	0°	3.50°	7.00°	Millimeter

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11. REVISION HISTORY

Date	Revision #	Description	Page
Dec. 28, 2009	1.5	Modify 2.FEATURES.	4
Aug. 31, 2009	1.4	Modify 6.5 LCD Controller/Driver.	13
Jul. 23, 2009	1.3	Modify section 7.2 DC Characteristics.	16
Nov. 03, 2008	1.2	1. Modify the FEATURES in section 2. 2. Add capacitance value for reference in Application circuit.	3 17 - 21
Sep. 11, 2008	1.1	Remove emulating LB31A function.	4, 5, 10
APR. 24, 2008	1.0	1. Modify the SIGNAL DESCRIPTIONS in section 5. 2. Modify the DC Characteristics in section 7.2.	7 - 8 17
JAN. 04, 2008	0.4	1. Modify the “DC characteristics” in section 7.2. 2. Modify the Application Circuits in section 8.1 and 8.2	17 18, 19
OCT. 02, 2007	0.3	Modify the “SIGNAL DESCRIPTIONS” in section 5.	7, 8
JUL. 11, 2007	0.2	1. Add the “PIN Map” in section 5.3. 2. Add the “Package Information” in section 9.3.	9 25
JUN. 27, 2007	0.1	Preliminary Data Sheet.	25