DATA SHEET

GPLB30B

640 Dots LCD Controller with 48KB ROM

Apr. 16, 2009

Version 1.1

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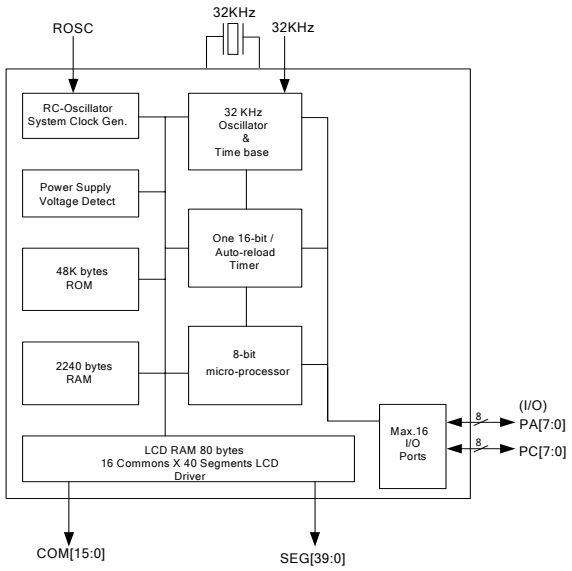
LCD CONTROLLER

1. GENERAL DESCRIPTION

The GPLB30B, an 8-bit CMOS microprocessor, contains 2240 bytes working RAM, 48K bytes ROM, 16 I/Os, interrupt/wakeup controller, and automatic display controller/driver for LCD. Furthermore, a SLEEP (power-down) function is also built in to extend power life. The GPLB30B is designed with state-of-the-art technology to fulfill LCD application needs, especially for hand-held products.

2. BLOCK DIAGRAM



Note1: PC[0:7] share pins with SEG[39:32] (mask option).

3. FEATURES

■ Built in 8-bit processor
- — 2240 bytes SRAM
- — 48K bytes ROM
- — Max. operating speed: 5.0MHz @ 2.2V - 5.5V
- — CPU clock is software programmable, can be /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
- — Provides 4 wake-up sources
- — Provides 4 interrupt sources

■ Programmable LCD driver
- — Up to 40 segments, up to 16 commons, maximum 640 Dots
- — 1/3, 1/4, 1/5 bias; 1/4, 1/8, 1/16 duty capability
- — 80 bytes dedicated LCD RAM
- — Built-in voltage regulator to generate VLCD for LCD driver
- — 27-level contrast control (2.98V - 5.75V)

■ Power saving SLEEP mode

■ Low voltage reset
- — 2.1V Low voltage reset

■ Peripherals
- — Max. 16 I/O pins (PA[7:0], PC[7:0])
  . Dedicated I/Os: PA[0:7],
  . Shared pin I/Os:
  PC[0:7]/SEG[39:32]
- — Built-in System RC-oscillator
  Built-in RC 4MHz or Built-in C External R decided by mask option
- — Built-in 32.768KHz oscillator for real time clock function
  XTAL or Built-in RC oscillator or Built-in C External 3MΩ R oscillator decided by mask option
- — One 16-bit reloadable timer/counters
- — Watchdog Timer for reliable operation

■ Low power consumption:
- — 650μA typical @ 3.0V, F_{CPU} = 1.0MHz, F_{OSC} = 4.0MHz
- — 25μA typical halt current @ 3.0V
- — <1μA typical standby current @ 3.0V

■ Wide operating voltage range:
- — 2.2V - 5.5V

4. APPICATION FIELD

- Scientific calculator
- Data bank

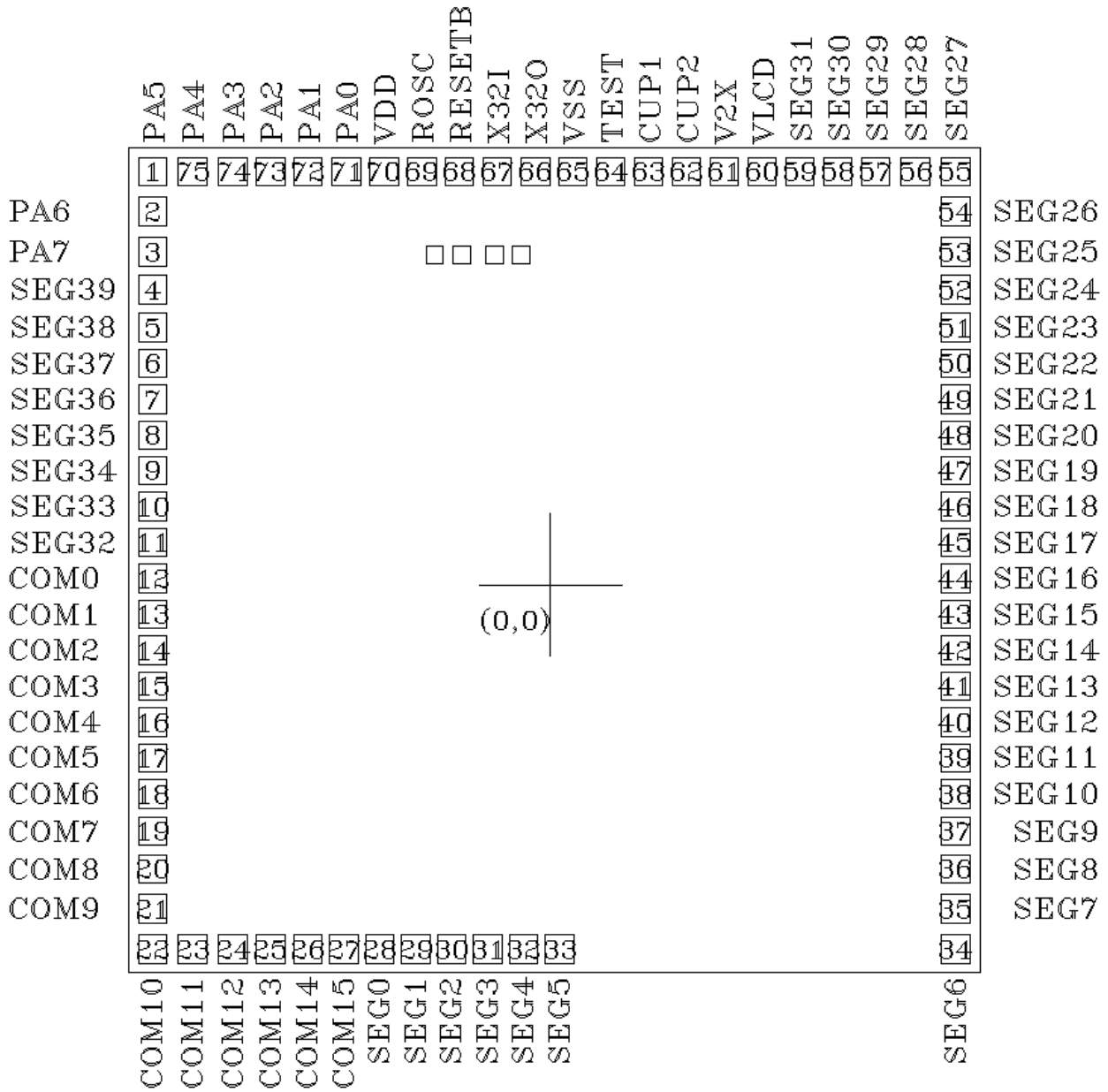
5. SIGNAL DESCRIPTIONS

Total: 75 pins

Mnemonic	PIN No.	Type	Description
SEG31 - 0	59-28,	O	LCD driver segment output.
SEG39 - 32 / PC0 - 7	4-11	I/O	SEG39 - 32 optioned to PC0 - 7.
COM15 - 0	27-12	O	LCD driver common output.
PA7 - 0	3-1, 75-71	I/O	Port A is a bi-directional I/O port, which can be software programmed as wake up I/O.
ROSC	69	I	R-oscillator input, connect to VDD through a resistor.
RESETB	68	I	System reset input, low active.
X32I	67	I	32.768KHz crystal input or connect to VDD through a resistor (option).
X32O	66	O	32.768KHz crystal output.
TEST	64	I	Test input.
CUP1, CUP2	63, 62	P	LCD voltage generator. Charge pump capacitor inter-connection pins
V2X	61	P	LCD voltage generator for VDD*2.
VLCD	60	P	LCD voltage generator.
VDD	70	P	Power supply voltage input.
VSS	65	P	Ground reference.

Legend: I = Input, O = Output, P = Power

5.1. PAD Assignment



6. FUNCTIONAL DESCRIPTIONS

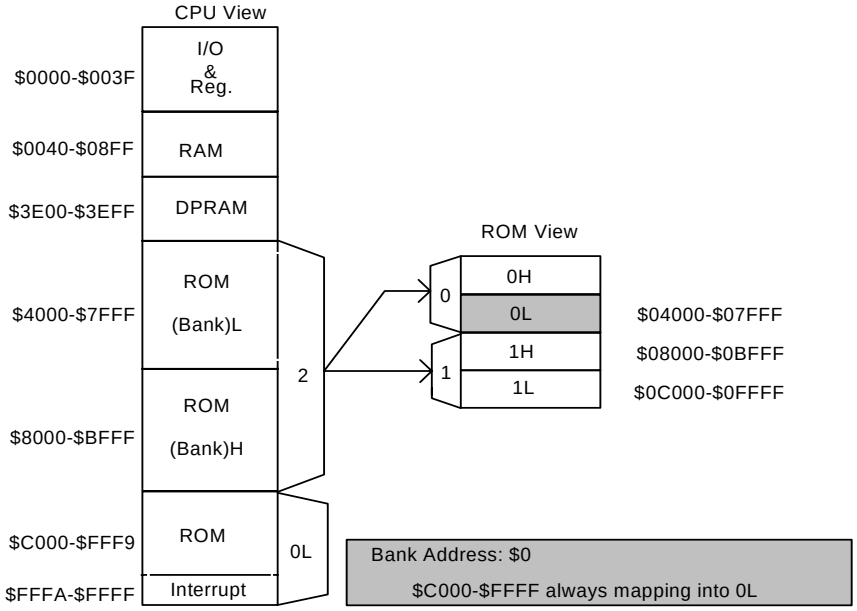
6.1. Memories

The GPLB30B contains 48K-byte ROM and 2240-byte SRAM.

6.2. Map of Memory and I/Os

***INT SOURCE:**

- EXT INT
- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0



1. User's program should start from $C000. $8000-$87FF in bank0 is the test program area.
2. User's program interrupt vector: $FFFA ~ $FFFF.
3. Test program interrupt vector: $FFF2 ~ $FFF7.

6.3. Operating States

There are three operation modes in GPLB30B: standby, halt and operating. The following table shows the differences between these modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

6.3.1. Operating mode

In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated. Generally speaking, this mode consumes the highest power.

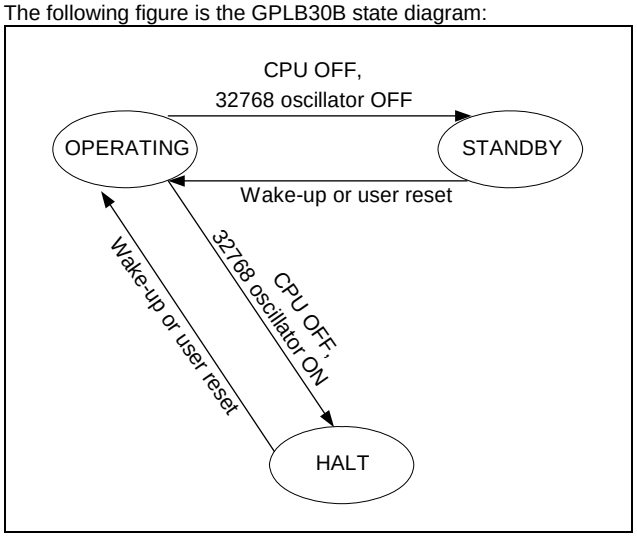
6.3.2. Standby mode

Turn off CPU and 32768Hz oscillator to activate standby mode. The standby mode is a mode that the device is placed in its lowest current consumption state. In standby mode, all functions are turned off; in addition, RAM and I/Os will remain in their previous states.

6.3.3. Halt mode

Entering halt mode turns off CPU but still keeps 32768Hz oscillator running. In halt mode, CPU clock halts and waits for an event (key press, timer overflow) to wake up. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode.

The following figure is the GPLB30B state diagram:



GPLB30B State Diagram

6.4. LCD Controller/Driver

The GPLB30B contains a 640-dot LCD controller/driver. Programmer is able to define the LCD configuration by setting the LCD Control Register. Once the LCD configuration is completed, the desired pattern can be displayed by filling the LCD buffer with proper data. The LCD driver can also operate during sleep by keeping 32768Hz oscillator running. The LCD driver in GPLB30B supports 1/16 duty and 1/5 bias.

6.5. LCD Voltage Generator

The GPLB30B offers a voltage regulator and a charge-pumping circuit. The voltage regulator supplies the charge-pumping circuit a reference voltage to generate VLCD. Users can get the desired VLCD by changing the output reference voltage (writing to register) of the voltage regulator. Enabling the voltage regulator and charge-pumping circuit gets a stable VLCD that will not be affected by VDD. The VLCD is adjustable from 2.98V to 5.75V with 27 levels.

6.6. Low Voltage Reset

The GPLB30B provides a low voltage reset function. The voltage detector will generate a system reset if power supply voltage drops below 2.1V.

6.7. Watchdog Timer (WDT)

An on-chip watchdog timer is also available in the GPLB30B. The WDT is designed to recover the system from abnormal operation. In some cases, if WDT is not cleared for one second, the WDT will generate a system reset to restart system. If WDT is enabled, the WDT should be cleared through software programming every 0.5 seconds to avoid accidental reset. Note that the WDT only works when 32768Hz clock is activated.

6.8. Mask Options

6.8.1. 32768 oscillator

— X'TAL32K
— Rosc32K

6.8.2. Watchdog timer

— Enable
— Disable

6.8.3. PC[0:7]/SEG[39:32]

Each port/segment can be optioned as I/O or LCD segment individually.

6.8.4. Rosc32k select

1). Built in RC
2). Built in C External R

6.8.5. System R_{OSC} select

1). Built in RC
2). Built in C External R

6.8.6. Low voltage reset

1). Disable
2). Enable

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

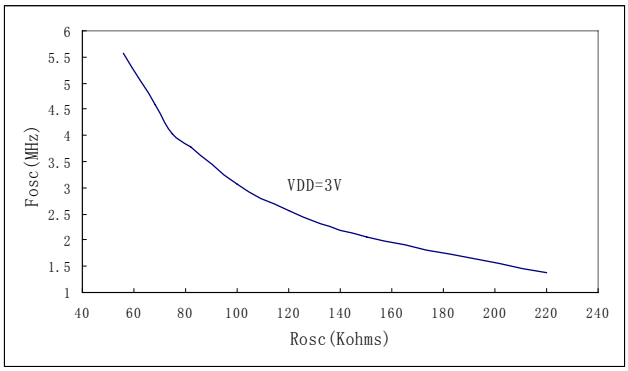
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

7.2. DC Characteristics

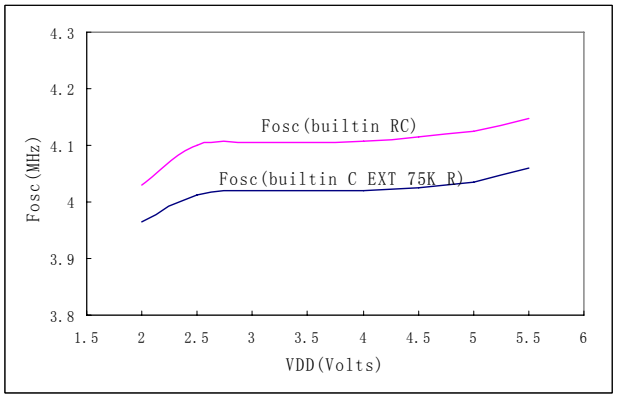
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.2	-	5.5	V	
Operating Current	I_{OP}	-	650	-	μA	VDD = 3.0V, F_{CPU} = 1.0MHz, F_{OSC} = 4.0MHz, no load
Halt Current	I_{HALT1}	-	25	-	μA	VDD = 3.0V, 32K X'tal ON, Maximum VLCD, Strobe on, no LCD panel
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, all off
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (I/O)	I_{OH}	-1.0	-	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (I/O)	I_{OL}	1.0	-	-	mA	VDD = 3.0V, V_{OL} = 0.8V
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	2.98	-	5.75	V	VDD = 3.0V, 1/5 bias, no load
OSC Resistor	R_{OSC}	-	75K	-	Ω	F_{OSC} = 4.0MHz @ 3.0V
System oscillator Frequency	F_{OSC}	-10%	4.1	+10%	MHz	Built-in C external 75k Resistor oscillator or Built-in RC 4MHz oscillator @ 3.0V
32K oscillator Frequency	F32k	-	32.768	-	KHz	XTAL32K
		-10%	34	+10%		Built-in C external 3M Resistor oscillator
		-30%	36	+30%		Built-in RC oscillator@ 3.0V

Note1: V_{LCD} should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.
Note2: If not mentioned specially, the test condition is 2.2V~5.5V@25℃

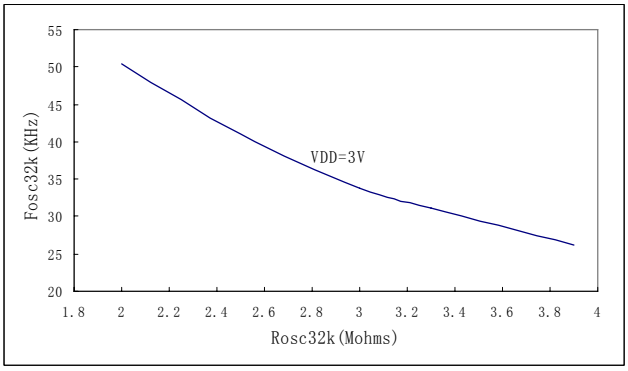
7.3. The Relationships between the F_{OSC} and the R_{OSC}



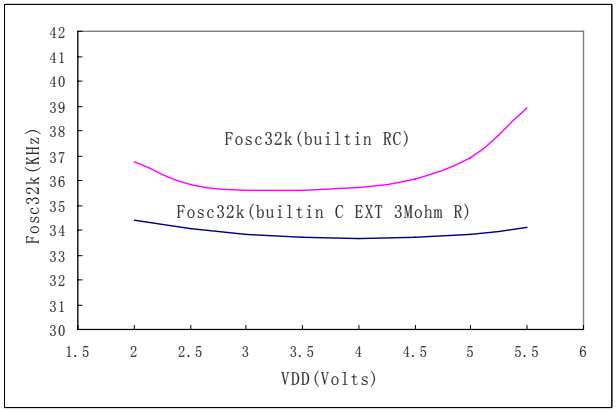
7.4. The Relationships between the F_{OSC} and the VDD



7.5. The Relationships between the F_{OSC32K} and the R_{OSC32K}

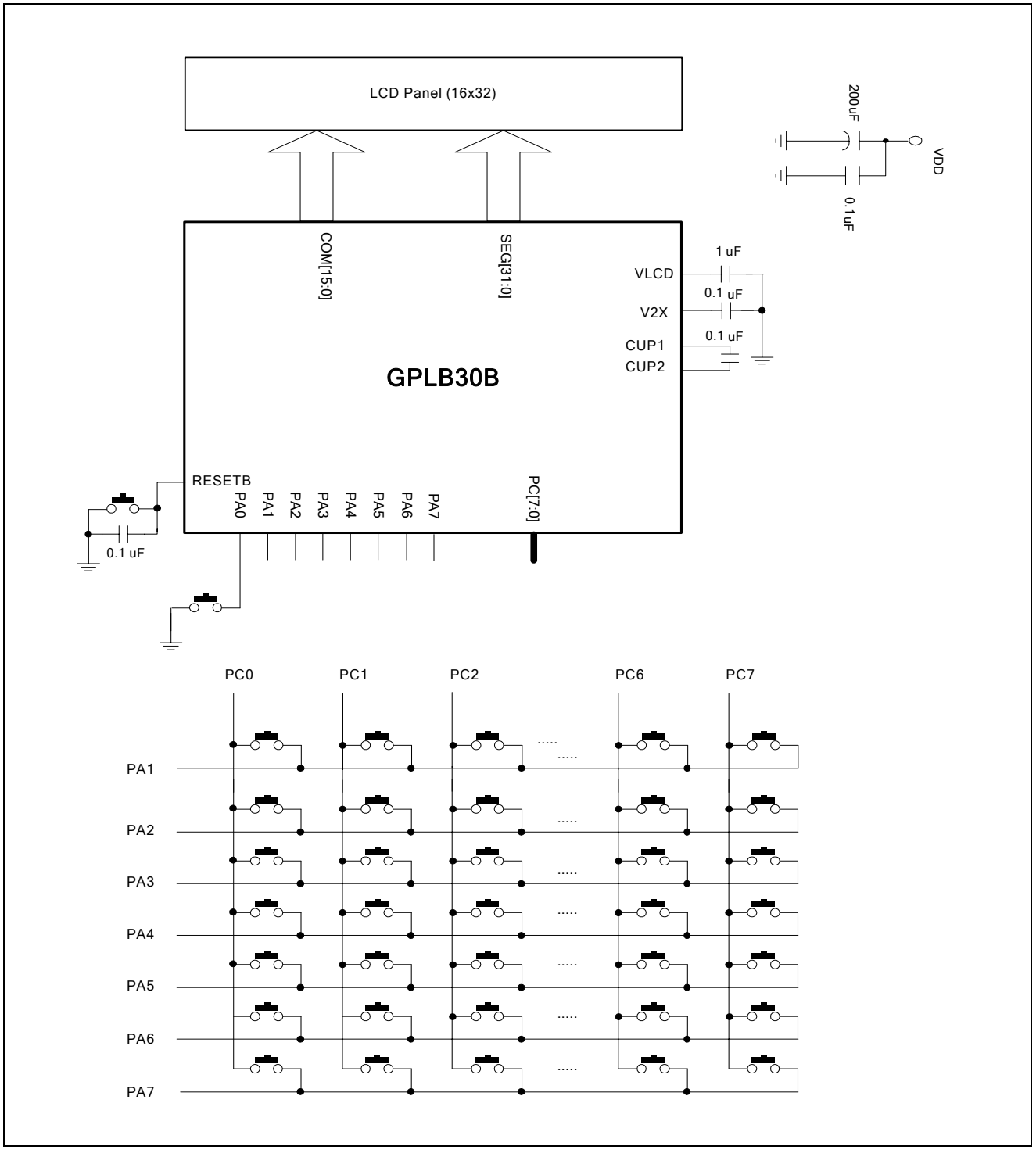


7.6. The Relationships between the F_{OSC32K} and the VDD



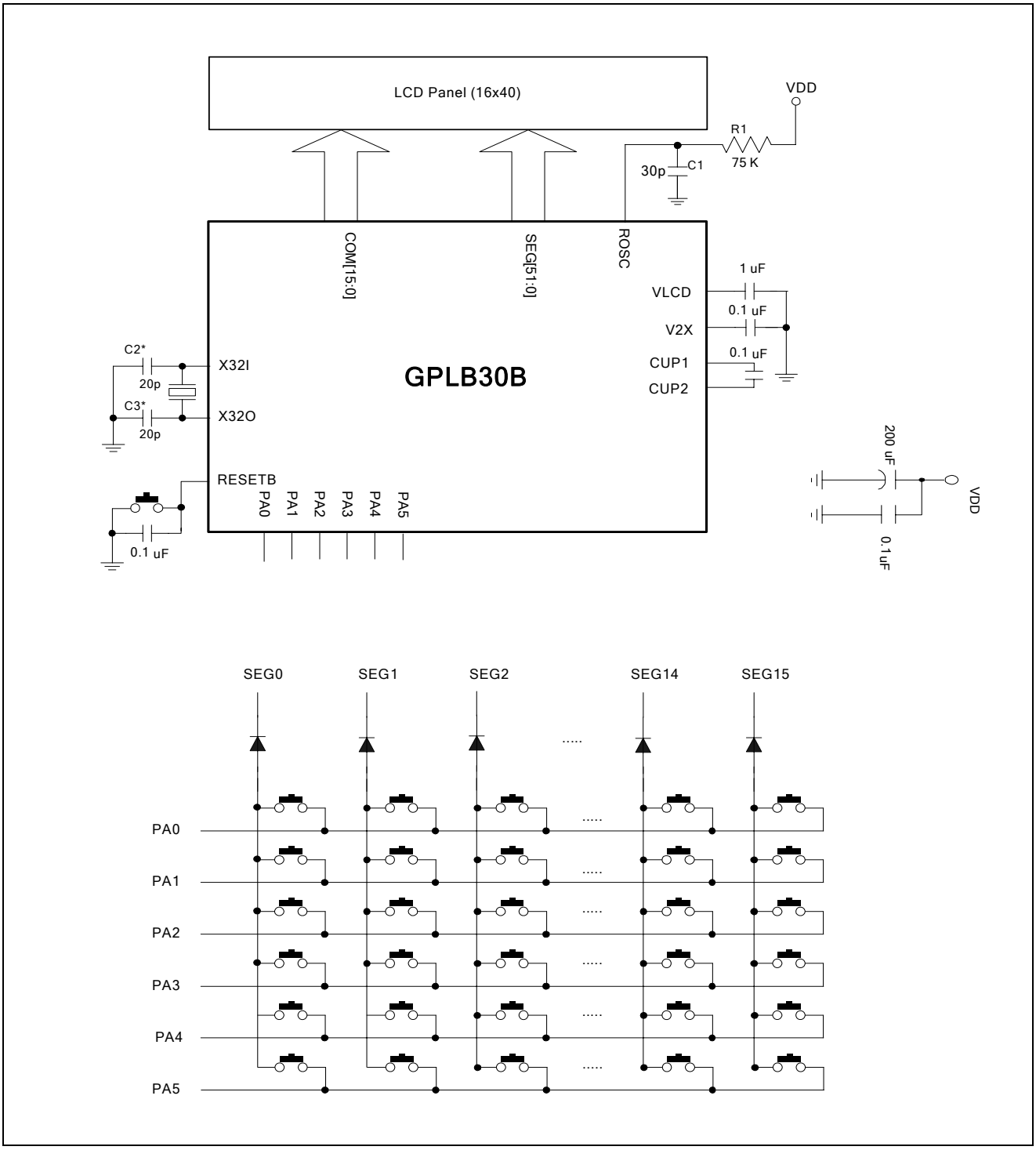
8. APPLICATION CIRCUITS

8.1. 512 Dots LCD Driver, 32 Segments × 16 Commons, 1/5 Bias, 56 Keys + On/Off Key, Internal ROSC - (1)



* Using segments for LCD display only; system ROSC select built in RC ROSC4M; 32K oscillator select built in RC ROSC32K.

8.2. 640 Dots LCD Driver, 40 Segments × 16 Commons, 1/5 Bias, 96 Keys, XTAL + External ROSC - (2)



* Using segments for both LCD display and key scan; system ROSC select built in C external 75K ROSC; 32K oscillator select XTAL.

Note1: C2/C3 values in above application circuit are for design guidance only. Different capacitor values may be required for different crystal used. Usually, the values of C2/C3 are in the range 12~20pF.

Note2: To avoid the noise interference on PCB around R-Oscillator and crystal circuit, following rules are recommended:

1). R1 and C1 should be placed as close as possible to ROSC pin.

2). C2, C3 and crystal should be placed as close as possible to X32I and X32O. A shielding by ground is suggested.

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPLB30B-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
APR. 16, 2009	1.1	1. Add relationship waveform for frequency at section 7.3, 7.4, 7.5, 7.6	9
		2. Modified Application circuit in section 8.1 & 8.2	10,11
Mar. 6, 2009	1.0	1.Modified ROM size from 50K to 48K	3,6
		2.Modified max operating speed	3
		3.Modified low power consumption;	3
		4.Modified DC characteristics	8
OCT. 23, 2008	0.1	Preliminary data sheet	10