DATA SHEET

GPLB32A3

2000 Dots LCD Controller with 512KB ROM

Mar. 04, 2009

Version 1.1

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2000 Dots LCD Controller with 512KB ROM

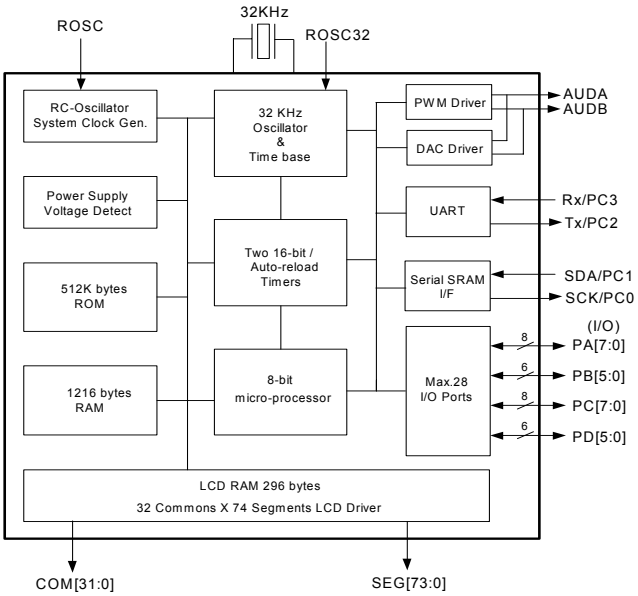
1. GENERAL DESCRIPTION

The GPLB32A3, an 8-bit CMOS microprocessor, features 1216 bytes working RAM, 512K bytes ROM, 8 I/Os, interrupt/wakeup controller, UART for serial communication and Serial SRAM interface for memory expansion, and automatic display controller/driver for LCD. It also carries one PWM/DAC driver with two audio channels to produce attractive sound effects easily. Its large ROM area can be used to store both program and audio data. The built-in UART speeds up data transmission between two devices. Plus, a SLEEP (power-down) function is also built in to extend power life. The GPLB32A3 is designed with GENERALPLUS state-of-the-art technology to fulfill LCD application needs, especially for hand-held products.

2. FEATURES

- Built in 8-bit processor
  - **1216 bytes SRAM**
  - **512K bytes ROM**
  - Max. Operating Speed: 4.0MHz @ 2.4V - 3.6V
    5.0MHz @ 3.6V - 5.5V
  - Programmable CPU Clock: /1 /2 /4 /8 /16 /32 /64 ROSC freq.
  - 6 wake-up sources
  - 7 interrupt sources
- Universal Asynchronous Receiver and Transmitter (UART)
- Serial SRAM Interface
- Key Scan Function
  - SEG[15:0] can be used to send key scan output
- Programmable LCD Driver
  - **74 segments, 16 commons, maximum 1184 dots or 64 segments, 32 commons, maximum 2048 dots**
  - 1/5, 1/6 bias; 1/16, 1/32 duty driving capability
  - **296 bytes dedicated LCD RAM**
  - Built-in voltage regulator to generate VLCD for LCD driver
  - 32-level contrast control (2.45V - 5.75V, in 1/5 bias)
    32-level contrast control (2.95V - 6.85V, in 1/6 bias)
- Power Saving SLEEP Mode
- **Low Voltage Detector**
  - **8-level 2.9V - 2.2V/4.35V - 3.3V detection**
  - **2.2V Low Voltage Reset**
- Low Power Consumption:
  - 600μA typical @ 3.0V, F_{CPU} = 1.0MHz, F_{OSC} = 4.0MHz
  - 25μA typical halt current @ 3.0V
  - <1μA typical standby current @ 3.0V
- Peripherals
  - **Max. 28 I/O pins (PA[7:0], PB[5:0], PC[7:0], PD[5:0])**
    . Dedicated I/Os: PA[0:5]
    . Shared pin I/Os:
    PA[6:7] / SEG[63:62]
    PC[0:1] / SSRAM SCK, SDA/SEG[61:60]
    PC[3:2] / UART Rx/Tx
    PC[4:7] / SEG[73:70] / COM[25:22]
    PB[0:5] / SEG[69:64] / COM[21:16]
    PD[0:5] / COM[31:26]
  - 32.768KHz oscillator circuit for RTC
  - RC-oscillator (only one resistor required)
  - Two 16-bit reloadable timer/counters
  - **8-bit DAC resolution, 2-channel PWM/DAC audio outputs**
  - Watchdog Timer for Reliable Operation
- Wide Operating Voltage Range:
  - 2.4V - 3.6V
  - 3.6V - 5.5V

3. BLOCK DIAGRAM



Note1: PA [6:7] share pins with SEG [63:62] (mask option).
Note2: PC [0:1] share pins with Serial SRAM interface SCK/SDA.
Also share pins with SEG [61:60] (mask option).
Note3: PC [2:3] share pins with UART Tx /Rx.
Note4: PC [4:7] share pins with SEG [73:70].
Also share pins with COM [25:22] (mask option).
Note5: PB [0:5] share pins with SEG [69:64].
Also share pins with COM [21:16] (mask option).
Note6: PD [0:5] share pins with COM [31:26] (mask option).

4. APPLICATION FIELD

- Educational Learning Aids (ELA)
- Handheld Game
- Scientific Calculator
- Talking Calculator, Talking Clock
- Talking Instrument Controller
- General Speech Synthesizer
- Data Bank

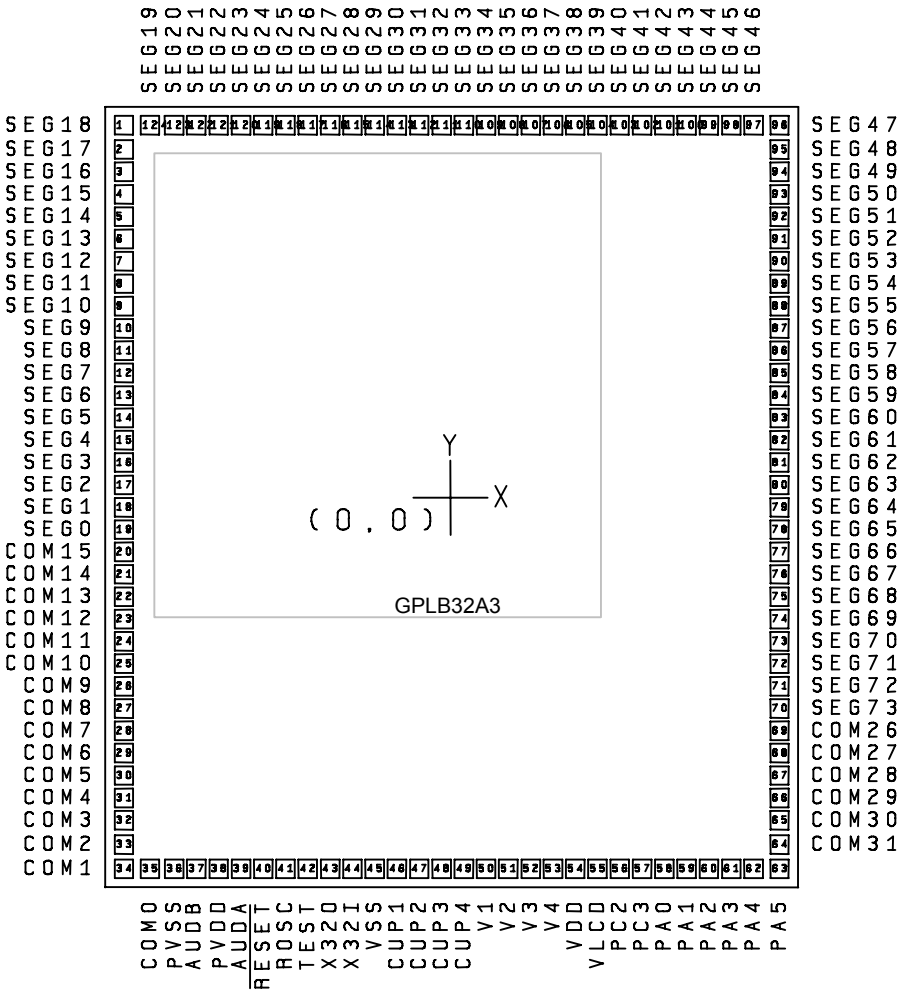
5. SIGNAL DESCRIPTIONS

Total: 124 pins

Mnemonic	PIN No.	Type	Description
SEG59 - 19	84-124	O	LCD driver segment output. SEG15 - 0 share pin with key scan port.
SEG18 - 0	1 - 19	O	
SEG63 - 62 / PA6 - 7	80 - 81	I/O	SEG63 - 62 optioned to PA6 - 7.
SEG61- 60 / PC0 - 1/SCK, SDA	82 - 83	I/O	SEG61 - 60 optioned to PC0 - 1 / SCK, SDA.
SEG73 - 70 / COM25 - 22 / PC4 – 7	70 - 73	I/O	SEG73 - 70 optioned to COM25 - 22 or PC4 – 7(PortC 4, 5 shared with Ext-I, Ext-ck).
SEG69 - 64 / COM21-16 / PB0-5	74 - 79	I/O	SEG69 - 64 optioned to COM21 - 16 or PB0 - 5.
COM15 - 0	20 - 35	O	LCD driver common output.
COM31 - 26 / PD0 - 5	64 - 69	I/O	
PA5 - 0	63 - 58	I/O	Port A is a bi-directional I/O port, which can be software programmed as wake up I/O.
PC3 / Rx	57	I/O	UART input. Share pin with PC3.
PC2 / Tx	56	I/O	UART output. Share pin with PC2.
ROSC	41	I	R-oscillator input, connect to VDD through a resistor.
$\overline{\text{RESET}}$	40	I	System reset input, low active.
AUDA, AUDB	39, 37	O	PWM/DAC audio output.
X32I	44	I	32.768KHz crystal input or connect to VDD through a resistor (option).
X32O	43	O	32.768KHz crystal output.
TEST	42	I	Test input.
CUP4 - 1	49 - 46	P	LCD voltage generation. Charge pump capacitor inter-connection pins.
VLCD	55	P	LCD voltage generation.
V4 - 1	53 - 50	P	LCD voltage generation.
VDD	54	P	Power supply voltage input.
VSS	45	P	Ground reference.
PVDD	38	P	PWM driver power.
PVSS	36	P	PWM driver ground reference.

Legend: I = Input, O = Output, P = Power

5.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.
Note2: The shaped area shows the internal ROM block in order to identify the location of the first pin.

6. FUNCATIONAL DESCRIPTIONS

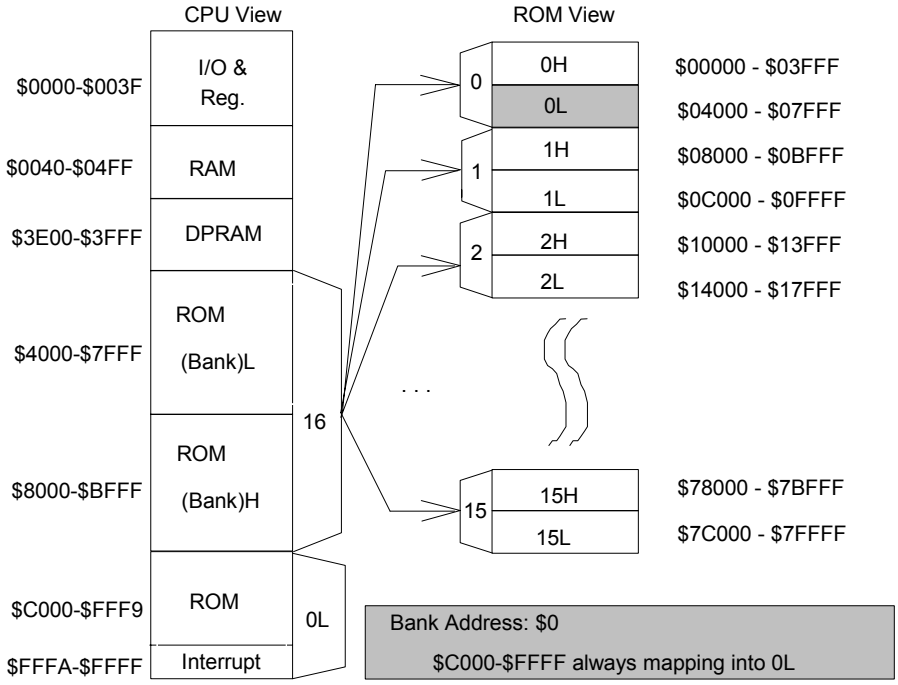
6.1. Memories

The GPLB32A3 contains 512K-byte ROM and 1216-byte SRAM. The Serial SRAM interface is provided in GPLB32A3; thus, SRAM space can be extended by Generalplus Serial SRAM, GPRS256B or GPRS512C.

6.2. Map of Memory and I/Os

*NMI SOURCE:
- LV DETECT
- TIMER1

*INT SOURCE:
- EXT INT
- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



Note1: User program should start from $C800. $C000-$C7FF is the test program area.
Note2: User program interrupt vector: $FFFA ~ $FFFF.
Note3: Test program interrupt vector: $FFF2 ~ $FFF7.

6.3. Operation Modes

The GPLB32A3 has three operation modes: standby, halt and operating. The following table shows the differences between these modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

6.4. Operating Mode

In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated. Generally speaking, this mode consumes the highest power.

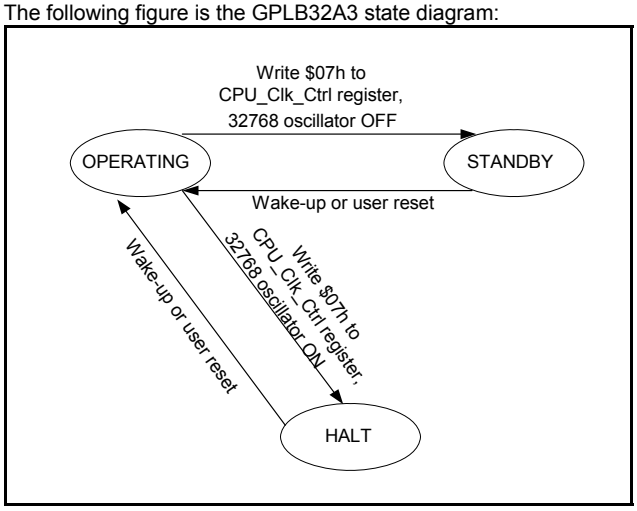
6.5. Standby Mode

The standby mode is a mode where the device is placed in its lowest current consumption state. In standby mode, all functions are turned off; in addition, RAM and I/Os will remain in their previous states.

6.6. Halt Mode

In halt mode, CPU clock halts and waits for an event (key press, timer overflow) to be awake. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode.

The following figure is the GPLB32A3 state diagram:



GPLB32A3 State Diagram

6.7. Speech and Melody

In speech synthesis, GPLB32A3 offers several timer interrupts for precise sampling frequency. The sound data can be stored into ROM and played back. Several algorithms are recommended for high fidelity and good compression of sound such as PCM and ADPCM.

For melody synthesis, the GPLB32A3 provides a dual tone mode. Once in the dual tone mode, users only need to program the tone frequency for each channel by writing to the timer/counter TM0 and TM1, and set the envelope of each channel. The hardware will toggle the tone wave automatically.

6.8. LCD Controller/Driver

The GPLB32A3 contains a 2048-dot LCD controller/driver. Programmers are able to define the LCD configuration by setting the LCD Control Register. Once the LCD configuration is completed, the desired pattern is displayed by filling up the LCD buffer with proper data. The LCD driver can also operate during sleep by keeping 32768Hz oscillator running. The LCD driver supports 1/16 ~ 1/32 duty and 1/5 ~ 1/6 bias.

6.9. LCD Voltage Generation

The GPLB32A3 offers a voltage regulator and a charge-pumping circuit. The voltage regulator provides the charge-pump circuit a reference voltage (V2) to generate $V_{LCD.}$. Users can get the preferred V_{LCD} by changing the output reference voltage (writing to register) of the voltage regulator. Enabling the voltage regulator and charge-pump circuit gets a stable V_{LCD} that will not be affected by VDD. The V_{LCD} is adjustable from 2.95V to 6.85V in 1/6 bias and from 2.45V to 5.75V in 1/5 bias.

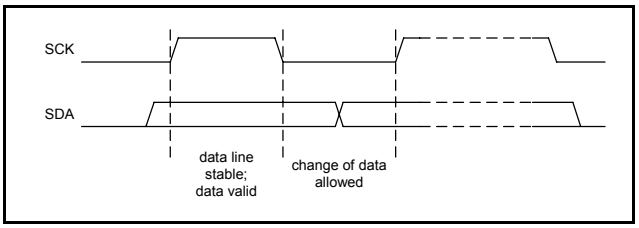
6.10. Audio Output

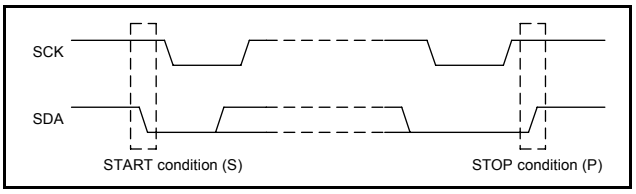
Internally, the GPLB32A3 supports two audio output modes: PWM or DAC. The GPLB32A3 has a pair of PWM drivers, supporting two sound channels. Each channel is able to play speech or tone individually. The PWM drivers can directly drive speaker or buzzer without buffer or amplifying circuit.

In DAC mode, GPLB32A3 supports 2-channel DAC current output with 8-bit resolution. The DAC current signal of each channel outputs through pin AUDA and AUDB respectively.

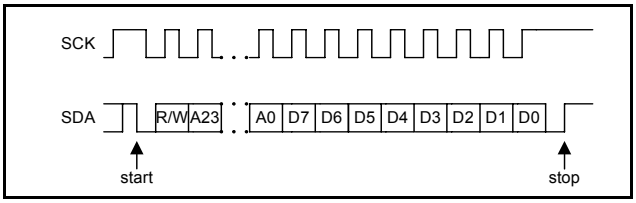
6.11. Serial SRAM Interface

The Serial SRAM interface is able to expand the data storage SRAM. The Control Registers are $30 - $36. Note that the SDA and SCK pins are shared with PC [1:0] and therefore, users should define PC [1:0] as Serial SRAM interface.

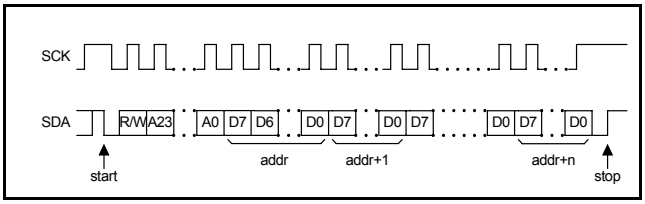




6.11.1. Read/Write timing



6.11.2. Continuous READ/WRITE timing



6.12. Asynchronous Serial Interface (UART)

The GPLB32A3 supports a 1-channel UART, bit-rate up to 115.2kbps, for serial communications. The UART operations are mainly controlled by UART command registers, including Tx/ Rx interrupt, parity check, parity even/odd, and clock source. Two interrupts are generated by Rx and Tx. The Rx or Tx interrupt activates when a byte is received or transmitted. Reading the status register determines the interrupt is generated by Rx or Tx. Frame, overrun and parity errors are detected as each byte is received and the error status can be read from status register.

The UART supports clock auto calibration. If auto calibration is selected, standard baud rate from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to the baud rate control registers. The supported baud rates and their minimum R-oscillator clock frequency requirements are shown in the table below.

Baud Rate(bps)	Min. Frosc(Hz)
1200	24000
2400	48000
4800	96000
9600	192000
19200	384000
38400	768000
51200	1024000
57600	1152000
102400	2048000
115200	2304000

If the auto calibration is not selected, users can get desired baud rates by writing appropriate values to pre-scalar registers. Non-standard baud rates can be obtained by this method. In non-calibration mode, users must understand that the R-oscillator frequency may alter due to manufacturing process variations, supply voltage, operating temperature and tolerance of external R components used.

6.13. Low Voltage Detection

The 8-level (software programmable) low voltage detector detects when a low voltage event occurs. Users can turn on the low detection to monitor VDD periodically to check if it is lower than the given value. In addition, if LV NMI is enabled, a NMI will be issued to notify CPU if power voltage drops below the given value. Also, the voltage detector will generate a system reset if power supply voltage drops below 2.2V. ***When LVR function is enabled, care must be taken not to turn off 32KHz crystal oscillator. Or, an unexpected reset may occur when 32KHz crystal is being turned on again.***

6.14. Key Scan Function

GPLB32A3 supports key scan function. The LCD driver will generate a key strobe signal in the period of every common. When PA receives this strobe signal, a wake-up is issued. Then, program can send the key scan signal through SEG [15:0] to determine the location of the depressed key.

6.15. Watchdog Timer (WDT)

An on-chip watchdog timer is also available in the GPLB32A3. The WDT is designed to recover the system from abnormal operation. In some cases, if WDT is not cleared for one second, the WDT will generate a system reset to restart system. If WDT is enabled, prevent the system from accidental reset by clearing WDT every 0.5 seconds. The WDT can be cleared through software programming. Note that the WDT only works when 32768Hz clock is activated.

6.16. Mask Options

6.16.1. 32768 oscillator

1). X'TAL
2). R-oscillator

6.16.2. Watchdog timer

1). Enable
2). Disable

6.16.3. Audio output select

1). PWM
2). DAC

6.16.4. Low voltage reset

1). Enable
2). Disable

6.16.5. PA[6:7] / SEG[63:62]

Each port/segment can be optioned as I/O or LCD segment individually.

6.16.6. PC[0:1] / SCK, SDA / SEG[61:60]

Each port/segment can be optioned as I/O or LCD segment individually.

6.16.7. PC[4:7] / SEG[73:70] / COM[25:22]

Each port/segment/common can be optioned as I/O or LCD segment/common individually.

6.16.8. PB[0:5] / SEG[69:64] / COM[21:16]

Each port/segment/common can be optioned as I/O or LCD segment/common individually.

6.16.9. PD[0:5] / COM[31:26]

Each port/common can be optioned as I/O or LCD common individually.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to + 60℃
Storage Temperature	T_{STO}	-50℃ to + 150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

7.2. DC Characteristics

VDD=3.0V, T_A=25℃

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
		3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	600	-	μA	F_{CPU} = 1.0MHz @ 3.0V F_{OSC} = 4.0MHz, no load
Halt Current	I_{HALT}	-	25	-	μA	VDD = 3.0V, 32K X'TAL ON, LCD ON, no LCD panel
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, all off
Audio Output Current (PWM)	I_{OH}	-	-20	-	mA	VDD = 3.0V, V_{OH} = 2.5V
		-	-40	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Audio Output Current (PWM)	I_{OL}	-	20	-	mA	VDD = 3.0V, V_{OL} = 0.5V
		-	40	-	mA	VDD = 3.0V, V_{OL} = 1.0V
Audio Output Current (DAC)	I_{DAC}	-	3.0	-	mA	VDD = 5.0V, full scale
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (I/O)	I_{OH}	-1.0	-	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (I/O)	I_{OL}	1.0	-	-	mA	VDD = 3.0V, V_{OL} = 0.8V
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	2.45	-	5.75	V	VDD = 3.0V, 1/5 bias, no load
		2.95	-	6.85	V	VDD = 3.0V, 1/6 bias, no load
OSC Resistor	R_{OSC}	-	180K	-	Ω	F_{OSC} = 2.0MHz @ 3.0V
OSC 32KHz Resistor	R_{32k}	-	700K	-	Ω	F_{32K} = 32KHz@ 3.0V
CPU Clock	F_{CPU}	-	-	4.0	MHz	F_{CPU} = F_{OSC}/1 @ 2.4V
		-	-	5.0	MHz	F_{CPU} = F_{OSC}/1 @ 3.6V

Note: V_{LCD} should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

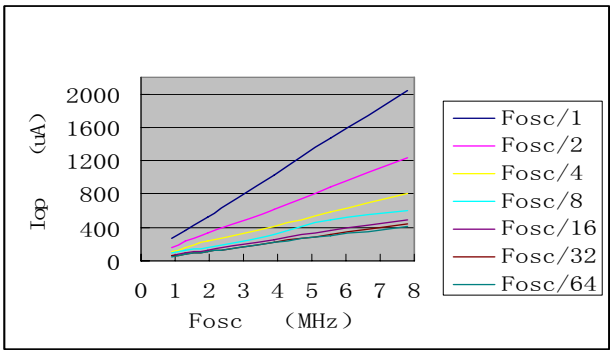
VDD=4.5V, T_A=25℃

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	1400	-	μA	F_{CPU} = 1.0MHz @ 4.5V F_{OSC} = 4.0MHz, no load
Halt Current	I_{HALT}	-	40	-	μA	VDD = 4.5V, 32K X'TAL ON, LCD ON, no LCD panel
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 4.5V, all off
Audio Output Current (PWM)	I_{OH}	-	-40	-	mA	VDD = 4.5V, V_{OH} = 4.0V
		-	-80	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Audio Output Current (PWM)	I_{OL}	-	40	-	mA	VDD = 4.5V, V_{OL} = 0.5V
		-	80	-	mA	VDD = 4.5V, V_{OL} = 1.0V
Audio Output Current (DAC)	I_{DAC}	-	3.0	-	mA	VDD = 5.0V, full scale
Input High Level	V_{IH}	0.8VDD	-	-	V	VDD = 4.5V
Input Low Level	V_{IL}	-	-	0.2VDD	V	VDD = 4.5V
Output High Current (I/O)	I_{OH}	-2.0	-	-	mA	VDD = 4.5V, V_{OH} = 4.0V
Output Sink Current (I/O)	I_{OL}	2.0	-	-	mA	VDD = 4.5V, V_{OL} = 0.5V
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	2.45	-	5.75	V	VDD = 4.5V, 1/5 bias, no load
		2.95	-	6.85	V	VDD = 4.5V, 1/6 bias, no load
OSC Resistor	R_{OSC}	-	180K	-	Ω	F_{OSC} = 2.0MHz @ 4.5V
OSC 32KHz Resistor	R_{32k}	-	780K	-	Ω	F_{32K} = 32KHz@ 4.5V
CPU Clock	F_{CPU}	-	-	5.0	MHz	F_{CPU} = F_{OSC}/1 @ 3.6V~5.5V

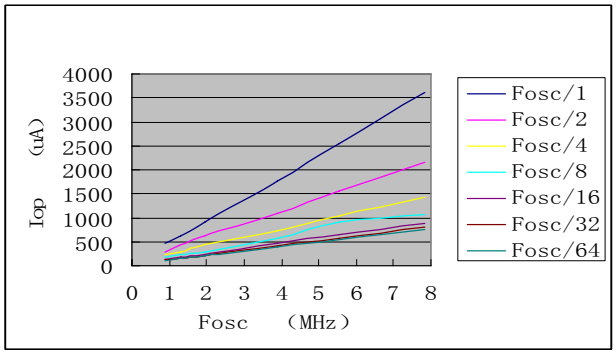
Note: V_{LCD} should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

7.3. The Relationships between the F_{OSC} and the I_{OP}

7.3.1. VDD = 3.0V

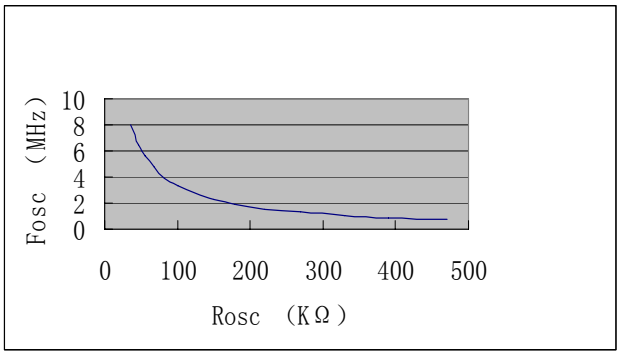


7.3.2. VDD = 4.5V

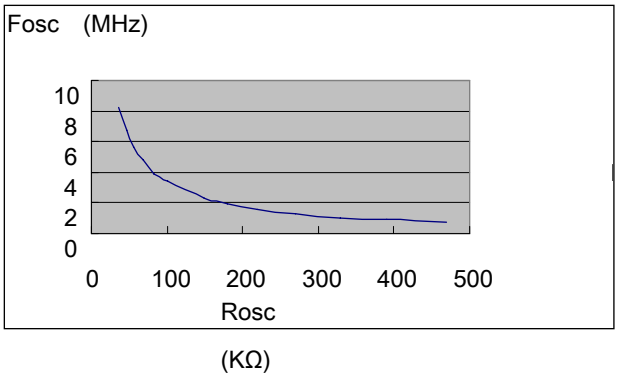


7.4. The Relationships between the R_{osc} and the F_{osc}

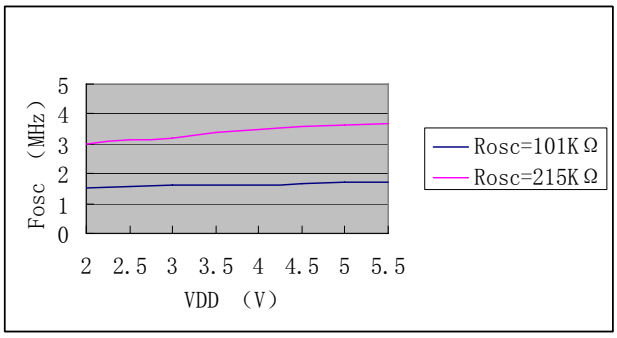
7.4.1. VDD = 3.0V



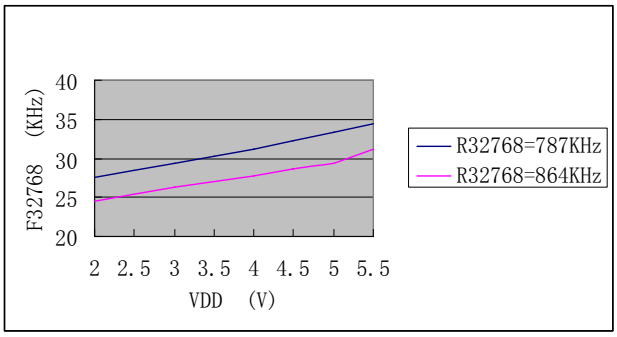
7.4.2. VDD= 4.5V



7.5. The Relationships between the VDD and the F_{osc}

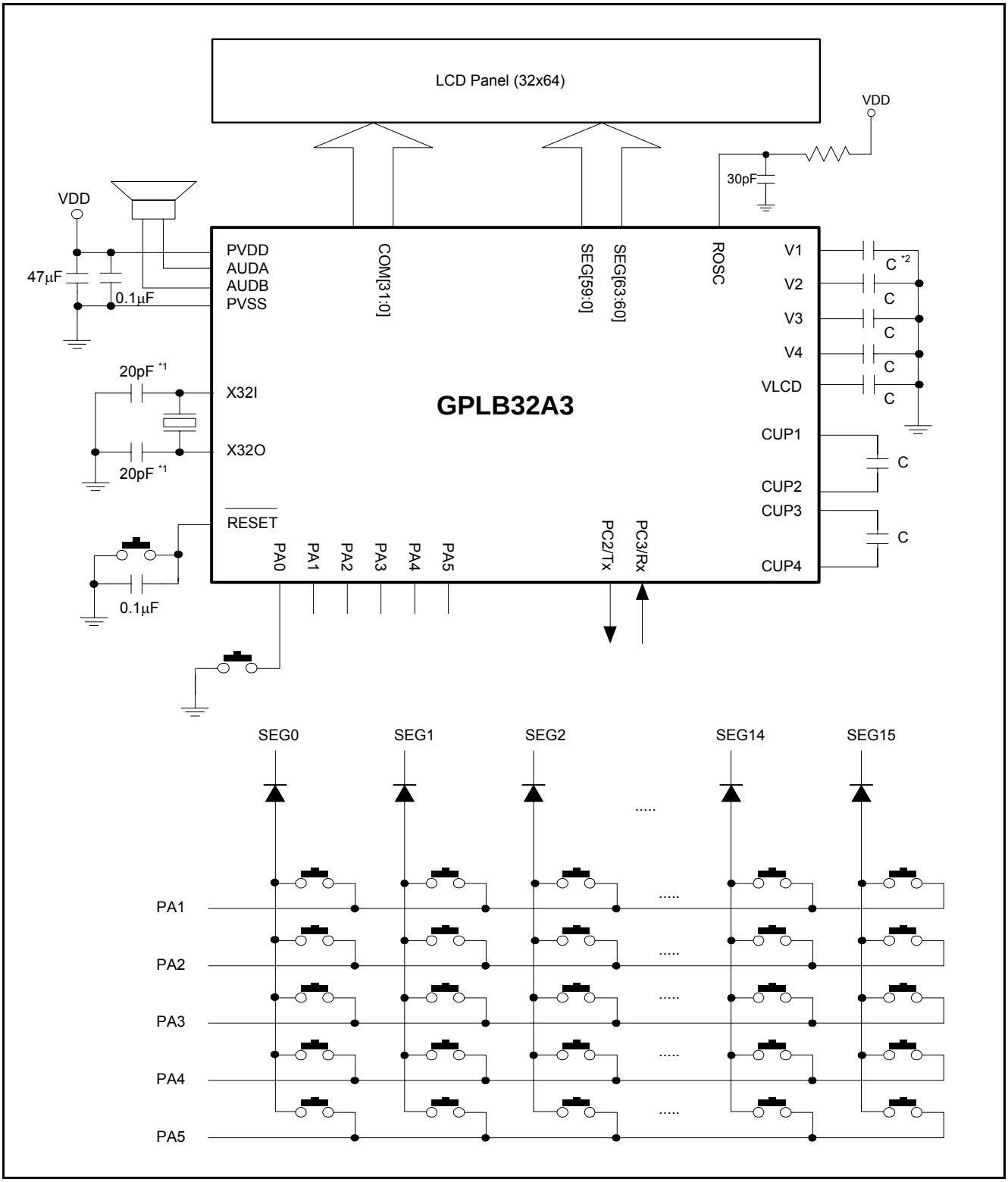


7.6. The relationships between the VDD and the F_{32768}



8. APPLICATION CIRCUITS

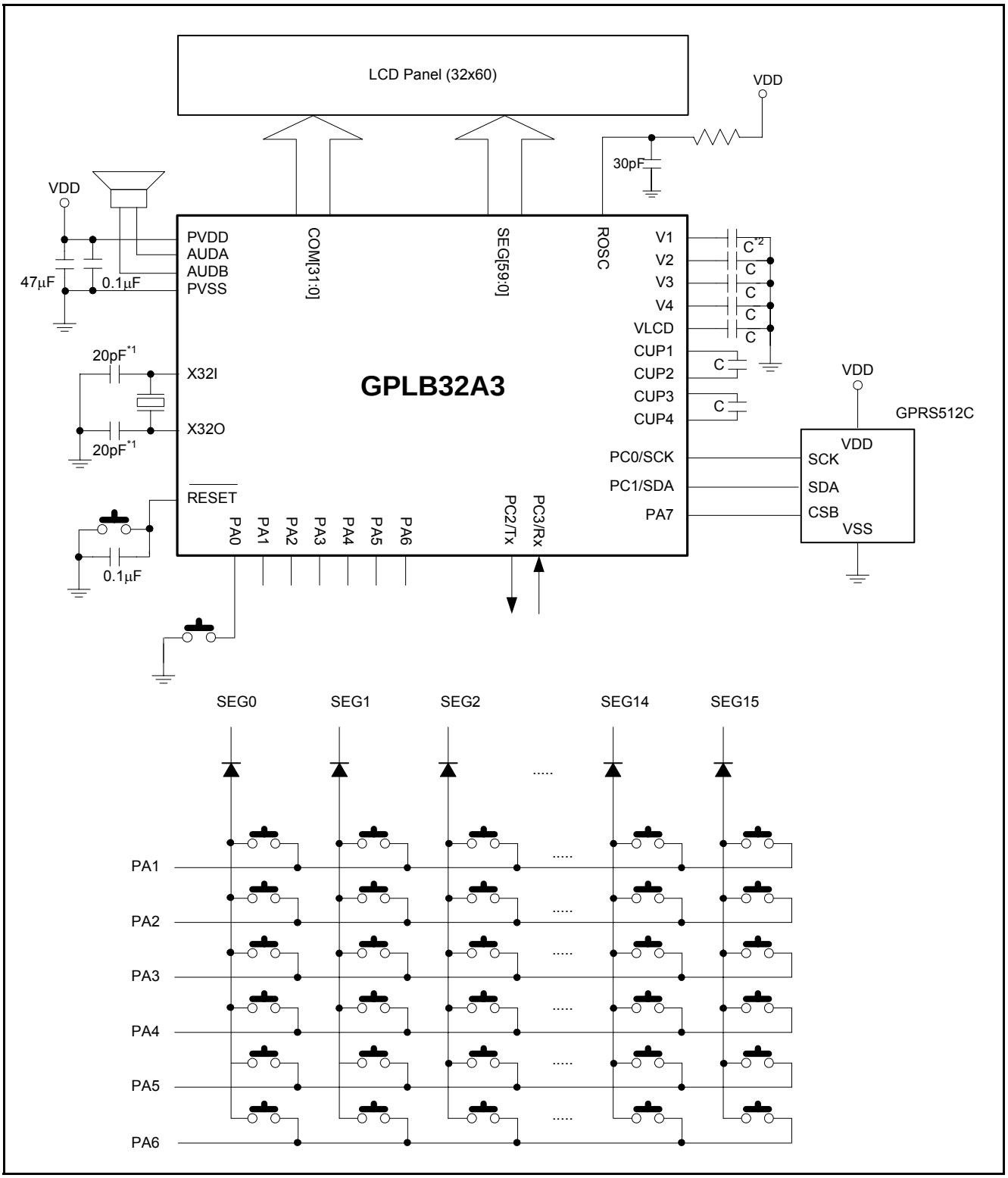
8.1. 2048 Dots LCD Driver, 64 Segments × 32 Commons, 1/5 or 1/6 Bias with External Serial SRAM - (1)



Note*1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*2: The value of the capacitance(C) would range from 0.1μF to 4.7μF to stable the output voltage.

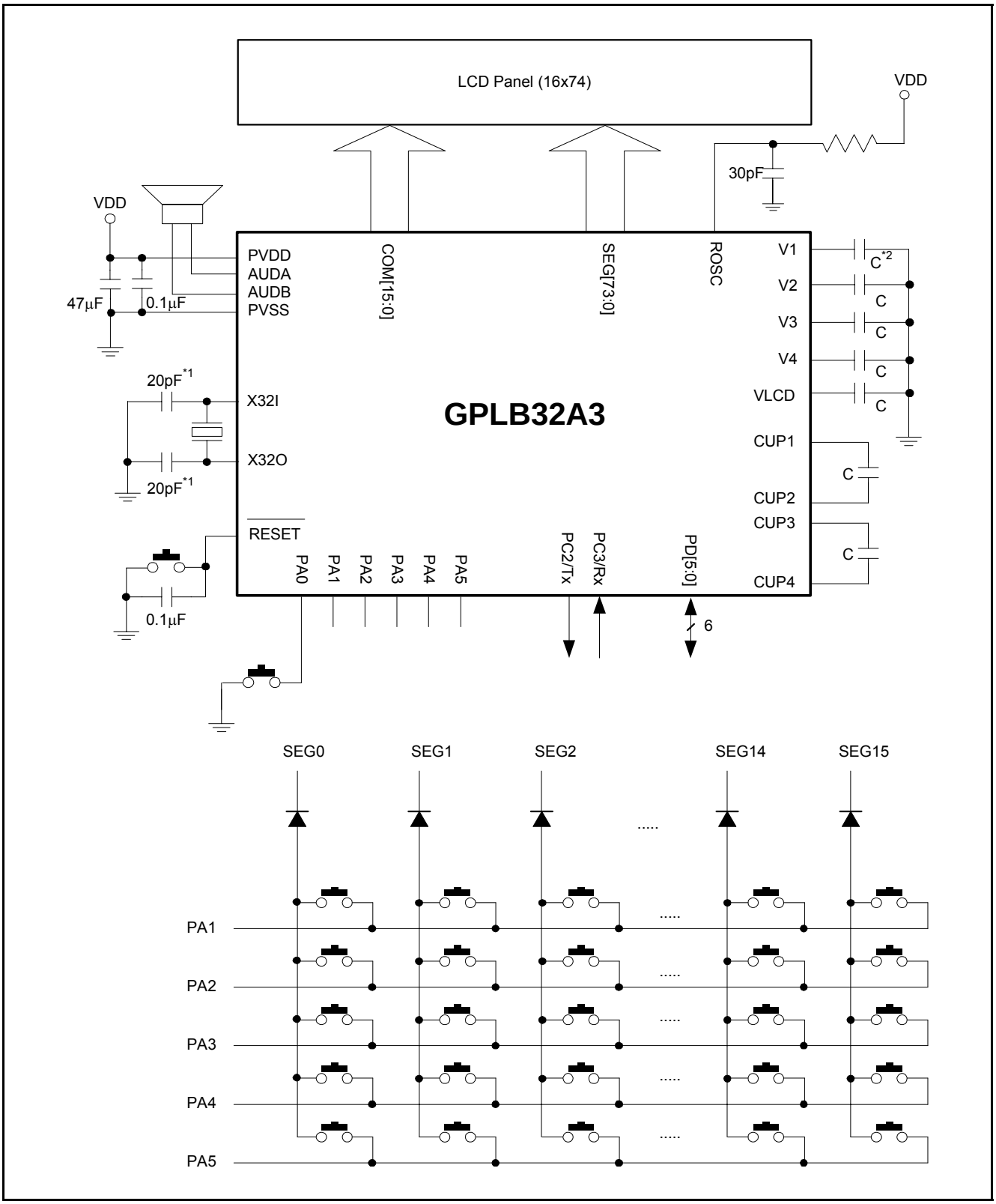
8.2. 1920 Dots LCD Driver, 60 Segments × 32 Commons, 1/5 or 1/6 Bias with External Serial SRAM - (2)



Note*1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*2: The value of the capacitance(C) would range from 0.1μF to 4.7μF to stable the output voltage.

8.3. 1184 Dots LCD Driver, 74 Segments × 16 Commons, 1/5 Bias - (3)

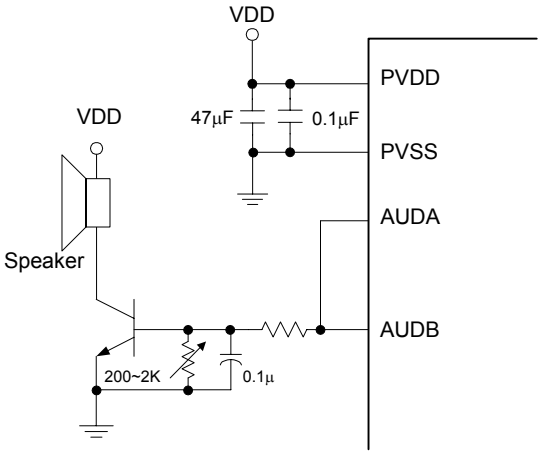


Note*1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

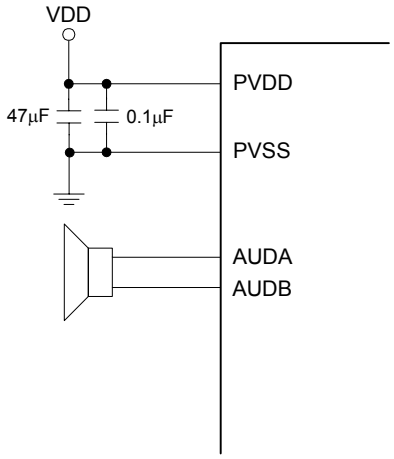
Note*2: The value of the capacitance(C) would range from 0.1μF to 4.7μF to stable the output voltage.

8.4. Audio Output Connections - (4)

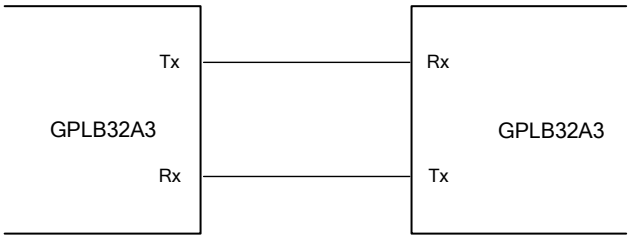
1). DAC Audio Output



2). PWM Audio Output



8.5. Serial Communications between Two GPLB32A3s- (5)



9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPLB32A3-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
Mar. 04, 2009	1.1	Modify the document title.	1, 3
Dec. 18, 2008	1.0	Add 7.4 The Relationships between the ROSC and the FOSC.	12
Oct. 09, 2008	0.1	Preliminary release.	19