DATA SHEET

GPLB34A3

2368 Dots LCD Controller with 1MB Rom

AUG. 18, 2010

Version 1.6

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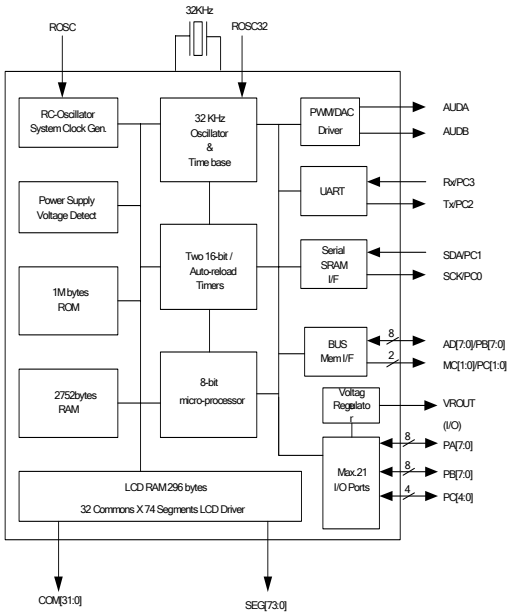
2368 DOTS LCD CONTROLLER WITH 1MB ROM

1. GENERAL DESCRIPTION

The GPLB34A3, an 8-bit CMOS microprocessor, contains 2752 bytes working RAM, 1M bytes ROM, 21 I/Os, interrupt/wakeup controller, UART for serial communication, Serial SRAM interface and Bus memory interface for memory expansion, and automatic display controller/driver for LCD. It also features one PWM driver with two audio channels to produce attractive sound effects easily. Its large ROM area can be used to store both program and audio data. The built-in UART speeds up data transmission between two devices. Furthermore, a SLEEP (power-down) function is also built-in to extend power life. The GPLB34A3 is designed with state-of-the-art technology to fulfill LCD application needs, especially for hand-held products.

2. BLOCK DIAGRAM



Note1: PB[7:0] share pins with Bus memory interface Addr/Data bus.
Note2: PC[1:0] share pins with Bus memory interface MC[1:0]. Also share pins with Serial SRAM interface SDA/SCK.
Note3: PC[3:2] share pins with UART Rx/Tx.
Note4: PC[4] share pins with external interrupt.

3. FEATURES

- Built-in 8-bit processor
  - **2752 bytes SRAM**
  - **1M bytes ROM**
  - Max. operating speed: 6.0MHz @ 2.4V - 3.6V
    6.0MHz @ 3.6V - 5.5V
  - CPU clock is software programmable, can be /1, /2, /4, /8, /16, /32, /64 R-oscillator clock frequency
  - 6 wake-up sources
  - 7 interrupt sources
- Asynchronous serial interface (UART)
- Serial SRAM interface
- Bus memory interface
- Built-in voltage regulator for external memory devices
- Key scan function
  - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
  - **Up to 74 segments, up to 32 commons, maximum 2368 dots**
  - 1/5, 1/6 bias; 1/16, 1/32 duty capability
  - **296 bytes dedicated LCD RAM**
  - Built-in voltage regulator to generate VLCD for LCD driver
  - 32-level contrast control
- Power saving SLEEP mode
- **Low voltage detector**
  - **6-level 2.9V ~ 2.2V detection**
  - **2.2V low voltage reset**
- Wide operating voltage range:
  - 2.4V - 3.6V
  - 3.6V - 5.5V
- Peripherals
  - **Max. 21 I/O pins (PA[7:0], PB[7:0], PC[4:0])**
    . Dedicated I/Os: PA[7:0]
    . Shared pin I/Os:
    PB[7:0]/BMI AD Bus [7:0]
    PC[1:0]/BMI MC[1:0]/SSRAM SDA, SCK
    PC[3:2]/UART Rx/Tx
  - 32.768KHz oscillator circuit for RTC
  - RC-oscillator (only one resistor is needed)
  - Two 16-bit reloadable timer/counters
  - **2-channel PWM audio output**
  - Watchdog Timer for reliable operation
- Low-power consumption:
  - 800μA typical @ 3.0V, F_{CPU} = 1.0MHz, F_{OSC}=4.0MHz
  - 50μA typical halt current @ 3.0V
  - <1.0μA typical standby current @ 3.0V

4. APPICATION FIELD

- ■ Hand held games
- ■ Scientific calculator
- ■ Talking calculator, talking clock
- ■ Talking instrument controller
- ■ General speech synthesizer
- ■ Data Bank

5. SIGNAL DESCRIPTIONS

Total: 148 pins

Mnemonic	PIN No.	Type	Description
SEG73 - 0	1 - 74	O	LCD driver segment output. SEG15 - 0 share pin with key scan port.
COM15 - 0 COM31 - 16	75 - 90 148 - 133	O	LCD driver common output.
PA7 - 0	105 - 98	I/O	Port A is a bi-directional I/O port, which can be software programmed as wake-up I/O.
PB7 - 0	113 - 120	I/O	Port B is a bi-directional I/O port. Share pin with Bus Memory Interface Addr/Data.
PC1 / MC1 / SDA PC0 / MC0 / SCK	122 121	I/O	Port C is a bi-directional I/O port. Share pin with Bus Memory MC1 - 0. Also share pin with SDA/SCK.
PC3 / Rx	96	I/O	UART input. Share pin with PC3.
PC2 / Tx	97	I/O	UART output. Share pin with PC2.
PC4	95		Port C is a bi-directional I/O port. Share pin and external interrupt.
ROSC	108	I	ROSC input, connect to VDD through a resistor.
$\overline{\text{RESET}}$	112	I	System reset input, low active.
AUDA, AUDB	93, 91	O	PWM audio output.
X32I	110	I	32.768KHz crystal input or connects to VDD through a resistor (option).
X32O	111	O	32.768KHz crystal output.
TEST	130	I	Test inputs.
VCI	125	O	The input voltage of charge pump.
CAP1P, CAP1N	126, 127	P	Charge pump capacitor interconnection pins.
CAP2P, CAP2N	129, 128	P	Charge pump capacitor interconnection pins.
VPP	131	P	Charge pump output (VCI X2 or X3).
VLCD	132	O	LCD top voltage.
VROUT	123	P	Internal regulator output. Enable or disable via mask option. Should be connected to VDD if internal Regulator is disabled.
VDD	107	P	Positive supply for logic and IO pins.
VSS	106	P	Ground reference for logic and IO pins.
AVDD	124	P	Analog power pin.
PVDD	92	P	Positive supply for PWM driver.
PVSS	94	P	Ground reference for PWM driver.
VSSL	109	P	Ground for segments and commons.

Legend: I = Input, O = Output, P = Power

Note1: The power and ground pads should be double wire bonded to reduce ground bouncing.

Note2: The separation of VSS and VSSL PCB traces is recommended to reduce ground noise.

5.1. PAD Assignment

This IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, bond all VDD and VSS/VSSL pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

6. FUNCTIONAL DESCRIPTIONS

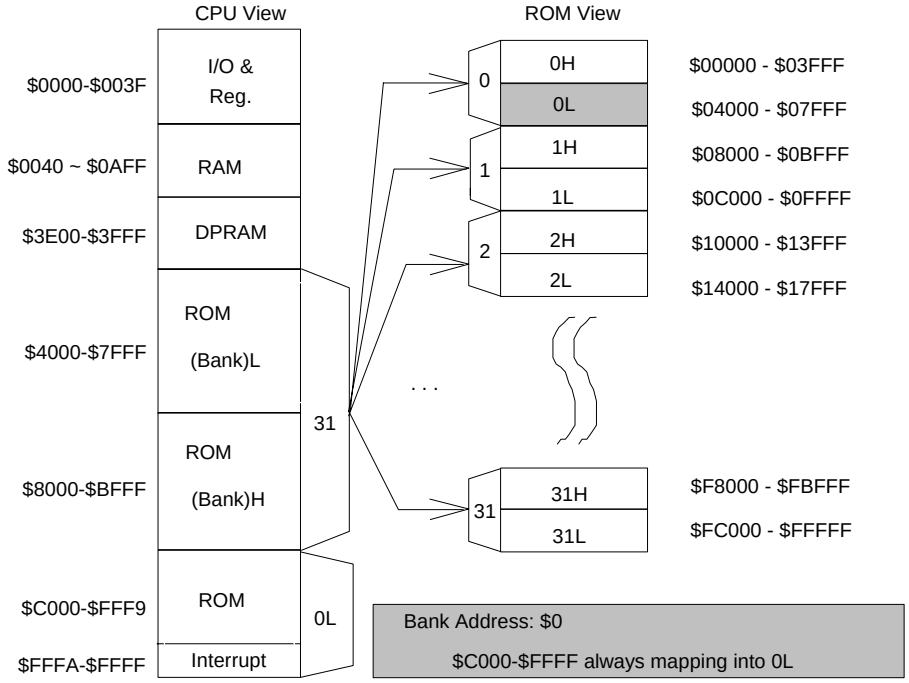
6.1. Memory

The GPLB34A3 contains 1M-byte ROM and 2752-byte SRAM. Cooperating with Generalplus bus extender, GPBA01B, the external memory, either RAM or ROM, can be extended up to 4MB. Serial SRAM interface is also provided in GPLB34A3, thus SRAM space can be extended by using Generalplus Serial SRAM, GPRS256B or GPRS512C.

6.2. Map of Memory and I/Os

***NMI SOURCE:**
- LV DETECT
- TIMER1

***INT SOURCE:**
- EXT INT
- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1
- UART TX
- UART RX



1. $4000-$BFFF can be external memory if MEXT ($03.7) = 1 and Bank port ($00.7) = 1.
2. $C000-$FFFF can be external memory if MEXT ($03.7) = 1 and EXC($0b.1) = 1.
3. User's program should start from $C800. $C000-$C7FF is the test program area.
4. User's program interrupt vector: $FFFA ~ $FFFF
5. Test program interrupt vector: $FFF2 ~ $FFF7

6.3. Operating States

There are three operation modes involved in GPLB34A3: standby, halt and operating. The following table shows the differences between these modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

6.3.1. Operating Mode

In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated. Generally speaking, this mode consumes the highest current.

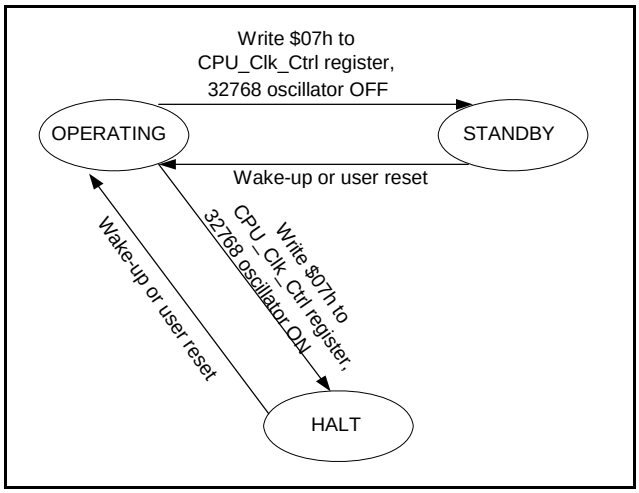
6.3.2. Standby Mode

Write "07H" to P_04H_CPU_Clk_Ctrl Register ($04) and turn off 32768Hz oscillator to activate standby mode. The standby mode is a mode, where the device is placed in its lowest current consumption state. In standby mode, all functions are turned off; in addition, RAM and I/Os will remain in their previous states.

6.3.3. Halt Mode

Write "07H" to P_04H_CPU_Clk_Ctrl Register ($04) but still keeps 32768Hz oscillator running to enter halt mode. In halt mode, CPU clock halts and waits for an event (e.g. key press, timer overflow) to wake up. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode.

The following figure is the GPLB34A3 state diagram:



GPLB34A3 State Diagram

6.4. Speech and Melody

For speech synthesis, the GPLB34A3 provides several timer interrupts for a precise sampling frequency. The sound data can be stored into ROM and be played back. Several algorithms are recommended for high fidelity and good compression of sound such as PCM and ADPCM.

For melody synthesis, the GPLB34A3 provides a dual tone mode. In the dual tone mode, users only need to program the tone frequency for each channel by writing to the timer/counter TM0 and TM1, and set the envelope of each channel. The hardware will toggle the tone wave automatically.

6.5. LCD Controller/Driver

The GPLB34A3 contains a 2368-dot LCD controller/driver. Programmers are able to define the LCD configuration by setting up the LCD Control Register. Once the LCD configuration is completed, the desired pattern can be displayed by filling the LCD buffer with proper data. The LCD driver can also operate during sleep by keeping 32768Hz oscillator running. The LCD driver in GPLB34A3 supports 1/16 - 1/32 duty and 1/5 - 1/6 bias.

6.6. LCD Voltage Generation

The GPLB34A3 offers a voltage regulator and a charge-pumping circuit. The charge-pumping circuit provides VPP as the power source for voltage regulator. The voltage regulator generates the LCD bias voltages (VLCD, V1~V4) needed for the LCD driver. VPP and VLCD can be adjusted by program settings. Enabling the voltage regulator and charge-pumping circuit gets a stable VLCD that will not be affected by VDD. The VLCD is adjustable from 2.45V to 5.75V (in 1/5 bias), or 2.95V to 6.85V (in 1/6 bias) with 32 levels.

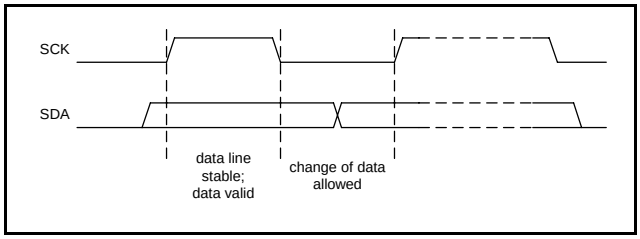
Users should be noted that the difference between VPP and VLCD voltage should be larger than 0.5V (VPP-VLCD>0.5V) to optimize voltage regulator performance. Also, VDD should be higher than VPP/3 to keep VPP stable.

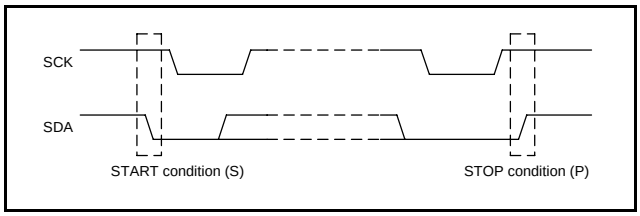
6.7. PWM Output

Internally, the GPLB34A3 has a pair of PWM drivers, supporting two sound channels. Each channel is able to play speech or tone individually. The PWM drivers can directly drive speaker or buzzer without buffer or amplification circuit.

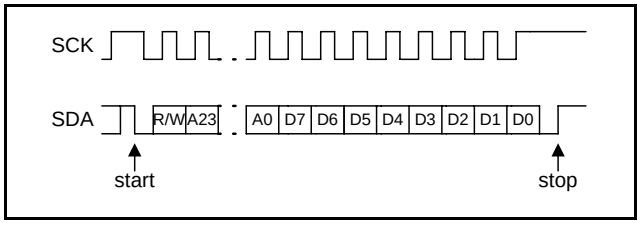
6.8. Serial SRAM Interface

The Serial SRAM interface is able to expand the data storage SRAM. The Control Registers are ranged from $30-$36. Note that the pins of SDA and SCK are shared with PC [1:0] and therefore, users should set PC[1:0] as Serial SRAM interface by writing to Port $27[1:0].

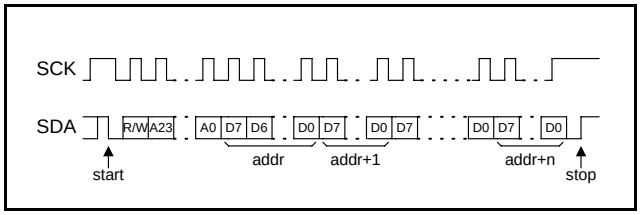




6.8.1. Read/Write Timing



6.8.2. Continuous Read/Write Timing



6.9. Bus Memory Interface

A built-in Bus memory interface is available in GPLB34A3. Through Bus memory interface, user can expand the memory space by using an external Bus memory (SRAM, mask ROM or Flash). The Bus memory interface includes 10 signal pins: MC1, MC0 and AD BUS[7:0] which shared pad with Port B. Before using the Bus memory interface, users should set MEXT=1 ($03.7) and BANK register ($0), then access address $4000-BFFF to read or write data from external bus memory. Note that when using Bus memory interface, CPU clock setting can not be set as F_{OSC}/1, should be /2 or slower.

MC1	MC0	AD BUS [7:0]
L	L	Data for Write
L	H	Data for Read
H	L	AL (Address Low byte)
H	H	AH (Address High byte)

6.10. Voltage Regulator

The GPLB34A3 offers a voltage regulator, which supplies power source for external memory devices. The voltage regulator can output four voltage levels, 2.5V/2.6V/2.7V/3.0V via mask option. The output voltage level should be properly selected based on the electrical characteristics of external memory devices involved.

6.11. Asynchronous Serial Interface

The GPLB34A3 supports a 1-channel UART for serial communications. The bit-rate is up to 115.2kbps. UART operation is controlled by UART command registers. Configurations such as Tx/Rx interrupt, parity check, parity even/odd and clock source can be configured in the command registers. Two interrupts are generated by Rx and Tx. The Rx or Tx interrupt will be activated when a byte is received or transmitted. Reading the status register informs whether the interrupt is generated by Rx or Tx. Frame, overrun and parity errors are detected, as each byte is received and all error status can be read from status register.

The UART supports clock auto calibration. If auto calibration is selected, standard baud rate from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to the baud rate control registers. The supported baud rates and their minimum R-oscillator clock frequency requirements are shown in the table below.

Baud Rate(bps)	Min. Frosc(Hz)
1200	24000
2400	48000
4800	96000
9600	192000
19200	384000
38400	768000
51200	1024000
57600	1152000
102400	2048000
115200	2304000

If the auto calibration is not selected, users can get desired baud rates by writing appropriate values to pre-scalar registers. Non-standard baud rates can be obtained by this method. In the non-calibration mode, users should understand that the R-oscillator frequency may alter due to manufacturing process variations, supply voltage, operating temperature and tolerance of external R components used.

6.12. Low Voltage Detection

The GPLB34A3 provides a 6-level (Software programmable) low voltage detector to detect low voltage events. Users can turn on the low detection to monitor VDD periodically to check if it is lower than the given value. In addition, if LV NMI is enabled, a NMI will be issued to notify CPU if power voltage drops below the given value. Also, the voltage detector will generate a system reset if power supply voltage drops below 2.2V. *When LVR function is enabled, care must be taken not to turn off 32KHz crystal oscillator. Otherwise an unexpected reset may occur when 32KHz crystal is being turned on again.*

6.13. Watchdog Timer (WDT)

An on chip watchdog timer is also available in the GPLB34A3. The WDT is designed to recover the system from abnormal operation. In some cases, if WDT is not cleared within one second, the WDT will generate a system reset to restart system. If WDT is enabled, the WDT should be cleared periodically to avoid accidental reset. The WDT can be cleared through software programming. Note that the WDT only works when 32768Hz clock is activated.

6.14. Mask Options

6.14.1. 32768 Oscillator

1). X'TAL

2). R-oscillator

6.14.2. Watchdog Timer

1). Enable

2). Disable

6.14.3. Voltage Regulator for External Memory Devices

1). Enable

2). Disable

6.14.4. Regulator Output Voltage Selection

1). 2.5V

2). 2.6V

3). 2.7V

4). 3.0V

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
		3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	800	-	μA	F_{CPU} = 1.0MHz @ 3.0V F_{ROSC} = 4.0MHz, no load
Halt Current	I_{HALT}	-	100	-	μA	VDD = 3.0V, 32K X'tal ON, LCD ON, Charge Pump=3X, 1/5 Bias, VLCD=5.75V, no LCD panel
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, all off
Audio Output Current	I_{OH}	-	-20	-	mA	VDD = 3.0V, V_{OH} = 2.5V
		-	-40	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Audio Output Current	I_{OL}	-	20	-	mA	VDD = 3.0V, V_{OL} = 0.5V
		-	40	-	mA	VDD = 3.0V, V_{OL} = 1.0V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (I/O)	I_{OH}	-1.0	-	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (I/O)	I_{OL}	1.0	-	-	mA	VDD = 3.0V, V_{OL} = 0.8V
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	2.45	-	5.75	V	VDD = 3.0V, 1/5 bias, no load
		2.95	-	6.85	V	VDD = 3.0V, 1/6 bias, no load
Regulator Output Voltage	V_{REG}	-	2.5	-	V	Output voltage is selected by bonding option
		-	2.6	-		
		-	2.7	-		
		-	3.0	-		
Regulator Output Voltage Drop	V_{RDROP}	-	-	100	mV	I_L = 1.0mA, VDD = 3.6V
OSC Resistor	R_{OSC}	-	150	-	KΩ	F_{OSC} = 2.0MHz @ 3.0V
OSC(ROSC32K) Resistor	R_{OSC32k}	-	680	-	KΩ	F_{OSC} = 32KHz @ 3.0V
CPU Clock	F_{CPU}	-	-	6.0	MHz	F_{CPU} = F_{OSC}/1 @ 2.4V
		-	-	6.0	MHz	F_{CPU} = F_{OSC}/1 @ 3.6V

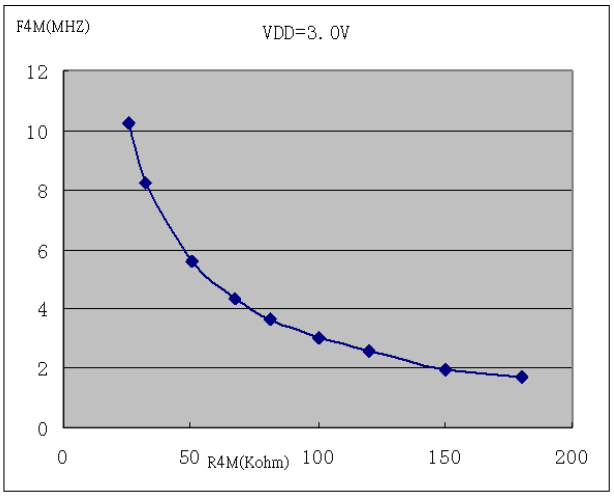
Note: V_{LCD} should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

7.3. Power and Ground Pads Bonding

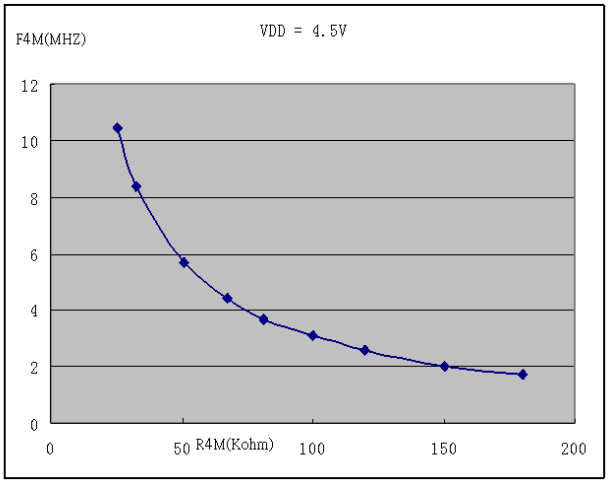
The power and ground pads should be double wire bonded to reduce ground bouncing.

7.4. The Relationship between the R_{OSC} and the F_{OSC}

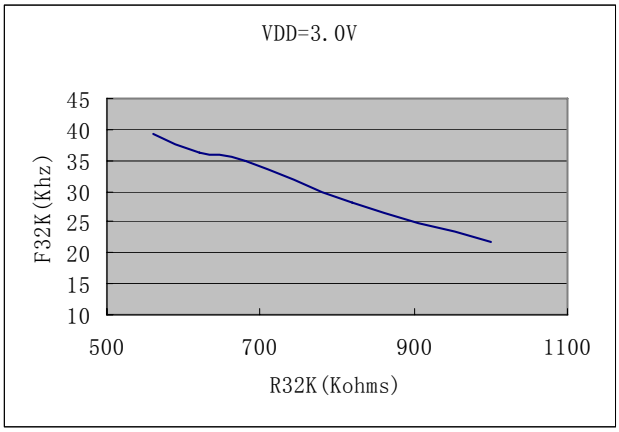
7.4.1. VDD = 3.0V, T_A = 25℃



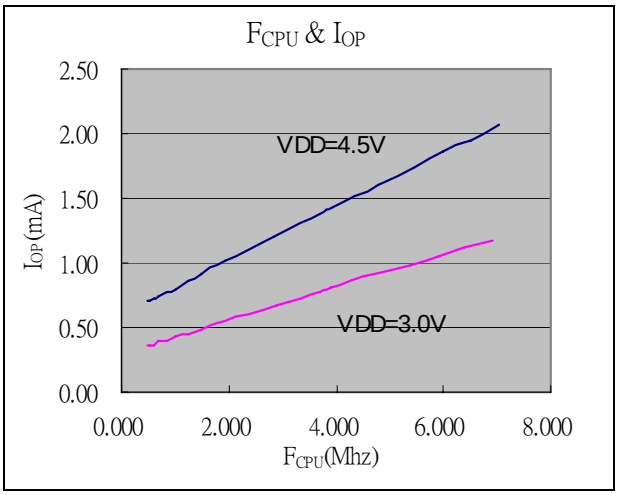
7.4.2. VDD = 4.5V, T_A = 25℃



7.5. The Relationship between the F32K and the R32K

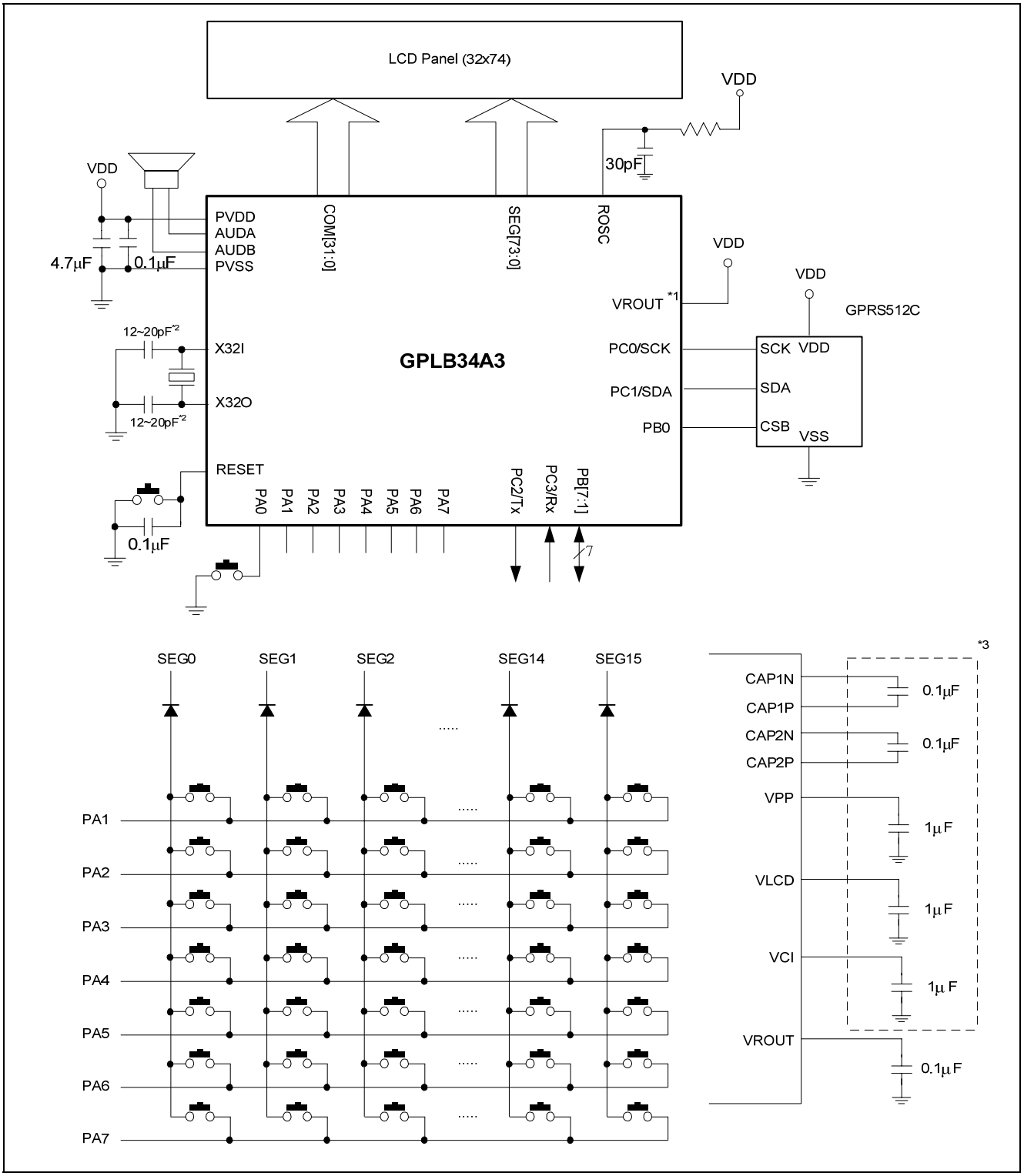


7.6. The Relationship between the F_{CPU} and the I_{OP}



8.APPLICATION CIRCUITS

8.1. 2368 Dots LCD Driver, 74 Segments × 32 Commons with External Serial SRAM, Regulator Disabled - (1)

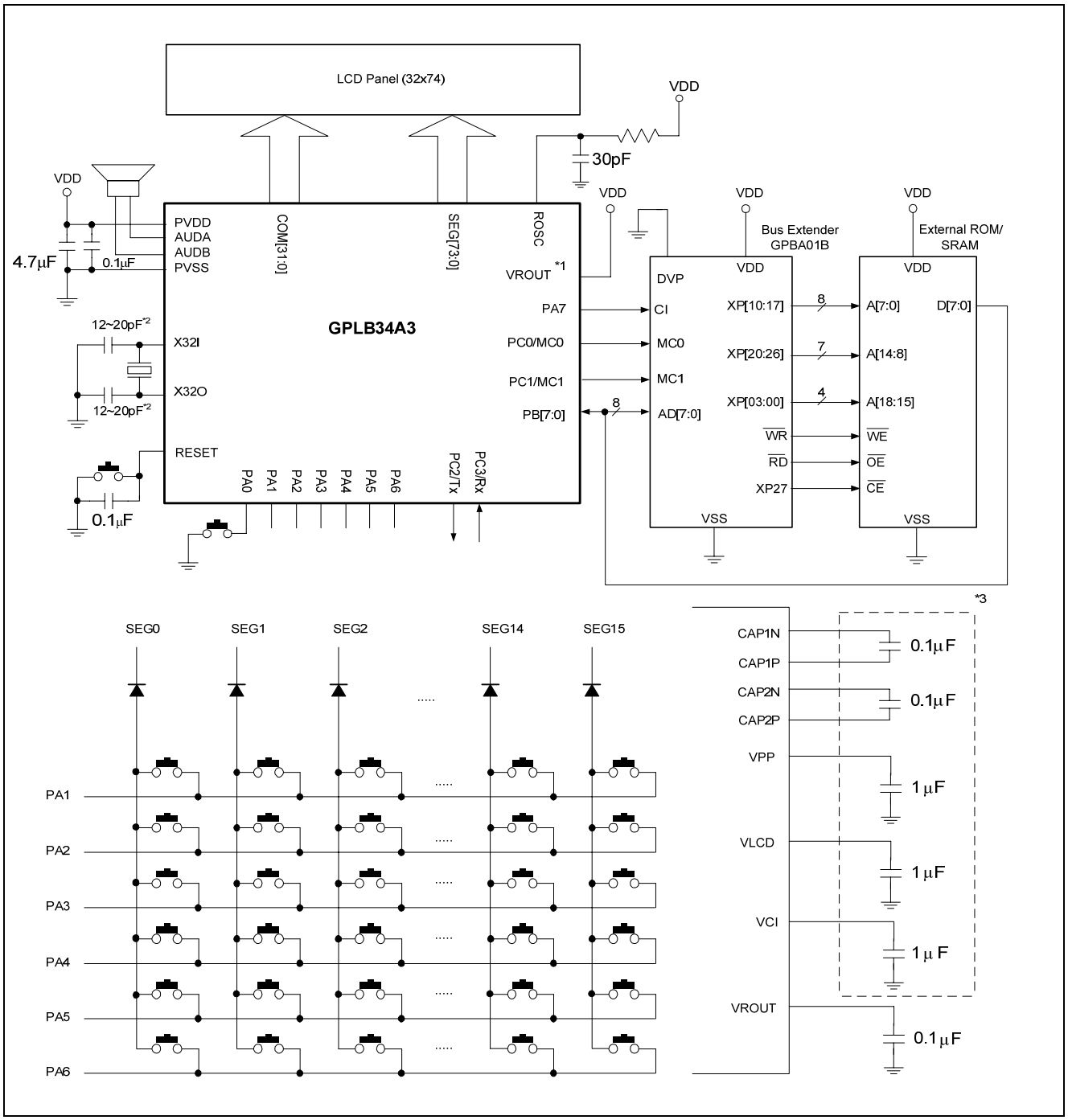


Note*1: Pin VROUT should be connected to VDD if internal Regulator is disabled.

Note*2: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*3: These capacitor values are for design guidance only. Different capacitor values may be required for different LCD panel connected.

8.2. 2368 Dots LCD Driver, 74 Segments × 32 Commons with Bus Extender, Regulator Disabled - (2)

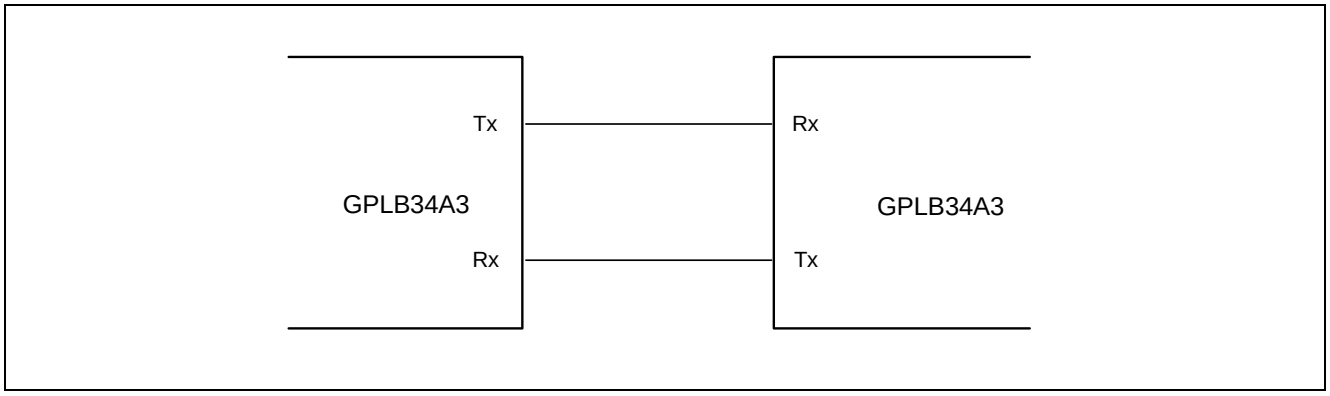


Note*1: Pin VROUT should be connected to VDD if internal Regulator is disabled.

Note*2: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*3: These capacitor values are for design guidance only. Different capacitor values may be required for different LCD panel connected.

8.3. Serial Communications between two GPLB34A3s - (3)



9.PACKAGE/PAD LOCATION

9.1. Ordering Information

Product Number	Package Type
GPLB34A3 - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
AUG. 18, 2010	1.6	Modify 2. BLOCK DIAGRAM	3
SEP. 08, 2009	1.5	1. Modify 3.FEATURES. Modify 7.2 DC Characteristics.	3 10
DEC. 30, 2008	1.4	Revise working frequency	
OCT. 13, 2008	1.3	1. Modify section 3.FEATURES. 2. Modify section 7.2 DC Characteristics.	3 10
JUL. 07, 2008	1.2	Modify the diagrams in section 7.4.	11
JAN. 07, 2008	1.1	Modify the diagrams in section 8. APPLICATION CIRCUITS.	12 - 14
NOV. 05, 2007	1.0	Original	17