DATA SHEET

GPLB38B

LCD Controller with 512KB ROM

MAY 10, 2010

Version 1.3

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LCD CONTROLLER WITH 512KB ROM

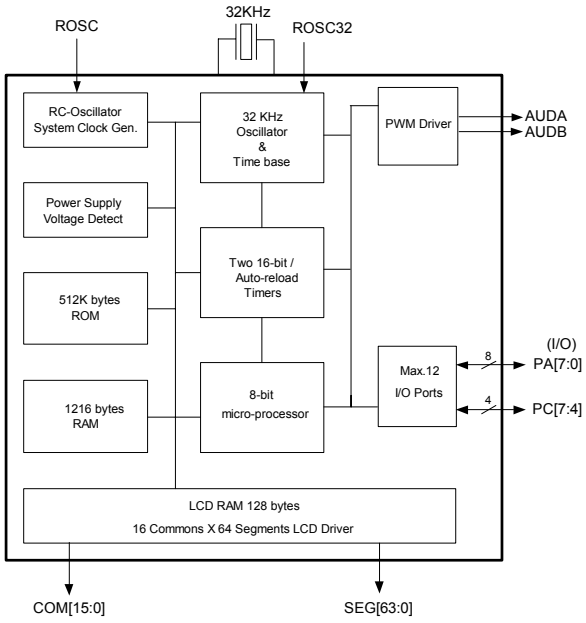
1. GENERAL DESCRIPTION

The GPLB38B, an 8-bit CMOS microprocessor, contains 1216 bytes working RAM, 512K bytes ROM, 12 I/Os, interrupt/wakeup controller, and automatic display controller/driver for LCD. It also features one PWM driver with two audio channels to produce attractive sound effects easily. Its large ROM area can be used to store both program and audio data. Furthermore, a SLEEP (power-down) function is also built in to extend power life. The GPLB38B is designed with GENERALPLUS state-of-the-art technology to fulfill LCD application needs, especially for hand-held products.

2. FEATURES

- Built in 8-bit processor
  - **1216 bytes SRAM**
  - **512K bytes ROM**
  - Max. operating speed: 8.0MHz @ 2.4V - 3.6V
  - Programmable CPU clock: /1, /2, /4, /8, /16, /32, /64 of ROSC Frequency.
  - 5 wake-up sources
  - 5 interrupt sources
- Key scan function
  - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
  - **64 segments, 16 commons, maximum 1024 dots**
  - 1/5 bias; 1/16 duty capability
  - **128 bytes dedicated LCD RAM**
  - Built-in voltage regulator to generate VLCD for LCD driver
  - 27-level contrast control (2.98V - 5.75V, in 1/5 bias)
- Power saving SLEEP mode
- **Low Voltage Detector**
  - **6-level 2.9V - 2.4V detection**
  - **2.2V Low voltage reset**
- Low power consumption:
  - 1.2mA typical @ 3.0V, F_{CPU} = 2.0MHz, F_{OSC} = 8.0MHz
  - 30μA typical halt current @ 3.0V
  - <1μA typical standby current @ 3.0V
- Peripherals
  - **Dedicated I/Os: PA[0:7], PC[4:7]**
  - 32.768KHz oscillator circuit for RTC
  - RC-oscillator (only one resistor is needed)
  - Two 16-bit reloadable timer/counters
  - **2-channel PWM audio outputs**
  - Watchdog Timer for reliable operation
- Wide operating voltage range:
  - 2.4V - 3.6V

3. BLOCK DIAGRAM



4. APPLICATION FIELD

- Handheld game
- Scientific calculator
- Talking calculator, Talking clock
- Talking instrument controller
- General speech synthesizer
- Data bank

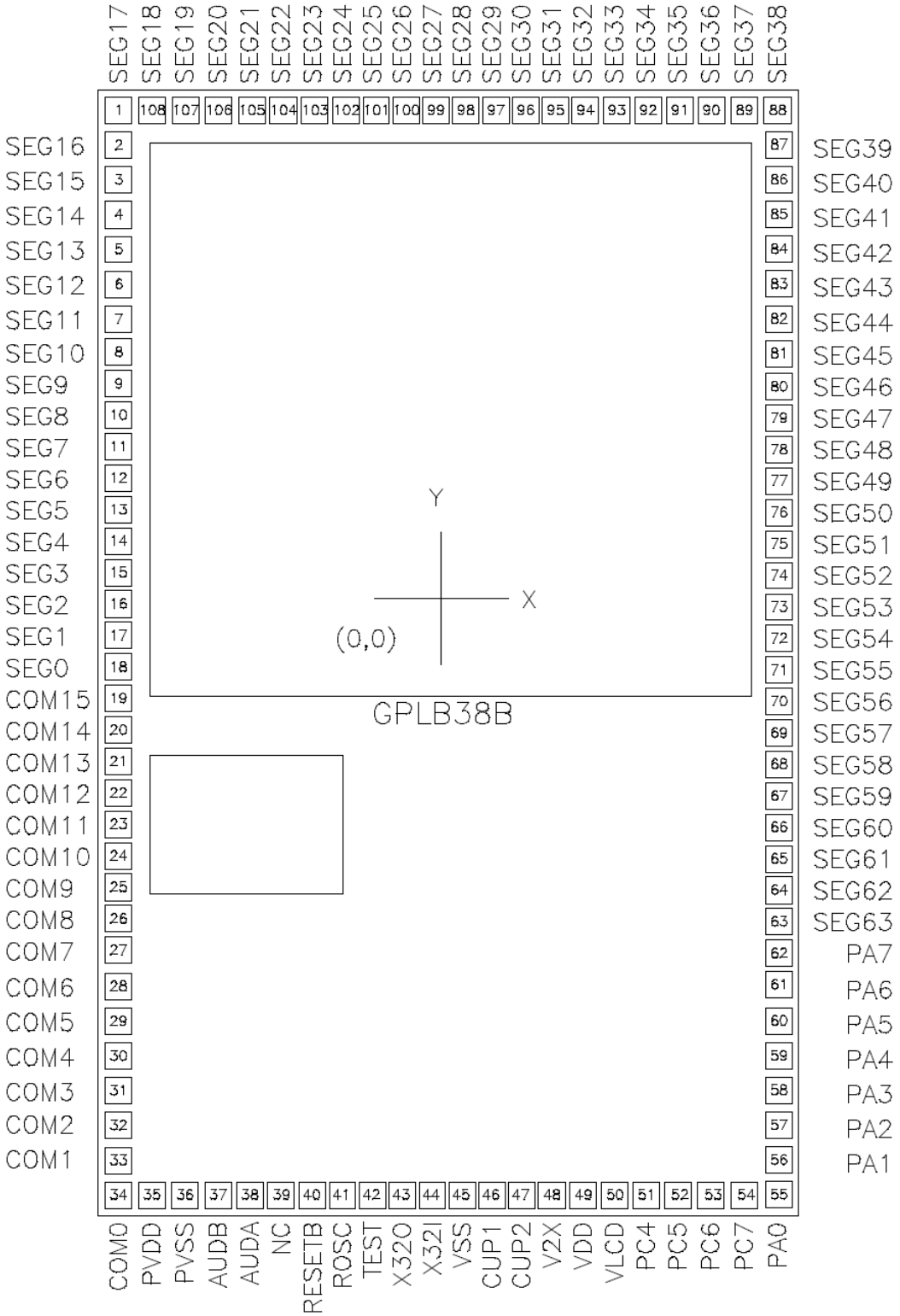
5. SIGNAL DESCRIPTIONS

Total: 107pins

Mnemonic	PIN No.	Type	Description
SEG63 - 0	63-108,1-18	O	LCD driver segment output.
COM15 - 0	19-34	O	LCD driver common output.
PA7 - 0	62-55	I/O	Port A is a bi-directional I/O port, which can be software programmed as wake up I/O.
PC7 - 4	54-51	I/O	Port C is a bi-directional I/O port.
ROSC	41	I	R-oscillator input, connect to VDD through a resistor.
$\overline{\text{RESET}}$	40	I	System reset input, low active.
AUDA, AUDB	38,37	O	PWM audio output.
X32I	44	I	32.768KHz crystal input or connects to VDD through a resistor (option).
X32O	43	O	32.768KHz crystal output.
TEST	42	I	Test input.
CUP2 - 1	47,46	P	LCD voltage generation. Charge pump capacitor inter-connection pins.
V2X	48	P	Pump 2X output.
VLCD	50	P	LCD voltage generation.
VDD	49	P	Power supply voltage input.
VSS	45	P	Ground reference.
PVDD	35	P	PWM driver power.
PVSS	36	P	PWM driver ground reference.
NC	39		

Legend: I = Input, O = Output, P = Power

5.1. PAD Assignment



The IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

6. FUNCATIONAL DESCRIPTIONS

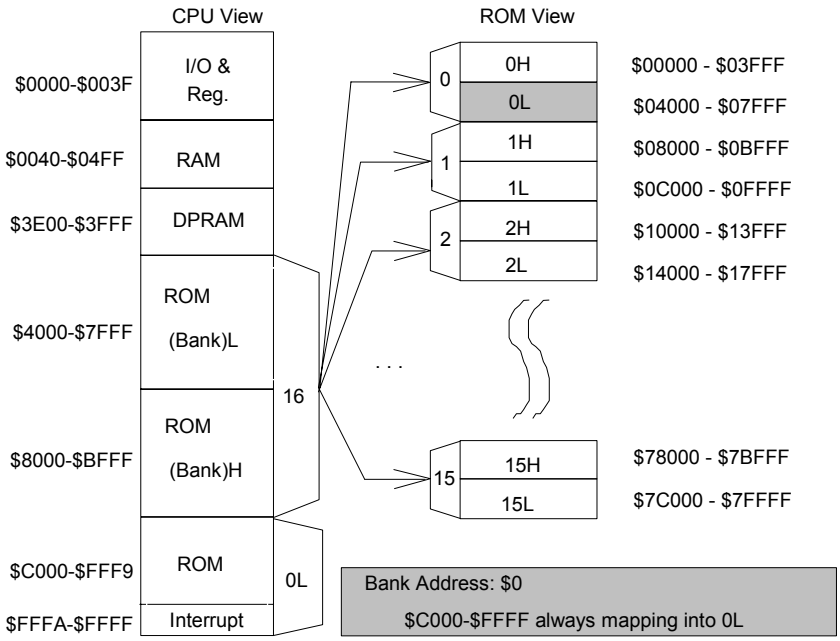
6.1. Memories

The GPLB38B contains 512K-byte ROM and 1216-byte SRAM.

6.2. Map of Memory and I/Os

*NMI SOURCE:
- LV DETECT
- TIMER1

*INT SOURCE:
- EXT INT
- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1



Note1: User program should start from $C800. $C000-$C7FF is the test program area.
Note2: User program interrupt vector: $FFFA ~ $FFFF
Note3: Test program interrupt vector: $FFF2 ~ $FFF7

6.3. Operation Modes

There are three operation modes involved in GPLB38B: standby, halt and operating. The following table shows the differences between these modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

6.4. Operating Mode

In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated. Generally speaking, this mode consumes the highest power.

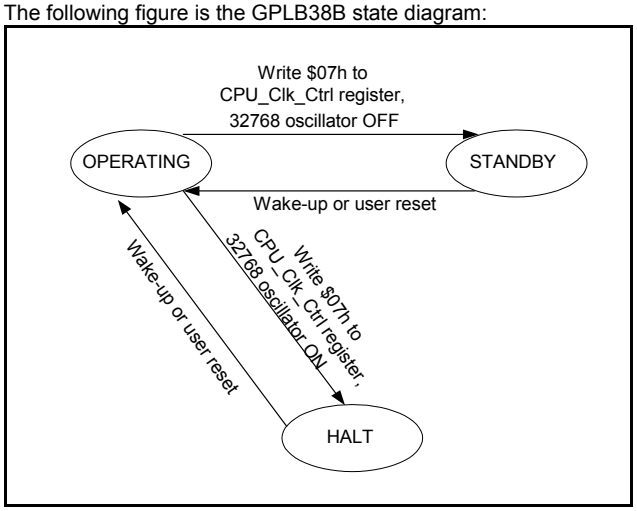
6.5. Standby Mode

The standby mode is a mode where the device is placed in its lowest current consumption state. In standby mode, all functions are turned off; in addition, RAM and I/Os will remain in their previous states.

6.6. Halt Mode

In halt mode, CPU clock halts and waits for an event (key press, timer overflow) to wake up. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode.

The following figure is the GPLB38B state diagram:



GPLB38B State Diagram

6.7. Speech and Melody

For speech synthesis, the GPLB38B provides several timer interrupts for a precise sampling frequency. The sound data can be stored into ROM and be played back. Several algorithms are recommended for high fidelity and good compression of sound such as PCM and ADPCM.

For melody synthesis, the GPLB38B provides a dual tone mode. Once in the dual tone mode, users only need to program the tone frequency for each channel by writing to the timer/counter TM0 and TM1, and set the envelope of each channel. The hardware will toggle the tone wave automatically.

6.8. LCD Controller/Driver

The GPLB38B contains a 1024-dot LCD controller/driver. Programmers are able to define the LCD configuration by setting up the LCD Control Register. Once the LCD configuration is completed, the desired pattern can be displayed by filling the LCD buffer with proper data. The LCD driver can also operate during sleep by keeping 32768 oscillator running. The LCD driver in GPLB38B supports 1/16 duty and 1/5 bias.

6.9. LCD Voltage Generation

The GPLB38B offers a voltage regulator and a charge-pumping circuit. The voltage regulator provides a reference voltage for the charge-pumping circuit to generate V_{LCD}. Users can get the desired V_{LCD} by changing the output reference voltage (writing to register) of the voltage regulator. Enabling the voltage regulator and charge-pumping circuit gets a stable V_{LCD} that will not be affected by VDD. The V_{LCD} is adjustable from 2.98V to 5.75V in 1/5 bias.

6.10. Audio Output

Internally, the GPLB38B supports PWM audio output. The GPLB38B has a pair of PWM drivers, supporting two sound channels. Each channel is able to play speech or tone individually. The PWM drivers can directly drive speaker or buzzer without buffer or amplification circuit.

6.11. Low Voltage Detection

The GPLB38B provides a 6-level (software programmable) low voltage detector to detect a low voltage event. Users can turn on the low detection to monitor VDD periodically to check if it is lower than the given value. In addition, if LV NMI is enabled, a NMI will be issued to notify CPU if power voltage drops below the given value. Also, the voltage detector will generate a system reset if power supply voltage drops below 2.2V.

6.12. Key Scan Function

GPLB38B supports key scan function. The LCD driver will generate a key strobe signal in the period of every common. When PA receives this strobe signal, a wake-up is issued. Then, program can send the key scan signal through SEG [15:0] to determine the location of the depressed key.

6.13. Watchdog Timer (WDT)

An on-chip watchdog timer is also available in the GPLB38B. The WDT is designed to recover the system from abnormal operation. In some cases, if WDT is not cleared for one second, the WDT will generate a system reset to restart system. If WDT is enabled, the WDT should be cleared every 0.5 second to avoid accidental reset. The WDT can be cleared through software programming. Note that the WDT only works when 32768Hz clock is activated.

6.14. Mask Options

6.14.1. 32768 oscillator

1). X'TAL
2). R-oscillator

6.14.2. Watchdog timer

1). Enable
2). Disable

6.14.3. Low voltage reset

1). Enable
2). Disable

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to + 60℃
Storage Temperature	T_{STO}	-50℃ to + 150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

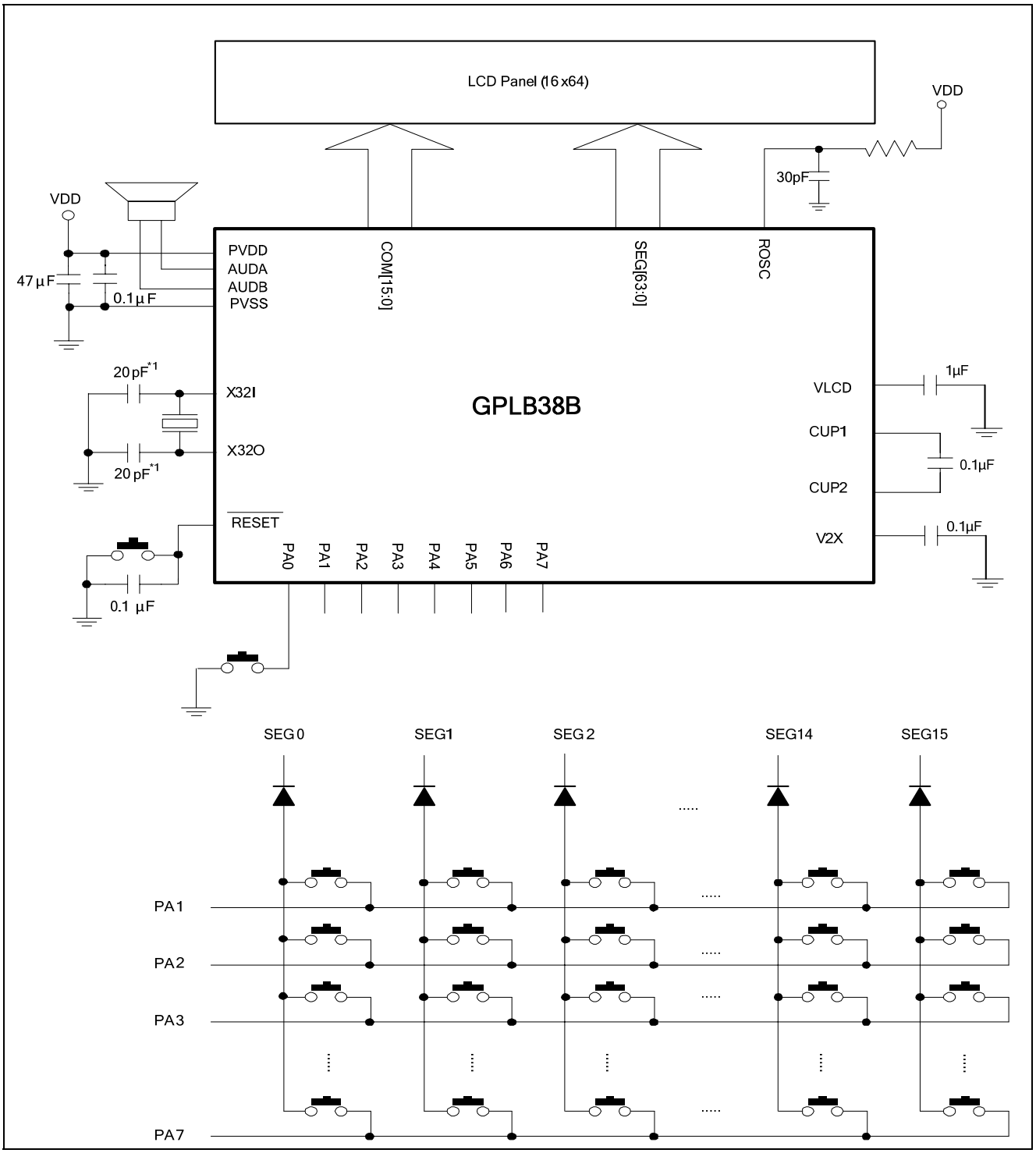
7.2. DC Characteristics(T_A=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1.2	-	mA	F_{CPU} = 2.0MHz @ 3.0V F_{OSC} = 8.0MHz, no load
Halt Current	I_{HALT}	-	30	45	μA	VDD = 3.0V, 32K X'TAL ON, LCD ON, no LCD panel
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, all off
Audio Output Current (PWM)	I_{OH}	-	-20	-	mA	VDD = 3.0V, V_{OH} = 2.5V
		-	-40	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Audio Output Current (PWM)	I_{OL}	-	20	-	mA	VDD = 3.0V, V_{OL} = 0.5V
		-	40	-	mA	VDD = 3.0V, V_{OL} = 1.0V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (I/O)	I_{OH}	-1.0	-	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (I/O)	I_{OL}	1.0	-	-	mA	VDD = 3.0V, V_{OL} = 0.8V
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	2.98	-	5.75	V	VDD = 3.0V, 1/5 bias, no load
OSC Resistor	R_{OSC}	-	32K	-	Ω	F_{OSC} = 8.0MHz @ 3.0V
CPU Clock	F_{CPU}	-	-	7.0	MHz	F_{CPU} = F_{OSC}/1 @ 2.2~2.4V
		-	-	8.0	MHz	F_{CPU} = F_{OSC}/1 @ 2.4~3.6V

Note: V_{LCD} should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

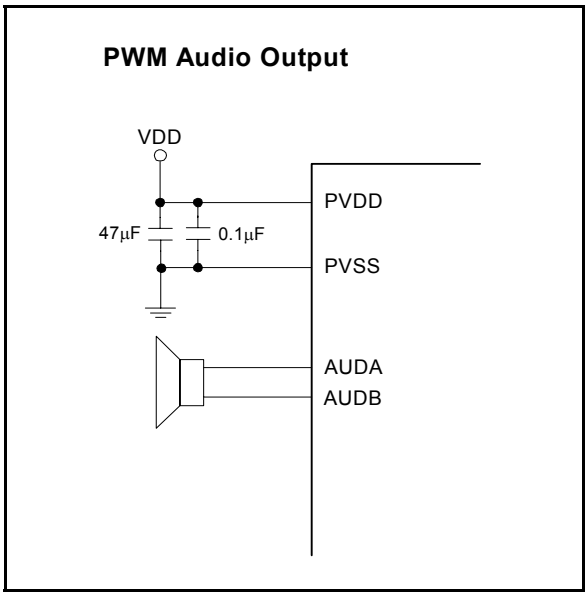
8. APPLICATION CIRCUITS

8.1. 1024 Dots LCD Driver, 64 Segments × 16 Commons, 1/5 Bias - (1)



Note*1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8.2. Audio Output Connections - (2)



9. PACKAGE/ORDERING INFORMATION

9.1. Ordering Information

Product Number	Package Type
GPLB38B-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
MAY 10, 2010	1.3	Modify 2. FEATURES.	3
AUG.15, 2008	1.2	1. Modify 5. SIGNAL DESCRIPTION. 2. Modify 5.1 Pad Assignment.	4 5
NOV. 30, 2007	1.1	1. Modify DC characteristics of max. halt mode current. 2. Modify diagram of section 8.1.	7 9
AUG. 07, 2007	1.0	1. Modify Features: (1) Modify max. operating frequency to 8MHz. (2) Modify “8 wake-up source” to “5 wake-up source”. (3) Modify “32-level LCD contrast control level” to “27-level LCD contrast control level”. (4) Modify operation current “600uA @ FOSC=4.0MHz” to “1.2mA @ FOSC=8.0MHz”. (5) Modify I/Os from “PA[0:7],PB[0:3]” to “PA[0:7], PC[4:7]”. 2. Modify block diagram, “PC[3:0]” to “PC[7:4]”. 3. Modify signal description table: “PIN Number” 4. Modify DC characteristic stable: (1) Modify operation current “600uA @ FOSC=4.0MHz” to “1.2mA @ FOSC=8.0MHz”. (2) Modify ROSC resistor from “180K” to “32K”. 5. Add pad diagram.	3 3 4 7 10
JUN. 13, 2007	0.2	1. Remove serial interface description. 2. Remove INT source of UART.	5
DEC. 5, 2006	0.1	Original	