DATA SHEET

GPLB38C

1024 dots LCD Controller with 512KB ROM

Jun. 26, 2017

Version 1.5

Table of Contents

PAGE

1024 DOTS LCD CONTROLLER WITH 512KB ROM

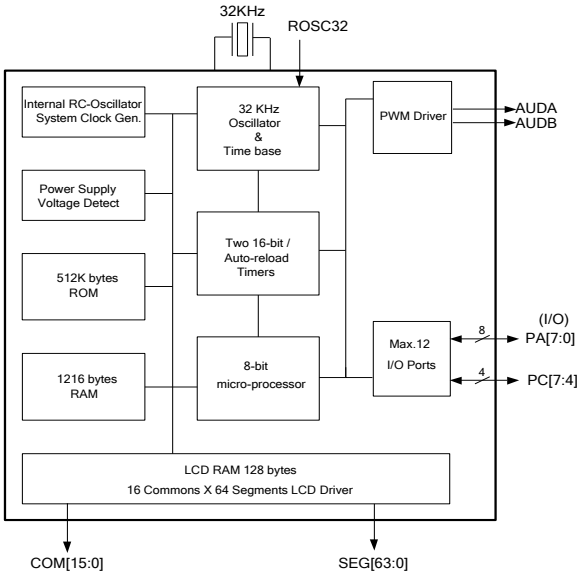
1. GENERAL DESCRIPTION

GPLB38C, an 8-bit CMOS microprocessor for LCD handheld application, contains 1216 bytes working RAM, 512K bytes ROM, 12 I/Os, interrupt/wakeup controller, and automatic display controller/driver for LCD. It also features one PWM driver with two audio channels to produce attractive sound effects easily. Its large ROM area allows user to store both program and audio data in one place. In addition, a SLEEP (power-down) function is featured to extend battery life.

2. FEATURES

- Built-in 8-bit processor
  - **1216 bytes SRAM**
  - **512K bytes ROM**
  - Max. operating speed: 8.0MHz @ 2.4V – 5.5V
  - Programmable CPU clock: /1, /2, /4, /8, /16, /32, /64 of ROSC Frequency.
  - 5 wake-up sources
  - 5 interrupt sources
- Key scan function
  - SEG[15:0] can be used to send key scan output
- Programmable LCD driver
  - **64 segments, 16 commons, maximum 1024 dots**
  - 1/5 bias, 1/16 duty capability
  - **128 bytes dedicated LCD RAM**
  - Built-in voltage regulator to generate VLCD for LCD driver
  - 26-level contrast control (2.98V - 5.75V)
- Power saving SLEEP mode
- **Low Voltage Detector**
  - **6-level 2.9V - 2.4V detection**
- Low power consumption:
  - 1.2mA typical @ 3.0V, F_{CPU} = 2.0MHz, F_{OSC} = 8.0MHz
  - 30uA typical halt current @ 3.0V
  - <1uA typical standby current @ 3.0V
  - Watchdog timer for reliable operation
- Peripherals
  - **Dedicated I/Os: PA[0:7], PC[4:7]**
  - 32.768KHz oscillator circuit for RTC
  - Internal RC-oscillator (no resistor needed)
  - Two 16-bit reloadable timer/counters
  - **2-channel PWM audio outputs**
  - Watchdog Timer for reliable operation
- Wide operating voltage range:
  - 2.4V – 5.5V
- Built-in regulator
  - Internal built-in regulator to supply core power (3.3V, for 3-battery application). Also, it can turn off internal built-in regulator, and use external 3.6V power to supply core power (for 2-battery application.)

3. BLOCK DIAGRAM



4. APPLICATION FIELD

- Handheld game
- Scientific calculator
- Talking calculator, Talking clock
- Talking instrument controller
- General speech synthesizer
- Data bank

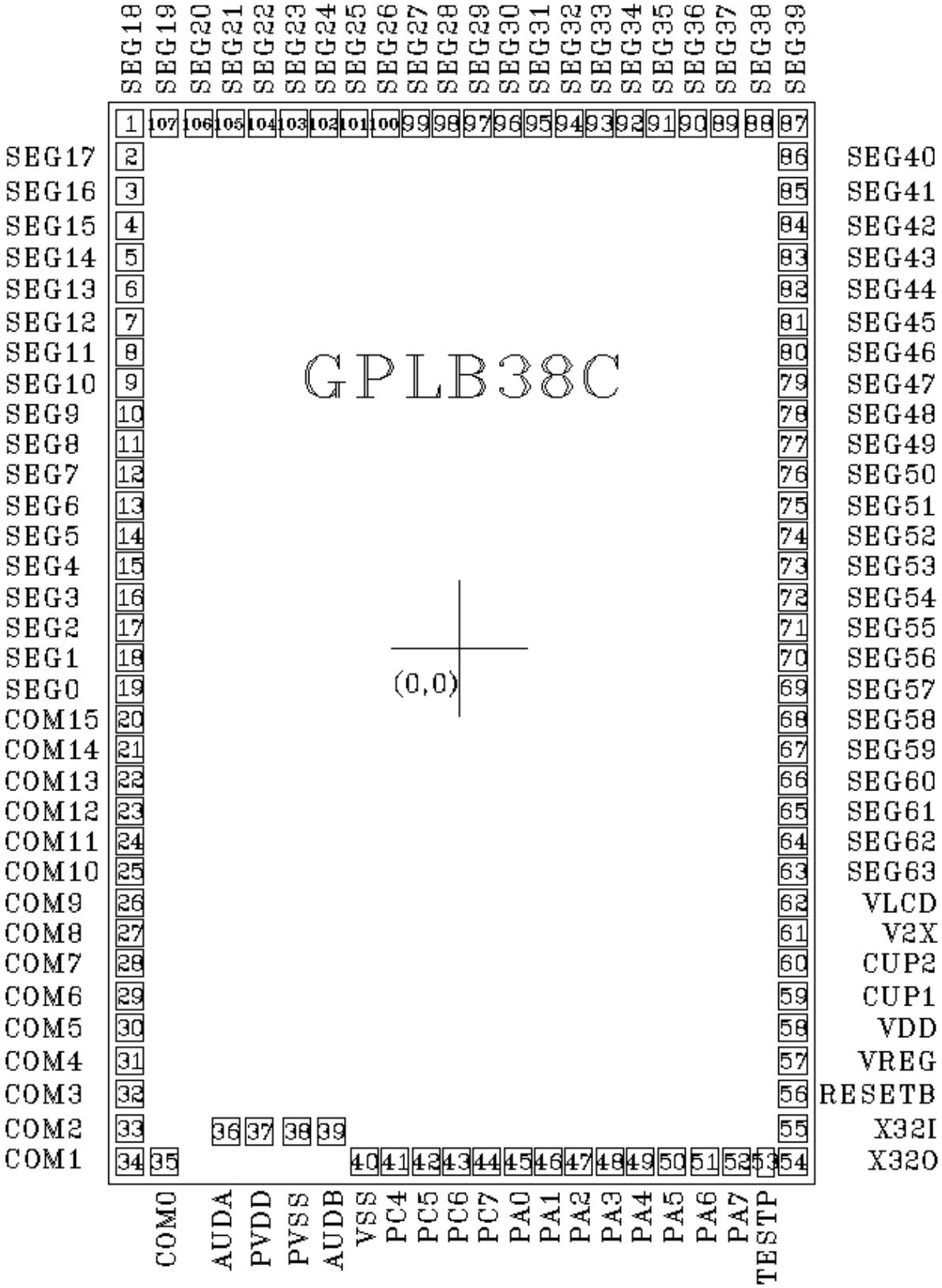
5. SIGNAL DESCRIPTIONS

Total: 107pins

Mnemonic	PIN No.	Type	Description
SEG63 - 0	1~19,63~107	O	LCD driver segment output.
COM15 - 0	20~35	O	LCD driver common output.
PA7 - 0	45~52	I/O	Port A is a bi-directional I/O port, which can be software programmed as wakeup I/O.
PC7 - 4	41~44	I/O	Port C is a bi-directional I/O port
RESETB	56	I	System reset input, low active.
AUDA, AUDB	36,39	O	PWM audio output.
X32I	55	I	32.768KHz crystal input or connect to VREG through a resistor (option).
X32O	54	O	32.768KHz crystal output.
TESTP	53	I	Test input, high active.
CUP2 - 1	59,60	P	LCD voltage generation. Charge pump capacitor inter-connection pins.
V2X	61	P	Pump 2X output.
VLCD	62	P	LCD voltage generation.
VDD	58	P	Power supply voltage input.
VSS	40	P	Ground reference.
PVDD	37	P	PWM driver power.
PVSS	38	P	PWM driver ground reference.
VREG	57	P	Regulator out pin

Legend: I = Input, O = Output, P = Power

5.1. PAD Assignment



Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

6. FUNCTIONAL DESCRIPTIONS

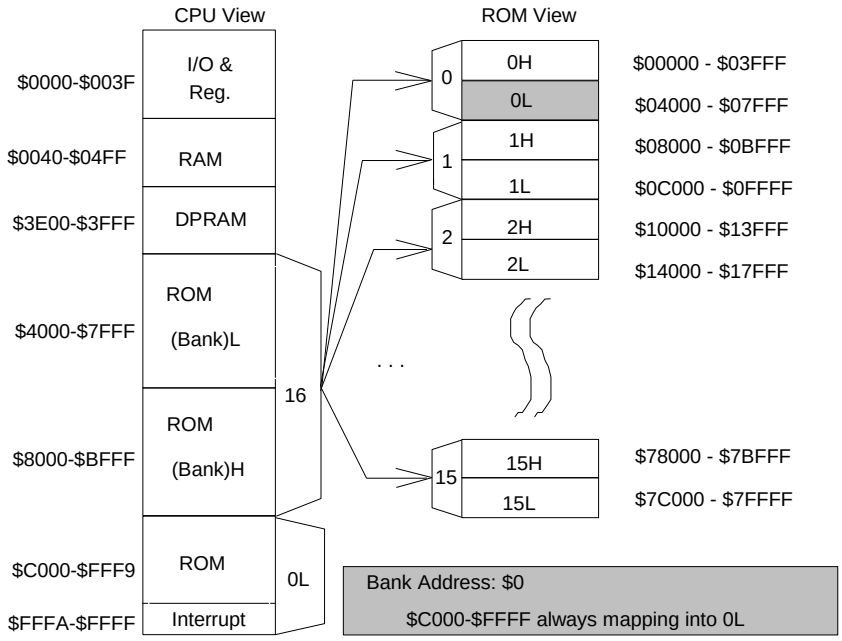
6.1. Memories

GPLB38C contains 512K-byte ROM and 1216-byte SRAM.

6.2. Map of Memory and I/Os

*NMI SOURCE:
- LV DETECT
- TIMER1

*INT SOURCE:
- EXT INT
- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1



Note1: User program should start from $C800. $C000-$C7FF is the test program area.
Note2: User program interrupt vector: $FFFA ~ $FFFF
Note3: Test program interrupt vector: $FFF2 ~ $FFF7

6.3. Operation Modes

There are three operation modes involved in GPLB38C: standby, halt and operating. The following table shows the differences among these modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

6.4. Operating Mode

In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated. Generally speaking, this mode consumes the highest power.

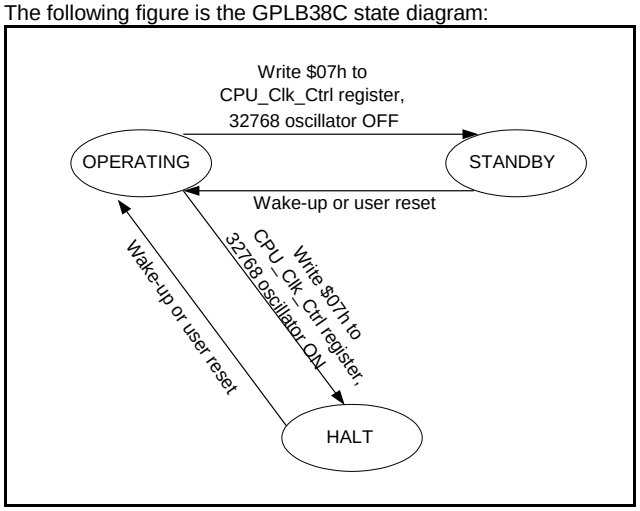
6.5. Standby Mode

The standby mode is a mode where the device is placed in its lowest current consumption state. In standby mode, all functions are turned off; in addition, RAM and I/Os will remain in their previous states.

6.6. Halt Mode

In halt mode, CPU clock halts and waits for an event (key press, timer overflow) to wake up. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode.

The following figure is the GPLB38C state diagram:



GPLB38C State Diagram

6.7. Speech and Melody

For speech synthesis, the GPLB38C provides several timer interrupts for a precise sampling frequency. The sound data can be stored into ROM and be played back. Several algorithms are recommended for high fidelity and good compression of sound such as PCM and ADPCM.

For melody synthesis, the GPLB38C provides a dual tone mode. Once in the dual tone mode, users only need to program the tone frequency for each channel by writing to the timer/counter TM0 and TM1, and set the envelope of each channel. The hardware will toggle the tone wave automatically.

6.8. LCD Controller/Driver

The GPLB38C contains a 1024-dot LCD controller/driver. Programmers are able to define the LCD configuration by setting up the LCD Control Register. Once the LCD configuration is completed, the desired pattern can be displayed by filling the LCD buffer with proper data. The LCD driver can also operate during sleep by keeping 32768Hz oscillator running. The LCD driver in GPLB38C supports 1/16 duty and 1/5 bias.

6.9. LCD Voltage Generation

The GPLB38C offers a voltage regulator and a charge-pumping circuit. The voltage regulator provides a reference voltage (V2x) for the charge-pumping circuit to generate V_{LCD}. Users can get the desired V_{LCD} by changing the output reference voltage (writing to register) of the voltage regulator. Enabling the voltage regulator and charge-pumping circuit gets a stable V_{LCD} that will not be affected by VDD. The V_{LCD} is adjustable from 2.98V to 5.75V.

6.10. Audio Output

Internally, the GPLB38C supports PWM audio output. The GPLB38C has a pair of PWM drivers, supporting two sound channels. Each channel is able to play speech or tone individually. The PWM drivers can directly drive speaker or buzzer without buffer or amplification circuit.

6.11. Low Voltage Detection

The GPLB38C provides a 6-level (software programmable) low voltage detector to detect a low voltage event. Users can turn on the low detection to monitor VDD periodically to check if it is lower than the given value. In addition, if LV NMI is enabled, a NMI will be issued to notify CPU if power voltage drops below the given value. Also, the voltage detector will generate a system reset if power supply voltage drops below 2.3V.

6.12. Key Scan Function

GPLB38C supports key scan function. The LCD driver will generate a key strobe signal in the period of every common. When PA receives this strobe signal, a wake-up is issued. Then, program can send the key scan signal through SEG [15:0] to determine the location of the depressed key.

6.13. Watchdog Timer (WDT)

An on-chip watchdog timer is also available in the GPLB38C. The WDT is designed to recover the system from abnormal operation. In some cases, if WDT is not cleared for one second, the WDT will generate a system reset to restart system. If WDT is enabled, the WDT should be cleared every 0.5 seconds to avoid accidental reset. The WDT can be cleared through software programming. Note that the WDT only works when 32768Hz clock is activated.

6.14. Mask Options

6.14.1. 32768Hz oscillator

1). X'TAL
2). R-oscillator

6.14.2. Watchdog timer

1). Enable
2). Disable

6.14.3. Internal oscillator frequency

1). 8MHz
2). 4MHz

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to + 60℃
Storage Temperature	T_{STO}	-50℃ to + 150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD=3.0V, for 2-battery application, internal regulator disable, T_A =25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1.2	2.5	mA	F_{CPU} = 2.0MHz @ 3.0V F_{OSC} = 8.0MHz, no load
Halt Current	I_{HALT}	-	30	60	uA	VDD = 3.0V, 32K X'TAL ON, Strobe off LCD ON, 1/5 bias, VLCD=5.75V, no LCD panel
Standby Current	I_{STBY}	-	0.6	1.0	uA	VDD = 3.0V, all off
PWM Driver Current	I_{PWM}	-	100	-	mA	VDD = 3.0V, 8 Ohms load
Input High Level	V_{IH}	0.7*VDD	-	VDD	V	VDD = 3.0V
Input Low Level	V_{IL}	0	-	0.3*VDD	V	VDD = 3.0V
Output High Current (I/O)	I_{OH}	2.0	2.6	3.3	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (I/O)	I_{OL}	3.0	4.0	5.0	mA	VDD = 3.0V, V_{OL} = 0.8V
Input Pull-Low Resistor						
PA	R_{PL1}	90	180	270	KΩ	VDD=3.0V
PC4~PC7	R_{PL2}	35	70	105	KΩ	VDD=3.0V
Input Pull_high Resistor						
PA	R_{PH1}	150	300	450	KΩ	VDD=3.0V
PC4~PC7	R_{PH2}	45	90	135	KΩ	VDD=3.0V
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	2.98	-	5.75	V	VDD = 3.0V, no load
OSC32K Resistor	R_{OSC32K}	-	6.2	-	MΩ	F_{OSC32K}=32768Hz@3.0V
CPU Clock	F_{CPU}	-	-	8	MHz	F_{CPU}=F_{OSC}/2@2.4V

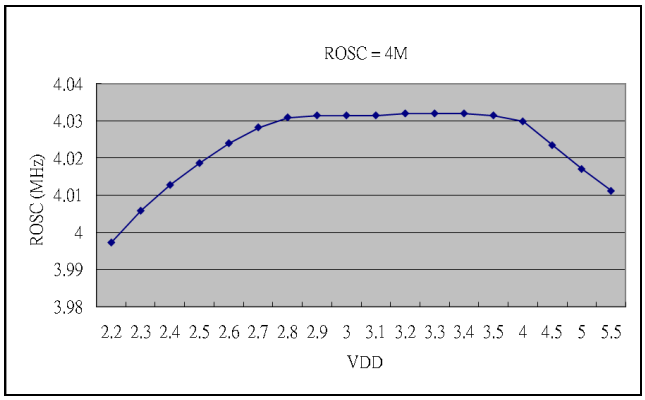
7.3. DC Characteristics (VDD=4.5V, for 3-battery application, internal regulator enable, T_A =25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.7	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	1.5	3.0	mA	F_{CPU} = 2.0MHz @ 4.5V F_{OSC} = 8.0MHz, no load
Halt Current	I_{HALT}	-	40	80	uA	VDD = 4.5V, 32K X'TAL ON, LCD ON, no LCD panel
Standby Current	I_{STBY}	-	3.0	4.0	uA	VDD = 4.5V, all off
PWM Driver Current	I_{PWM}	-	200	-	mA	VDD = 4.5V, 8 Ohms load
Input High Level	V_{IH}	0.7*VDD	-	VDD	V	VDD = 4.5V

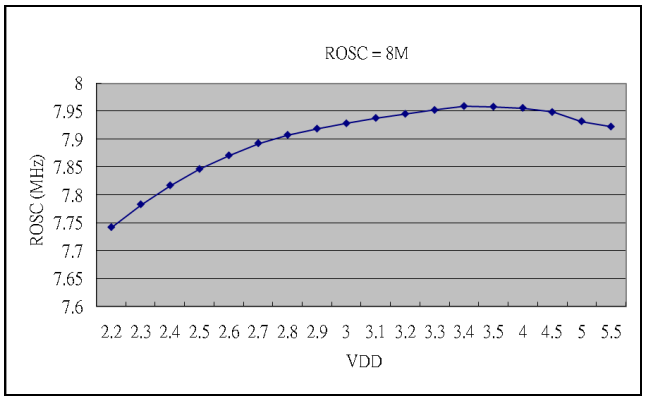
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Low Level	V_{IL}	0	-	0.3*VDD	V	VDD = 4.5V
Output High Current (I/O)	I_{OH}	4.0	5.4	6.8	mA	VDD = 4.5V, V_{OH} = 3.6V
Output Sink Current (I/O)	I_{OL}	3.6	4.8	6.0	mA	VDD = 4.5V, V_{OL} = 0.9V
Input Pull-Low Resistor						
PA	R_{PL1}	100	200	300	KΩ	VDD=4.5V
PC4~PC7	R_{PL2}	40	80	120	KΩ	VDD=4.5V
Input Pull_high Resistor						
PA	R_{PH1}	90	180	270	KΩ	VDD=4.5V
PC4~PC7	R_{PH2}	30	60	90	KΩ	VDD=4.5V
LCD Driver Voltage(V_{LCD} - VSS)	V_{LCD}	4.47	-	5.75	V	VDD = 4.5V, no load
OSC32K Resistor	R_{OSC32K}	-	6.2	-	MΩ	F_{OSC32K}=32768Hz@4.5V
CPU Clock	F_{CPU}	-	-	8	MHz	$F_{CPU}=F_{OSC}/2$@2.7V
Regulator voltage	Vreg	3.15	3.3	3.45	V	
Regulator dropout voltage	Vdrop	-	-	100	mV	VDD=2.4v, iout=15mA,
Regulator Max. output current	Imax	-	-	30	mA	VDD = 4.5V

Note: V_{LCD} should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

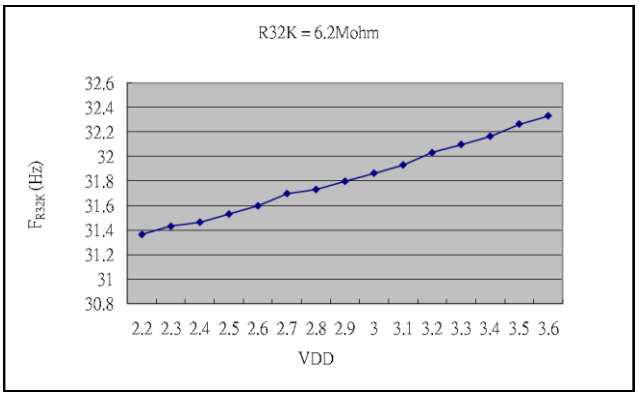
7.4. The Relationships between the F_{osc4M} and the VDD



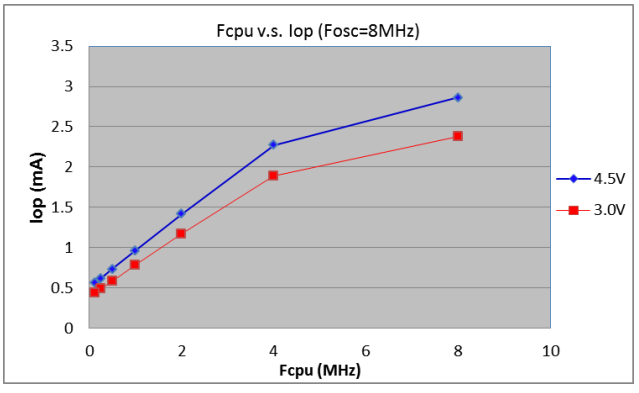
7.5. The Relationships between the F_{osc8M} and the VDD



7.6. The Relationships between the F_{osc32k} and the VDD

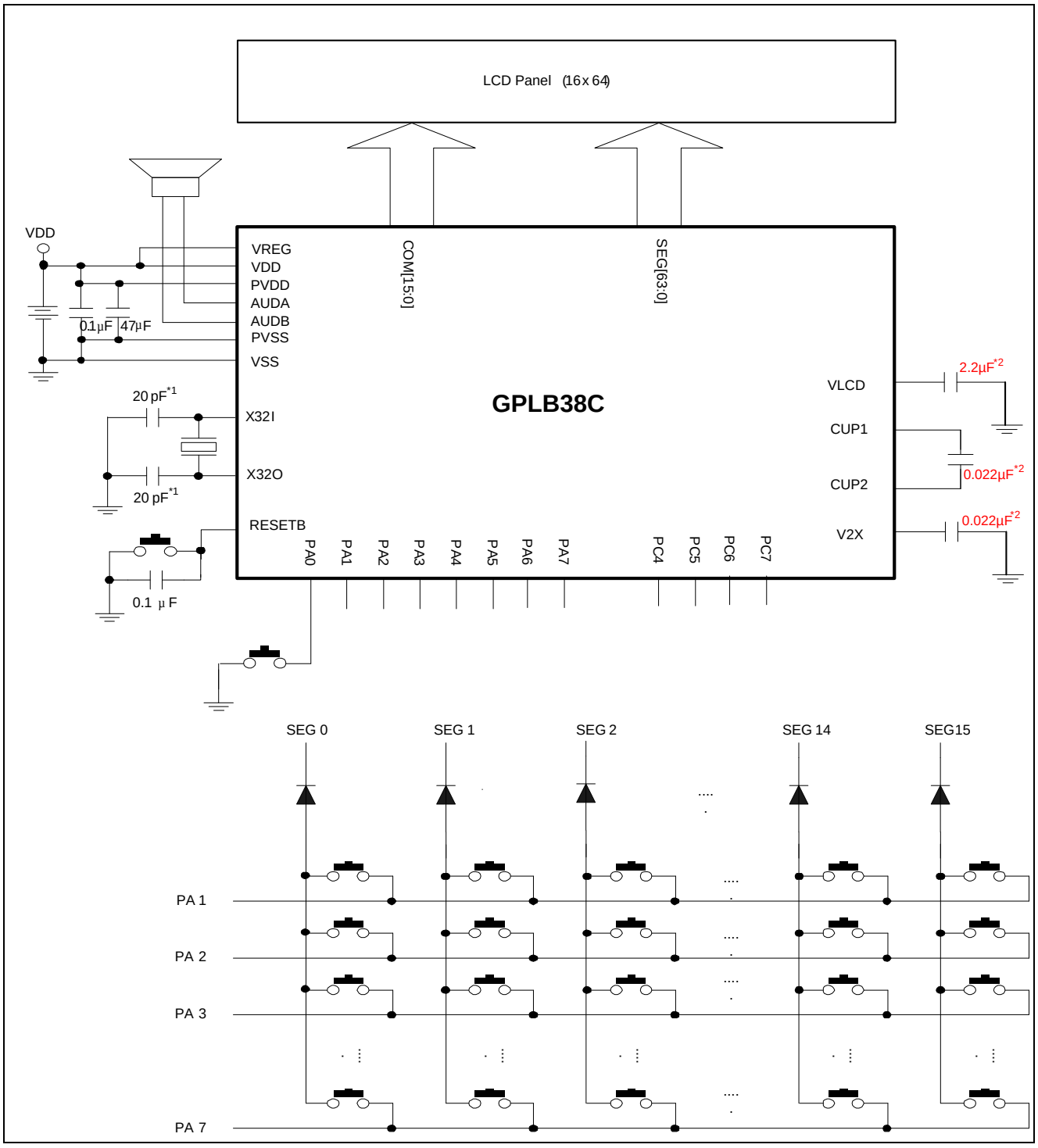


7.7. The Relationships between the F_{CPU} and the Iop



8. APPLICATION CIRCUITS

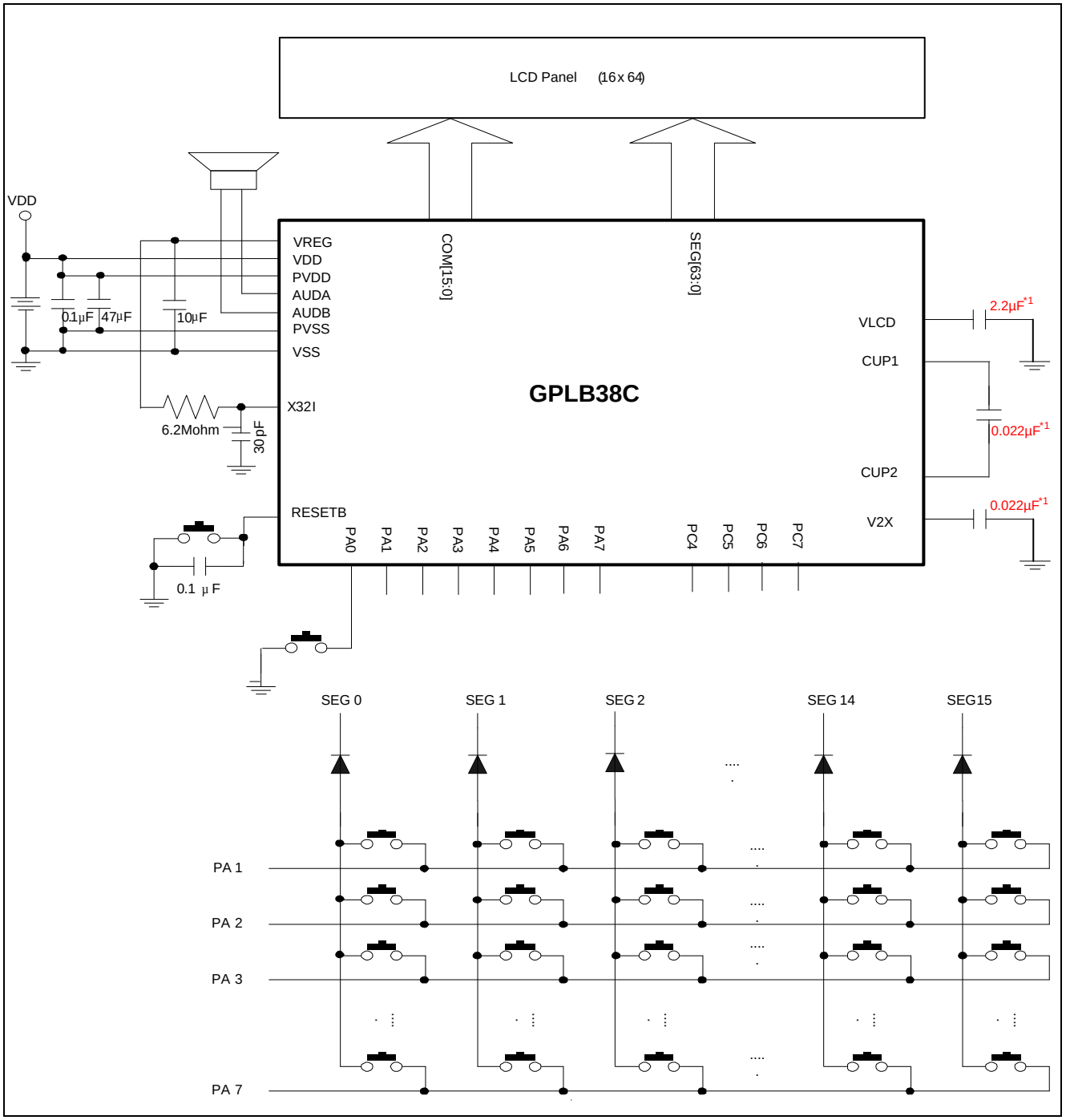
8.1. 1024 Dots LCD Driver, 64 Segments × 16 Commons, 2-battery application, internal regulator disabled, Xtal 32K selected (1)



Note*1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*2: The LCD pump and VLCD capacitors are suggested using 0.022uF and 2.2uF for small or light loading of LCD panel, and 0.047uF and 2.2uF for large or heavy loading of LCD panel.

8.2. 1024 Dots LCD Driver, 64 Segments × 16 Commons, 3-battery application, internal regulator enabled, Rosc32K selected (2)



Note*1: The LCD pump and VLCD capacitor are suggested using 0.022uF and 2.2uF for small or light loading of LCD panel, and 0.047uF and 2.2uF for large or heavy loading of LCD panel.

9. PACKAGE INFORMATION

9.1. Ordering Information

Product Number	Package Type
GPLB38C-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Generalplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. GENERALPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, GENERALPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. GENERALPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by GENERALPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

11. REVISION HISTORY

Date	Revision #	Description	Page
Jun. 26, 2017	1.5	1. Modified DC characteristics in section 7.2, 7.3. 2. Add “The Relationships between the FCPU and the Iop” in section7.7.	9 10
Jul 31, 2014	1.4	1. Modified features 2. Modified DC characteristics	3 8
DEC. 20, 2013	1.3	Modified LCD pump capacitor of Application circuit in section 8.1&8.2;	10~11
APR. 7, 2012	1.2	1.Modified Application circuit in section 8.2； 2.PAD assignment in section 9.1 removed；	11 12
SEP. 29, 2010	1.1	1.Modified features; 2.Add “Vdrop” & “Imax” of Regulator in section7.3; 3.Add relationship waveform of Frequency vs VDD in section 7.4, 7.5 & 7.6; 4.Modified Application circuit in section 8.1 & 8.2	3 8 9 10~11
APR. 28, 2010	1.0	1.Modified features; 2.Modified Signal description; 3.Modified Functional description; 4.DC characteristics; 5. Add “Pad Assignment and Locations” to section 9.1.	3 4 6 7 10
Jul. 8, 2009	0.1	Original	12