DATA SHEET

# GPLB52640A
# GPLB52320A
# GPLB51640A
# GPLB51320A

## 1000/2000 Dots Mono/4-Gray-Level LCD Controller/Driver with 8-CH SPU

Sep 12, 2013

Version 2.2

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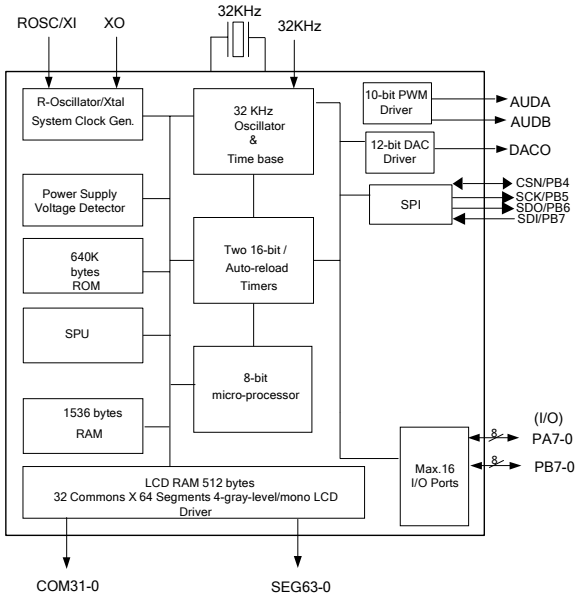
# 1000/2000 DOTS MONO/4-GRAY-LEVEL LCD CONTROLLER/DRIVER WITH 8CH SPU

## 1. GENERAL DESCRIPTION

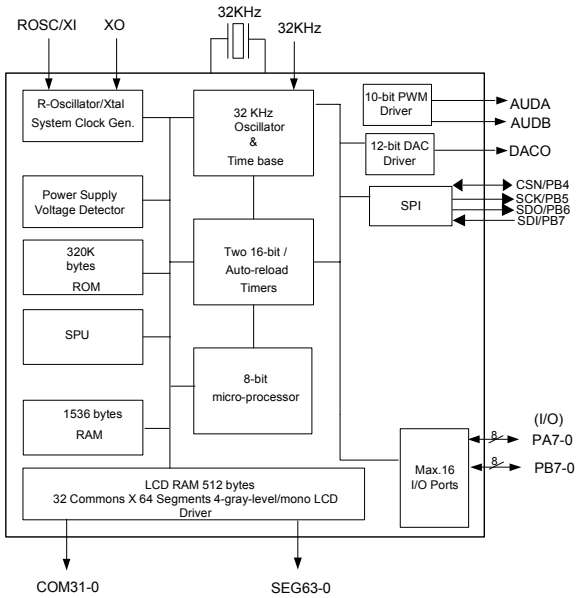
The GPLB52640A/GPLB52320A/GPLB51640A/GPLB51320A, an 8-bit CMOS microprocessor, contain 1536 bytes working RAM, 16 I/Os, interrupt/wakeup controller, two 16-bit timers, SPI interface, one 12-bit DAC, one 10-bit PWM, and automatic display controller/driver for mono/4-gray-level LCD. The GPLB52640A/ GPLB51640A contains 640K bytes ROM memory and the GPLB52320A/GPLB51320A features 320K bytes ROM memory. The GPLB52640A/GPLB52320A contains up to 64 segments and 32 commons, forming a maximum of 2048 dots LCD resolution, and the GPLB51640A/GPLB51320A has up to 74 segments and 22 commons, forming a maximum of 1628 dots LCD. The microprocessor can implement software for audio processing, functional control and others. For audio processing, melody and speech can be mixed into one output. The GPLB52640A/ GPLB52320A/ GPLB51640A/ GPLB51320A implement a high performance SPU voice engine to achieve 8-channel voice with ADPCM/PCM data. It operates over a wide voltage range from 2.4V through 5.5V and a Low Voltage Reset function to assure CPU operation properly under a low voltage condition. It also features one 10-bit PWM driver and one 12-bit DAC with 8 audio channels to produce attractive sound effects easily. Its large ROM area can be used to store both program and audio data. There is a Serial Peripheral Interface (SPI) controller built-in to facilitate communicating with other devices. Furthermore, a SLEEP (power-down) function is also built-in to extend battery life. The GPLB52640A/ GPLB52320A/ GPLB51640A/ GPLB51320A are designed with state-of-the-art technology to fulfill LCD application needs, especially for hand-held products.

## 2. BLOCK DIAGRAM

### 2.1. GPLB52640A




### 2.2. GPLB52320A



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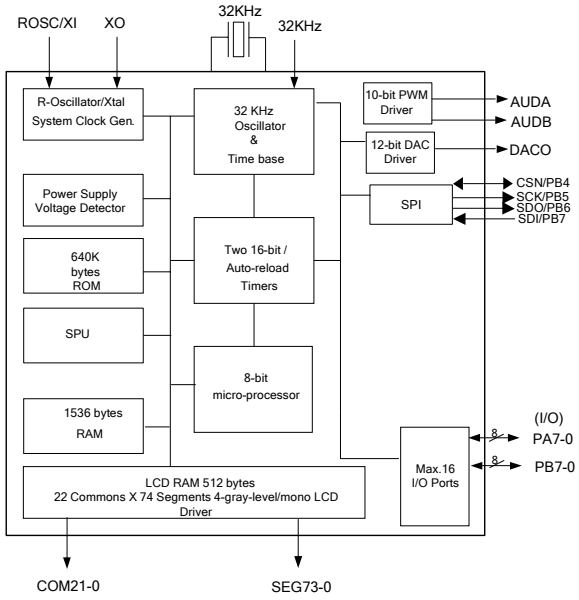
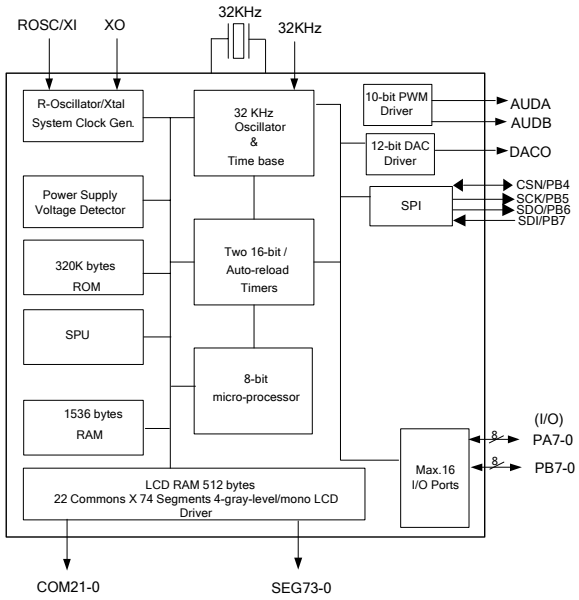



### 2.4. GPLB51320A




## 3. FEATURES

- 8-bit micro-processor
- **1536 bytes SRAM**
- **ROM Size Table:**

| | GPLB52640A | GPLB52320A | GPLB51640A | GPLB51320A |
|---|---|---|---|---|
| **ROM Size** | 640K bytes | 320K bytes | 640K bytes | 320K bytes |

- Operating voltage: 2.4V – 5.5V
- Max. CPU operating speed:
  - 8.0MHz @ 2.4V with 16MHz X'TAL
  - 8.0MHz @ 2.4V with 16MHz ROSC
- Programmable CPU clock: /2, /4, /8, /16, /32, /64 and /128 R-oscillator clock frequency
- Six wake-up sources
- Nine IRQ & two NMI Interrupts
- Internal built-in regulator to supply core power (3.3V, for 3-battery application). Also it can turn off internal built-in regulator, and use external 3.6V power to supply core power (for 2-battery application).
- Programmable LCD driver
  - **LCD Size Table:**

| | GPLB52640A | GPLB52320A | GPLB51640A | GPLB51320A |
|---|---|---|---|---|
| **Segment** | 64 | 64 | 74 | 74 |
| **Common** | 32 | 32 | 22 | 22 |
| **LCD Dots** | 2048 | 2048 | 1628 | 1628 |

  - 4-gray-level or mono LCD, 1/3, 1/4, 1/5, 1/6, 1/7 bias capability
  - Supports from 1/2 duty up to 1/32 duty
  - 512 bytes dedicated LCD RAM
  - Supports normal type-B & type-C LCD waveform with or without key scan
  - Built-in voltage regulator to generate VLCD for LCD driver
  - 32-level contrast control (VLCD=2.95V~6.85V)
  - Power saving SLEEP mode
- **Low Voltage Detector**
  4-level (2.4V/2.6V/3.0V/3.3V) voltage detector
- **2.2V Low Voltage Reset**
- Peripherals
  - Max. 16 I/O pins (PA[7:0], PB[7:0])
  - Built-in 32.768KHz oscillator circuit for real time clock function (X'tal or R-osc)
  - Built-in R-oscillator for system operating clock (X'tal or R-osc)
  - Internal time base generator
  - Two 16-bit reloadable timer/counters
  - Watchdog timer
  - **12-bit DAC output and 10-bit PWM audio outputs**
  - Key scan function
  - SEG[15:0] can be used to send key scan output
  - IR carrier output
  - One SPI serial interface I/O
- Powerful 8-ch Sound Processing Unit (SPU)
  - Variable tone-color sampling rate: maximum 54KHz@CPU_Clock=7MHz
  - 8-voice polyphony

- Supports PCM/ADPCM tone-color table

## 4. APPICATION FIELD

- Handheld LCD game
- Educational toys (Electronic Learning Aid)
- Data bank
- Dictionary
- Translator

## 5. SIGNAL DESCRIPTIONS

### 5.1. GPLB52640A/GPLB52320A

| Mnemonic | PIN No. | Type | Description |
|---|---|---|---|
| SEG63 – 55<br>SEG54 – 0 | 131-139<br>1-55 | O | LCD driver segment output. SEG15 - 0 share pin with key scan port. |
| COM22 – 31 | 121-130 | O | LCD driver common output. |
| COM21 – 16<br>COM15 – 0 | 120-115<br>56-71 | O | LCD driver common output. |
| PA7 – 0 | 92-85 | I/O | PA7-0 is a bi-directional I/O port, which can be software programmed as wake up I/O. |
| PB0/ECLK | 77 | I/O | PB0 is shared pin with external timer clock input ECLK. |
| PB1/EXTI | 78 | I/O | PB1 is shared pin with external timer clock input EXTI. |
| PB2 | 79 | I/O | PB2 is a bi-directional I/O port. |
| PB3 | 80 | I/O | PB3 is shared pin with IR carrier output IRO. |
| PB4/SPI_CSN | 81 | I/O | PB4 is shared pin with SPI chip select SPI_CSN. |
| PB5/SCK | 82 | I/O | PB5 is shared pin with SPI clock output SCK. |
| PB6/SDO | 83 | I/O | PB6 is shared pin with SPI data output SDO. |
| PB7/SDI | 84 | I/O | PB7 is shared pin with SPI data input SDI. |
| ROSC/XI | 97 | I | Crystal input or ROSC input, connect to VDD (3V) through a resistor (option). |
| XO | 96 | O | Crystal output. |
| RESETB | 99 | I | System reset input, low active. |
| AUDA, AUDB | 76, 73 | O | PWM audio output. |
| DACO | 72 | O | DAC output. |
| X32I | 100 | I | 32.768KHz crystal input or connects to VDD (3V) through a resistor (option). |
| X32O | 101 | O | 32.768KHz crystal output. |
| TEST | 102 | I | Test input. Reserved for Generalplus testing. |
| CAP1P, CAP1N | 105, 106 | P | LCD voltage generator. Charge pump capacitor interconnection pins. |
| CAP2P, CAP2N | 107, 108 | P | LCD voltage generator. Charge pump capacitor interconnection pins. |
| VOUT | 109 | P | LCD voltage generator. Voltage generated by charge pump. |
| V4 | 111 | P | LCD voltage generator. |
| V3 | 112 | P | LCD voltage generator. |
| V2 | 113 | P | LCD voltage generator. |
| V1 | 114 | P | LCD voltage generator. |
| VLCD | 110 | P | LCD voltage generator. The highest voltage for LCD display. |
| VDD5V | 94 | P | Positive supply for regulator input. |
| VSSO | 93 | P | Ground for regulator. |
| VDDA | 104 | P | Power for Charge pump and IO pins. |
| VSSA | 103 | P | Ground for Charge pump and IO pins. |
| VDD | 95 | P | 3.3V power output from regulator. Regulator can be turned off when external 3.3V is supplied. |
| VSS | 98 | P | Ground reference for logic. |
| PVDD | 75 | P | Positive supply for PWM driver. |
| PVSS | 74 | P | Ground reference for PWM driver. |

Legend: I = Input, O = Output, P = Power

### 5.2. GPLB51640A/GPLB51320A

| Mnemonic | PIN No. | Type | Description |
|---|---|---|---|
| SEG63 – 55<br>SEG54 – 0 | 131-139<br>1-55 | O | LCD driver segment output. SEG15 - 0 share pin with key scan port. |
| SEG73 – 64 | 121-130 | O | LCD driver segment output. |
| COM21 – 16<br>COM15 – 0 | 120-115<br>56-71 | O | LCD driver common output. |
| PA7 – 0 | 92-85 | I/O | PA7-0 is a bi-directional I/O port, which can be software programmed as wake up I/O. |
| PB0/ECLK | 77 | I/O | PB0 is shared pin with external timer clock input ECLK. |
| PB1/EXTI | 78 | I/O | PB1 is shared pin with external timer clock input EXTI. |
| PB2 | 79 | I/O | PB2 is a bi-directional I/O port. |
| PB3 | 80 | I/O | PB3 is shared pin with IR carrier output IRO. |
| PB4/SPI_CSN | 81 | I/O | PB4 is shared pin with SPI chip select SPI_CSN. |
| PB5/SCK | 82 | I/O | PB5 is shared pin with SPI clock output SCK. |
| PB6/SDO | 83 | I/O | PB6 is shared pin with SPI data output SDO. |
| PB7/SDI | 84 | I/O | PB7 is shared pin with SPI data input SDI. |
| ROSC/XI | 97 | I | Crystal input or ROSC input, connect to VDD (3V) through a resistor (option). |
| XO | 96 | O | Crystal output. |
| RESETB | 99 | I | System reset input, low active. |
| AUDA, AUDB | 76, 73 | O | PWM audio output. |
| DACO | 72 | O | DAC output. |
| X32I | 100 | I | 32.768KHz crystal input or connects to VDD (3V) through a resistor (option). |
| X32O | 101 | O | 32.768KHz crystal output. |
| TEST | 102 | I | Test input. Reserved for Generalplus testing. |
| CAP1P, CAP1N | 105, 106 | P | LCD voltage generator. Charge pump capacitor interconnection pins. |
| CAP2P, CAP2N | 107, 108 | P | LCD voltage generator. Charge pump capacitor interconnection pins. |
| VOUT | 109 | P | LCD voltage generator. Voltage generated by charge pump. |
| V4 | 111 | P | LCD voltage generator. . |
| V3 | 112 | P | LCD voltage generator. . |
| V2 | 113 | P | LCD voltage generator. . |
| V1 | 114 | P | LCD voltage generator. . |
| VLCD | 110 | P | LCD voltage generator. The highest voltage for LCD display. |
| VDD5V | 94 | P | Positive supply for regulator input. |
| VSSO | 93 | P | Ground for regulator. |
| VDDA | 104 | P | Power for charge pump and IO pins. |
| VSSA | 103 | P | Ground for Charge pump and IO pins. |
| VDD | 95 | P | 3.3V power output from regulator. Regulator can be turned off when external 3.3V is supplied. |
| VSS | 98 | P | Ground reference for logic. |
| PVDD | 75 | P | Positive supply for PWM driver. |
| PVSS | 74 | P | Ground reference for PWM driver. |

Legend: I = Input, O = Output, P = Power

# 6. FUNCTIONAL DESCRIPTIONS

## 6.1. Memories

The GPLB52640A and GPLB51640A contain 640K-byte ROM and 1536-byte SRAM.

The GPLB52320A and GPLB51320A contain 320K-byte ROM and 1536-byte SRAM.

## 6.2. Map of Memory and I/Os

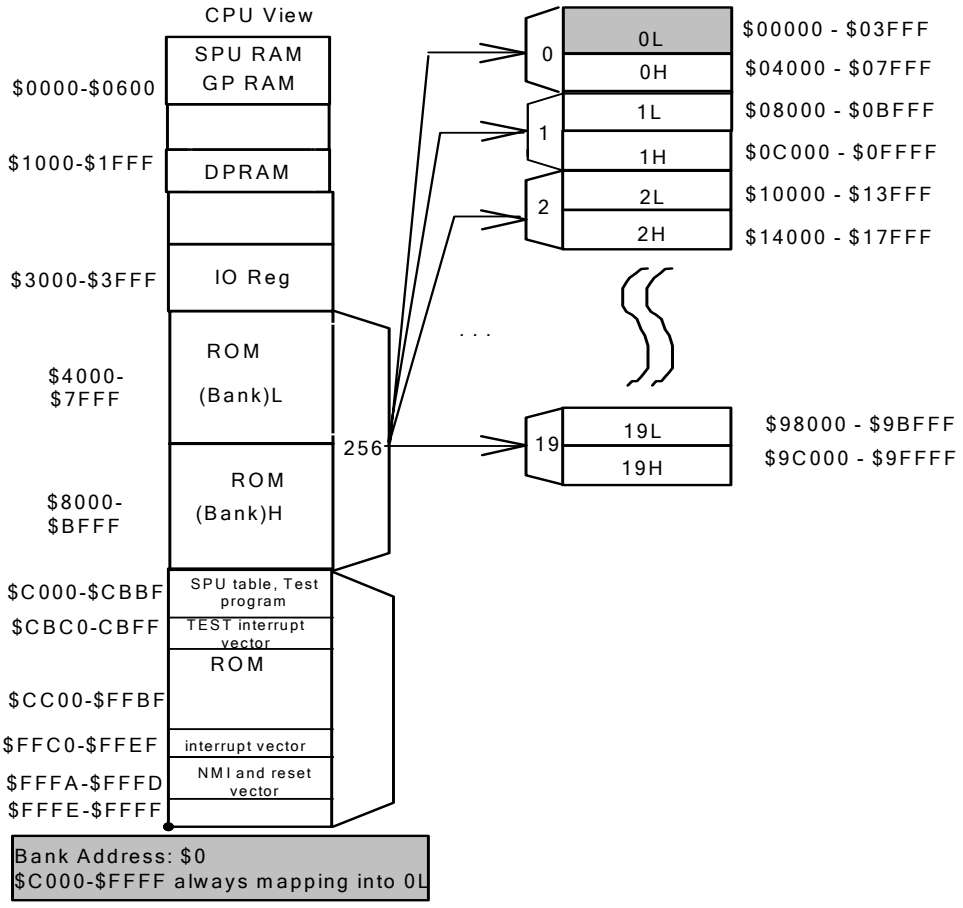
### 6.2.1. GPLB52640A/GPLB51640A

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1
- SPI
- SPU
- FP (LCD frame)




1. User program starts from $CC00. $C000-$CBFF is the test program area. $C000-$C103 is SPU ADPCM table data.
2. User program interrupt vector: $FFC0 ~ $FFEF.
3. Test program interrupt vector: $CBC0 ~ $CBFF.

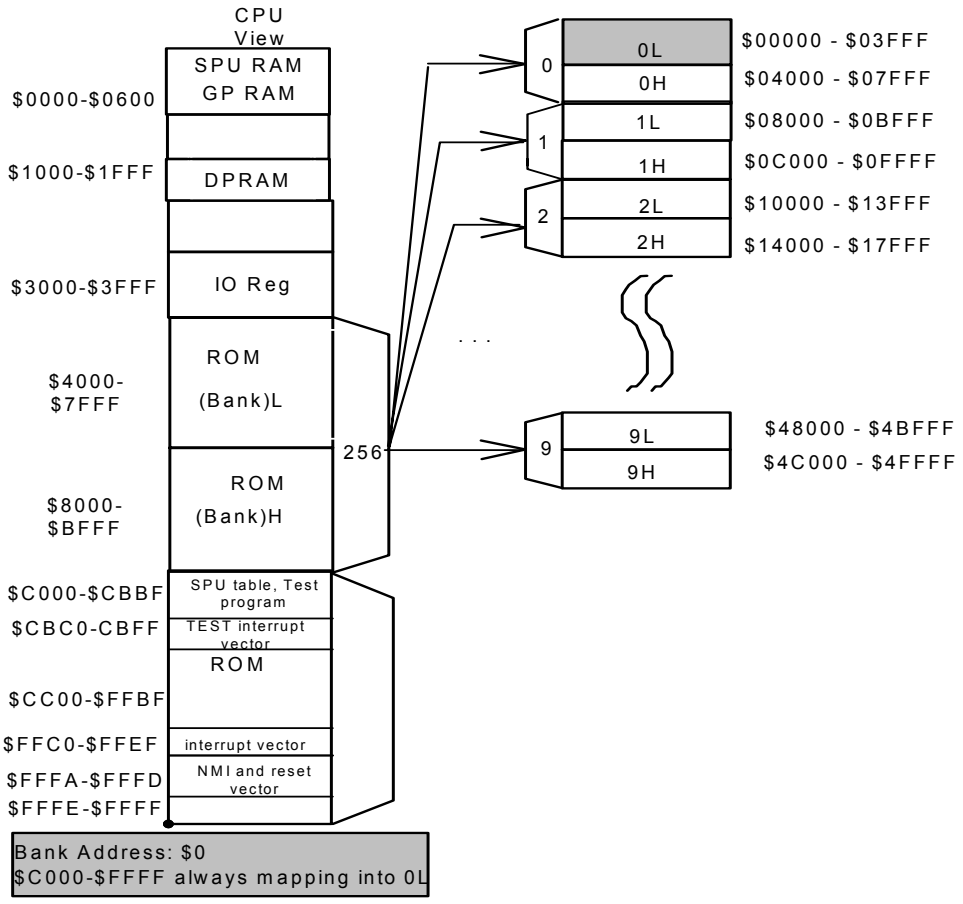
### 6.2.2. GPLB52320A/GPLB51320A

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1
- SPI
- SPU
- FP (LCD frame)




1. User program starts from $CC00. $C000-$CBFF is the test program area. $C000-$C103 is SPU ADPCM table data.
2. User program interrupt vector: $FFC0 ~ $FFEF.
3. Test program interrupt vector: $CBC0 ~ $CBFF.

## 6.3. Operating States

There are three operation modes in GPLB52640A/ GPLB52320A/ GPLB51640A/ GPLB51320A: standby, halt and operating mode. The following table shows the differences between these modes.

| | Operating | Halt | Standby |
|---|---|---|---|
| **CPU** | ON | OFF | OFF |
| **32768Hz oscillator** | ON | ON | OFF |
| **LCD driver** | ON | ON/OFF | OFF |

### 6.3.1. Operating Mode

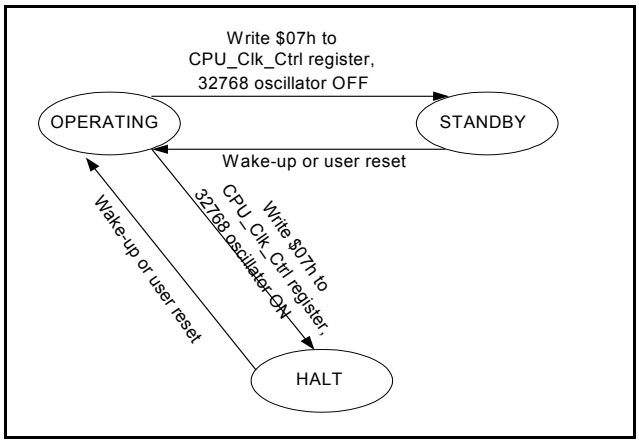
In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated. Generally speaking, this mode consumes the highest power.

### 6.3.2. Standby Mode

Write “07H” to P_3001H_ClkCtrl Register ($3001) and activate standby mode by turning off 32768Hz oscillator. The standby mode is a mode where the device is placed in its lowest current consumption state. In standby mode, all functions are turned off; in addition, RAM and I/Os will remain in their previous states.

### 6.3.3. Halt Mode

Write “07H” to P_3001H_ClkCtrl Register ($3001) but still keeps 32768Hz oscillator running to enter halt mode. In halt mode, CPU clock halts and waits for an event (e.g. key press, timer overflow) to wake up. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode. The following figure is the GPLB52640A/GPLB52320A/ GPLB51640A/ GPLB51320A state diagram:




**GPLB52640A/GPLB52320A/GPLB51640A/GPLB51320A State Diagram**

### 6.4. Speech and Melody, PWM and DAC

The GPLB52640A/ GPLB52320A/ GPLB51640A/ GPLB51320A use a high performance SPU voice engine to archive 8-channel voice with ADPCM/PCM code. The SPU also supports automatic zero-crossing concatenate function. A hardware multiplier is also embedded in this SPU for software usage. The fixed address of RAM area $0000 - $007F is designed as address pointers and a data buffer for the 8-channel speech/melody generator. There is one 12-bit D/A converter with 4mA driving current capability for audio output, DACO. There is one 10-bit PWM for audio outputs, AUDA and AUDB.

### 6.5. LCD Controller/Driver

The GPLB52640A/ GPLB52320A/ GPLB51640A/ GPLB51320A contain a LCD controller/driver and support monochrome and 4 gray LCD control. The GPLB52640A/GPLB52320A contain up to 64 segments and 32 commons, forming a maximum of 2048 dots LCD resolution, and the GPLB51640A/GPLB51320A contain up to 74 segments and 22 commons, forming a maximum of 1628 dots LCD. Programmers are able to define the LCD configuration by setting up the LCD Control Register. Once the LCD configuration is completed, the desired pattern can be displayed by filling the LCD buffer with proper data. The LCD driver can also operate during sleep by keeping 32768Hz oscillator running. The LCD driver in GPLB52640A/GPLB52320A/GPLB51640A/GPLB51320A supports 1/2 – 1/32 duty and 1/3 - 1/7 bias.

### 6.6. LCD Voltage Generation

To achieve highly integrated circuit and save external components as possible, the GPLB52640A/ GPLB52320A/ GPLB51640A/ GPLB51320A has built-in charge pump circuit and operational amplifiers to generate LCD's bias voltages VLCD, V4, V3, V2 and V1. The charge pump circuit can generate VPP approx. to 8V. With VPP as power source, an operational amplifier is further to provide LCD panel's power supply, VLCD. The level of VLCD can be adjusted by software. It is suggested that VLCD must be 0.7V higher than VDD or abnormal operation will occur.

### 6.7. Low Voltage Detection

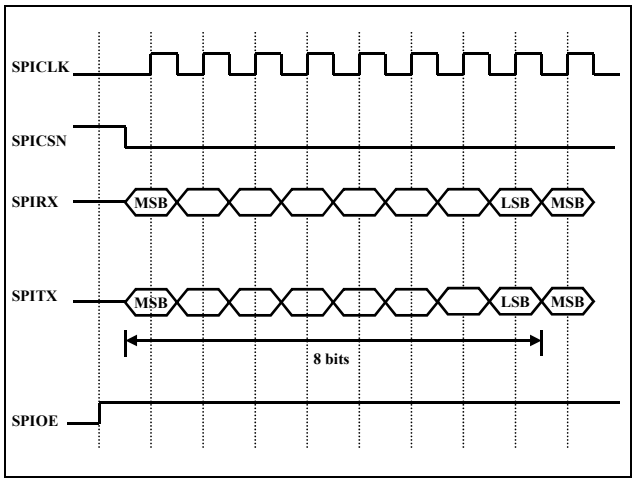
The GPLB52640A/ GPLB52320A/ GPLB51640A/ GPLB51320A provide a 4-level (Software programmable) low voltage detector to detect low voltage events. Users can turn on the low voltage detection to monitor VDD periodically, checking if it is lower than the given value. In addition, if LV NMI is enabled, an NMI will be issued to notify CPU if power voltage drops below the given value. Also, the voltage detector will generate a system reset if power supply voltage drops below 2.2V.

### 6.8. Watchdog Timer (WDT)

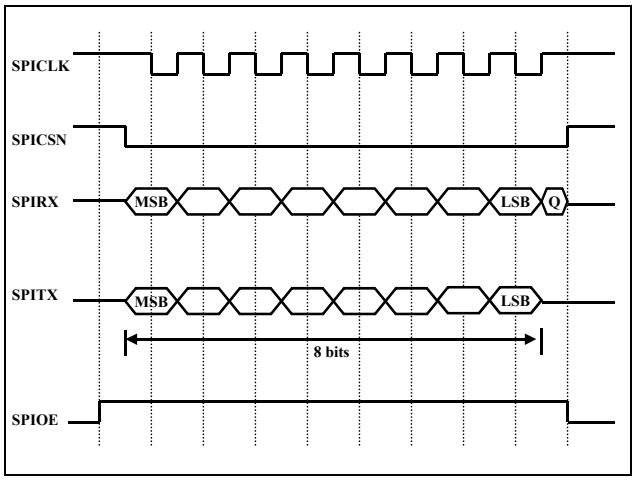
An on-chip watchdog timer is also available in the GPLB52640A/ GPLB52320A/ GPLB51640A/ GPLB51320A. The WDT is designed to recover system from unexpected operations. In some cases, if WDT is not cleared within one second, the WDT will generate a system reset to restart system. If WDT is enabled, the WDT should be cleared periodically to avoid accidental reset. The WDT can be cleared through software programming. Note that the WDT only works when 32768Hz clock is activated.

### 6.9. SPI Controller

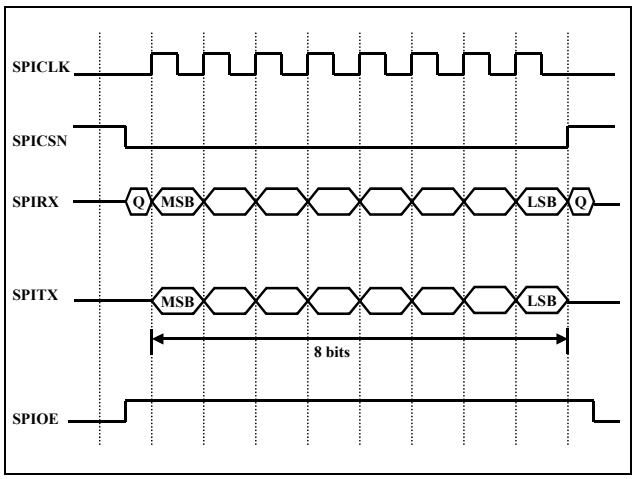
A Serial Peripheral Interface (SPI) controller is built in GPLB52640A/ GPLB52320A/ GPLB51640A/ GPLB51320A to facilitate communication with other devices. There are four control signals on SPI, including SPICSN, SPICLK (SCK), SPIRX (SDI), and SPITX (SDO). The four signals are shared with PortB4, PortB5, PortB6 and PortB7. While SPI module is enabled by corresponding control bit, these four pins cannot be GPIOs, and any setting on corresponding GPIO control register will have no effect. Four types of operation modes are supported as follows:



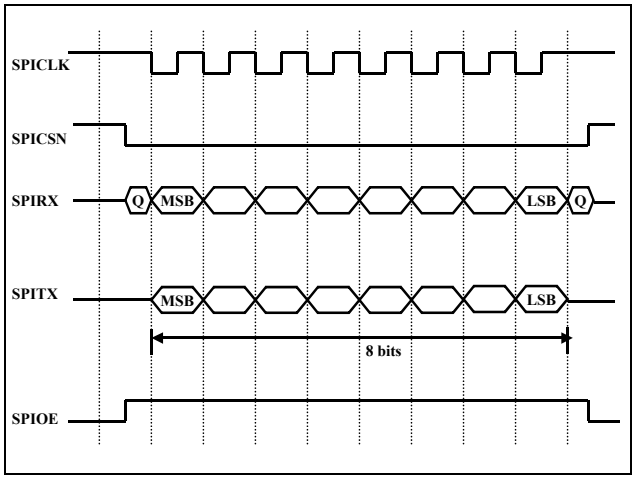

Master Mode, SPO = 0, SPH=0




Master Mode, SPO = 1, SPH=0




Master Mode, SPO = 0, SPH=1




Master Mode, SPO = 1, SPH=1

## 6.10. Mask Options

### 6.10.1. 32768 Oscillator

1). X'TAL

2). R-oscillator

### 6.10.2. System Clock Oscillator

1). R-oscillator

2). X'TAL

### 6.10.3. Internal VDD Regulator

1). Internal VDD regulator on

2). Internal VDD regulator off

# 7. ELECTRICAL SPECIFICATIONS

## 7.1. Absolute Maximum Ratings

| Characteristics | Symbol | Ratings |
|---|---|---|
| DC Supply Voltage | $V_+$ | < 7.0V |
| Input Voltage Range | $V_{IN}$ | -0.5V to $V_+$ + 0.5V |
| Operating Temperature | $T_A$ | 0℃ to +70℃ |
| Storage Temperature | $T_{STO}$ | -50℃ to +150℃ |

**Note:** Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

## 7.2. DC Characteristics (VDD5V=5.0V, for 3-battery application, internal regulator enabled output, $T_A$=25℃)

| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage | VDD5V | 2.7 | - | 5.5 | V | For 3-battery |
| Operating Current | $I_{OP1}$ | - | 4 | - | mA | $F_{CPU}$ = 6.0MHz @ 5.0V<br>$F_{XTAL}$ = 12.0MHz, no load, DAC disabled, PWM disabled. |
| | $I_{OP2}$ | - | 5 | - | mA | $F_{CPU}$ = 8.0MHz @ 5.0V<br>$F_{ROSC}$ = 16.0MHz, no load, DAC disabled, PWM disabled. |
| Halt Current | $I_{HALT}$ | - | 100 | - | μA | VDD5V = 5.0V, 32K X'tal ON, Strobe off, LCD ON, 1/7 Bias, VLCD=6.85V, no LCD panel |
| Standby Current (Regulator on) | $I_{STBYR}$ | - | - | 10 | μA | VDD5V = 5.0V, VDD regulator on, all off |
| PWM Audio Output Current | $I_{OH}$ | - | -30 | - | mA | VDD5V = 5.0V, $V_{OH}$ = 4.5V |
| | | - | -60 | - | mA | VDD5V = 5.0V, $V_{OH}$ = 4.0V |
| PWM Audio Output Current | $I_{OL}$ | - | 30 | - | mA | VDD5V = 5.0V, $V_{OL}$ = 0.5V |
| | | - | 60 | - | mA | VDD5V = 5.0V, $V_{OL}$ = 1.0V |
| Input High Level | $V_{IH}$ | 0.7VDD | - | - | V | VDD5V = 5.0V |
| Input Low Level | $V_{IL}$ | - | - | 0.3VDD | V | VDD5V = 5.0V |
| Output High Current (I/O) | $I_{OH}$ | -1.0 | - | - | mA | VDD5V = 5.0V, $V_{OH}$ = 4.5V |
| Output Sink Current (I/O) | $I_{OL}$ | 1.0 | - | - | mA | VDD5V = 5.0V, $V_{OL}$ = 0.5V |
| Input Pull-Low Resistor<br>PA(weak pull)<br>PA(strong pull)<br>PB,PC | $R_{PL}$ | - | <br>250<br>100<br>80 | - | KΩ | $V_{IN}$ = 5.0V |
| Input Pull-High Resistor<br>PA(weak pull)<br>PA(strong pull)<br>PB,PC | $R_{PH}$ | - | <br>160<br>50<br>50 | - | KΩ | $V_{IN}$ = 0V |
| LCD Driver Voltage | $V_{LCD}$ | 2.98 | - | 5.75 | V | VDD5V = 5.0V, 1/5 bias, no load |
| ($V_{LCD}$ - VSS) | | 2.95 | - | 6.85 | V | VDD5V = 5.0V, 1/6 bias, no load |
| OSC Resistor | $R_{OSC}$ | - | 33 | - | KΩ | $F_{OSC}$ = 14MHz @ 5.0V |
| CPU Clock | $F_{CPU}$ | - | - | 8.0 | MHz | $F_{CPU}$ = $F_{OSC}$/2 @ 2.4V |

**Note:** $V_{LCD}$ should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

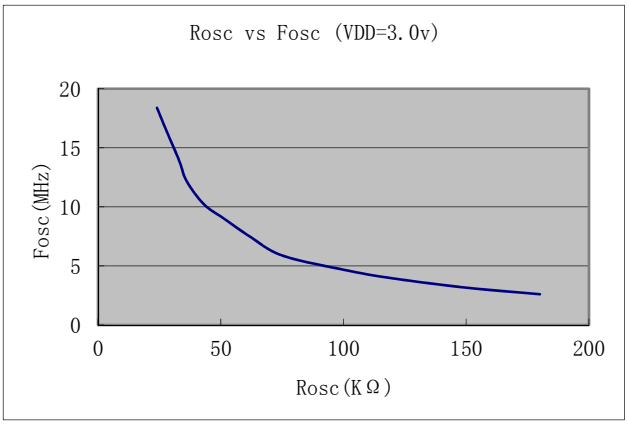
### 7.3. DC Characteristics (VDD5V=VDD=3.0V, for 2-battery application, internal regulator output disabled, $T_A$=25℃)

| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage | VDD5V | 2.4 | - | 3.6 | V | For 2-battery |
| Operating Current | $I_{OP1}$ | - | 4 | - | mA | $F_{CPU}$ = 6.0MHz @ 3.0V<br>$F_{XTAL}$ = 12.0MHz, no load, DAC disabled, PWM disabled. |
| | $I_{OP2}$ | - | 5 | - | mA | $F_{CPU}$ = 8.0MHz @ 3.0V<br>$F_{ROSC}$ = 16.0MHz, no load, DAC disabled, PWM disabled. |
| Halt Current | $I_{HALT}$ | - | 80 | - | μA | VDD5V = 3.0V, 32K X'tal ON, Strobe off, LCD ON, 1/7 Bias, VLCD=6.85V, no LCD panel |
| Standby Current (Regulator off) | $I_{STBY}$ | - | - | 1.0 | μA | VDD5V = 3.0V, all off |
| PWM Audio Output Current | $I_{OH}$ | - | -20 | - | mA | VDD5V = 3.0V, $V_{OH}$ = 2.5V |
| | | - | -40 | - | mA | VDD5V = 3.0V, $V_{OH}$ = 2.0V |
| PWM Audio Output Current | $I_{OL}$ | - | 20 | - | mA | VDD5V = 3.0V, $V_{OL}$ = 0.5V |
| | | - | 40 | - | mA | VDD5V = 3.0V, $V_{OL}$ = 1.0V |
| Input High Level | $V_{IH}$ | 0.7VDD | - | - | V | VDD5V = 3.0V |
| Input Low Level | $V_{IL}$ | - | - | 0.3VDD | V | VDD5V = 3.0V |
| Output High Current (I/O) | $I_{OH}$ | -1.0 | - | - | mA | VDD5V = 3.0V, $V_{OH}$ = 2.5V |
| Output Sink Current (I/O) | $I_{OL}$ | 1.0 | - | - | mA | VDD5V = 3.0V, $V_{OL}$ = 0.5V |
| Input Pull-Low Resistor<br>PA(weak pull)<br>PA(strong pull)<br>PB,PC | $R_{PL}$ | - | <br>180<br>60<br>60 | - | KΩ | $V_{IN}$ = 3.0V |
| Input Pull-High Resistor<br>PA(weak pull)<br>PA(strong pull)<br>PB,PC | $R_{PH}$ | - | <br>300<br>70<br>100 | - | KΩ | $V_{IN}$ = 0V |
| LCD Driver Voltage | $V_{LCD}$ | 2.98 | - | 5.75 | V | VDD5V = 3.0V, 1/5 bias, no load |
| ($V_{LCD}$ - VSS) | | 2.95 | - | 6.85 | V | VDD5V = 3.0V, 1/6 bias, no load |
| OSC Resistor | $R_{OSC}$ | - | 33 | - | KΩ | $F_{OSC}$ = 14MHz @ 3.0V |
| CPU Clock | $F_{CPU}$ | - | - | 8.0 | MHz | $F_{CPU}$ = $F_{OSC}$/2 @ 2.4V |

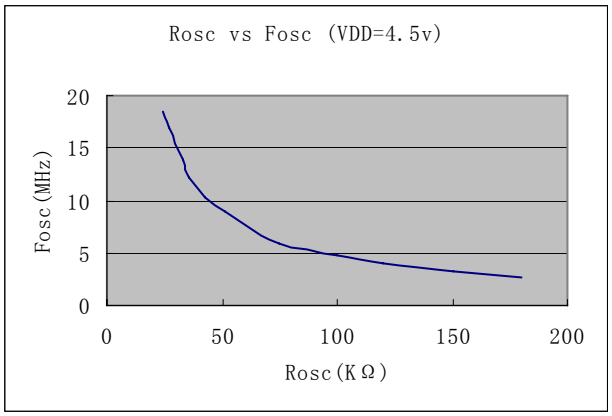
**Note:** $V_{LCD}$ should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

### 7.4. The Relationship between the $R_{OSC}$ and the $F_{OSC}$

#### 7.4.1. VDD = 3.0V, $T_A$ = 25℃

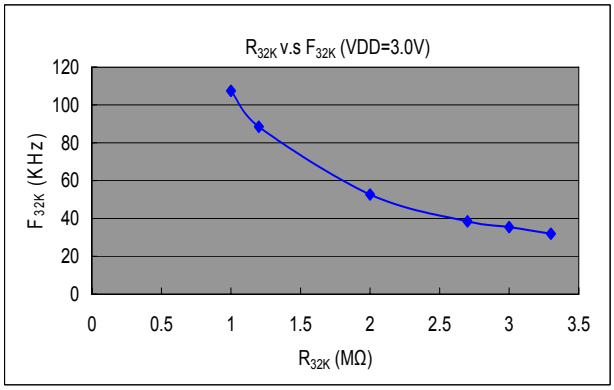



#### 7.4.2. VDD = 4.5V, $T_A$ = 25℃

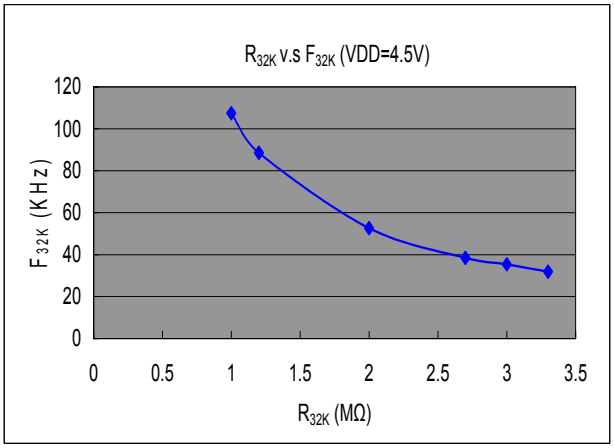



### 7.5. The Relationship between the F32K and the R32K

#### 7.5.1. VDD = 3.0V, $T_A$ = 25℃

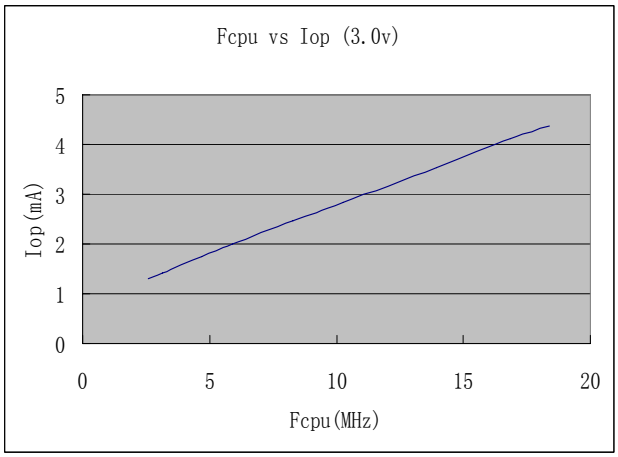



#### 7.5.2. VDD = 4.5V, $T_A$ = 25℃




### 7.6. The Relationships between the $F_{CPU}$ and the $I_{OP}$

#### 7.6.1. VDD = 3.0V, $T_A$ = 25℃

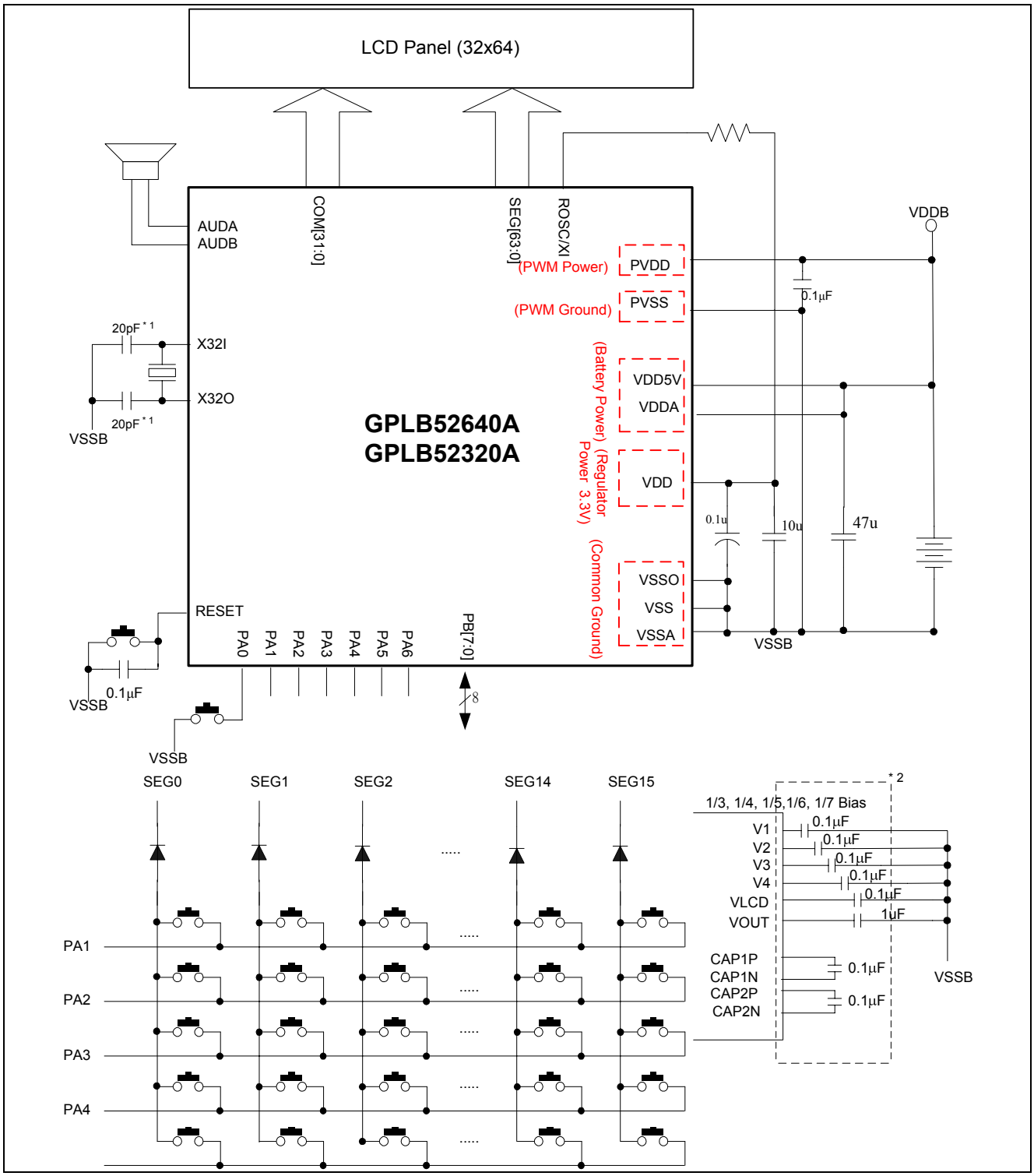


### 7.7. DAC Characteristics (VDD5V = 5.0V, $T_A$ = 25℃)

| Characteristics | Symbol | Limit | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Resolution of DAC | RESO | - | - | 12 | bit |
| THD+N | SNR | - | <-60 | - | dB |
| Noise at no signal | - | - | -80 | - | dBr A |
| Dynamic range(-60dB) | - | - | -75 | - | dBr A |
| Sample Rate | $F_S$ | - | - | 400K | Hz |

## 8. APPLICATION CIRCUITS

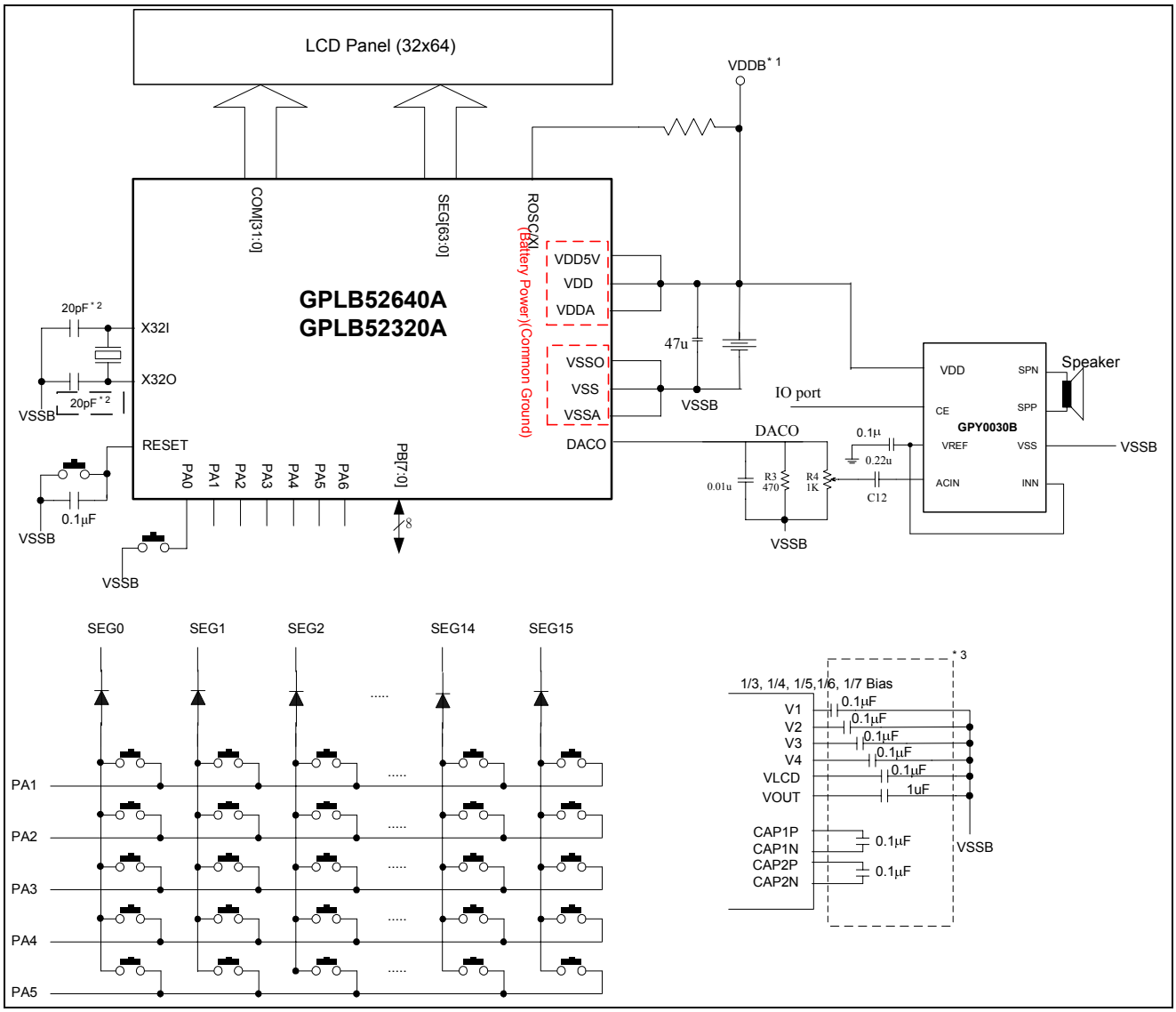
### 8.1. 2048 Dots LCD Driver, using GPLB52640A or GPLB52320A, 64 Segments × 32 Commons, for 3-battery application, Internal 3.3V Regulator Enabled, 10-bit PWM Driver Enabled, ROSC14M XTAL32K Selected- (1)




**Note*1:** These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading; for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

**Note*2:** These capacitor values are for design guidance only. The ratio of capacitance of VOUT to the capacitance of CAP1N/CAP1P/CAP2N/CAP2P is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and can't be greater than capacitance of VOUT. But in a larger LCD panel, 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for VOUT and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N is recommended.

### 8.2. 2048 Dots LCD Driver, using GPLB52640A or GPLB52320A, 64 Segments × 32 Commons, Internal 3.3V Regulator Disabled, for 2-battery application, 12-bit DAC Enabled, ROSC14M XTAL32K Selected - (2)

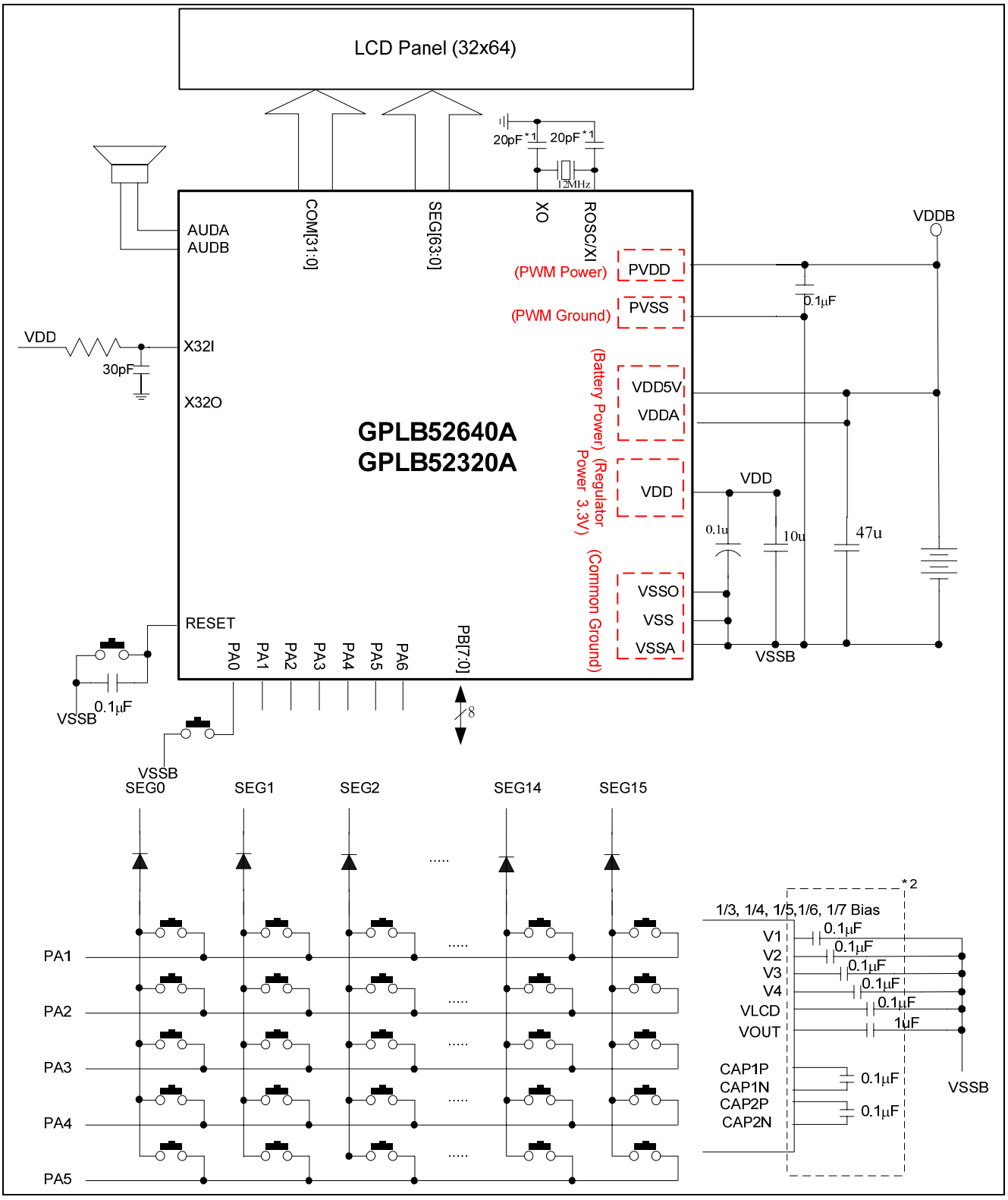



**Note*1:** VDD should not exceed 3.6V.

**Note*2:** These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading; for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

**Note*3:** These capacitor values are for design guidance only. The ratio of capacitance of VOUT to the capacitance of CAP1N/CAP1P/CAP2N/CAP2P is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and can't be greater than capacitance of VOUT. But in a larger LCD panel, 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for VOUT and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N is recommended.

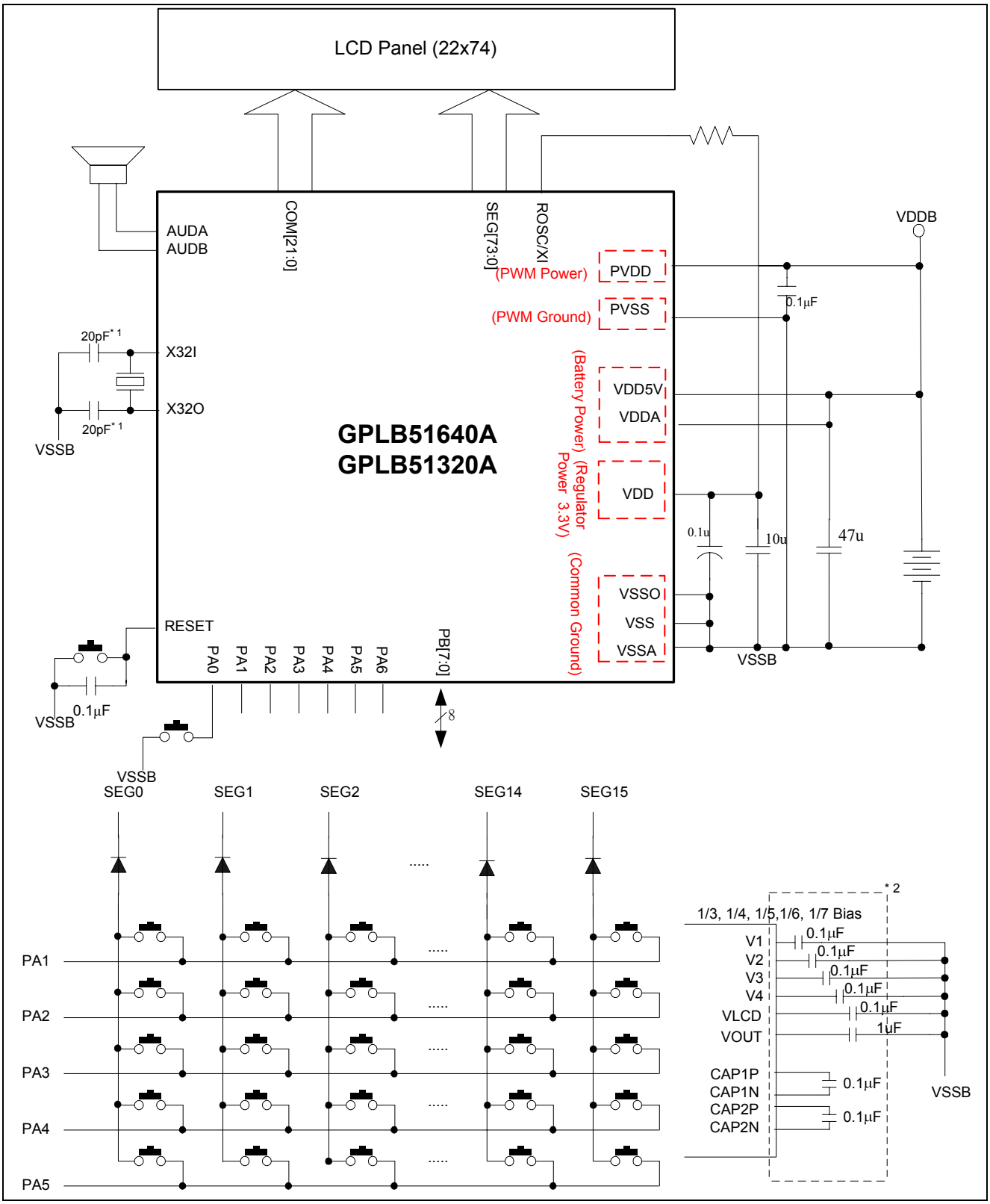
### 8.3. 2048 Dots LCD Driver, using GPLB52640A or GPLB52320A, 64 Segments × 32 Commons, for 3-battery application, Internal 3.3V Regulator Enabled, 10-bit PWM Driver Enabled, XTAL12M ROSC32K Selected - (3)




**Note*1:** These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

**Note*2:** These capacitor values are for design guidance only. The ratio of capacitance of VOUT to the capacitance of CAP1N/CAP1P/CAP2N/CAP2P is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and can't be greater than capacitance of VOUT. But in a larger LCD panel, 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for VOUT and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N is recommended.

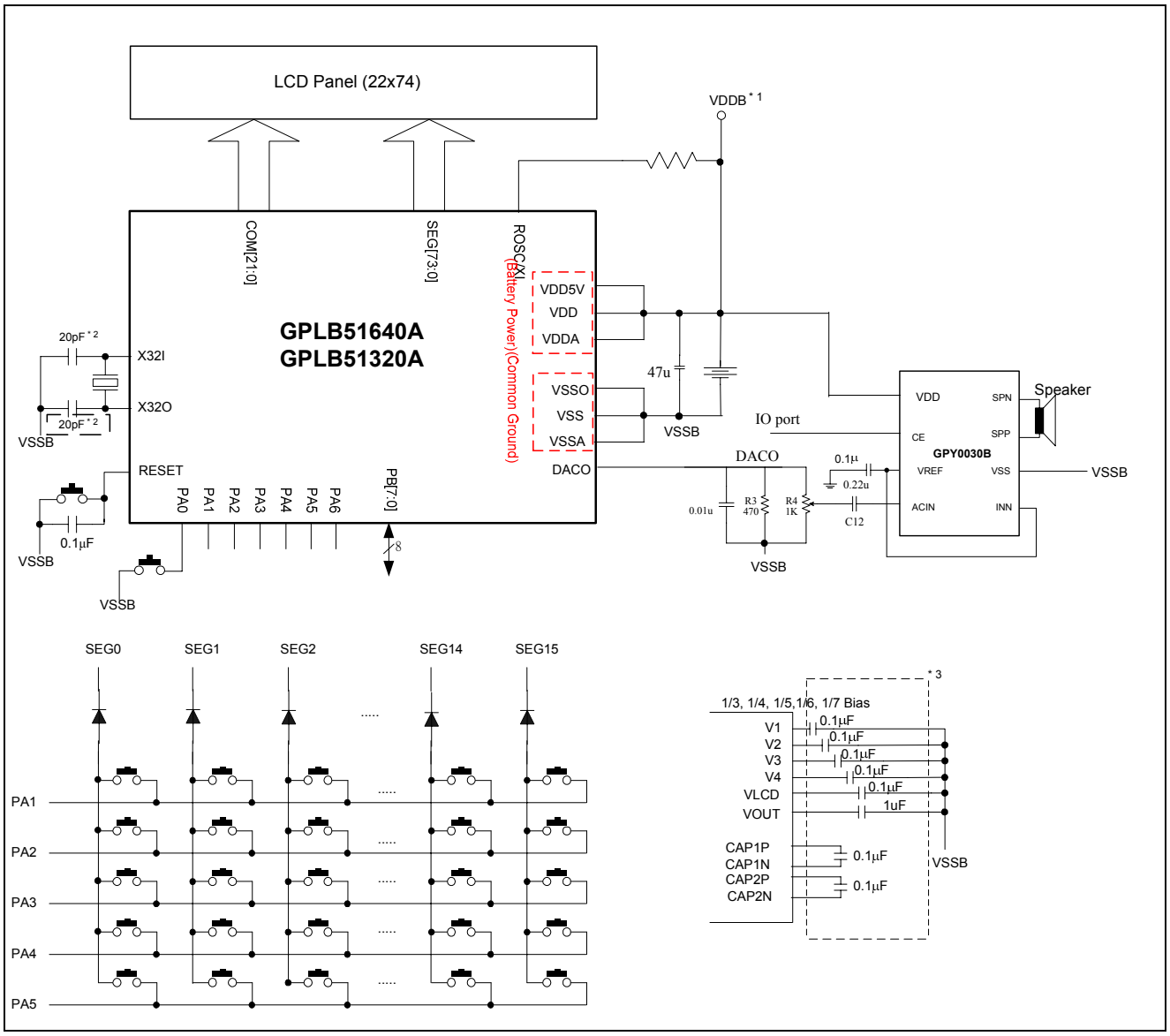
### 8.4. 1628 Dots LCD Driver, using GPLB51640A or GPLB51320A, 74 Segments × 22 Commons, for 3-battery application, Internal 3.3V Regulator Enabled, 10-bit PWM Driver Enabled, ROSC14M XTAL32K Selected- (1)




**Note*1:** These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading; for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

**Note*2:** These capacitor values are for design guidance only. The ratio of capacitance of VOUT to the capacitance of CAP1N/CAP1P/CAP2N/CAP2P is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and can't be greater than capacitance of VOUT. But in a larger LCD panel, 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for VOUT and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N is recommended.

### 8.5. 1628 Dots LCD Driver, using GPLB51640A or GPLB51320A, 74 Segments × 22 Commons, for 2-battery application, Internal 3.3V Regulator Disabled, 12-bit DAC Enabled, ROSC14M XTAL32K Selected - (2)

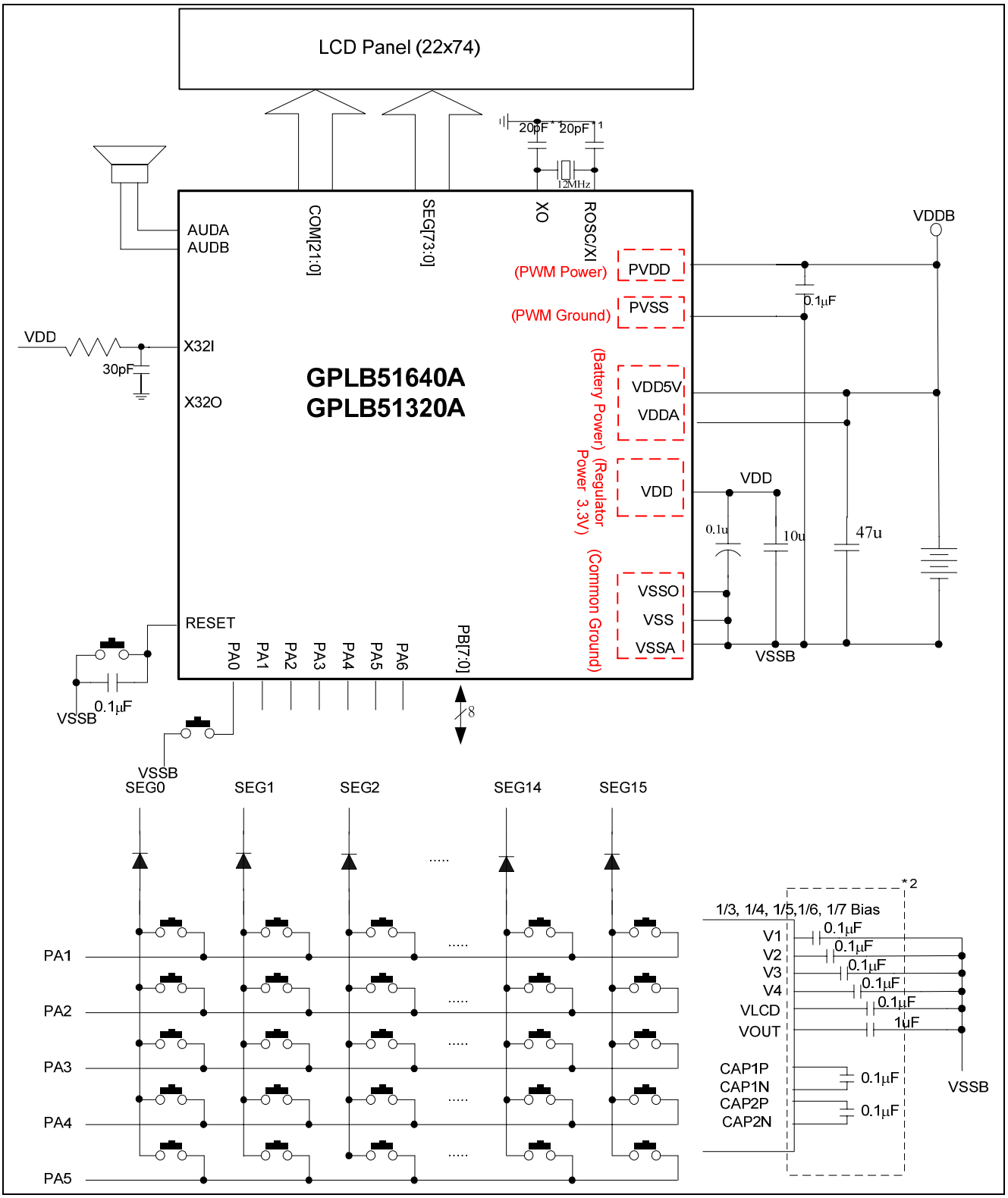



**Note*1:** VDD should not exceed 3.6V.

**Note*2:** These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~35K and CL1=CL2 =20~30pF (including PCB parasitic loading; for example, user should apply additional 14~24pF on X32I and X32O if PCB parasitic loading is 6pF)

**Note*3:** These capacitor values are for design guidance only. The ratio of capacitance of VOUT to the capacitance of CAP1N/CAP1P/CAP2N/CAP2P is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and can't be greater than capacitance of VOUT. But in a larger LCD panel, 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for VOUT and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N is recommended.

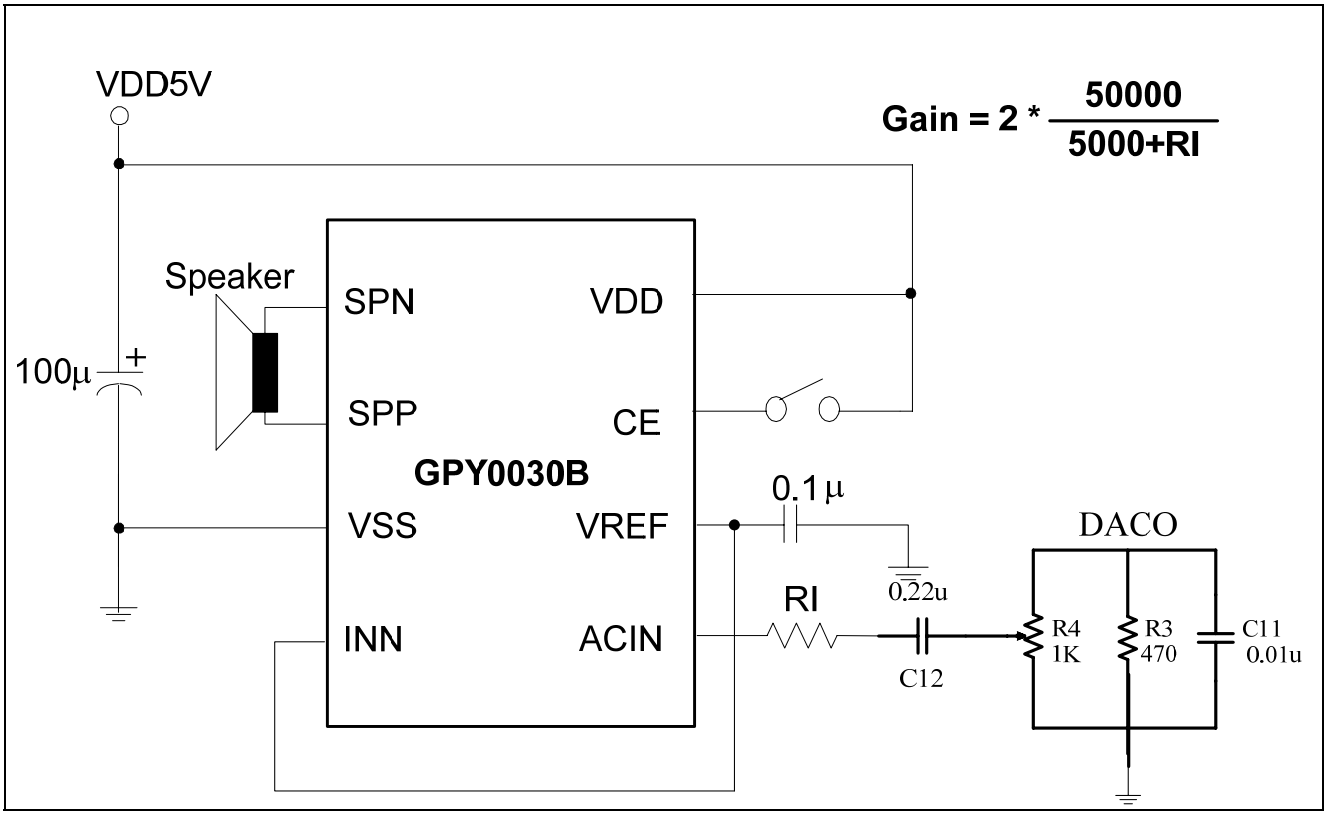
**8.6. 1628 Dots LCD Driver, using GPLB51640A or GPLB51320A, 74 Segments × 22 Commons, for 3-battery application, Internal 3.3V Regulator Enabled, 10-bit PWM Driver Enabled, XTAL12M ROSC32K Selected - (3)**




**Note*1:** These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

**Note*2:** These capacitor values are for design guidance only. The ratio of capacitance of VOUT to the capacitance of CAP1N/CAP1P/CAP2N/CAP2P is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and can't be greater than capacitance of VOUT. But in a larger LCD panel, 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for VOUT and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N is recommended.

### 8.7. DAC Output with Generalplus Audio Driver GPY0030B (for high quality audio output) - (4)



### 8.8. Current Mode DAC Speaker Driver with BJT- (5)

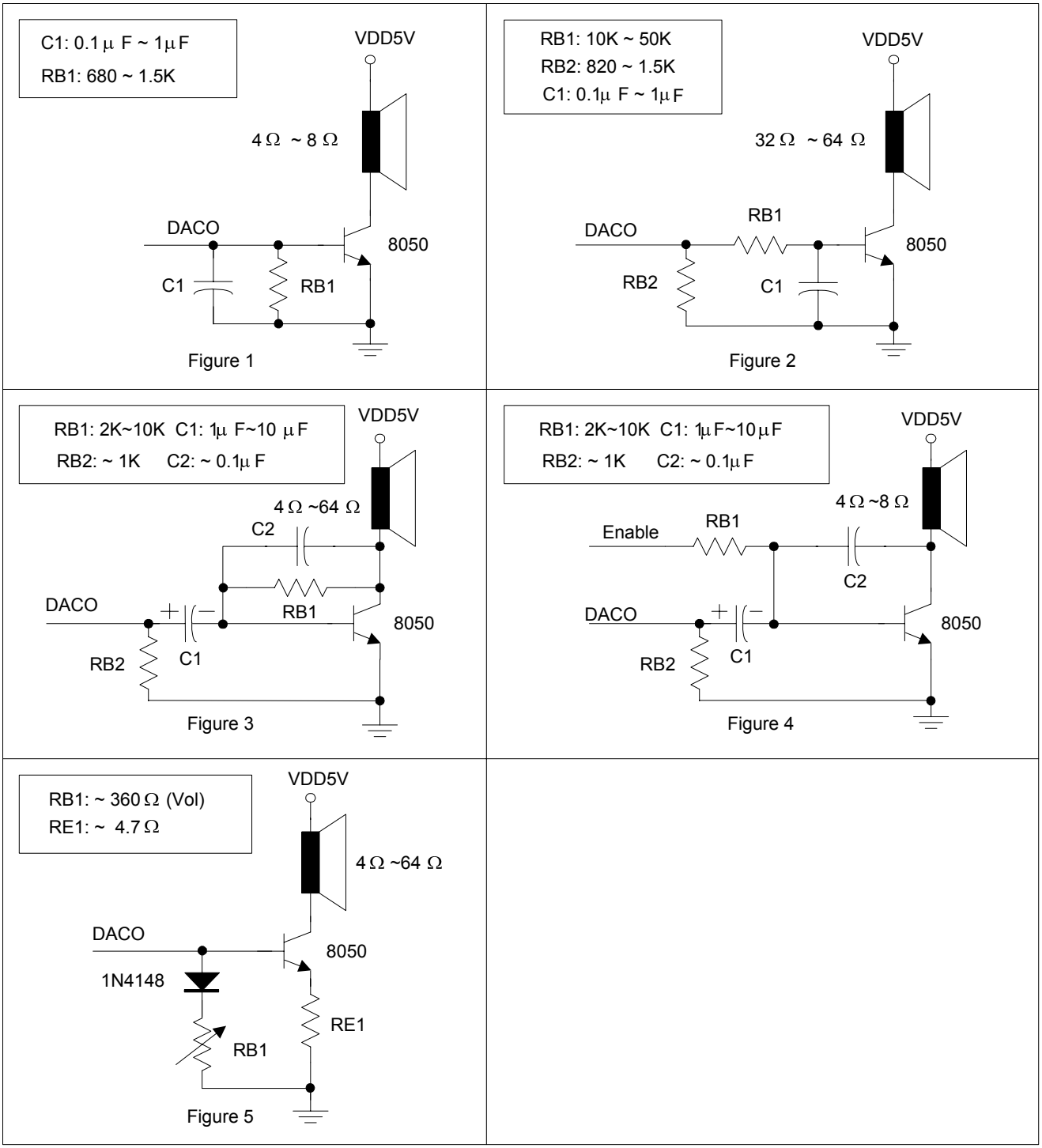



**Figure 1:** The simplest CKT uses with low impedance speaker. It has high operation current, but the cost is the cheapest.

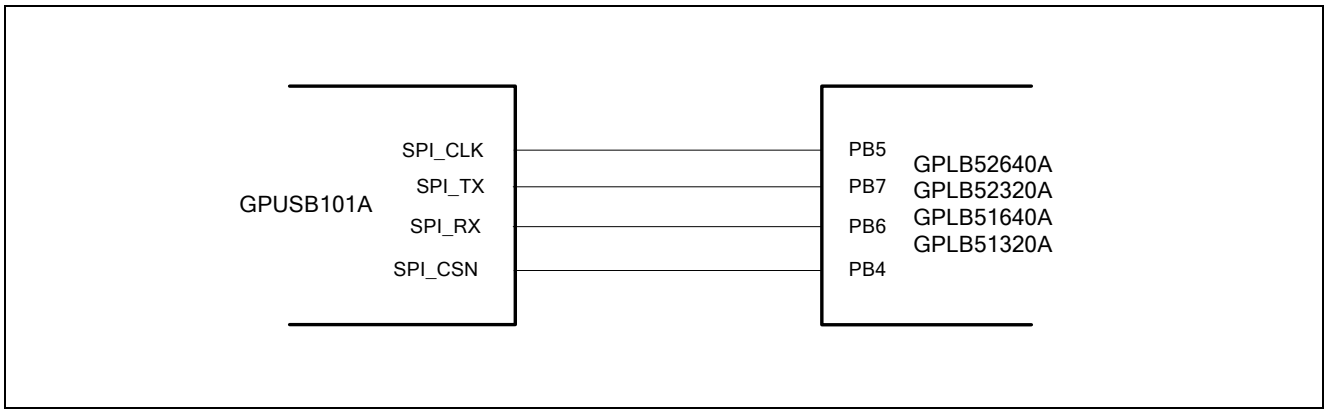
**Figure 2:** It is the same as Figure 1 but a high impedance speaker is used.

**Figure 3:** The CKT has low pass filter. It can provide higher speech quality, but it always takes high operation current.

**Figure 4:** Improved version of Figure 3. The standby current can be controlled by enable pin.

**Figure 5:** The current mirror mode. It is able to control the volume. In addition, it has more stable and lower operation current than Figure 1-3.

### 8.9. Serial Communications between GPLB52640A/GPLB52320A/GPLB51640A/GPLB51320A and GPUSB101A USB Controller- (6)



# 9. PACKAGE/PAD LOCATIONS

## 9.1. Ordering Information

| Product Number | Package Type |
|---|---|
| GPLB52640A - NnnV - C | Chip form |
| GPLB52320A - NnnV - C | Chip form |
| GPLB51640A - NnnV - C | Chip form |
| GPLB51320A - NnnV - C | Chip form |

**Note1:** Code number is assigned for customer.

**Note2:** Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

## 10. DISCLAIMER

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## 11. REVISION HISTORY

| Date | Revision # | Description | Page |
|---|---|---|---|
| Sep 12, 2013 | 2.2 | update capacitance value of Xtal 32K in APCKT. | |
| Jul 12, 2012 | 2.1 | Modify note for application circuit about recommended capacitor's value. | 17-22 |
| Nov. 23, 2011 | 2.0 | Modify 7.2 & 7.3 DC Characteristics. | 13, 14 |
| Dec. 30, 2010 | 1.9 | Modify 3. FEATURES. | 5 |
| Sep. 21, 2009 | 1.8 | 1. Modify 3. FEATURES.<br>2. Add 6.5 LCD Controller/Driver.<br>3. Add 6.6 LCD Voltage Generation.<br>4. Modify 8. APPLICATION CIRCUITS. | 5<br>15<br>15<br>21, 22 |
| Aug. 06, 2009 | 1.7 | 1. Modify 1.GENERAL DESCRIPTION.<br>2. Modify 6.2. Map of Memory and I/Os. | 4<br>13-14 |
| May 19, 2009 | 1.6 | Modify 5. SIGNAL DESCRIPTION. | 6, 7 |
| Apr. 02, 2009 | 1.5 | Modify the Absolute Maximum Ratings in section 7.1. | 17 |
| Mar. 10, 2009 | 1.4 | Modify section 8. APPLICATION CIRCUITS. | 21-26 |
| Dec. 8, 2008 | 1.3 | 1. Modify section 3. FEATURES.<br>2. Modify section 7.2 and 7.3 DC Characteristics.<br>3. Modify section 8. APPLICATION CIRCUITS. | 5<br>17<br>21-26 |
| Oct. 24, 2008 | 1.2 | 1. Modify section 5. SIGNAL DESCRIPTION.<br>2. Modify section 8.3 and 8.6 Application Circuits. | 6, 7<br>23, 26 |
| Aug. 29, 2008 | 1.1 | Modify section 8. APPLICATION CIRCUITS. | 21 |
| Jul. 22, 2008 | 1.0 | Release to 1.0 | 31 |
| Mar. 20, 2008 | 0.2 | Add body: GPLB52320A/GPLB51640A/GPLB51320A. | 24 |
| JAN. 08, 2008 | 0.1 | Preliminary data sheet. | 17 |