DATA SHEET

GPLB52A24B1
GPLB51A24B1

1000/2000 Dots Mono/LCD Controller/Driver with 8-CH SPU

Aug 20, 2013

Version 1.2

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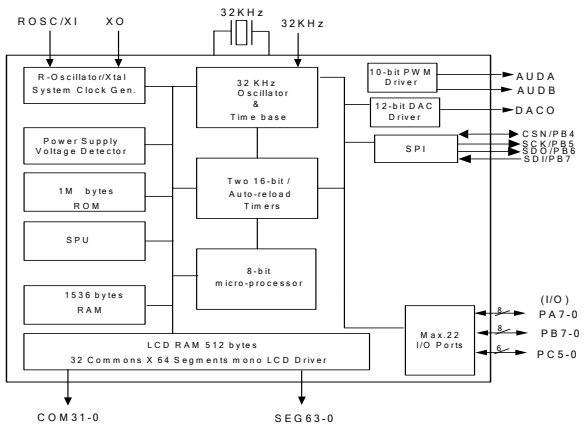
1000/2000 DOTS MONO/LCD CONTROLLER/ DRIVER WITH 8CH SPU

1. GENERAL DESCRIPTION

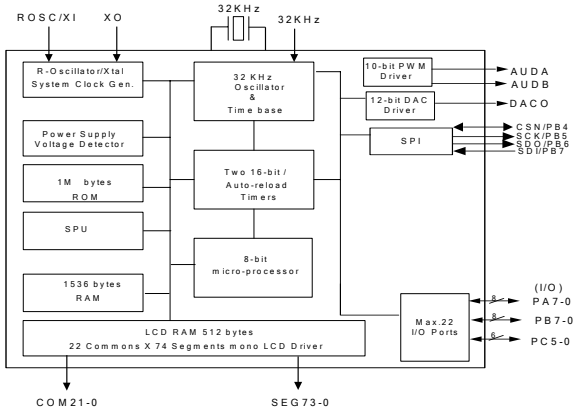
The GPLB52A24B1/ GPLB51A24B1, an 8-bit CMOS microprocessor, features 1536 bytes working RAM, 1M bytes ROM memory, 24 I/Os, interrupt/wakeup controller, 2 set 16-bit timers, SPI interface, 1 set of 12-bit DAC, 1 set of 10-bit PWM, and automatic display controller/driver for mono/LCD. The GPLB52A24B1 contains up to 64 segments and 32 commons, forming a maximum of 2048 dots LCD resolution, and GPLB51A24B1 contains up to 74 segments and 22 commons, forming a maximum of 1628 dots LCD. The microprocessor can implement software for audio processing, functional control and others. In audio processing, melody and speech can be mixed into one output. The GPLB52A24B1/ GPLB51A24B1 also carries a high performance SPU voice engine to achieve 8-channel voice with ADPCM/PCM data. It operates over a wide voltage range from 2.4V through 5.5V, plus Low Voltage Reset function to assure system is still functioning properly when power drops below a specific level. Also, it features one 10-bit PWM driver and one 12-bit DAC with 8 audio channels to produce attractive sound effects easily. Its large ROM area can be used to store both program and audio data. There is a Serial Peripheral Interface (SPI) controller built-in to facilitate communicating with other devices. Furthermore, a SLEEP (power-down) function is also built in to extend battery life. The GPLB52A24B1/ GPLB51A24B1 is designed with state-of-the-art technology to fulfill LCD application needs, especially for hand-held products.

2. BLOCK DIAGRAM

2.1. GPLB52A24B1



2.2. GPLB51A24B1



3. FEATURES

- 8-bit micro-processor
- **1536 bytes SRAM**
- **1M bytes ROM**
- Operating voltage: 2.4V – 5.5V
- Max. CPU operating speed:
  - 8.0MHz @ 2.4V with 16MHz X'TAL
  - 8.0MHz @ 2.4V with 16MHz ROSC
- Programmable CPU clock: /2, /4, /8, /16, /32, /64 and /128 R-oscillator clock frequency
- Six wake-up sources
- Nine IRQ & two NMI Interrupts
- Internal built-in regulator to supply core power (3.3V, for 3-battery application). Also it can turn off internal built-in regulator, and use external 3.6V power to supply core power (for 2-battery application).
- Programmable LCD driver
- **LCD size table:**

	GPLB52A24B1	GPLB51A24B1
Segment	64	74
Common	32	22
LCD Dots	2048	1628

  - Supports from 1/2 duty up to 1/32 duty
  - 512 bytes dedicated LCD RAM
  - Supports normal type-B & type-C LCD waveform with or without key scan
  - Built-in voltage regulator to generate VLCD for LCD driver
  - 32-level contrast control (VLCD=2.95V~6.85V)
  - Power saving SLEEP mode

- **Low Voltage Detector**
  4-level (2.4V/2.6V/3.0V/3.3V) voltage detector
- **2.2V Low Voltage Reset**
- Peripherals
  - Max. 22 I/O pins (PA[7:0], PB[7:0], PC[5:0])
  - Built-in 32.768KHz oscillator circuit for real time clock function (X'tal or R-osc)
  - Built-in R-oscillator for system operating clock (external resistor is needed)
  - Internal time base generator
  - Two 16-bit reloadable timer/counters
  - Watchdog timer
  - **12-bit DAC output and 10-bit PWM audio outputs**
  - Key scan function
  - SEG[15:0] can be used to send key scan output
  - IR carrier output
  - One SPI serial interface I/O
- **Powerful 8-ch Sound Processing Unit(SPU)**
  - Variable tone-color sampling rate: maximum 54KHz@CPU_Clock=7MHz
  - 8-voice polyphony
  - Supports PCM/ADPCM tone-color table

4. APPICATION FIELD

- Handheld LCD game
- Educational toys (Electronic Learning Aids)
- Data bank
- Dictionary
- Translator

5. SIGNAL DESCRIPTION

5.1. GPLB52A24B1

Mnemonic	PIN No.	Type	Description
SEG63 – 57 SEG56 – 0	140-146 1-57	O	LCD driver segment output. SEG15 - 0 share pin with key scan port.
COM31– 22	139-130	O	LCD driver common output.
COM21– 16 COM15 – 0	129-124 58-73	O	LCD driver common output. COM21 - 0.
PA7 – 0	101-94	I/O	PA7-0 is a bi-directional I/O port, which can be software programmed as wake up I/O.
PB0/ECLK	86	I/O	PB0 is a shared pin with external timer clock input ECLK.
PB1/EXTI	87	I/O	PB1 is a shared pin with external timer clock input EXTI.
PB2	88	I/O	PB2 is a bi-directional I/O port.
PB3	89	I/O	PB3 is a shared pin with IR carrier output IRO.
PB4/SPI_CSN	90	I/O	PB4 is a shared pin with SPI chip select SPI_CSN.
PB5/SCK	91	I/O	PB5 is a shared pin with SPI clock output SCK.
PB6/SDO	92	I/O	PB6 is a shared pin with SPI data output SDO.
PB7/SDI	93	I/O	PB7 is a shared pin with SPI data input SDI.
PC5 - 0	85-80	I/O	PC7-0 is a bi-directional I/O port.
ROSC/XI	106	I	Crystal input or ROSC input, connect to VDD(3V) through a resistor(option).
XO	105	O	Crystal output.
RESETB	108	I	System reset input, low active.
AUDA, AUDB	78,75	O	PWM audio output.
DACO	74	O	DAC output.
X32I	109	I	32.768KHz crystal input or connects to VDD(3V) through a resistor (option).
X32O	110	O	32.768KHz crystal output.
TEST	111	I	Test input. Reserved for Generalplus testing.
CAP1P, CAP1N	114,115	P	LCD voltage generation. Charge pump capacitor interconnection pins.
CAP2P, CAP2N	116,117	P	LCD voltage generation. Charge pump capacitor interconnection pins.
VOUT	118	P	LCD voltage generation. Voltage generated by charge pump.
V4	120	P	LCD voltage generation.
V3	121	P	LCD voltage generation.
V2	122	P	LCD voltage generation.
V1	123	P	LCD voltage generation.
VLCD	119	P	LCD voltage generation. The highest voltage for LCD display.
VDD5V	103	P	Positive supply for regulator input.
VSSO	102	P	Ground for regulator.
VDDA	113	P	Power for charge pump and IO pins.
VSSA	112	P	Ground for charge pump and IO pins.
VDDDAC	79	P	Positive supply for DAC (3.3V), connect to VDD.
VDD	104	P	3.3V power output from regulator. Regulator can be turned off when external 3.3V is supplied.
VSS	107	P	Ground reference for logic.

Mnemonic	PIN No.	Type	Description
PVDD	77	P	Positive supply for PWM driver.
PVSS	76	P	Ground reference for PWM driver and for DAC.

Legend: I = Input, O = Output, P = Power

5.2. GPLB51A24B1

Mnemonic	PIN No.	Type	Description
SEG63 – 57 SEG56 – 0	140-146 1-57	O	LCD driver segment output. SEG15 - 0 share pin with key scan port.
SEG64-73	139-130	O	LCD driver common output.
COM21– 16 COM15 – 0	129-124 58-73	O	LCD driver common output. COM21 - 0.
PA7 – 0	101-94	I/O	PA7-0 is a bi-directional I/O port, which can be software programmed as wake up I/O.
PB0/ECLK	86	I/O	PB0 is a shared pin with external timer clock input ECLK.
PB1/EXTI	87	I/O	PB1 is a shared pin with external timer clock input EXTI.
PB2	88	I/O	PB2 is a bi-directional I/O port.
PB3	89	I/O	PB3 is a shared pin with IR carrier output IRO.
PB4/SPI_CSN	90	I/O	PB4 is a shared pin with SPI chip select SPI_CSN.
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PB6/SDO	92	I/O	PB6 is a shared pin with SPI data output SDO.
PB7/SDI	93	I/O	PB7 is a shared pin with SPI data input SDI.
PC5 - 0	85-80	I/O	PC7-0 is a bi-directional I/O port.
ROSC/XI	106	I	Crystal input or ROSC input, connect to VDD(3V) through a resistor(option).
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AUDA, AUDB	78,75	O	PWM audio output.
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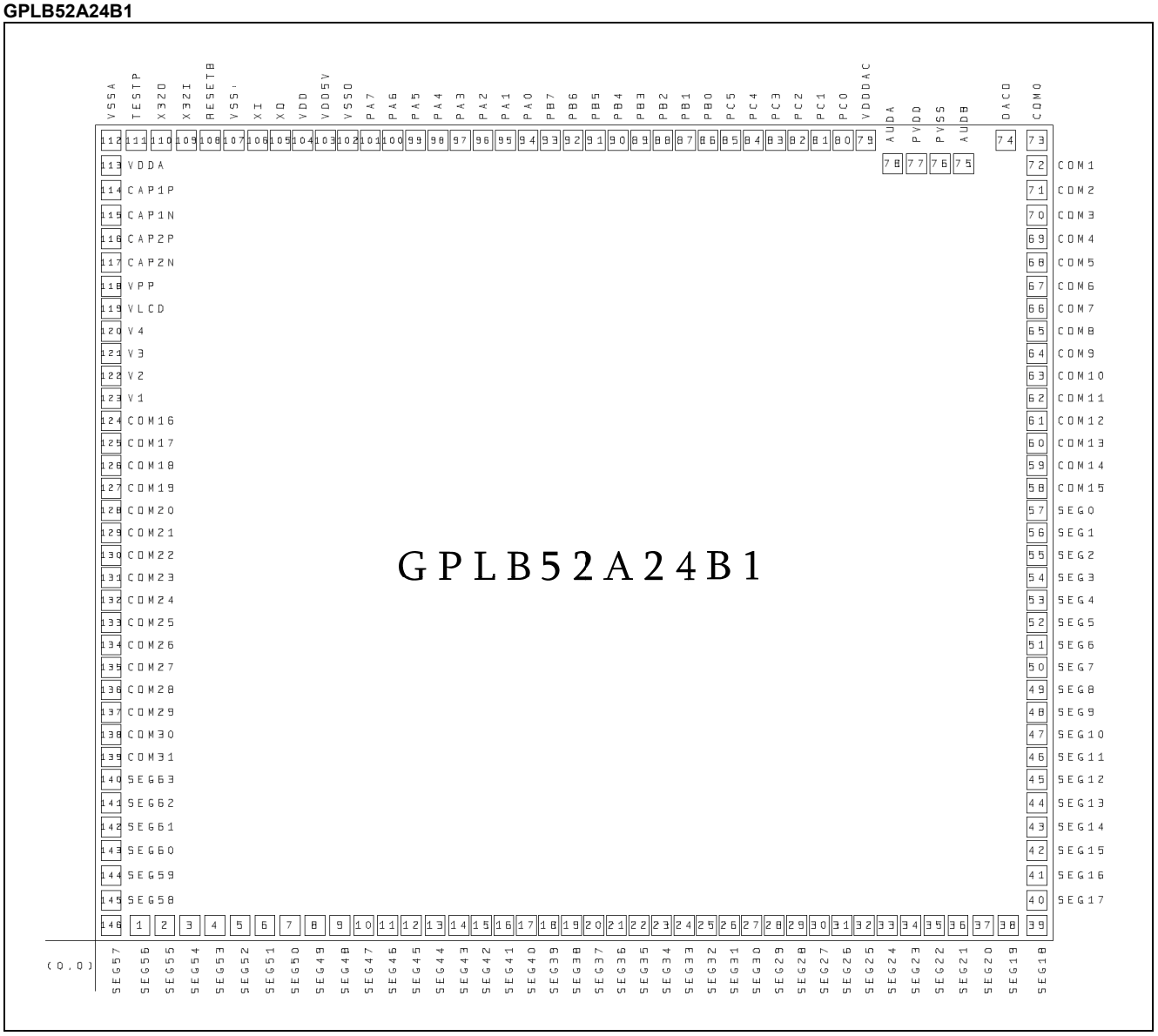
CAP2P, CAP2N	116,117	P	LCD voltage generation. Charge pump capacitor interconnection pins.
VOUT	118	P	LCD voltage generation. Voltage generated by charge pump.
V4	120	P	LCD voltage generation.
V3	121	P	LCD voltage generation.
V2	122	P	LCD voltage generation.
V1	123	P	LCD voltage generation.
VLCD	119	P	LCD voltage generation. The highest voltage for LCD display.
VDD5V	103	P	Positive supply for regulator input.
VSSO	102	P	Ground for regulator.
VDDA	113	P	Power for charge pump and IO pins.
VSSA	112	P	Ground for charge pump and IO pins.

Mnemonic	PIN No.	Type	Description
VDDDAC	79	P	Positive supply for DAC (3.3V), connect to VDD.
VDD	104	P	3.3V power output from regulator. Regulator can be turned off when external 3.3V is supplied.
VSS	107	P	Ground reference for logic.
PVDD	77	P	Positive supply for PWM driver.
PVSS	76	P	Ground reference for PWM driver and for DAC.

Legend: I = Input, O = Output, P = Power

5.3. PAD Assignment

GPLB52A24B1



This IC substrate should be connected to VSS or floated

Note: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

GPLB51A24B1

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6. FUNCTIONAL DESCRIPTIONS

6.1. Memories

The GPLB52A24B1/ GPLB51A24B1 contains 1M-byte ROM and 1536-byte SRAM.

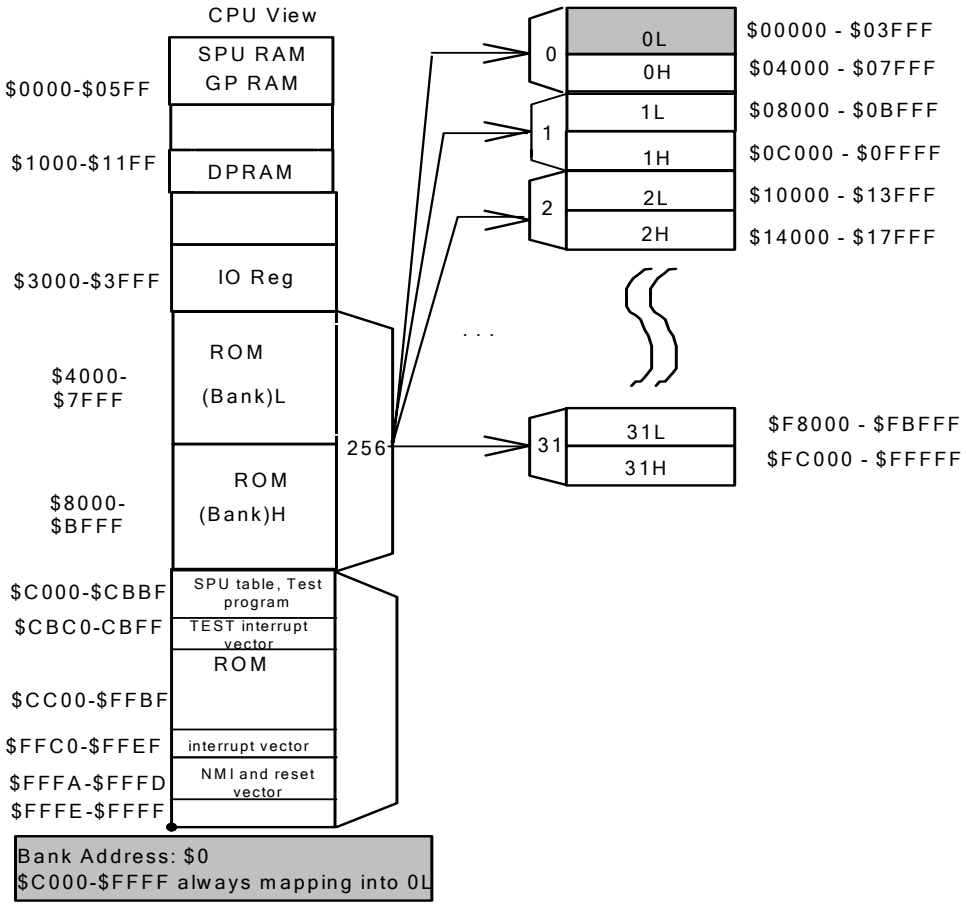
6.2. Map of Memory and I/Os

***NMI SOURCE:**

- LV DETECT
- TIMER1

***INT SOURCE:**

- TBL (2/4/8/16Hz)
- TBH (128/256/512/1KHz)
- TIMER0
- TIMER1
- SPI
- SPU
- FP (LCD frame)



1. User program should start from $CC00. $C000-$CBFF is the test program area. $C000-$C103 is SPU ADPCM table data.
2. User program interrupt vector: $FFC0 ~ $FFEF.
3. Test program interrupt vector: $CBC0 ~ $CBFF.

6.3. Operating States

There are three operation modes involved in GPLB52A24B1/ GPLB51A24B1 standby, halt and operating. The following table shows the differences between these modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

6.3.1. Operating mode

In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated. Generally speaking, this mode consumes the highest power.

6.3.2. Standby mode

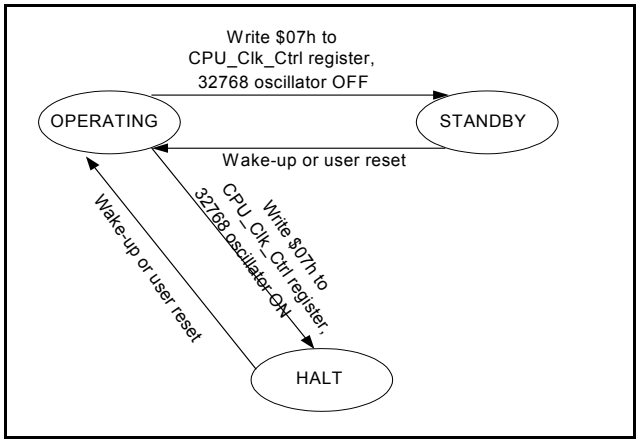
Write “07H” to P_3001H_ClkCtrl Register ($3001) and turn off 32768Hz oscillator to activate standby mode. The standby mode is a mode where the device is placed in its lowest current consumption state. In standby mode, all functions are turned off;

in addition, RAM and I/Os will remain in their previous states.

6.3.3. Halt mode

Write “07H” to P_3001H_ClkCtrl Register ($3001) but still keeps 32768Hz oscillator running to enter halt mode. In halt mode, CPU clock halts and waits for an event (e.g. key press, timer overflow) to wake up. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode.

The following figure is the GPLB52A24B1/ GPLB51A24B1 state diagram:



GPLB52A24B1/ GPLB51A24B1 State Diagram

6.4. Speech and Melody, PWM and DAC

The GPLB52A24B1/GPLB51A24B1 uses a high performance SPU voice engine to archive 8-channel voice with ADPCM/PCM code. The SPU also supports automatic zero-crossing concatenate function. A hardware multiplier is also embedded in this SPU for software usage. The fixed addresses of RAM area $0000 - $007F is designed as address pointers and a data buffer for the 8-channel speech/melody generation. There is one 12-bit D/A converter with 4mA driving current capability for audio output, DACO. There is one 10-bit PWM for audio outputs, AUDA and AUDB.

6.5. LCD Controller/Driver

The GPLB52A24B1/GPLB51A24B1 contains a 2048-dot LCD controller/driver and supports monochrome LCD control. Programmers are able to define the LCD configuration by setting up the LCD Control Register. Once the LCD configuration is completed, the desired pattern can be displayed by filling the LCD buffer with proper data. The LCD driver can also operate during sleep by keeping 32768Hz oscillator running. The LCD driver in GPLB52A24B1/GPLB51A24B1 supports 1/2 – 1/32 duty and 1/3 - 1/7 bias.

6.6. LCD Voltage Generation

To achieve highly integrated circuit and save external components as possible, the GPLB52A24B1/GPLB51A24B1 has built-in charge pump circuit and operational amplifiers to generate LCD’s bias voltages VLCD, V4, V3, V2 and V1. The charge pump circuit can generate VPP approx. to 8V. With VPP as power source, an operational amplifier is further to provide LCD panel’s power supply, VLCD. The level of VLCD can be adjusted by software. It is suggested that VLCD must be 0.7V higher than VDD or abnormal operation will occur.

6.7. Low Voltage Detection

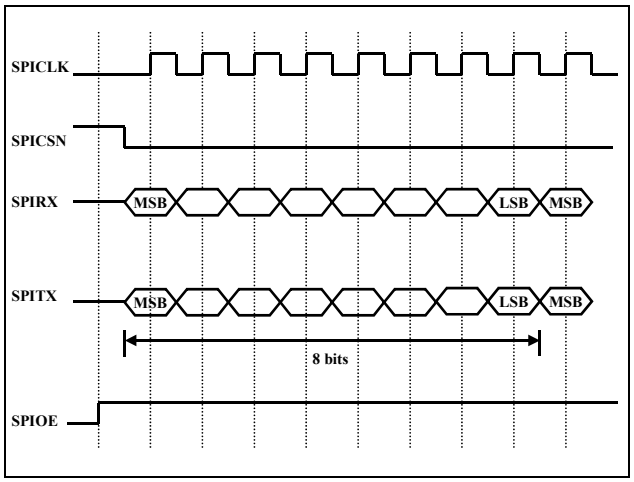
The GPLB52A24B1/GPLB51A24B1 provides a 4-level (Software programmable) low voltage detector to detect low voltage events. Users can turn on the low voltage detection that monitors VDD periodically to check whether it is lower than the given value. In addition, if LV NMI is enabled, an NMI will be issued to notify CPU if power voltage drops below the given value. Also, the voltage detector will generate a system reset if power supply voltage drops below 2.2V.

6.8. Watchdog Timer (WDT)

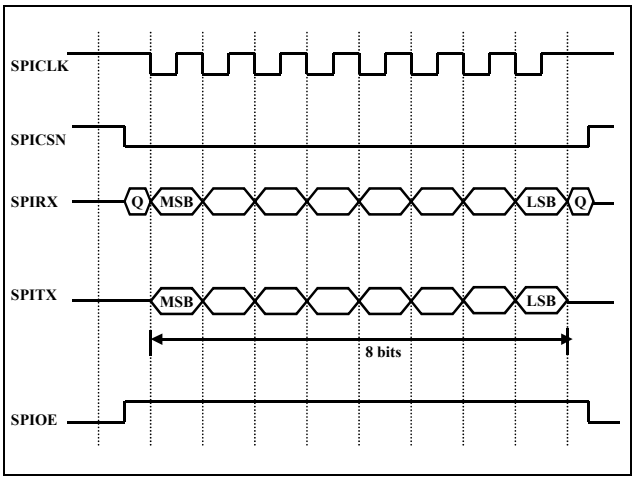
An on-chip watchdog timer is also available in the GPLB52A24B1/GPLB51A24B1. The WDT is designed to recover the system from unexpected operations. In some cases, if WDT is not cleared within one second, the WDT will generate a system reset to restart system. If WDT is enabled, the WDT should be cleared periodically to avoid accidental reset. The WDT can be cleared through software programming. Note that the WDT only works when 32768Hz clock is activated.

6.9. SPI Controller

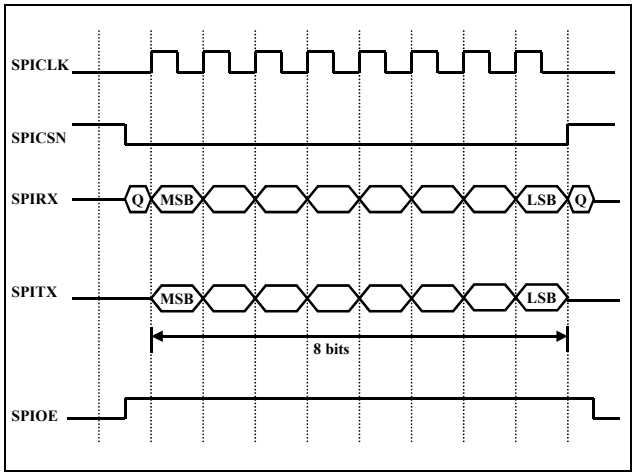
A Serial Peripheral Interface (SPI) controller is built in GPLB52A24B1/GPLB51A24B1 to facilitate communicating with other devices. There are four control signals on SPI including SPICSN, SPICLK (SCK), SPIRX (SDI), and SPITX (SDO). The four signals are shared with PortB4, PortB5, PortB6 and PortB7. While SPI module is enabled by corresponding control bit, these four pins cannot be GPIOs and any setting on corresponding GPIO control register will have no effect. Four types of operation mode are supported as follows:



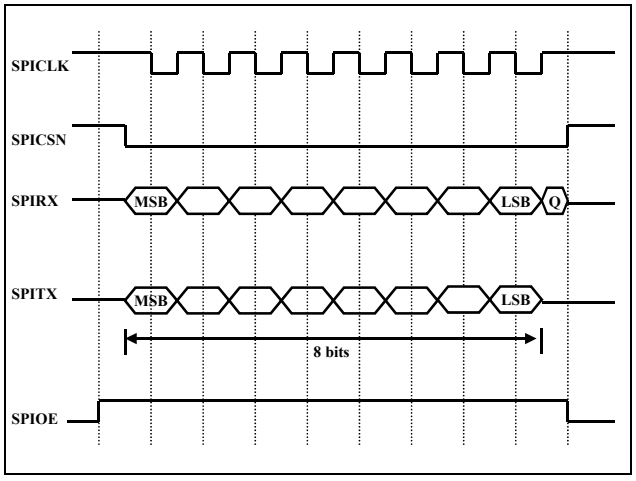
Master Mode, SPO = 0, SPH=0



Master Mode, SPO = 1, SPH=1



Master Mode, SPO = 0, SPH=1



Master Mode, SPO = 1, SPH=0

6.10. Mask Options

6.10.1. 32768Hz oscillator

1). X'TAL

2). R-oscillator

6.10.2. System clock oscillator

1). R-oscillator

2). X'TAL

6.10.3. Internal VDD regulator

1). Internal VDD regulator on

2). Internal VDD regulator off

6.10.4. LCD dots

1). 32 commons x 64 segments

2). 22 commons x 74 segments

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD5V=4.5V, for 3-battery application, internal regulator enabled output, T_A=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD5V	2.7	-	5.5	V	For 3-battery
Operating Current	I_{OP1}	-	5	-	mA	F_{CPU} = 6.0MHz @ 4.5V F_{XTAL} = 12.0MHz, no load, DAC disabled, PWM disabled.
	I_{OP2}	-	6	-	mA	F_{CPU} = 8.0MHz @ 4.5V F_{ROSC} = 16.0MHz, no load, DAC disabled, PWM disabled.
Halt Current	I_{HALT1}	-	40	-	μA	VDD5V = 4.5V, 32K X'tal ON, Strobe off, LCD ON, 1/7 Bias, VLCD=6.37V, no LCD panel.
	I_{HALT2}	-	15	-	μA	VDD5V = 4.5V, 32K X'tal ON, Strobe off, LCD OFF, no LCD panel.
Standby Current (Regulator on)	I_{STBYR}	-	-	10	μA	VDD5V = 4.5V, VDD regulator on, all off
PWM Audio Output Current	I_{OH}	-	-60	-	mA	VDD5V = 4.5V, V_{OH} = 4.05V
		-	-170	-	mA	VDD5V = 4.5V, V_{OH} = 3.15V
PWM Audio Output Current	I_{OL}	-	60	-	mA	VDD5V = 4.5V, V_{OL} = 0.45V
		-	160	-	mA	VDD5V = 4.5V, V_{OL} = 1.35V
Input High Level	V_{IH}	0.7VDD	-	-	V	VDD5V = 4.5V
Input Low Level	V_{IL}	-	-	0.3VDD	V	VDD5V = 4.5V
Output High Current (I/O)	I_{OH}	-7.0	-	-	mA	VDD5V = 4.5V, V_{OH} = 3.15V
Output Sink Current (I/O)	I_{OL}	4.0	-	-	mA	VDD5V = 4.5V, V_{OL} = 1.35V
Input Pull-Low Resistor PA(weak pull) PA(strong pull) PB,PC	R_{PL}	-	 200 65 65	-	KΩ	V_{IN} =4.5V
Input Pull-High Resistor PA(weak pull) PA(strong pull) PB,PC	R_{PH}	-	 240 45 45	-	KΩ	V_{IN} = 0V
LCD Driver Voltage	V_{LCD}	2.46	-	5.67	V	VDD5V = 4.5V, 1/5 bias, no load
(V_{LCD} - VSS)		2.93	-	6.75	V	VDD5V = 4.5V, 1/6 bias, no load
OSC Resistor	R_{OSC}	-	37	-	KΩ	F_{OSC} = 14MHz @ 4.5V
CPU Clock	F_{CPU}	-	-	8.0	MHz	F_{CPU} = F_{OSC}/2 @ 2.4V

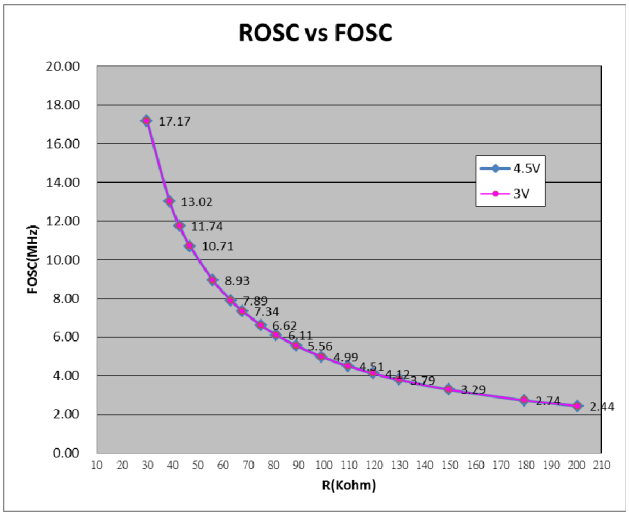
Note: V_{LCD} should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

7.3. DC Characteristics (VDD5V=VDD=3.0V, for 2-battery application, internal regulator output disabled, T_A=25℃)

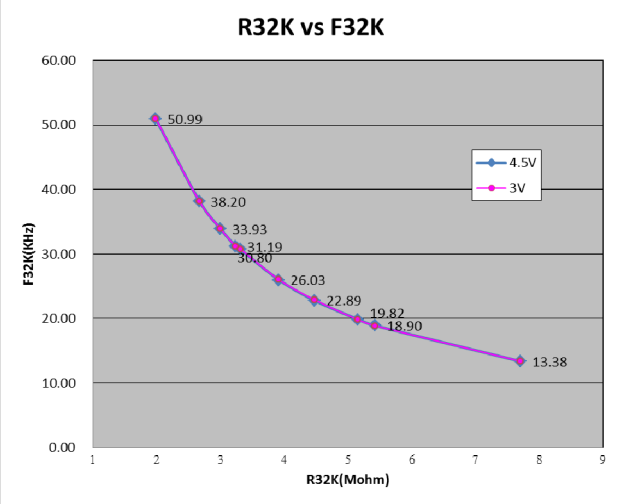
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD5V	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP1}	-	5	-	mA	F_{CPU} = 6.0MHz @ 3.0V F_{XTAL} = 12.0MHz, no load, DAC disabled, PWM disabled.
	I_{OP2}	-	6	-	mA	F_{CPU} = 8.0MHz @ 3.0V F_{ROSC} = 16.0MHz, no load, DAC disabled, PWM disabled.
Halt Current	I_{HALT1}	-	30	-	μA	VDD5V = 3.0V, 32K X'tal ON, Strobe off, LCD ON, 1/7 Bias, VLCD=6.37V, no LCD panel
	I_{HALT2}	-	10	-	μA	VDD5V = 3.0V, 32K X'tal ON, Strobe off, LCD OFF, no LCD panel
Standby Current (Regulator off)	I_{STBY}	-	1	2	μA	VDD5V = 3.0V, all off
PWM Audio Output Current	I_{OH}	-	-30	-	mA	VDD5V = 3.0V, V_{OH} = 2.7V
		-	-90	-	mA	VDD5V = 3.0V, V_{OH} = 2.1V
PWM Audio Output Current	I_{OL}	-	30	-	mA	VDD5V = 3.0V, V_{OL} = 0.3V
		-	80	-	mA	VDD5V = 3.0V, V_{OL} = 0.9V
Input High Level	V_{IH}	0.7VDD	-	-	V	VDD5V = 3.0V
Input Low Level	V_{IL}	-	-	0.3VDD	V	VDD5V = 3.0V
Output High Current (I/O)	I_{OH}	-3.0	-	-	mA	VDD5V = 3.0V, V_{OH} = 2.1V
Output Sink Current (I/O)	I_{OL}	3.0	-	-	mA	VDD5V = 3.0V, V_{OL} = 0.9V
Input Pull-Low Resistor PA(weak pull) PA(strong pull) PB,PC	R_{PL}	-	 165 55 55	-	KΩ	V_{IN} = 3.0V
Input Pull-High Resistor PA(weak pull) PA(strong pull) PB,PC	R_{PH}	-	 380 70 70	-	KΩ	V_{IN} = 0V
LCD Driver Voltage	V_{LCD}	2.46	-	5.67	V	VDD5V = 3.0V, 1/5 bias, no load
(V_{LCD} - VSS)		2.93	-	6.75	V	VDD5V = 3.0V, 1/6 bias, no load
OSC Resistor	R_{OSC}	-	37	-	KΩ	F_{OSC} = 14MHz @ 3.0V
CPU Clock	F_{CPU}	-	-	8.0	MHz	F_{CPU} = F_{OSC}/2 @ 2.4V

Note: V_{LCD} should be higher than VDD to prevent forward biasing the p-n junction of I/O output PMOS.

7.4. The Relationship between the R_{OSC} and the F_{OSC}, T_A = 25℃

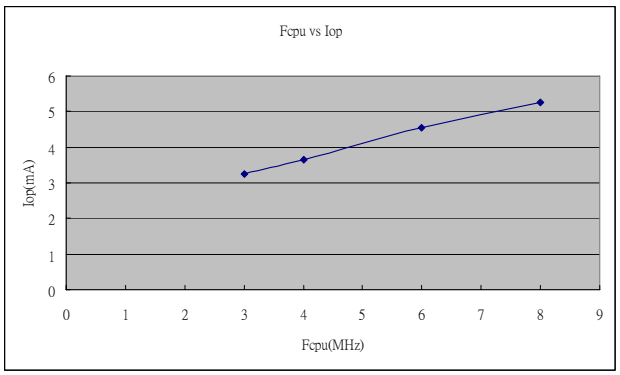


7.5. The Relationship between the F32K and the R32K , T_A = 25℃



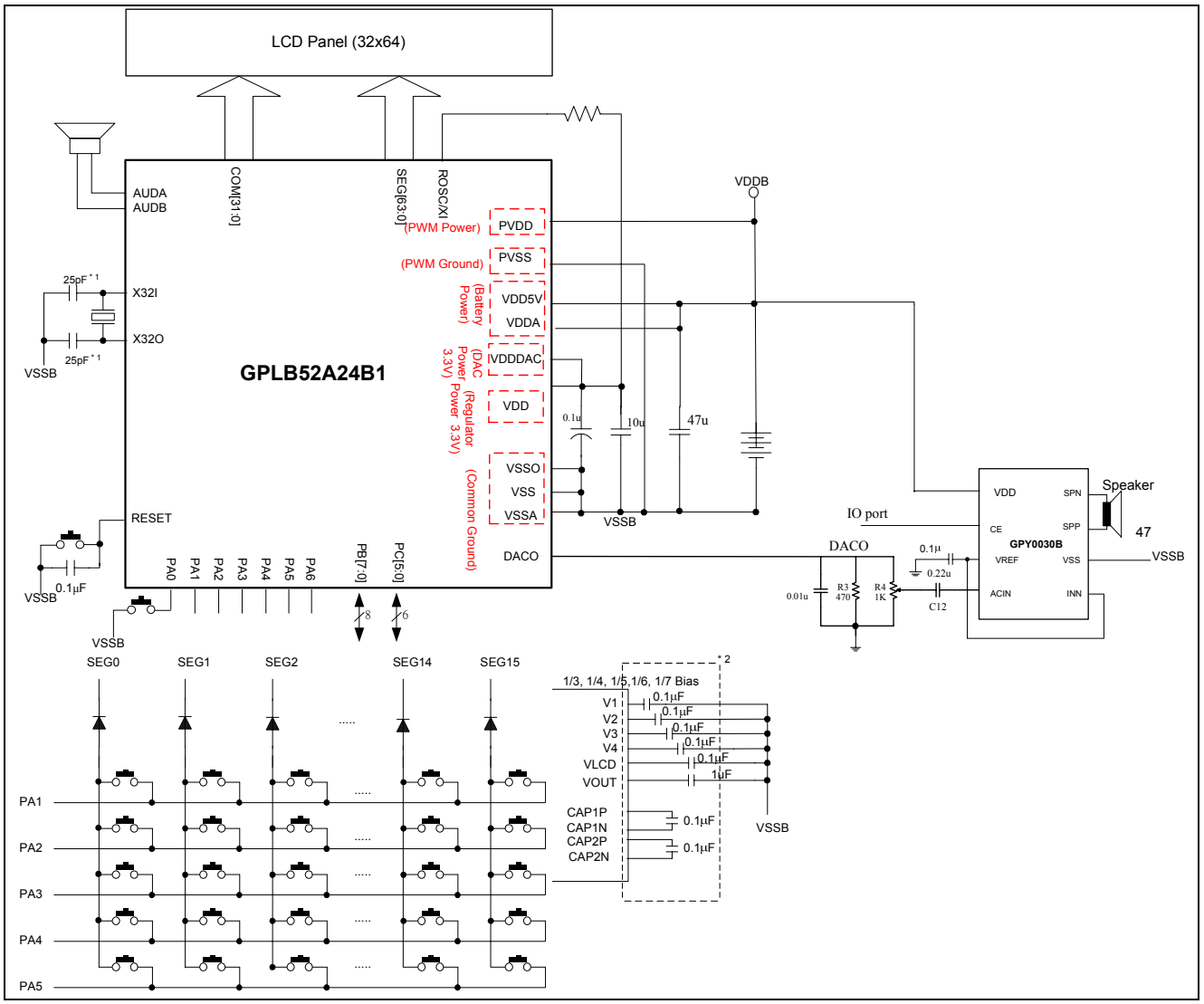
7.6. The Relationship between the F_{CPU} and the I_{OP}

7.6.1. VDD = 3.0V, T_A = 25℃



8. APPLICATION CIRCUITS

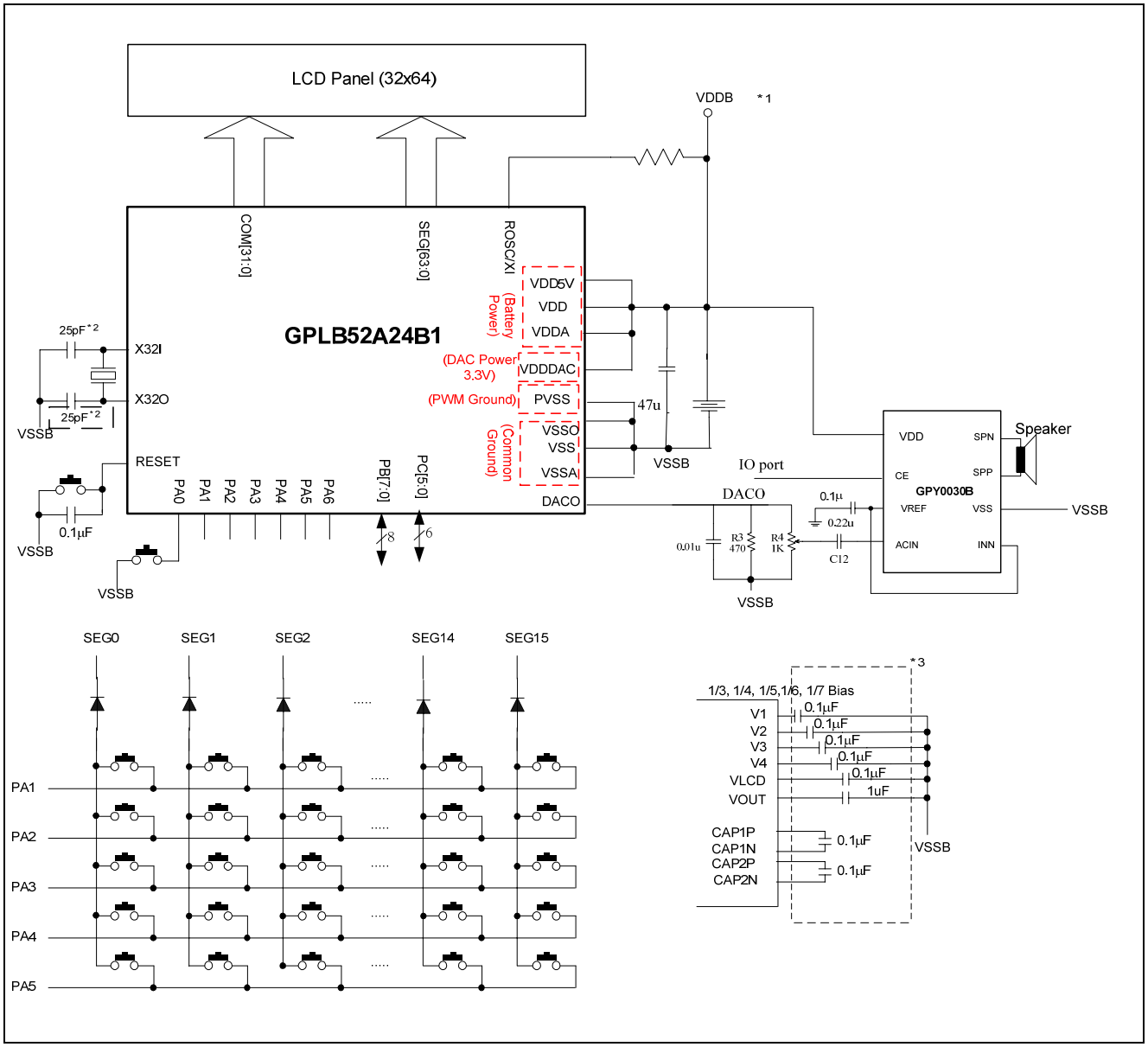
8.1. 2048 Dots LCD Driver, 64 Segments × 32 Commons, for 3-battery application, Internal 3.3V Regulator Enabled, 12-bit DAC Enabled, ROSC14M XTAL32K Selected- (1)



Note*1: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and CL1=CL2 =26~36pF (including PCB parasitic loading; for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF)

Note*2: These capacitor values are for design guidance only. The ratio of capacitance of VOUT to the capacitance of CAP1N/CAP1P/CAP2N/CAP2P is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and can't larger than capacitance of VOUT. But for larger LCD panel, 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for VOUT and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N is recommended.

8.2. 2048 Dots LCD Driver, 64 Segments × 32 Commons, Internal 3.3V Regulator Disabled, for 2-battery application, 12-bit DAC Enabled, ROSC14M XTAL32K Selected - (2)

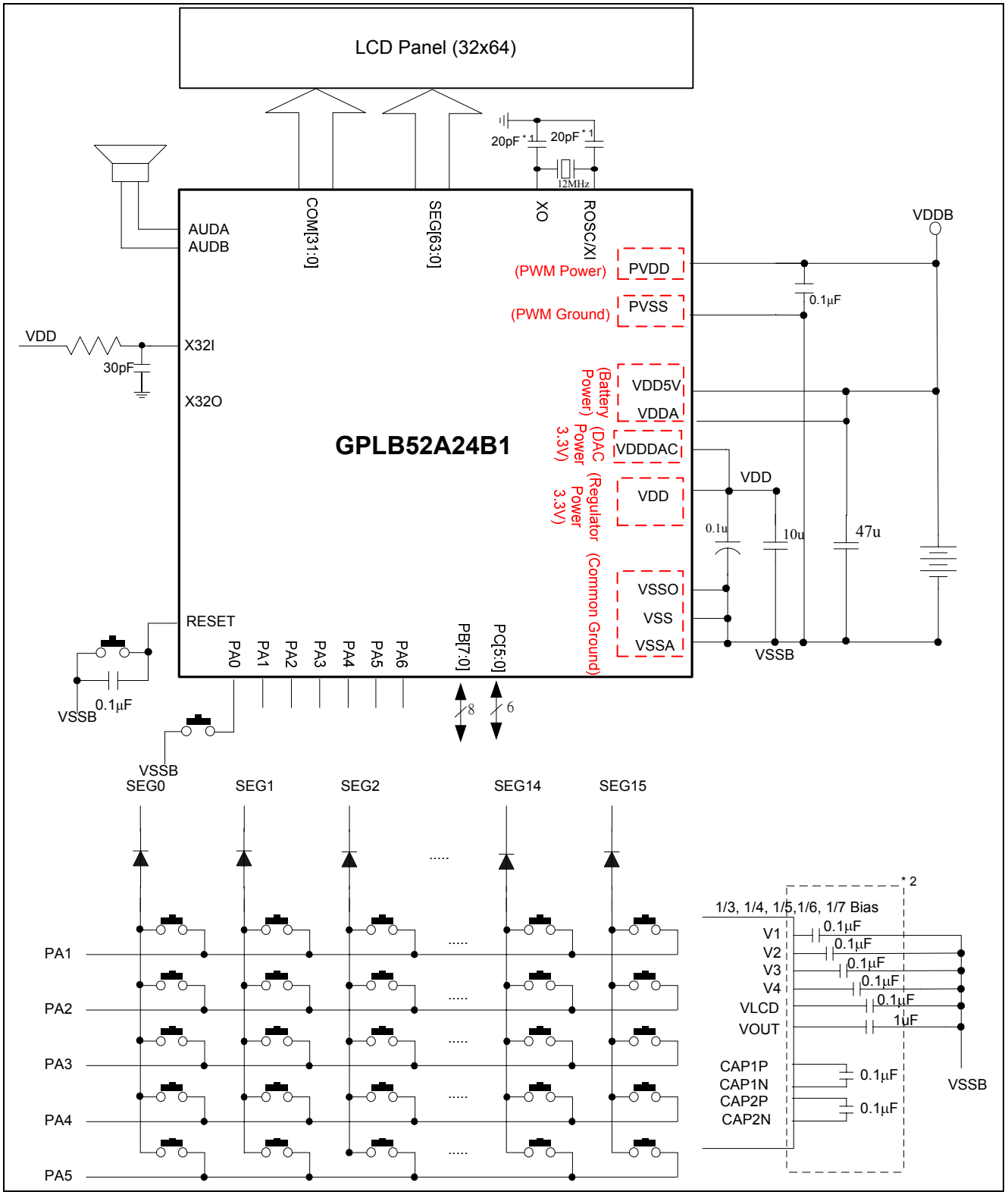


Note*1: VDD should not exceed 3.6V.

Note*2: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and CL1=CL2 =26~36pF (including PCB parasitic loading, for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF)

Note*3: These capacitor values are for design guidance only. The ratio of capacitance of VOUT to the capacitance of CAP1N/CAP1P/CAP2N/CAP2P is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and can't larger than capacitance of VOUT. But for larger LCD panel, 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for VOUT and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N is recommended.

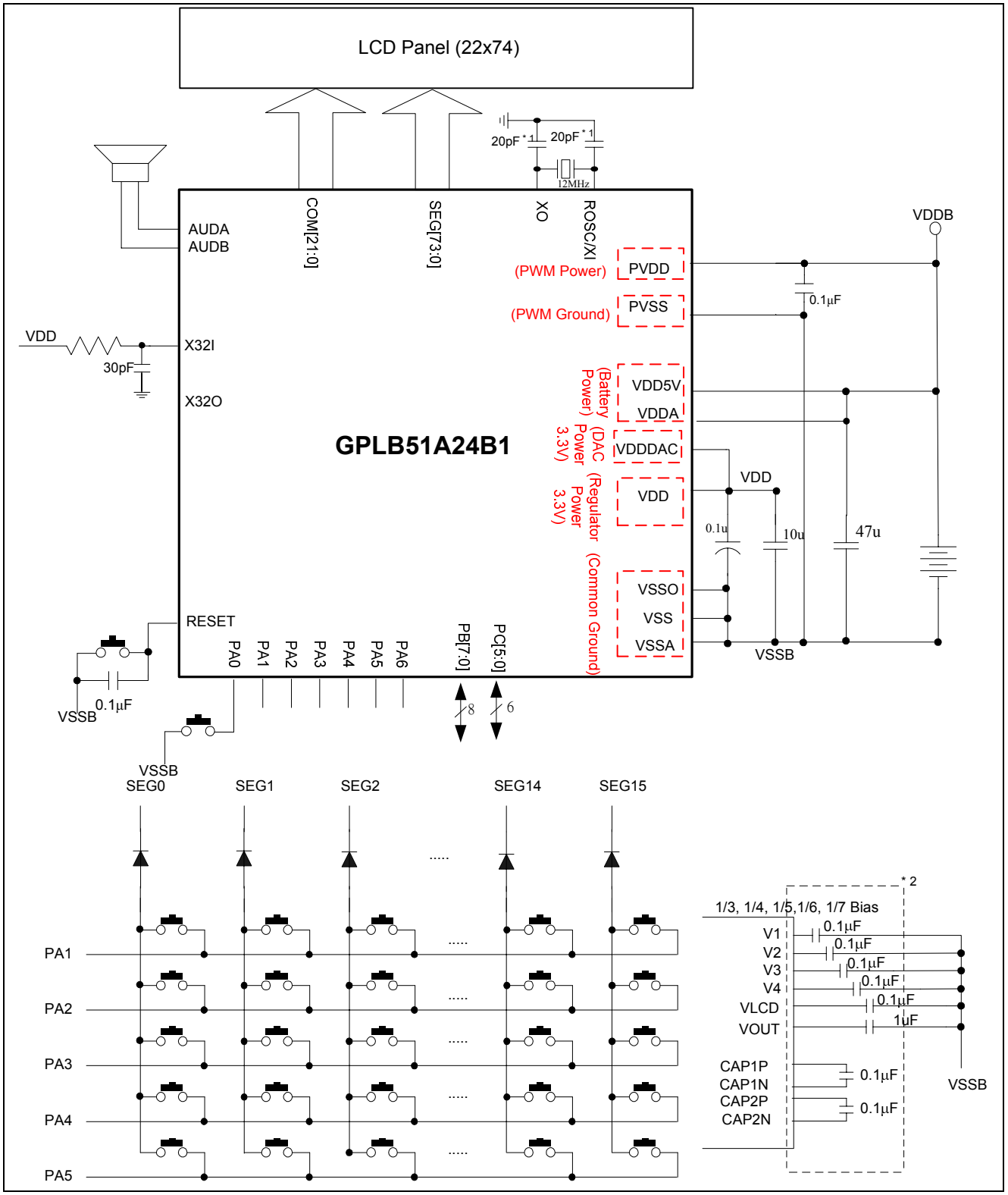
8.3. 2048 Dots LCD Driver, 64 Segments × 32 Commons, for 3-battery application, Internal 3.3V Regulator Enabled, 10-bit PWM Driver Enabled, XTAL12M ROSC32K Selected - (3)



Note*1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*2: These capacitor values are for design guidance only. The ratio of capacitance of VOUT to the capacitance of CAP1N/CAP1P/CAP2N/CAP2P is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and can't larger than capacitance of VOUT. But for larger LCD panel, 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for VOUT and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N is recommended.

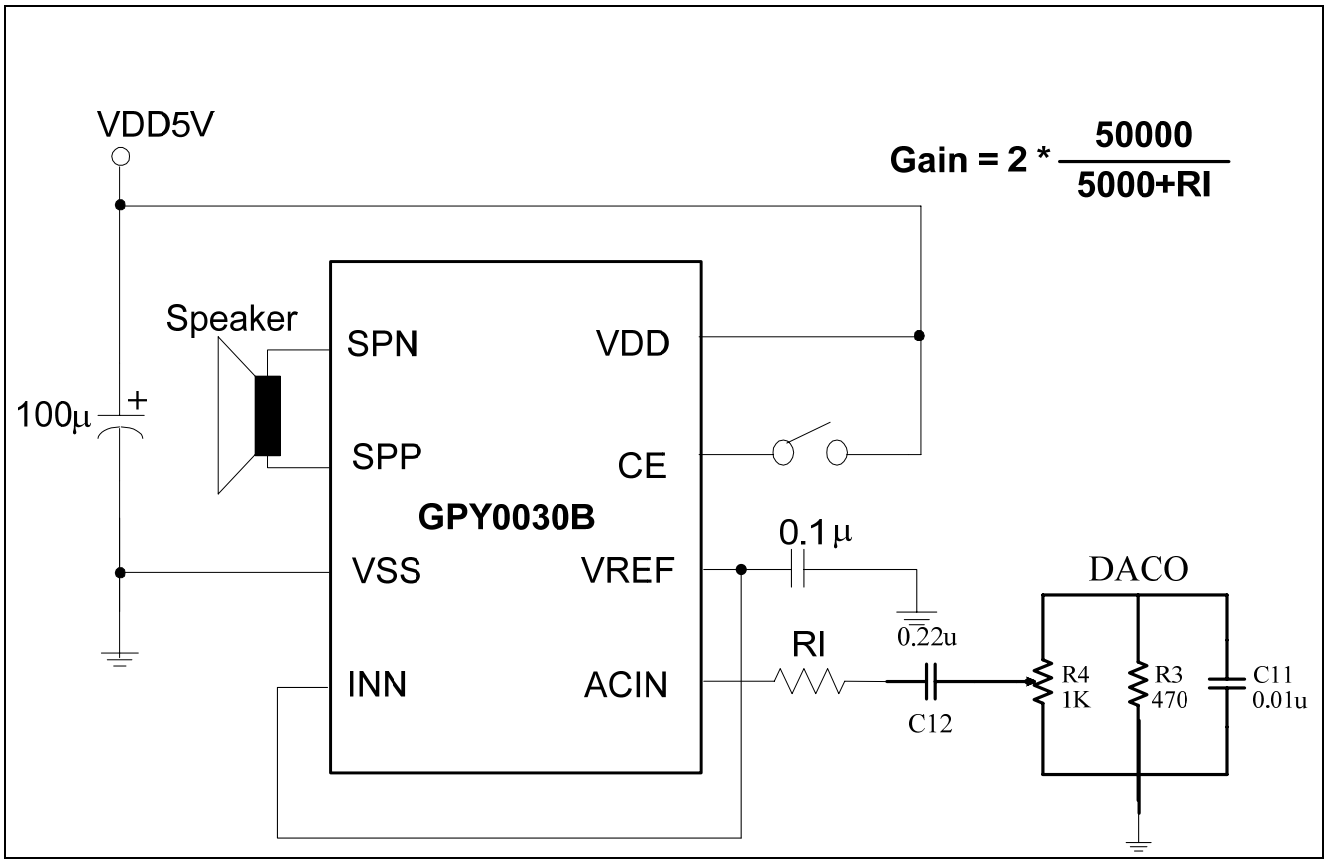
8.4. 1628 Dots LCD Driver, 74 Segments ×22 Commons, for 3-battery application, Internal 3.3V Regulator Enabled, 10-bit PWM Driver Enabled, XTAL12M ROSC32K Selected - (4)



Note*1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*2: These capacitor values are for design guidance only. The ratio of capacitance of VOUT to the capacitance of CAP1N/CAP1P/CAP2N/CAP2P is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and can't larger than capacitance of VOUT. But for larger LCD panel, 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for VOUT and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N is recommended.

8.5. DAC Output with Generalplus Audio Driver GPY0030B (for high quality audio output) - (4)



8.6. Current Mode DAC Speaker Driver with BJT

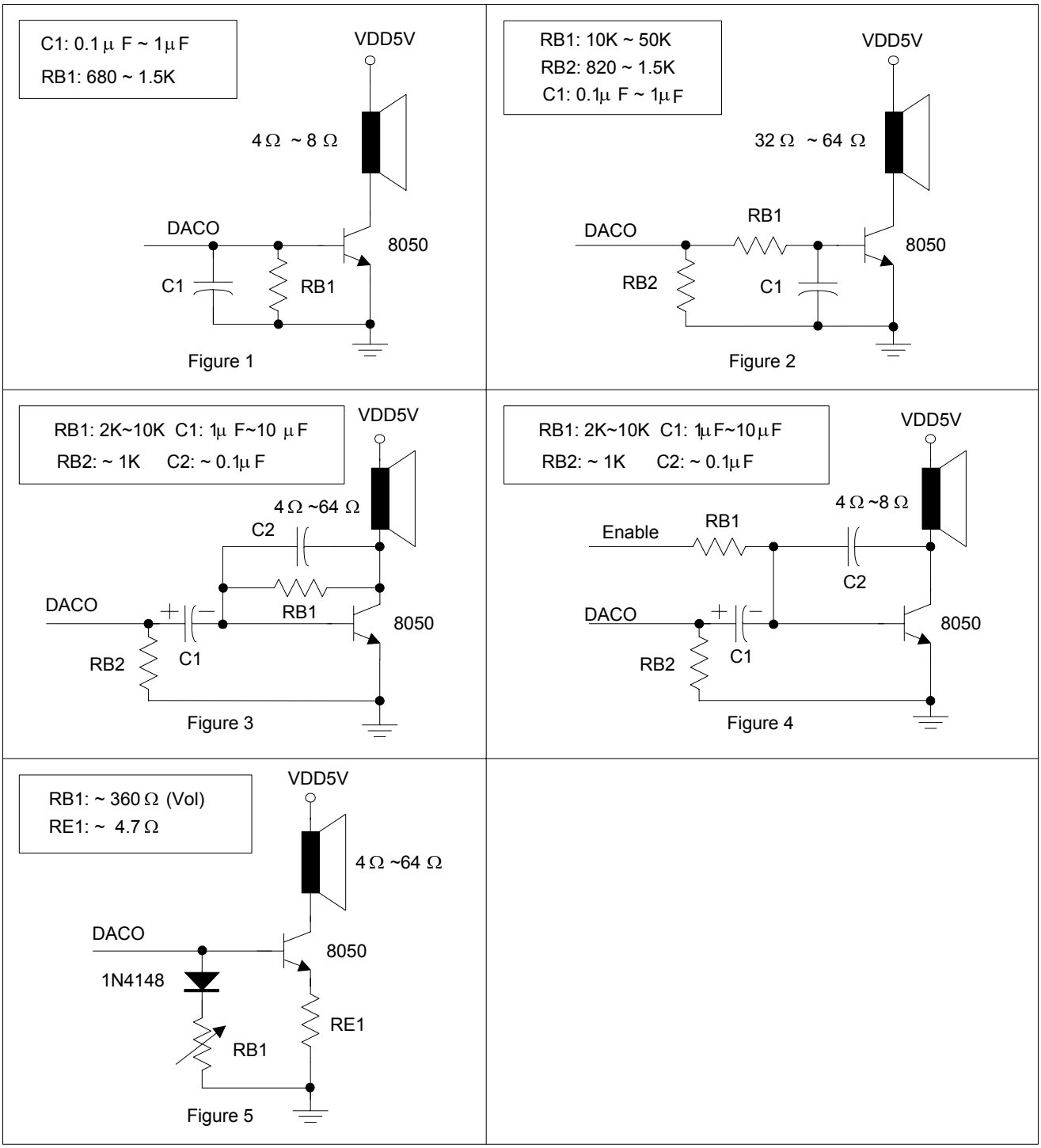
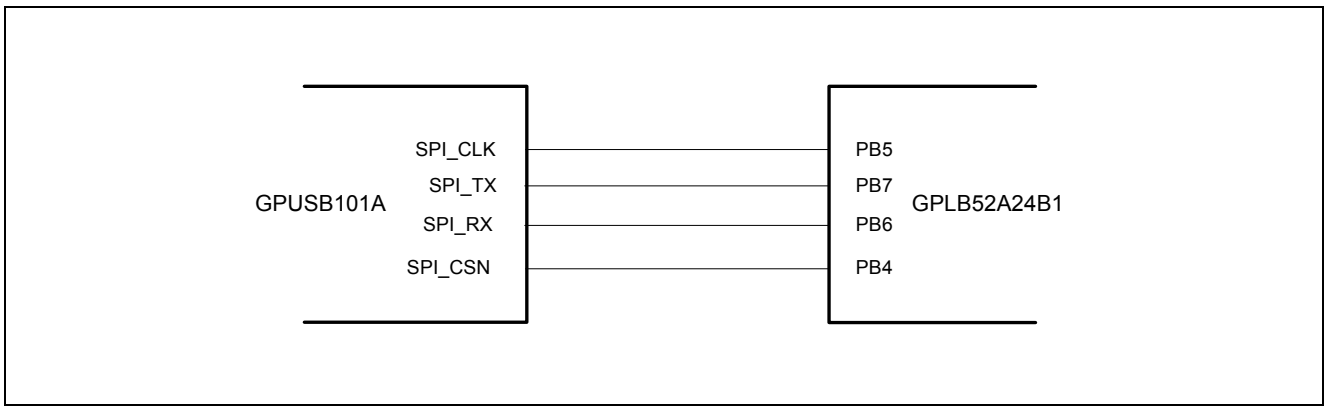


Figure 1: The simplest CKT uses with low impedance speaker. It has high operation current, but the cost is the cheapest.
Figure 2: It is the same as Figure 1 but a high impedance speaker is used.
Figure 3: The CKT has low pass filter. It can provide higher speech quality, but it always takes high operation current.
Figure 4: Improved version of Figure 3. The standby current can be controlled by enable pin.
Figure 5: The current mirror mode. It is able to control the volume. In addition, it has more stable and lower operation current than Figure 1-3.

8.7. Serial Communications between GPLB52A24B1/GPLB51A24B1 and GPUSB101A USB Controller- (6)



9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPLB51A24B1 - NnnV - C	Chip form
GPLB52A24B1 - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
Aug 20, 2013	1.2	update application circuit and it note for 32K XTAL	
Jun 14, 2012	1.1	Add section of 7.2~7.4	13
Jun. 10, 2011	1.0	Original	23