DATA SHEET

GPLD1080A

80 CHANNEL SEG/COM STN LCD DRIVER

MAY 23, 2007

Version 1.3

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80 Channel SEG/COM STN LCD Driver

1. GENERAL DESCRIPTION

The GPLD1080A is a 80-channel segment/common driver IC which is suitable for driving small/medium scale dot matrix LCD panels, and is used in hand-hold game or electronic dictionary. The GPLD1080A has seven modes that can be selected to set common and segment numbers by select pin. The GPLD1080A also has built-in DC/DC converter, voltage regulation and voltage follower to generate LCD driver voltage.

2. FEATURES

- Number of LCD drive outputs : 80
- Supply voltage for LCD drive: 12V (max.)
- Supply voltage for logic system: 2.4V to 5.5V
- 3-types LCD combination selectable by input pins

CS1	CS0	Configuration	Bias
0	0	48 COM * 32 SEG	1/8
0	1	64 COM * 16 SEG	1/9
1	1	80 COM	1/10

- Built-in DC-DC, Voltage Regulator and Voltage Follower
- Abundant command functions
- LCD bias set, electronic volume
- Shift data clock frequency
  - 6 MHz (max.) : V_{DD} = 2.4 V ~ 5.5 V
- 4 bit parallel / serial modes are selectable by PS pin.

3. PIN DESCRIPTIONS

Mnemonic	Type	Description
Y_{80-1}	O	LCD driver output pins.
V_0 ~ V_4	P	The bias voltages for LCD driving. Where V_{OUT} >V_0>V_1>V_2>V_3>V_4>$V_{SS.}$
FB	I	Gain adjustment input of V_0. By adjusting the R_A, R_B ratio between V_0, FB and $V_{SS,}$ the LCD driving voltage, V_0 is equal to V_{REF} (1+ R_B/R_A). Where the V_{REF} is the internal reference voltage.
VDD	P	Power supply for logic circuit. (+ 2.4V to + 5.5V)
EI	I	AT com/seg mix mode, when EI='H' the bus data DI_3 ~ DI_0 be accessed.
EO	O	Enable GPLD2080A signal
DI_3 ~ DI_0	I	Display data input at com/segment mode. 1). In 1-bit parallel input mode (PS="L"), input data into the 1 pins DI_0. Connect DI_{3-1} to VSS or VDD. 2). In 4-bit parallel input mode (PS="H"), input data into the 4 pins, DI_3 - DI_0.
DISOFFB	I	Display Off control input pin. Control input pin for output non-select level. When set to V_{SS}, the LCD drive output pins (Y_{0-79}) are set to level V_{SS}.
CP	I	Clock input for taking display data at com/seg mix mode. 1). Data is read at the falling edge of the clock pulse.
LP	I	Latch pulse input for display data at segment mode. Shift clock input for shift register at common mode. 1). Data is latched at the rising edge of the clock pulse.
M	I	AC converting signal input for LCD drive waveform.
FP	I	COMMOM data input
PS	I	Data input mode select pin. 1). When set to VSS, 1-bit parallel input mode is set. 2). When set to VDD, 4-bit parallel input mode is set.
VSS	I	Ground (0V).
VDDA	P	Power supply for analog circuit. (+ 2.4V to + 5.5V)

<table>
<tr><th>Mnemonic</th><th>Type</th><th>Description</th></tr>
<tr><td>VSSA</td><td>P</td><td>Ground (0V) for analog circuit</td></tr>
<tr><td>VSSH</td><td>P</td><td>Ground (0V) for driver circuit</td></tr>
<tr><td>CAP1</td><td>O</td><td>DC-DC voltage converter, capacitor for charge pump.</td></tr>
<tr><td>CAN1</td><td>O</td><td>DC-DC voltage converter, capacitor for charge pump.</td></tr>
<tr><td>CAP2</td><td>O</td><td>DC-DC voltage converter, capacitor for charge pump.</td></tr>
<tr><td>CAN2</td><td>O</td><td>DC-DC voltage converter, capacitor for charge pump.</td></tr>
<tr><td>CAP3</td><td>O</td><td>DC-DC voltage converter, capacitor for charge pump.</td></tr>
<tr><td>CAP4</td><td>O</td><td>DC-DC voltage converter, capacitor for charge pump.</td></tr>
<tr><td>CAP5</td><td>O</td><td>DC-DC voltage converter, capacitor for charge pump.</td></tr>
<tr><td>V_{OUT}</td><td>O</td><td>DC-DC voltage converter.</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial clock input pin for command decoder. Built-in pull high resister 100Kohm to VDD.</td></tr>
<tr><td>SDI</td><td>I</td><td>Serial data input pin for command decoder. Built-in pull high resister 100Kohm to VDD.</td></tr>
<tr><td>CS1 ~CS0</td><td>I</td><td>3-types LCD combination selectable by CS1 ~ CS0
<table>
<tr><td>CS1</td><td>CS0</td><td>Configuration</td><td>Bias</td></tr>
<tr><td>0</td><td>0</td><td>48 COM * 32 SEG</td><td>1/8</td></tr>
<tr><td>0</td><td>1</td><td>64 COM * 16 SEG</td><td>1/9</td></tr>
<tr><td>1</td><td>1</td><td>80 COM</td><td>1/10</td></tr>
</table>
</td></tr>
</table>

4. FUNCTIONAL DESCRIPTIONS

4.1. Segment outputs

M	Latch data	DISOFFB	Driver Output Voltage Level
L	L	H	V_2
L	H	H	V_0
H	L	H	V_3
H	H	H	V_{SS}
X	X	L	V_{SS}

4.2. Common outputs

M	Latch data	DISOFFB	Driver Output Voltage Level
L	L	H	V_1
L	H	H	V_{SS}
H	L	H	V_4
H	H	H	V_0
X	X	L	V_{SS}

Note1: $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_0$, L: VSS (0V), H: VDD (+2.4V to +5.5V), X: Don't care.

Note2: "Don't care" should be fixed to "H" or "L", avoiding floating. There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supply regular voltage which is assigned by specification for each power pin.

4.3. Mix mode (common/segment mode)

When (CS1, CS0) = (0, 0) → Select 48 com/32 seg mode

4.4. Segment side of mix mode (48COMX32SEG)

(A) 4-bit parallel mode

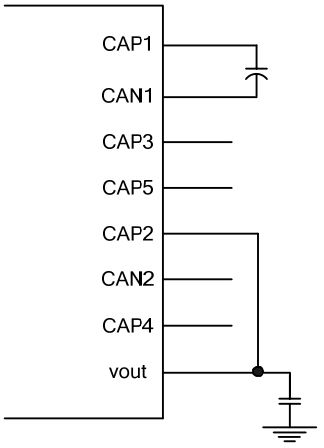
Input Data	Figure of Clock								
	8 Clock	7 Clock	6 Clock	• • •	• • •	• • •	3 Clock	2 Clock	1 Clock
DI_0	Y_{48}	Y_{52}	Y_{56}	• • •	• • •	• • •	Y_{68}	Y_{72}	Y_{76}
DI_1	Y_{49}	Y_{53}	Y_{57}	• • •	• • •	• • •	Y_{69}	Y_{73}	Y_{77}
DI_2	Y_{50}	Y_{54}	Y_{58}	• • •	• • •	• • •	Y_{70}	Y_{74}	Y_{78}
DI_3	Y_{51}	Y_{55}	Y_{59}	• • •	• • •	• • •	Y_{71}	Y_{75}	Y_{79}

(B) 1-bit serial mode

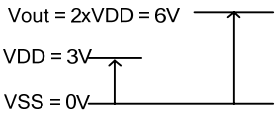
Input Data	Figure of Clock								
	32 Clock	31 Clock	30 Clock	• • •	• • •	• • •	3 Clock	2 Clock	1 Clock
DI_0	Y_{48}	Y_{49}	Y_{50}	×	×	×	Y_{77}	Y_{78}	Y_{79}

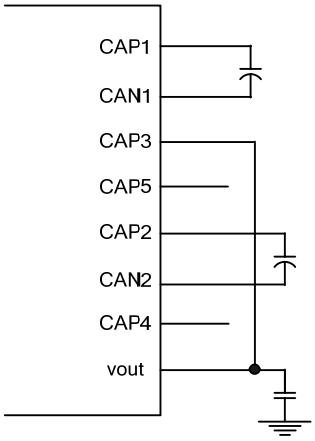
4.5. Booster Circuit

Using the booster voltage circuits equipped within the GPLD1080A chips, it is possible to product 2X/3X/4X/5X/6X step-up of the (V_{DD} - V_{SS}) voltage levels.

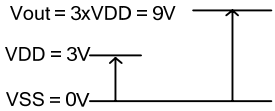


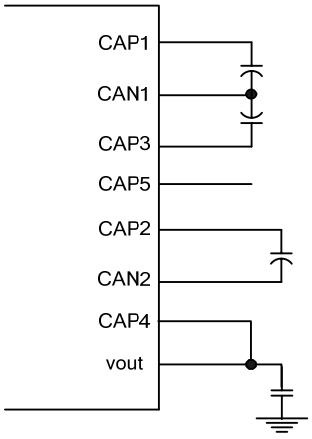
2 x (VDD-VSS)



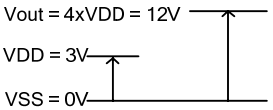


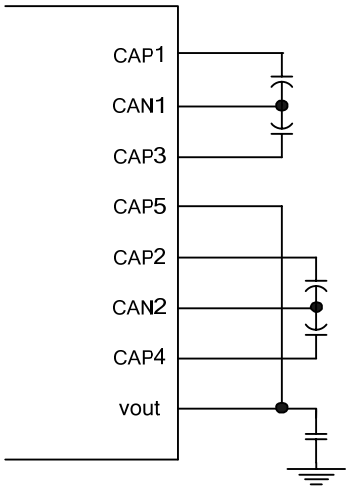
3 x (VDD-VSS)



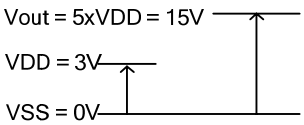


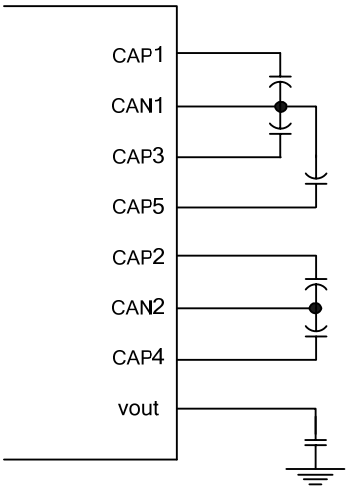
4 x (VDD-VSS)



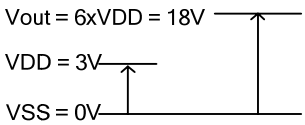


5 x (VDD-VSS)





6 x (VDD-VSS)



Note: all the capacitors value is 1uF

Please keep this relation: V_{OUT} – V0 > 2V

V_{OUT} will be clamped about 15.6V

4.6. Regulator Circuits

The booster voltage generated at V_{OUT} outputs, the liquid crystal driver voltage V_0 through the voltage regulator circuit. Because the GPLD1080A chips have an internal high-accuracy fixed voltage power supplies with a 32-level electronic volume function for the V_0 voltage regulator.

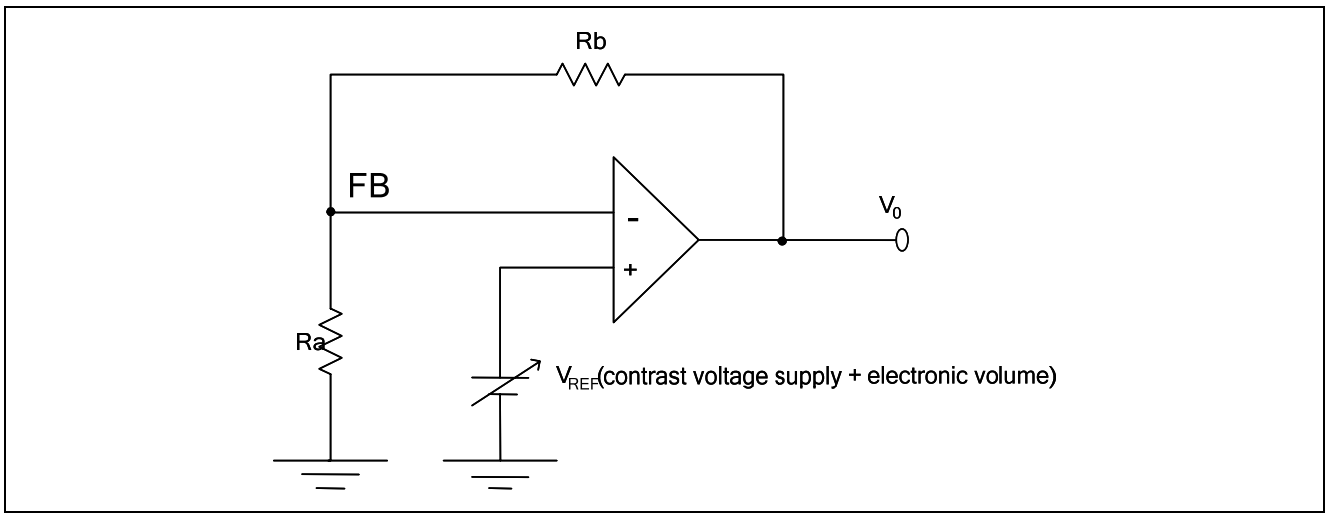
4.7. When the V_0 voltage regulator with external resistors are used

Through the use of the V_0 voltage regulator, external resistors and the electronic volume function, the liquid crystal power supply voltage, V_0, can be controlled by command alone, making it possible to adjust the liquid crystal display brightness. The V_0 voltage can be calculated by using equation E-1 over the range where $|V_0| < |V_{OUT}| - 2V$

The Rb and Ra are external resisters.

$V_0 = (1 + Rb/Ra) \bullet V_{REF}$

$= (1 + Rb/Ra) \bullet (1 - \alpha/220) \bullet 2.2$ -------- E-1



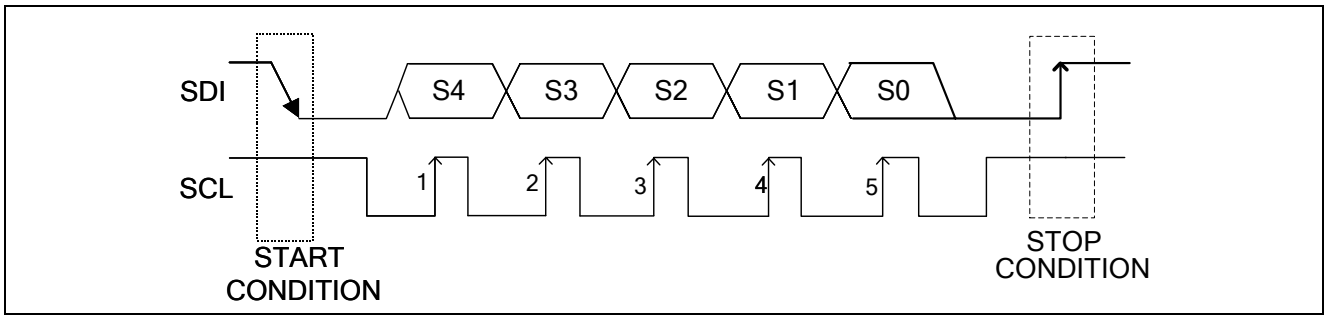
V_{REF} is the IC-internal fixed voltage supply and its voltage at T_A = 25°C is 2.04V. When use default value $\mathbf{S_4}$~$\mathbf{S_0}$.

For power saving please selection Rb > 1000Kohm (saving DC current from V0 through Rb, Ra to ground) α is set to 0 level of 31 possible levels by the electronic volume function depending on the data set in the 5-bit electronic volume register. The following table shows the value for depending on the electronic volume register settings.

S_4	S_3	S_2	S_1	S_0	α
0	0	0	0	0	31
0	0	0	0	1	30
0	0	0	1	0	29
:	:	:	:	:	:
0	1	1	1	1	16(default)
1	1	1	0	1	2
1	1	1	1	0	1
1	1	1	1	1	0

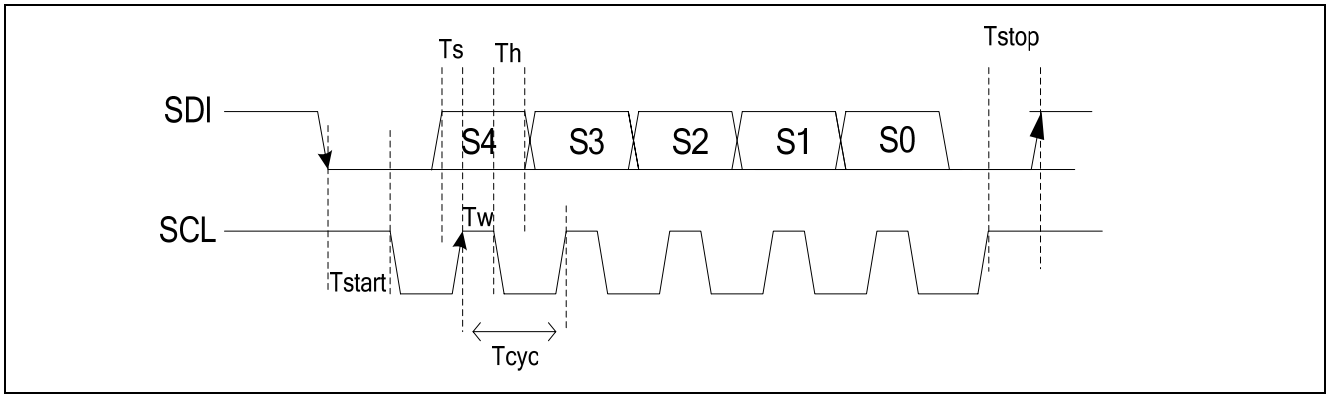
5. COMMAND DESCRIPTION

By setting SDI to “Low” and SCL to “High”, GPLD1080A is able to receive serial input data. Serial data is input in the order of “S4, S3, S2, S1, S0” from the serial data input pin (SDI) at the rising edge of serial clock (SCL). After the 5-bit data have been read into the shift register, the shift register will automatically convert serial data to change V0 voltage.



Timing Diagram of Serial Data Transfer

5.1.1. Timing characteristic of command interface:



Parameter	Symbol	Min.	Typ.	Max.	Unit
The Hold Time of SDI Falling to SCL Falling	Tstart	100	-	-	ns
SCL Period	Tcyc	200	-	-	ns
SCL High Width	Tw	50	-	-	ns
SCL Setup Time in Order to Latch SDI Data	Ts	50	-	-	ns
SDI Hold Time That Is from SCL Falling to SDI Change	Th	50	-	-	ns
SCL Rising to SDI Rising in Order to Load Data to Register	Tstop	50	-	-	ns

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable Pins	Ratings	Unit
Supply Voltage (1)	VDD	T_A = +25℃ Referenced to VSS (0V)	VDD	-0.3 to +6.5	V
Supply Voltage (2)	V_0		V_0	-0.3 to +16	V
	V_1		V_1	-0.3 to V0 + 0.3	V
	V_2		V_2	-0.3 to V0 + 0.3	V
	V_3		V_3	-0.3 to V0 + 0.3	V
	V_4		V_4	-0.3 to V0 + 0.3	V
Input Voltage	V_I		DI_{3-0}, CP, LP,M, PS, CS1,CS0, FP,SCL,SDI,EI, DISOFFB	-0.3 to VDD + 0.3	V
Storage Temperature	T_{STG}	-	-	-45 to + 125	℃

Note1: T_A = +25℃

Note2: The maximum applicable voltage on any pin with respect to VSS (0V).

Note3: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Supply Voltage (1)	VDD	Referenced to VSS (0V)	VDD	+2.4	-	+5.5	V
Supply Voltage (2)	V_0		V_0	+8	-	+12	V
Operating Temperature	T_{OPR}	-	-	-20	-	+75	℃

Note1: The applicable voltage on any pin with respect to VSS (0V).

Note2: Ensure that voltage are set such that $VSS < V_4 < V_3 < V_2 < V_1 < V_0$

6.3. DC Characteristics

6.3.1. COM/Segment mode (VSS = 0V, VDD = +2.4V to +5.5V, V_0 = +8V to +12V, T_A = +25℃)

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Input Voltage	V_{IH}	-	DI_{3-0}, CP, LP, M, PS, FP CS1,CS0, SCL, SDI, DISOFFB,EI	0.8VDD	-	-	V
	V_{IL}	-		-	-	0.2VDD	V
Output Voltage	V_{OH}	I_{OH} = -0.4mA	EO	VDD - 0.4	-	-	V
	V_{OL}	I_{OL} = +0.4mA		-	-	+0.4	V
Input Leakage Current	I_{LIH}	V_I = VDD	DI_{3-0}, CP, LP, M, PS,FP,CS1,CS0, SCL, SDI,EI DISOFFB	-	-	+1.0	μA
	I_{LIL}	V_I = VSS		-	-	-1.0	μA
Output Resistance	R_{ON}	$\lvert\triangle V_{ON}\rvert$ = 0.5V, V_0 = +12V	Y_{79-0}	-	1.0	2.0	KΩ
Stand-by Current	I_{STB}	DISOFFB=VSS	VDD	-	-	1.0	μA
Operation Current Consumption	I_{DD}	*1	VDD	-	100	-	μA

Note1: 48COM X 32SEG, VDD = 3.0V, V_0 = 8V(Rb=1000Kohm, Ra=342Kohm), V_{OUT}=9V, f_{CP} = 1MHz, No-load, E_I = VDD. The input data is turned over by data taking clock (4-bit parallel input mode).

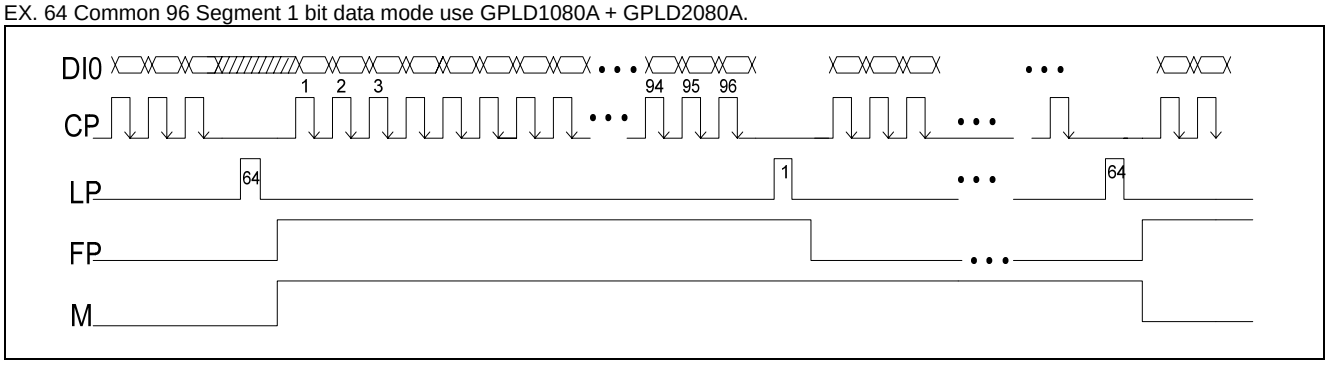
6.3.2. Common mode (VSS = 0V, VDD = +2.4V to +5.5V, V0 = +8V to +12V, T_A = +25℃)

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Input Voltage	V_{IH}	-	LP, M, FP,PS,CS1,CS0, SCL, SDI, DISOFFB	0.8VDD	-	-	V
	V_{IL}	-		-	-	0.2VDD	V
Output Voltage	V_{OH}	I_{OH} = -0.4mA	EO	VDD - 0.4	-	-	V
	V_{OL}	I_{OL} = +0.4mA		-	-	+0.4	V
Input Leakage Current	I_{LIH}	V_I = VDD	DI_{3-0}, CP, LP, M, PS, CS1,CS0, SCL, SDI, DISOFFB	-	-	+1.0	μA
	I_{LIL}	V_I = VSS		-	-	-1.0	μA
Output Resistance	R_{ON}	$\|\triangle V_{ON}\|$ = 0.5V, V_0 = +12V	Y_{79-0}	-	1.0	2.0	KΩ
VLCD Accuracy	V_0	Rb=1000k, Ra=240k	V_0	-1	-	+1	%
Stand-by Current	I_{STB}	DISOFFB=VSS	VDD	-	-	1	μA
Operation Current Consumption	I_{DD}	*1	VDD	-	200	-	μA

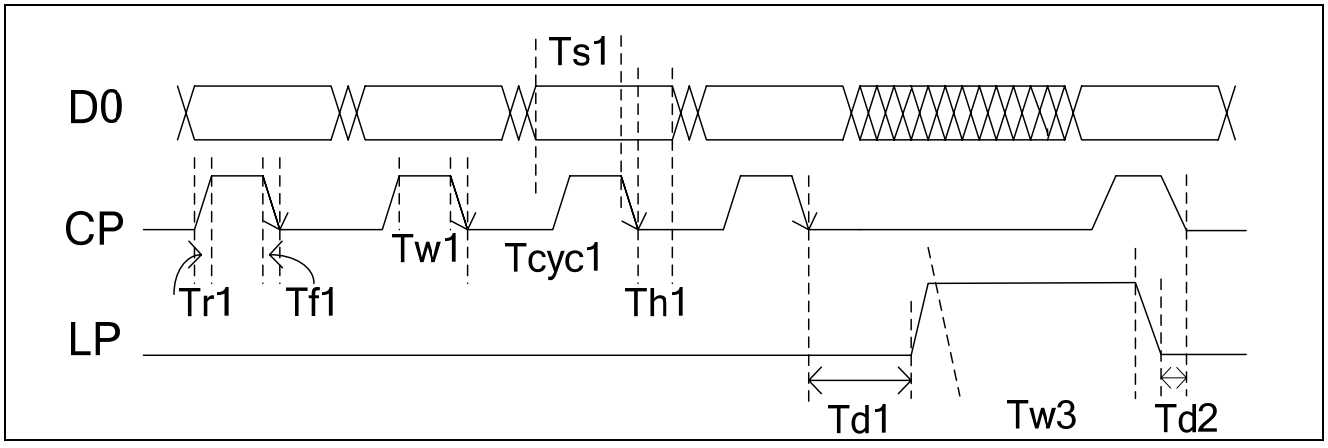
Note1: VDD = +3.0V, V_0 = +10.5V(Rb=1000Kohm, Ra=240Kohm), V_{OUT}=12V, f_{LP} =6.0 KHz, f_M = 35Hz in case of 1/80 duty operation, no-load.

6.4. AC Characteristics:

EX. 64 Common 96 Segment 1 bit data mode use GPLD1080A + GPLD2080A.



6.4.1. LCD control signal timing characteristic:



Parameter	Symbol	Min.	Typ.	Max.	Unit
CP Rising Time	Tr1	-	-	5	ns
CP Falling Time	Tf1	-	-	5	ns
CP Clock High Plus Width	Tw1	80	-	-	Ns
CP Clock Period	Tcyc1	160	-	-	Ns
The Setup Time That CP Clock Latch Data	Ts1	50	-	-	Ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
The Hold Time That CP Clock Latch Data	Th1	50	-	-	ns
The Delay Time from CP Falling to LP Rising	Td1	30	-	-	ns
The Timing from LP Falling to CP Falling	Td2	10	-	-	ns
LP Clock High Plus Width	Tw3	80	-	-	ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
LP Signal Rising Time	Tr2	-	-	5	ns
LP Signal Falling Time	Tf2	-	-	5	ns
LP Falling to FP Rising	Td3	0	-	-	ns
The Setup Time for LP to Latch FP	Ts2	200	-	-	ns
LP Pulse Width	Tw2	100	-	-	ns
LP Falling to FP Falling	Th2	0	-	-	ns

7. LCD DISPLAY DESIGN GUIDE

The data transferred from MCU to GPLD1080/GPLD2080 module will pass to last point.

Let's see the example. If we have an "E" word (Fig) in computer, and we want to show it from computer to LCD panel. We are going to get the four events below the section 7.1～7.4.

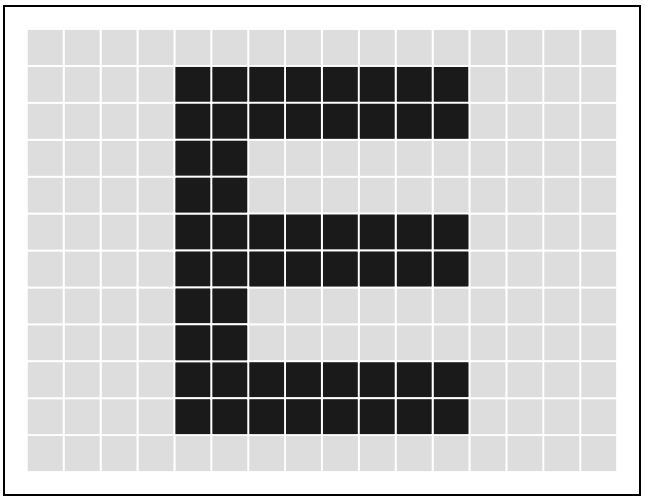
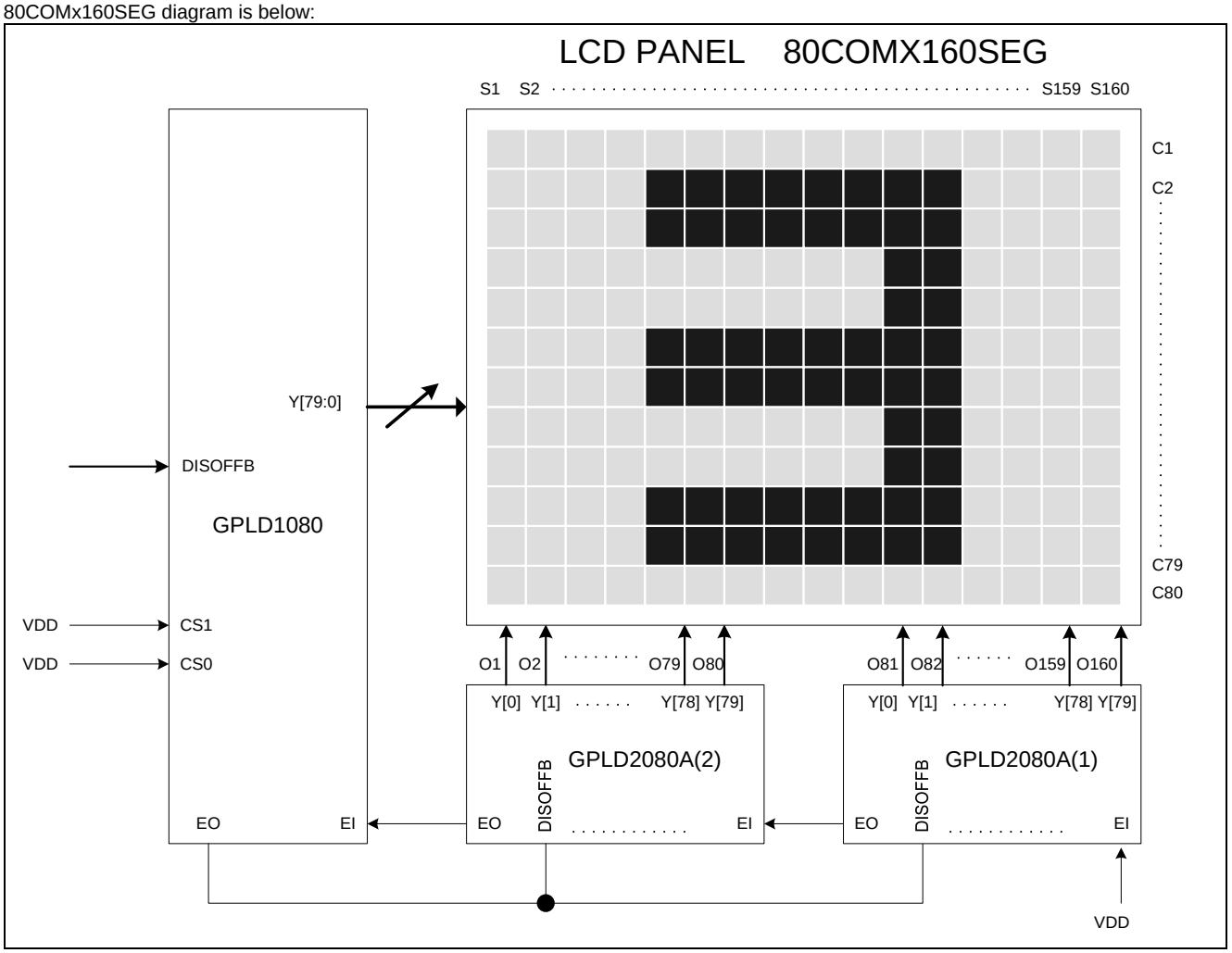


Fig. "E" word in computer

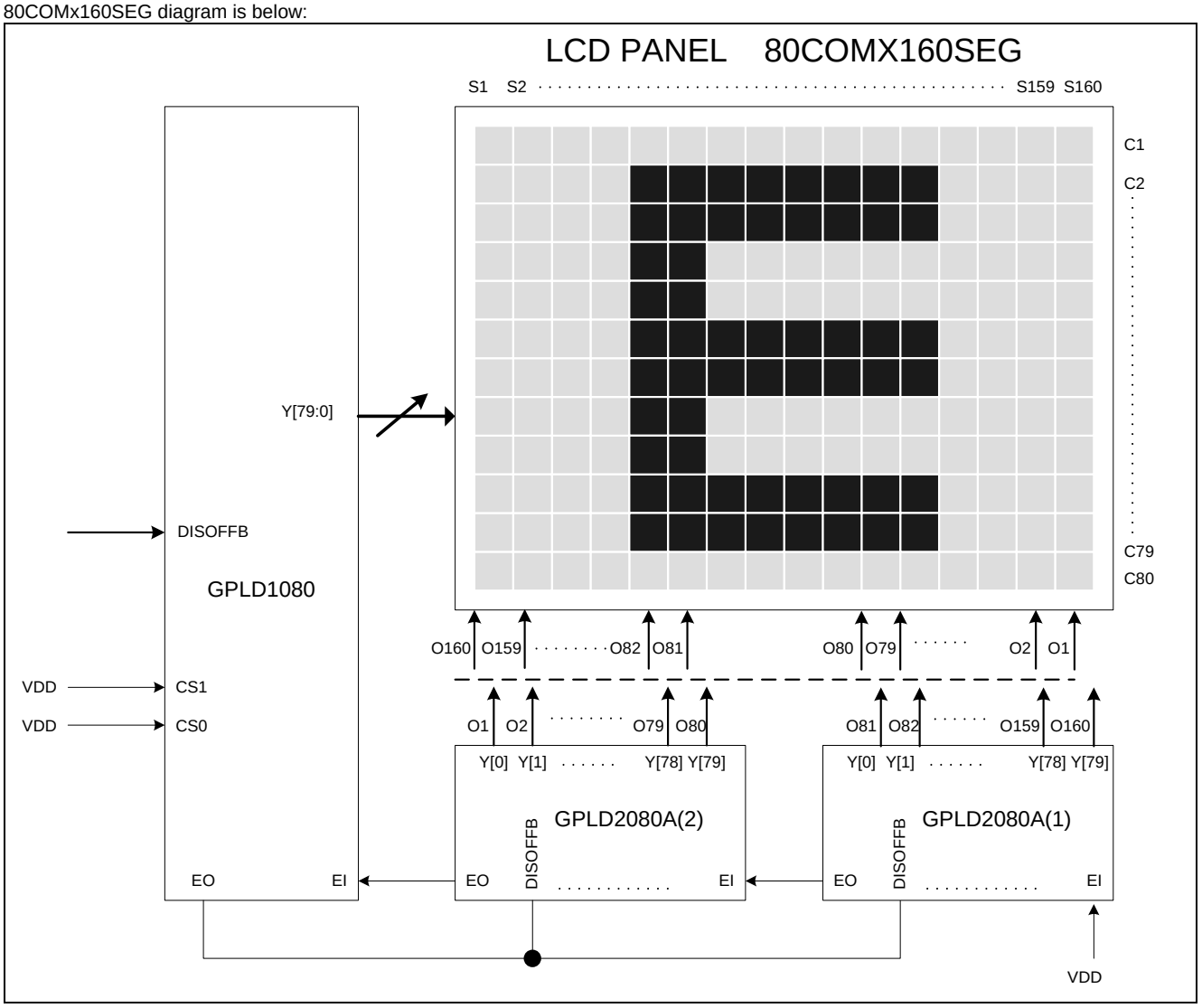
7.1. The 80COM x 160SEG (1)

The SEG signal connected to O1→ S1, O2→ S2……O159 → S159, O160 → S160, in PCB layout which it will mirror display on LCD. An 80COMx160SEG diagram is below:



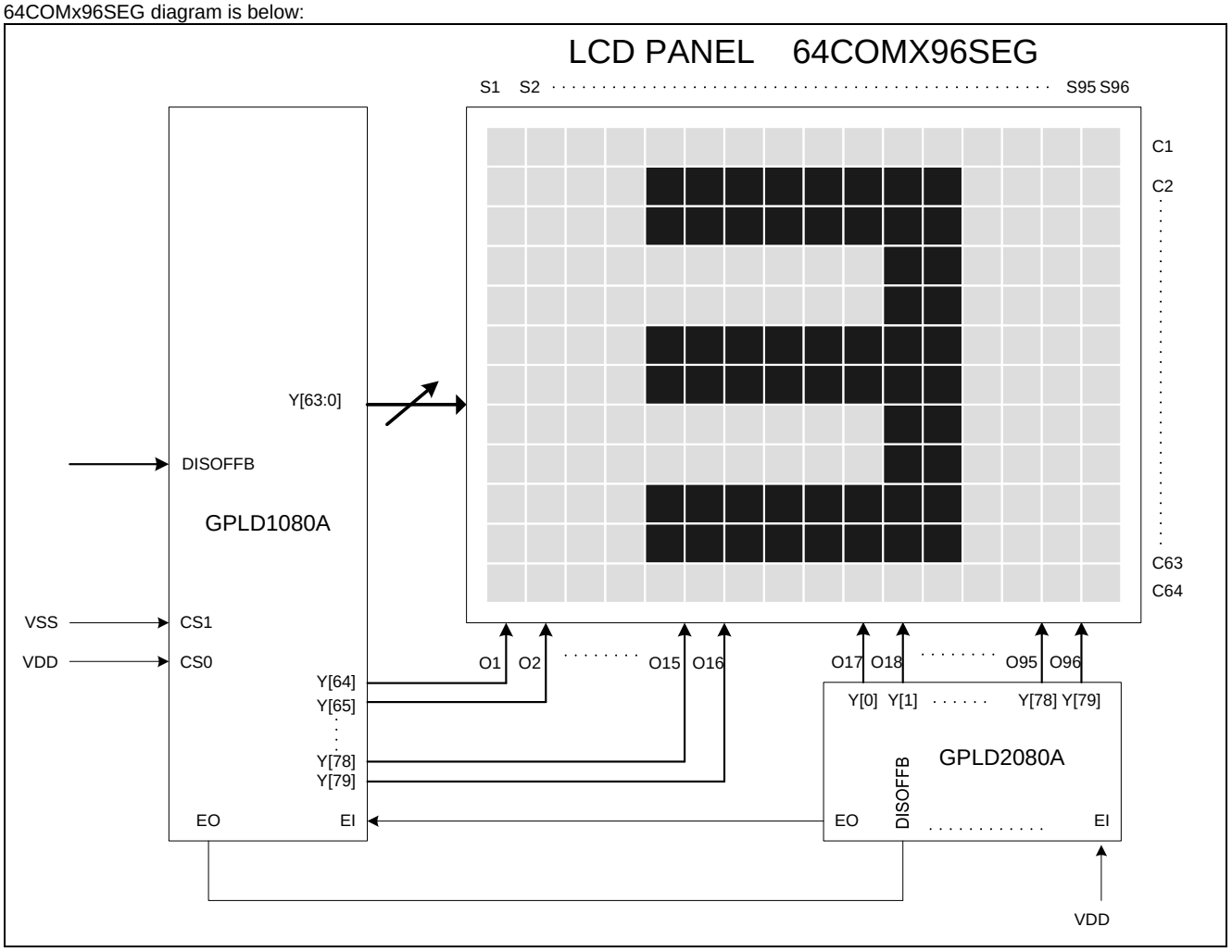
7.2. The 80COM x 160SEG (2)

The SEG signal connected to O1→ S160, O2→ S159……O159 → S2, O160 → S1, in PCB layout which it will mirror display on LCD. An 80COMx160SEG diagram is below:



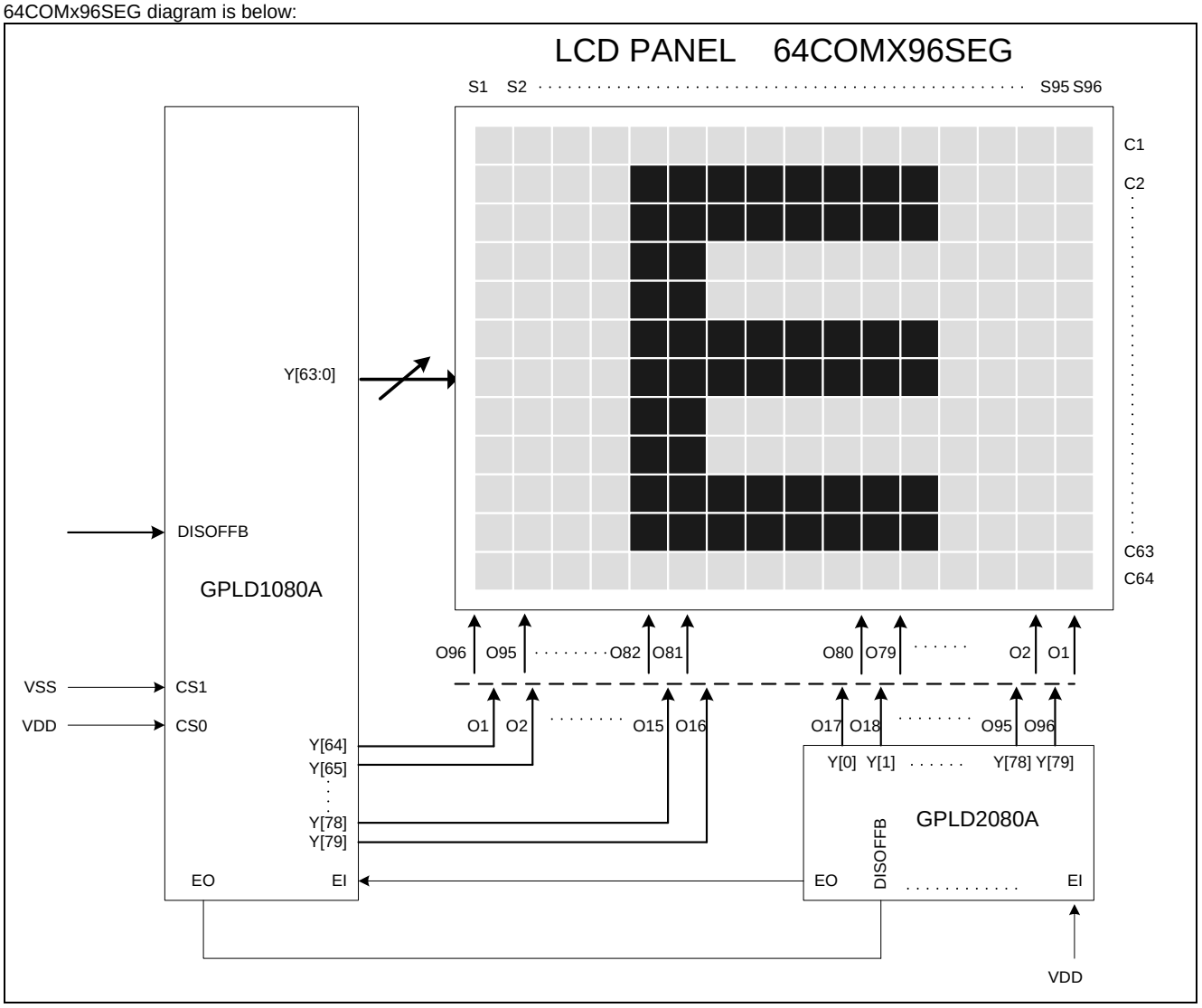
7.3. The 64COM x 96SEG (1)

The SEG signal connected to O1→ S1, O2→ S2……O95 → S95, O96 → S96, in PCB layout which it will mirror display on LCD. A 64COMx96SEG diagram is below:



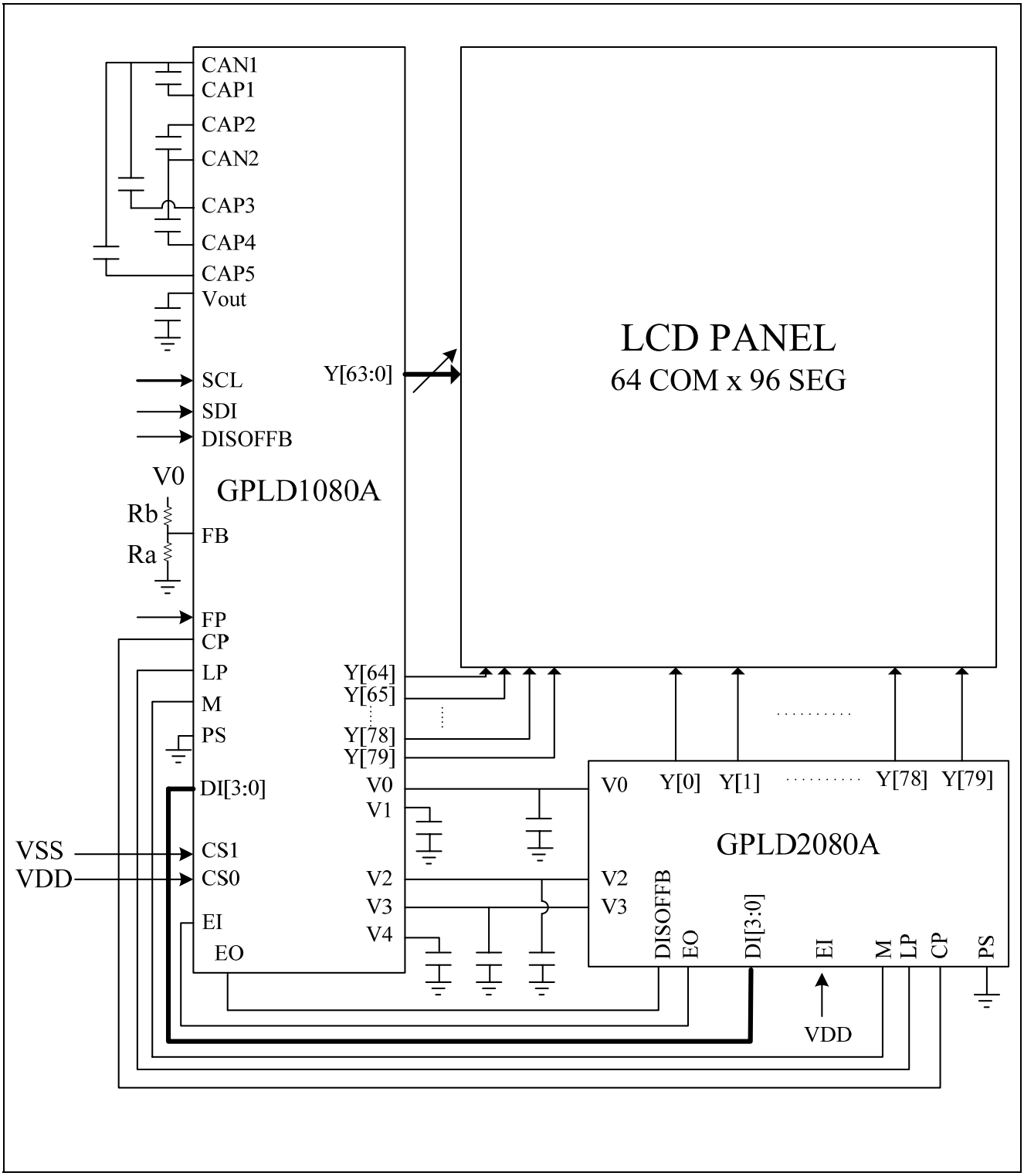
7.4. The 64COM x 96SEG (2)

The SEG signal connected to O1→ S96, O2→ S95……O95 → S2, O96 → S1, in PCB layout which it will mirror display on LCD. A 64COMx96SEG diagram is below:



8. APPLICATION CIRCUIT

8.1. 64 Common 96 Segment 1 Bit Data Mode

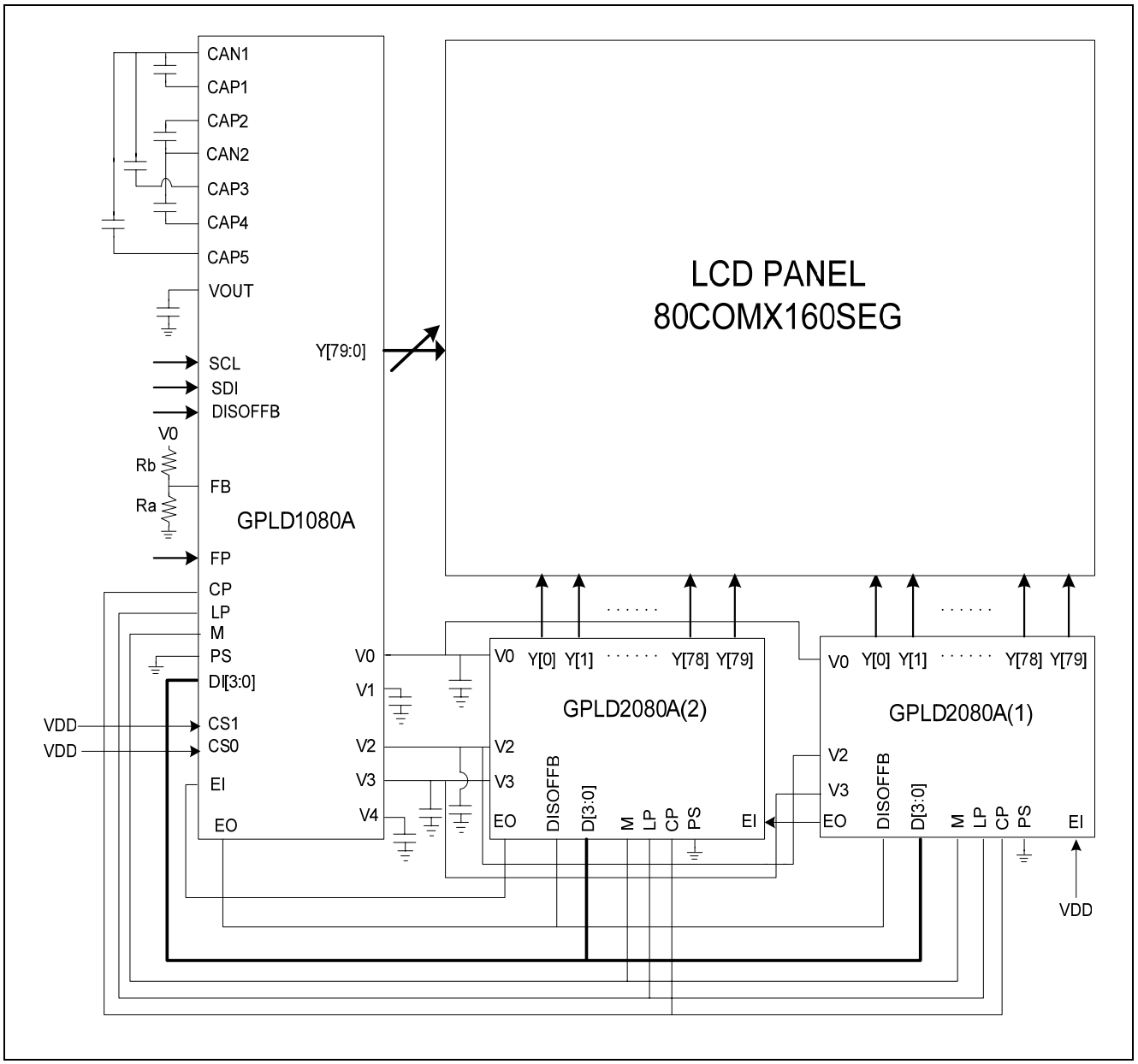


Note1: All capacitors value is 1uF.

Note2: If this panel >4 inch, then V0~V4 capacitors need to use 2.2uF.

Note3: GPLD2080A is the segment driver and Y[79] is first data in.

8.2. 80 Common 160 Segment 1 Bit Data Mode



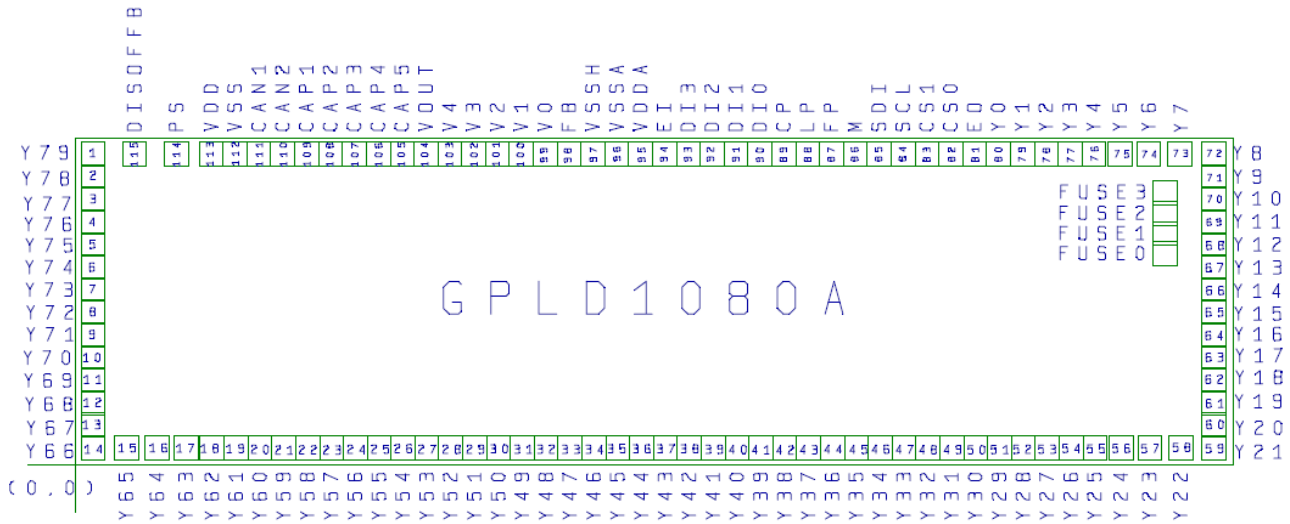
Note1: All capacitors value is 1uF.

Note2: If this panel >4 inch, then V0~V4 capacitors need to use 2.2uF.

Note3: GPLD2080A(1&2) are the segment drivers and Y[79] of GPLD2080A(1) is first data in.

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, bond all VDD and VSS pins.
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
GPLD1080A-NnnV-C	Chip form

Note1: Code number is assigned for customer.
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
MAY 23, 2007	1.3	1. Modify the diagram in section 5. 2. Add the “Timing characteristic of command interface” in section 5.1.1. 3. Add the “LCD control signal timing characteristic” in section 6.4.1. 4. Add the “LCD DISPLAY DESIGN GUIDE” in section 7.	8 8 10, 11 12
APR. 11, 2007	1.2	Modify the “DC Characteristics” in section 6.3.	9, 10
FEB. 12, 2007	1.1	1. Modify the “FEATURES” in section 2. 2. Modify the “PIN DESCRIPTIONS” in section 3. 3. Modify the “Application circuit: 64 common 96 segment 1 bit data mode” in section 7. 4. Add the note2 and note3 to section 7.1. Application circuit: 80 common 160 segment 1 bit data mode.	3 4 11 12
JAN. 05, 2007	1.0	Original	15