DATA SHEET

GPLD1120D

120-channel SEG/COM STN LCD Driver

Dec. 10, 2010

Version 1.0

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120-CHANNEL SEG/COM STN LCD DRIVER

1. GENERAL DESCRIPTION

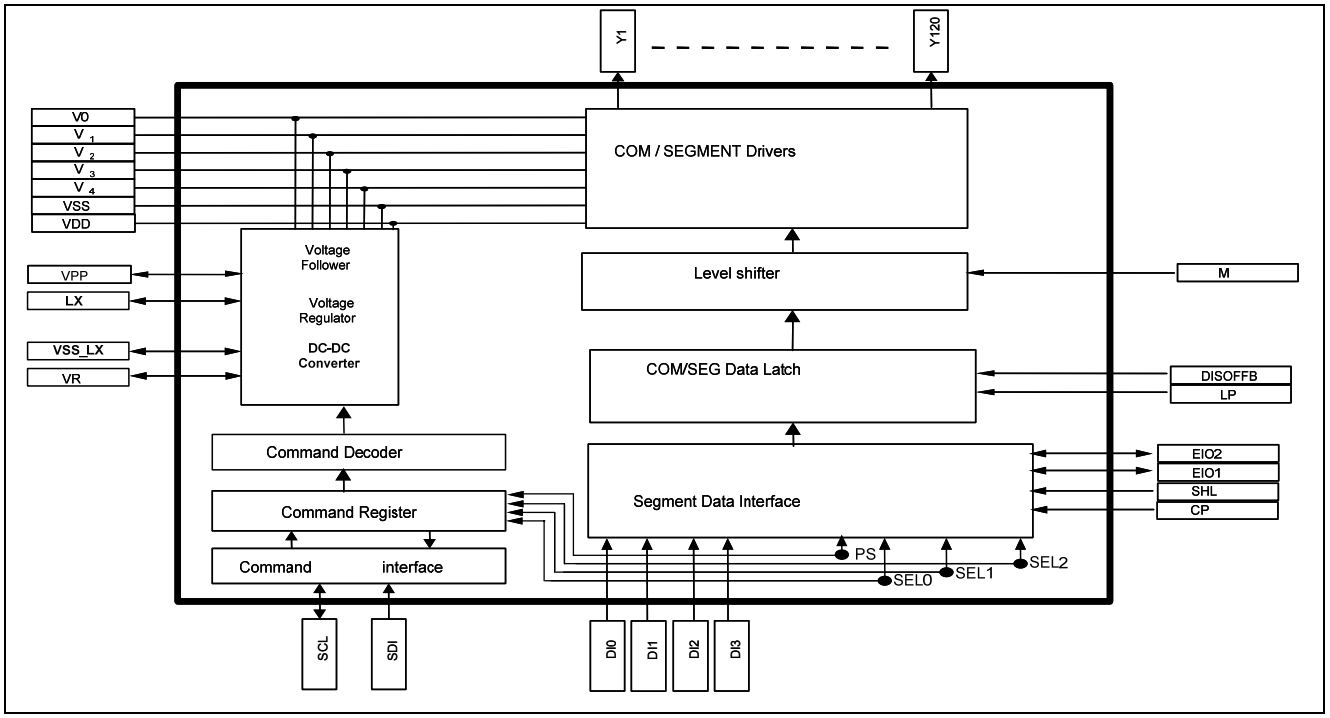
GPLD1120D, a 120-channel segment/common driver IC, is able to drive small/medium scale dot matrix LCD panels for the product fields of handheld game or electronic dictionary. GPLD1120D has eight modes that can be selected to set common and segment numbers by command selection. GPLD1120D also has built-in DC/DC converter, voltage regulation and voltage follower to generate LCD driver voltage.

SEL_2	SEL_1	SEL_0	Configuration
0	0	0	16 COM * 104 SEG
0	0	1	32 COM * 88 SEG
0	1	0	48 COM * 72 SEG
0	1	1	64 COM * 56 SEG
1	0	0	80 COM * 40 SEG (default)
1	0	1	96 COM * 24 SEG
1	1	0	112 COM * 8 SEG
1	1	1	120 COM

2.FEATURES

- The number of LCD drive outputs: 120
- Supply voltage to drive LCD: 14.5V (max.)
- Supply voltage for logic system: 2.4V to 5.5V
- 8 types of LCD combination selectable by command configuration
- Built-in DC-DC, Voltage Regulator and Voltage Follower
- Abundant command functions
- LCD bias set, electronic volume, voltage regulation external resistor ratio
- Shift clock frequency
  - 6 MHz (max.): V_{DD} = 2.4 V ~ 5.5 V
- 4-bit parallel / serial modes are selectable.

3. BLOCK DIAGRAM



3.1. Input/Output Circuits

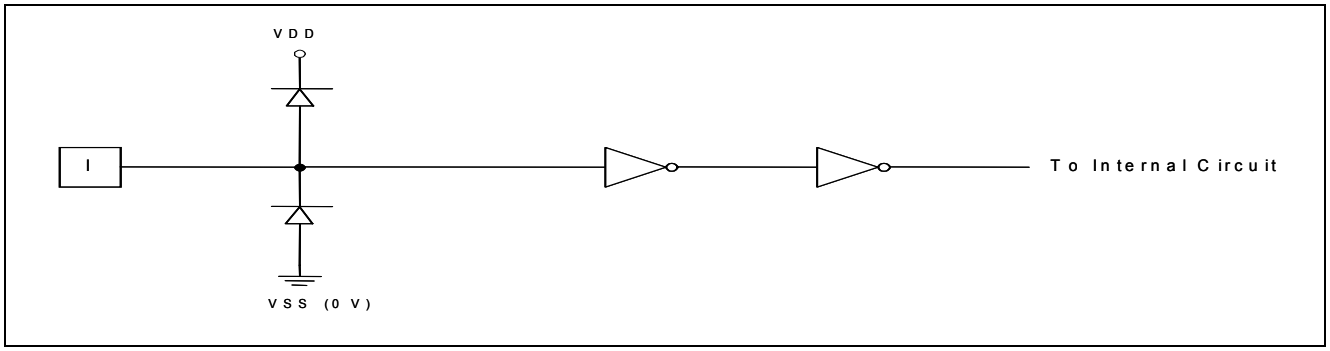


Figure 1: Input Circuit

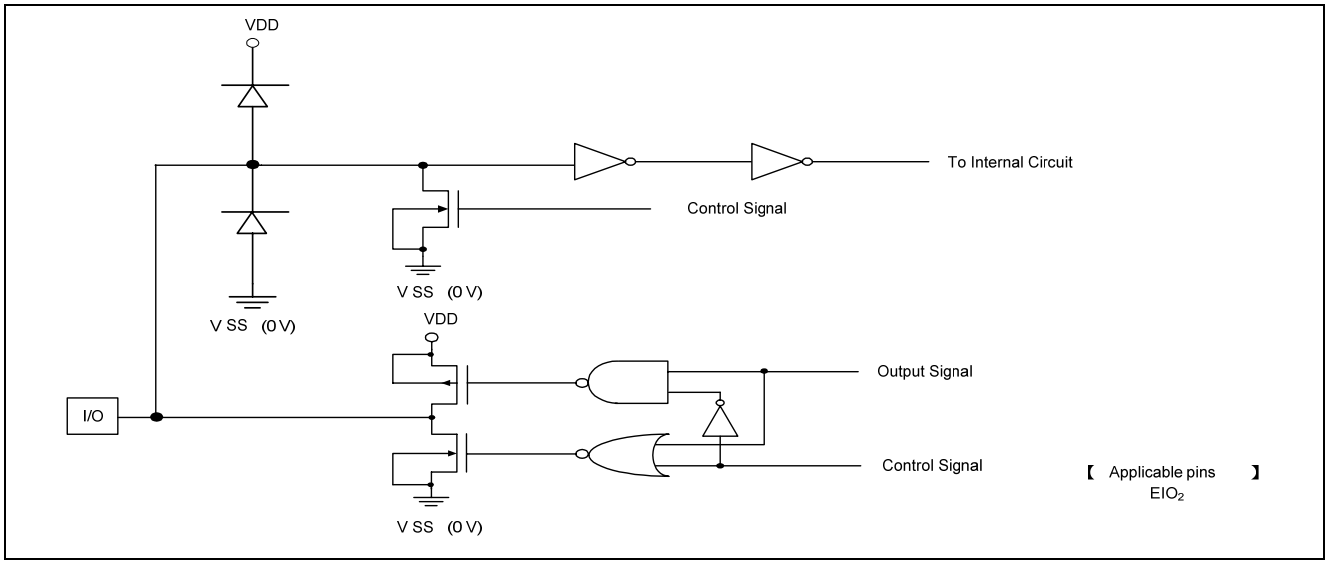
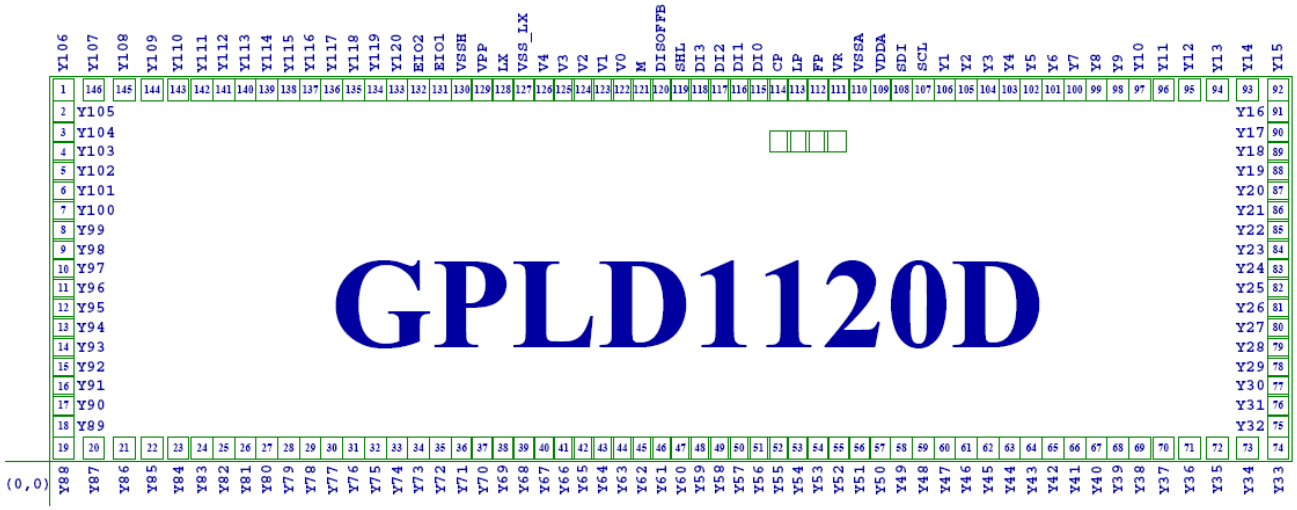


Figure 2: Input/Output Circuit

4. PIN DESCRIPTIONS

Mnemonic	Type	Description
Y_{120-1}	O	LCD driver output pins.
$V_0 \sim V_4$	P	The bias voltages for LCD driving where $V_{PP} > V_0 > V_1 > V_2 > V_3 > V_4 > V_{SS}$.
V_R	P	Gain adjustment input of V_0. By adjusting the R_A, R_B ratio between V_0, V_R and V_{SS}, the LCD driving voltage, V_0 is equal to V_{REF} (1+ R_B/R_A), where the V_{REF} is the internal reference voltage.
SHL	I	Display data shift direction selection. Input pin for selecting the reading direction of display data. 1). When set to VSS, data is read sequentially from Y_{120} to Y_{17}. 2). When set to VDD, data is read sequentially from Y_{17} to Y_{120}.
VDD	P	Power supply for logic system. (+ 2.4V to + 5.5V)
EIO_1,EIO_2	I/O	Input/output for chip selection at segment mode. FLM input/output function at common/segment mix mode or common mode. Input/output pins for chip selection. 1).When SHL input is set to VSS, EIO_1 is unused and EIO_2 is set for input. 2).When SHL input is set to VDD, EIO_1 is set for input and EIO_2 is set for output. 3). During output, it is set to “L”. After 120 bits of data have been read, it will be set to “H” for one cycle and return to “L” after the cycle. 4). During input, the chip is selected while EIO_1 is set to “H” after the LP signal. The chip is non-selected after 120 bits of data have been read.
$DI_3 \sim DI_0$	I	Display data input at segment mode. 1). In 1-bit serial input mode (PS=”L”), input data into the 1 pins DI_0. Connect DI_{1-3} to VSS or VDD. 2). In 4-bit parallel input mode (PS=”H”), input data into the 4 pins, $DI_0 – DI_3$.
DISOFFB	I	Display off control input pin. Control input pin for output non-select level. When set to V_{SS}, the LCD drive output pins (Y_{1-120}) are set to level V_{SS}.
M	I	AC converting signal input for LCD drive waveform.
FP	I	Frame pulse input. FP is the shift data input of common driver.
CP	I	Clock input for taking display data at segment mode. 1). Data is read at the falling edge of the clock pulse.
LP	I	Latch pulse input for displaying data at segment mode. Shift clock input for shifting register at common mode. 1). Data is latched at the rising edge of the clock pulse.
VSS	I	Ground (0V).
LX	I	Connect inductor to VDD_LX (external power supply) for DC-DC voltage converter.
VSSH	I	Ground for high voltage circuit (0V).
VSS_LX	I	Ground for DC-DC voltage converter.
VPP	O	DC-DC voltage converter output.
SCL	I	Serial clock input pin for command decoder.
SDI	I	Serial data input pin for command decoder.

4.1. PAD Assignment



The IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.
Note2: The 0.1F capacitor between VDD and VSS should be placed to IC as close as possible.

5. FUNCTIONAL DESCRIPTIONS

5.1. Function Operations

5.1.1. Truth table

5.1.1.1. Segment outputs

M	Latch data	DISOFFB	Driver output voltage level
L	L	H	V_2
L	H	H	V_0
H	L	H	V_3
H	H	H	V_{SS}
X	X	L	V_{SS}

5.1.1.2. Common outputs

M	Latch data	DISOFFB	Driver output voltage level
L	L	H	V_1
L	H	H	V_{SS}
H	L	H	V_4
H	H	H	V_0
X	X	L	V_{SS}

Note1: $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_0$, L: VSS (0V), H: VDD (+2.4V to +5.5V), X: Don't care.

Note2: To avoid floating, "Don't care" should be fixed to "H" or "L". There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supply regular voltage which is assigned by specification for each power pin.

5.2. Relationship between the Display Data and Driver Output Pins

5.2.1. Segment side of mix mode (80COMX40SEG)

When (SEL_2 SEL_1 SEL_0) = (1 0 0) → Selects 80-common/40-segment mode

5.2.1.1. 4-bit parallel mode

SHL	EIO_1	EIO_2	Input Data	Figure of Clock								
				1 Clock	2 Clock	3 Clock	• • •	• • •	• • •	8 Clock	9 Clock	10 Clock
L	----	Input	DI_0	Y_{117}	Y_{113}	Y_{109}	• • •	• • •	• • •	Y_{89}	Y_{85}	Y_{81}
			DI_1	Y_{118}	Y_{114}	Y_{110}	• • •	• • •	• • •	Y_{90}	Y_{86}	Y_{82}
			DI_2	Y_{119}	Y_{115}	Y_{111}	• • •	• • •	• • •	Y_{91}	Y_{87}	Y_{83}
			DI_3	Y_{120}	Y_{116}	Y_{112}	• • •	• • •	• • •	Y_{92}	Y_{88}	Y_{84}
H	Input	Output	DI_0	Y_{84}	Y_{88}	Y_{92}	• • •	• • •	• • •	Y_{112}	Y_{116}	Y_{120}
			DI_1	Y_{83}	Y_{87}	Y_{91}	• • •	• • •	• • •	Y_{111}	Y_{115}	Y_{119}
			DI_2	Y_{82}	Y_{86}	Y_{90}	• • •	• • •	• • •	Y_{110}	Y_{114}	Y_{118}
			DI_3	Y_{81}	Y_{85}	Y_{89}	• • •	• • •	• • •	Y_{109}	Y_{113}	Y_{117}

Note: To avoid floating, EIO1 should be fixed to V_{DD} when SHL is set as "L".

5.2.1.2. 1-bit serial mode

SHL	EIO_1	EIO_2	Input Data	Figure of Clock								
				1 Clock	2 Clock	3 Clock	• • •	• • •	• • •	38 Clock	39 Clock	40 Clock
L	----	Input	DI_0	Y_{120}	Y_{119}	Y_{118}	• • •	• • •	• • •	Y_{83}	Y_{82}	Y_{81}
			DI_1	×	×	×	×	×	×	×	×	×
			DI_2	×	×	×	×	×	×	×	×	×
			DI_3	×	×	×	×	×	×	×	×	×
H	Input	Output	DI_0	Y_{81}	Y_{82}	Y_{83}	• • •	• • •	• • •	Y_{118}	Y_{119}	Y_{120}
			DI_1	×	×	×	×	×	×	×	×	×
			DI_2	×	×	×	×	×	×	×	×	×
			DI_3	×	×	×	×	×	×	×	×	×

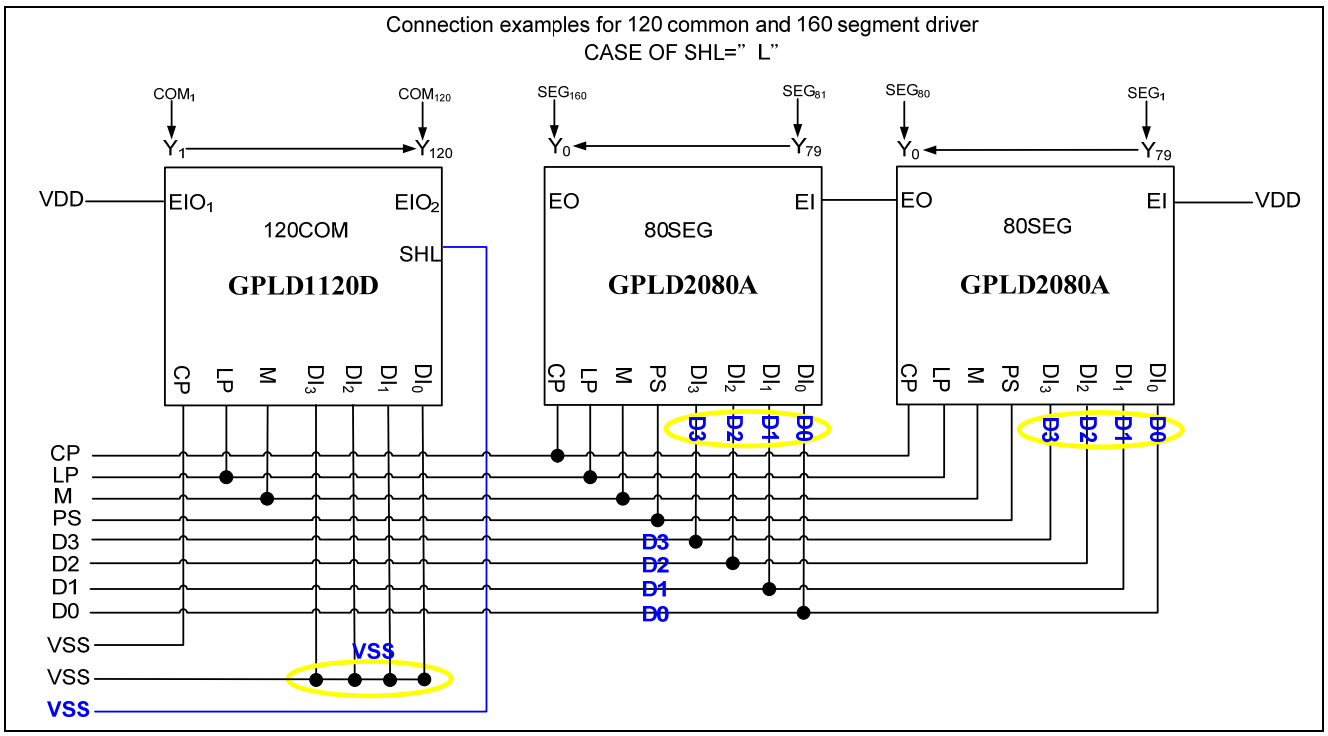
Note: To avoid floating, EIO1 should be fixed to V_{DD} when SHL is set as "L".

5.2.1.3. Common side of mix mode

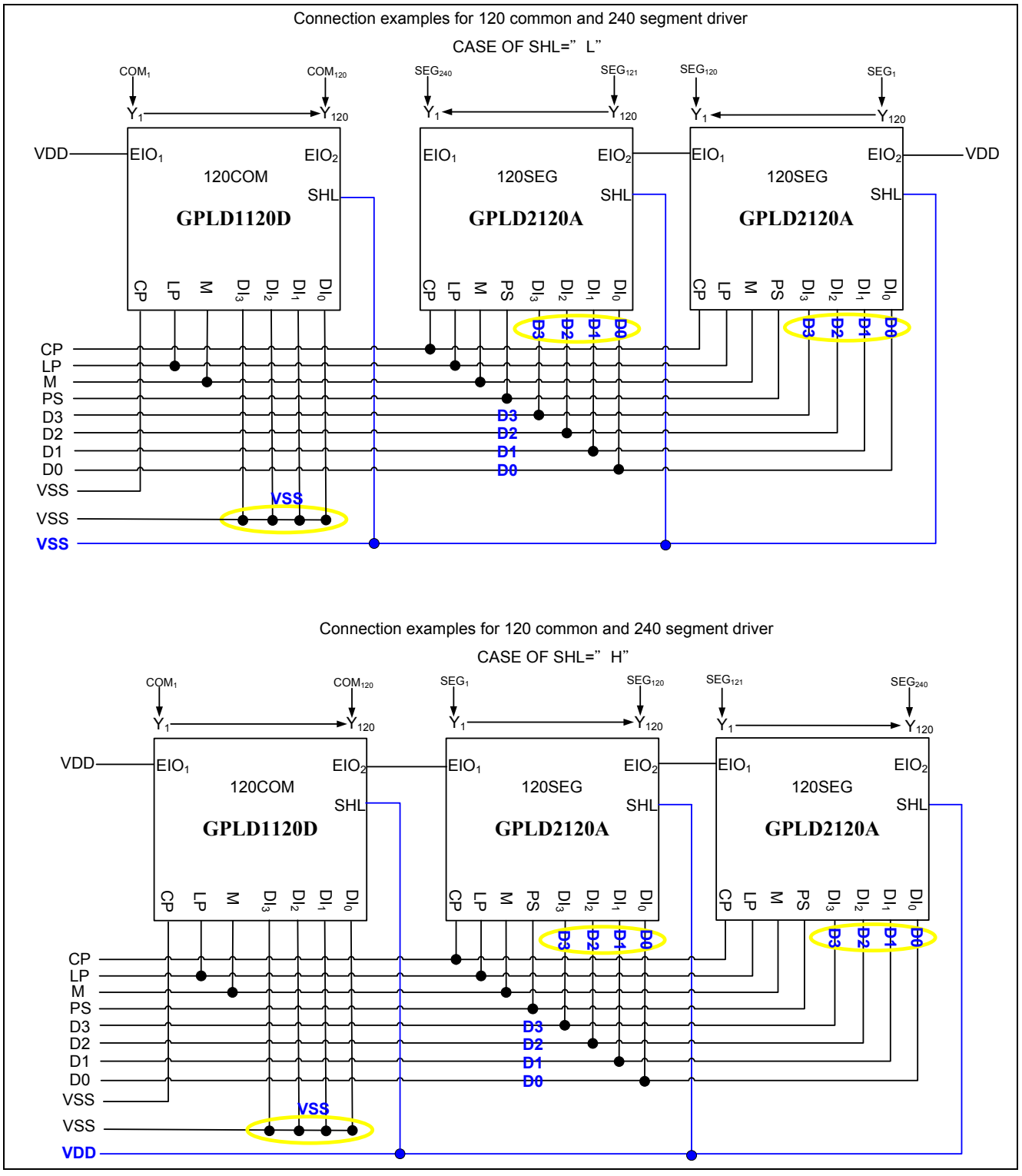
SHL	EIO_1	EIO_2	Data Transfer Direction
L	----	Common Input	Y_{120} → Y_{17}
H	Common Input	Segment Output	Y_{17} → Y_{120}

Note: To avoid floating, EIO1 should be fixed to V_{DD} when SHL is set as "L".

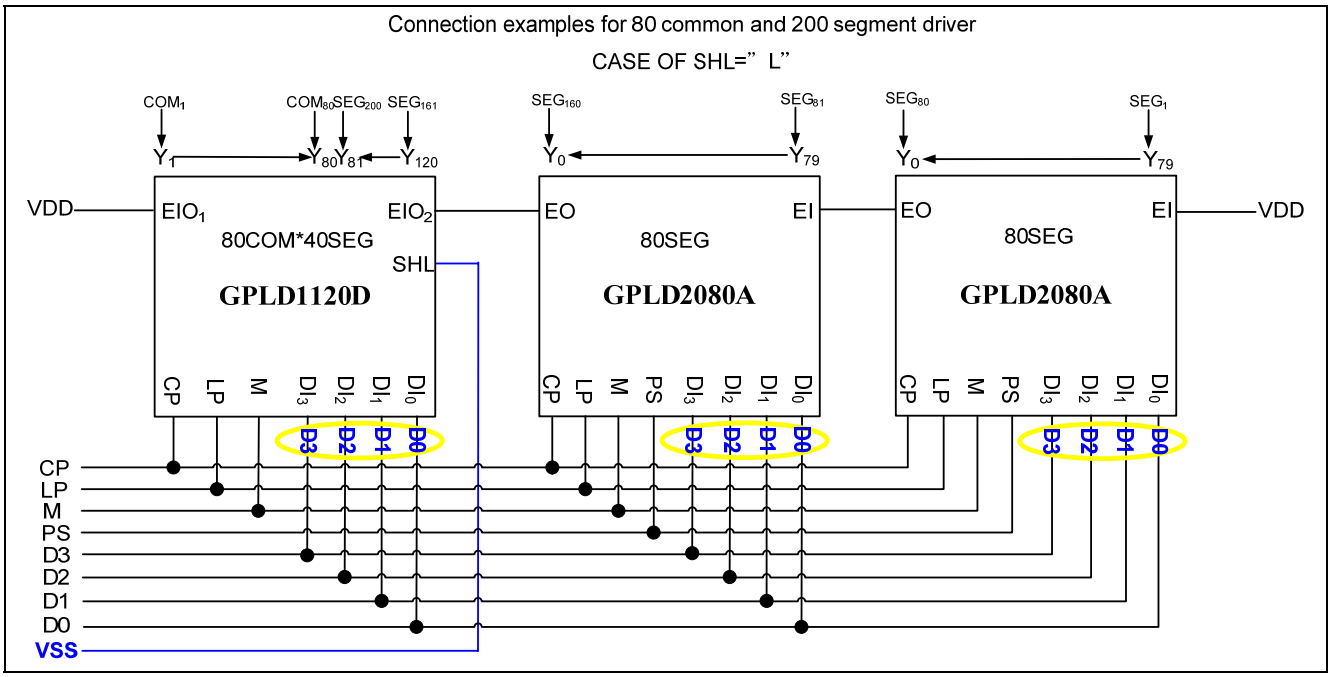
5.2.2. Connection examples for 120-common and 160-segment drivers



5.2.3. Connection examples for 120-common and 240-segment drivers



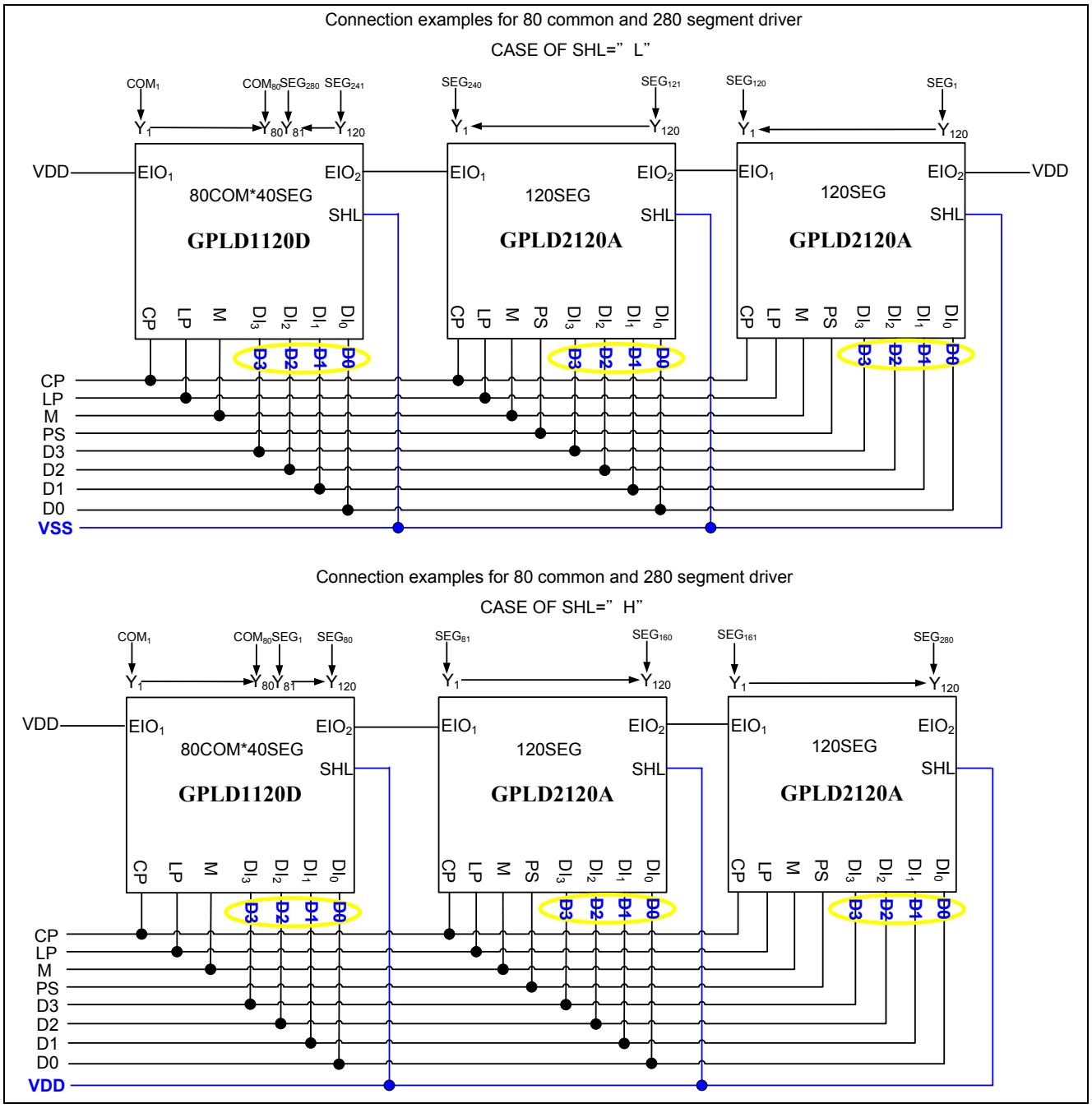
5.2.4. Connection examples for 80-common and 200-segment drivers



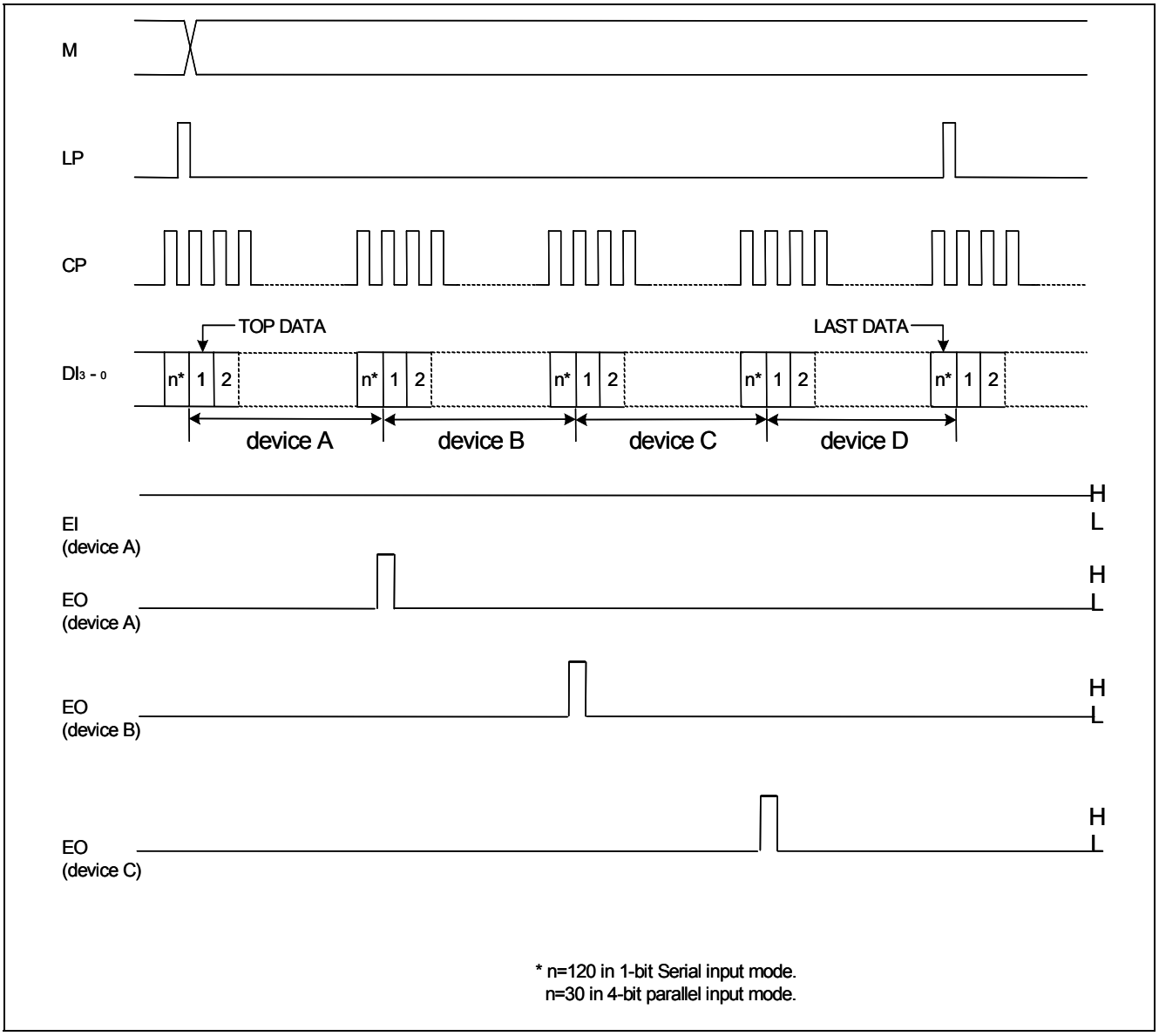
Note1: The segment data shifting direction from GPLD2080 to GPLD1120D is acceded only.

Note2: In the case of 80 COMs X 200 SEGs by GPLD1120D+GPLD2080X2, SHL can be connected to VSS only.

5.2.5. Connection examples for 80-common and 280-segment drivers

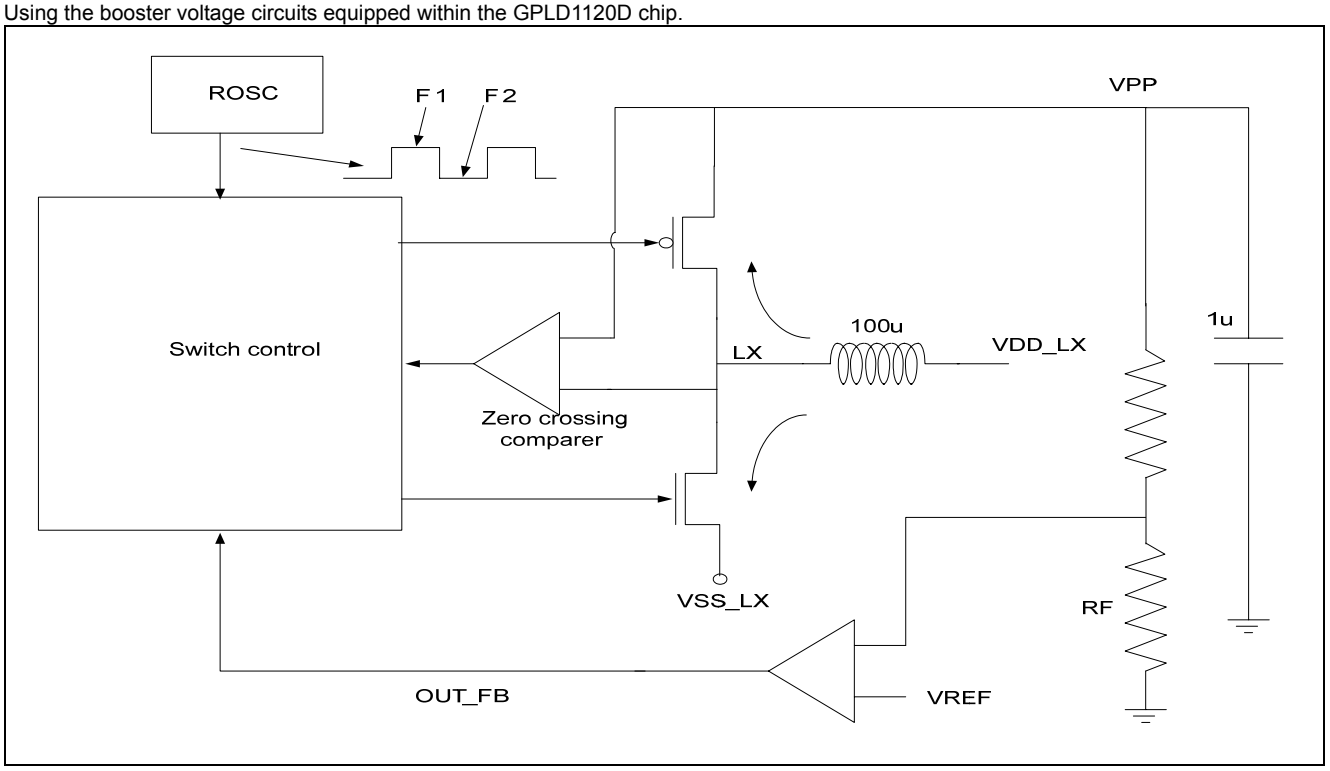


5.2.6. Timing characteristics of 4-device cascade connection of segment drivers



5.3. Booster Circuits

Using the booster voltage circuits equipped within the GPLD1120D chip.



Note: The booster inductor value is recommended 100 μH for VDD=5.5V~3.3V and 220 μH for VDD=3.3V~2.4V.

5.4. Regulator Circuits

The booster will pump the voltage up to V_{PP}, which further generates VLCD voltage, Vo, for the power of voltage regulator circuit. Under this circumstance, Vo is much more accurate and it can be easily adjusted via the internal 28-level electronic volume function.

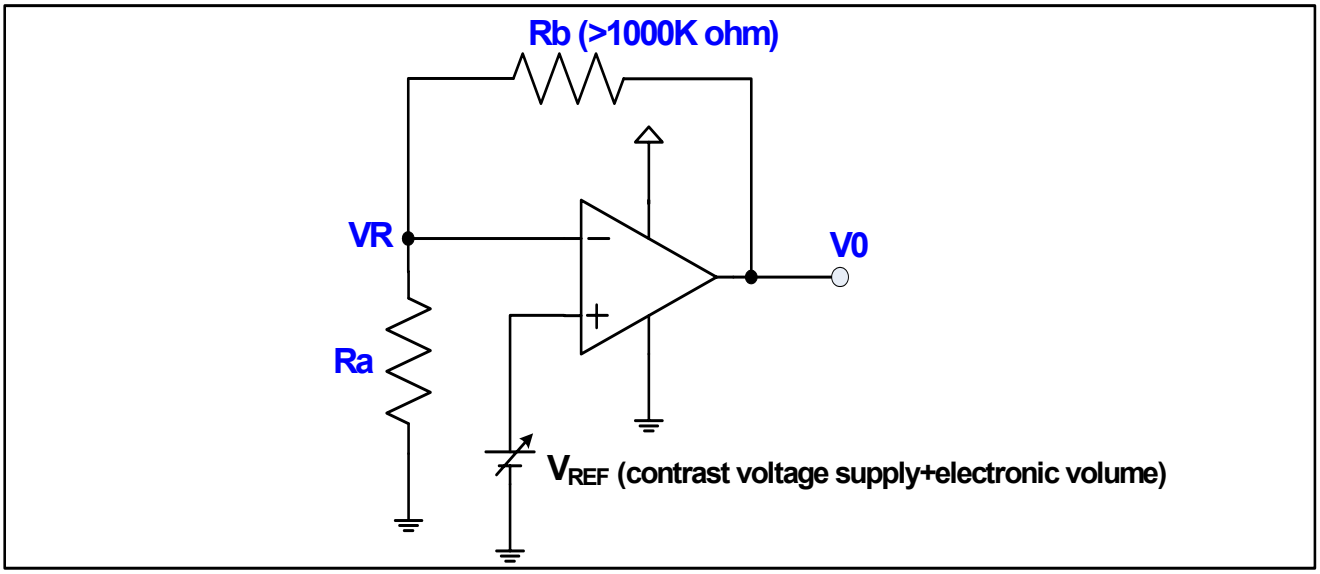
5.4.1. When the V_0 voltage regulator with external resistors are used

Through the use of the V_0 voltage regulator external resistors and the electronic volume function, the liquid crystal power supply voltage, V_0, can be controlled by commands alone, making it possible to adjust the liquid crystal display brightness. The V_0 voltage can be calculated by using equation E-1 over the range where $|V_0| < |V_{PP}|-1V$.

The Rb and Ra are external resistors.

$V_0 = (1 + Rb/Ra) \bullet V_{REF}$

$= (1 + Rb/Ra) \bullet (1 - \alpha/220) \bullet 2.2$ ----------Equation E-1



V_{REF} is the IC-internal fixed voltage supply and its voltage at T_A = 25°C is 2.04V when using default value EV4~EV0.

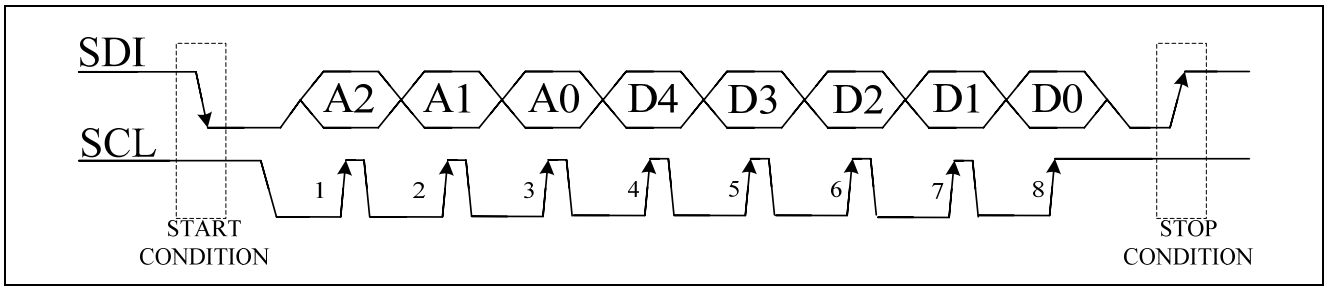
For power saving, please select Rb>1000K Ohms (saving DC current from V0 through Rb, Ra to ground), and then choose Ra to get desired V0.

α is set to one of 28 possible levels by the electronic volume function depending on the data set in the 5-bit electronic volume register EV4~EV0. The following table shows the corresponding values based on the electronic volume register settings.

EV_4	EV_3	EV_2	EV_1	EV_0	α
0	0	0	0	0	31
0	0	0	0	1	30
0	0	0	1	0	29
:	:	:	:	:	:
0	1	1	1	1	16 (default)
:	:	:	:	:	:
1	1	1	0	1	6
1	1	1	1	0	5
1	1	0	1	1	4
1	1	1	0	0	Not Used
1	1	1	0	1	Not Used
1	1	1	1	0	Not Used
1	1	1	1	1	Not Used

6. COMMAND DESCRIPTION

By setting SDI to “Low” and SCL to “High”, GPLD1120D is able to receive serial input data. Serial data is input in the order of “A2, A1, A0, D4, D3, D2, D1, D0” from the serial data input pin (SDI) at the rising edge of serial clock (SCL). After the 8-bit data has been read into the shift register, the shift register will automatically convert serial data to parallel data changing V0 voltage or Common/Segment set. Those command settings are effective only when DISOFFB is “High”. To avoid abnormal display at initial frame, the command settings must be done within 3*FP time period after DISOFFB releases from “Low” to “High”.



Timing Diagram of Serial Data Transfer

GPLD1120D Command functions are shown in the following table.

Command	Command Code								Function
	A2	A1	A0	D4	D3	D2	D1	D0	
Electronic Volume	0	1	0	EV_4	EV_3	EV_2	EV_1	EV_0	Brightness adjustment
PS and Com / Seg Selection Set	1	0	1	1	PS	SEL2	SEL1	SEL0	8 types of LCD combination selection and PS Signal Control

6.1. PS Mode Set

When power-on initialization or hardware reset is executed, the default values are indicated in the following table.

PS	Data Input Mode
0	1-bit (default)
1	4-bit

6.2. LCD Bias Set

When power-on initialization or hardware reset is executed, the default values are indicated in the following table.

SEL2	SEL1	SEL0	DUTY	BIAS
0	0	0	1/16	1/5
0	0	1	1/32	1/6
0	1	0	1/48	1/8
0	1	1	1/64	1/9
1	0	0	1/80	1/10 (default)
1	0	1	1/96	1/10
1	1	0	1/112	1/11
1	1	1	1/120	1/12

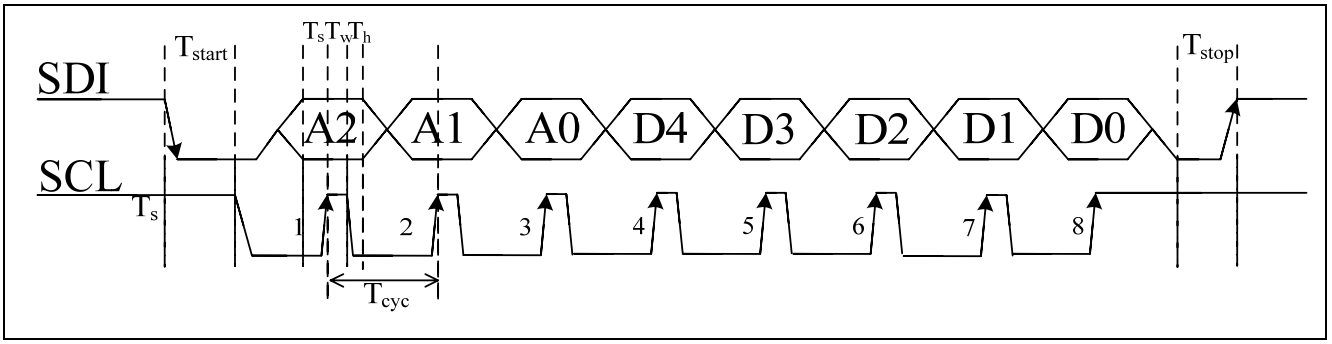
6.3. The Electronic Volume Register Set

This command makes it possible to adjust the LCD brightness by controlling the liquid crystal drive voltage V_0. Use this command to set 5-bit data to the electronic volume register, the liquid crystal driving voltage, V_0, assumes one of the 28 voltage levels.

EV_4	EV_3	EV_2	EV_1	EV_0	α
0	0	0	0	0	31
0	0	0	0	1	30
0	0	0	1	0	29
:	:	:	:	:	:
0	1	1	1	1	16 (default)
:	:	:	:	:	:
1	1	1	0	1	6
1	1	1	1	0	5
1	1	0	1	1	4
1	1	1	0	0	No Use
1	1	1	0	1	No Use
1	1	1	1	0	No Use
1	1	1	1	1	No Use

When power on or hardware reset, the default value is (DB5 DB4 DB3 DB2 DB1 DB0) = (0 1 1 1 1), α = 16.

6.4. Timing Characteristic of Command Interface



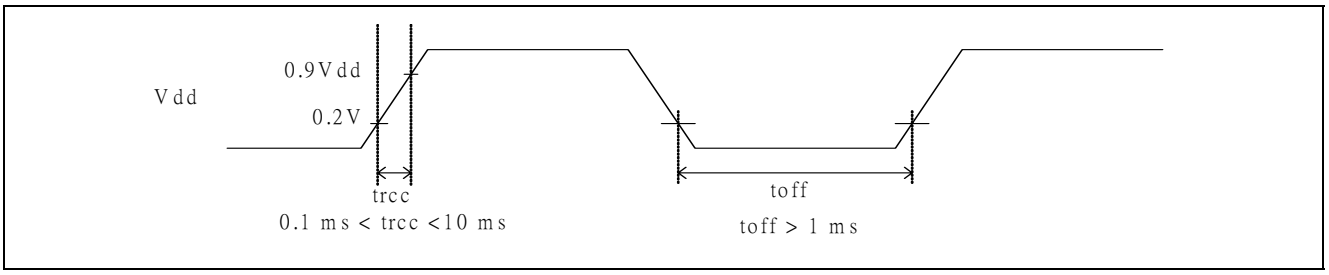
Parameter	Symbol	Min.	Typ.	Max.	Unit
The Hold Time of SDI Falling to SCL Falling	T_{start}	100	-	-	ns
SCL Period	T_{cyc}	200	-	-	ns
SCL High Width	T_w	50	-	-	ns
SCL Setup Time in Order to Latch SDI Data	T_s	50	-	-	ns
SDI Hold Time That is from SCL Falling to SDI Change	T_h	50	-	-	ns
SCL Rising to SDI Rising in Order to Load Data to Register	T_{stop}	50	-	-	ns

7.POWER ON INITIALIZATION AND HARDWARE RESET

GPLD1120D has two methods to initialize the register; one is power-on initialization, and the other is hardware reset.

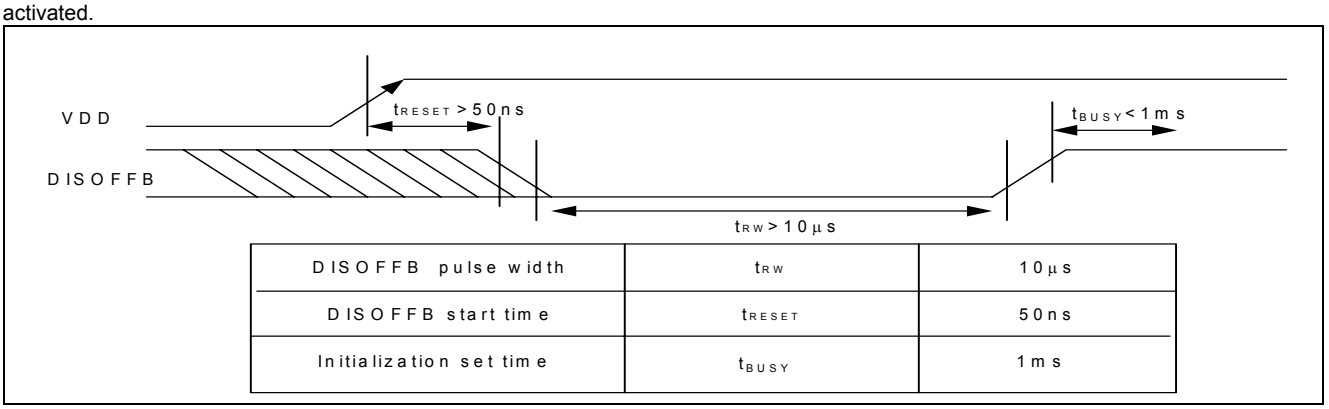
7.1. Power on Initialization

GPLD1120D features a power-on reset circuit. If the power-on timing fits the following timing diagram, GPLD1120D will execute initialization; otherwise, GPLD1120D will not be activated.



7.2. Hardware Reset

If the hardware reset timing fits the following timing diagram, GPLD1120D will execute initialization; otherwise, GPLD1120D will not be activated.



DISOFFB pulse width	t_{RW}	10µs
DISOFFB start time	t_{RESET}	50ns
Initialization set time	t_{BUSY}	1ms

8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable Pins	Ratings	Unit
Supply Voltage (1)	VDD	T_A = +25℃ Referenced to VSS (0V)	VDD	-0.3 to +6.5	V
Supply Voltage (2)	V_0		V_0	-0.3 to +14.5	V
	V_1		V_1	-0.3 to V0 + 0.3	V
	V_2		V_2	-0.3 to V0 + 0.3	V
	V_3		V_3	-0.3 to V0 + 0.3	V
	V_4		V_4	-0.3 to V0 + 0.3	V
Input Voltage	V_I		DI_{3-0}, CP, LP, SHL, M, SCL, SDI, EIO_1, EIO_2, DISOFFB	-0.3 to VDD + 0.3	V
Storage Temperature	T_{STG}	-	-	-45 to + 125	℃

Note1: T_A = +25℃

Note2: The maximum applicable voltage on any pin with respect to VSS (0V).

Note3: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

8.2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Supply Voltage (1)	VDD	Referenced to VSS (0V)	VDD	+2.4	-	+5.5	V
Supply Voltage (2)	V_0		V_0	+3	-	+14.5	V
Operating Temperature	T_{OPR}	-	-	-20	-	+75	℃

Note1: The applicable voltage on any pin with respect to VSS (0V).

Note2: Ensure that voltage are set such that $VSS < V_4 < V_3 < V_2 < V_1 < V_0$.

8.3. DC Characteristics

8.3.1. Segment side of mix mode (VSS = 0V, VDD = + 2.4V to + 5.5V, V_0 = + 3V to + 14.5V, T_A = + 25℃)

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Input Voltage	V_{IH}	-	DI_{3-0}, CP, LP, SHL, M, SCL, SDI, DISOFFB	0.8VDD	-	-	V
	V_{IL}	-		-	-	0.2VDD	V
Output Voltage	V_{OH}	I_{OH} = -0.4mA	EIO_1, EIO_2	VDD - 0.4	-	-	V
	V_{OL}	I_{OL} = +0.4mA		-	-	+0.4	V
Input leakage Current	I_{LIH}	V_I = VDD	DI_{3-0}, CP, LP, SHL, M, SCL, SDI, DISOFFB	-	-	+1.0	μA
	I_{LIL}	V_I = VSS		-	-	-1.0	μA
Output Resistance	R_{ON}	$\lvert\triangle V_{ON}\rvert$ = 0.5V, V_0 = +14.5V	Y_{120-1}	-	1.0	2.0	KΩ
Stand-by Current	I_{STB}	*1	VSS	-	-	1.0	μA
Supply Current (1)	I_{DD2}	*2	VDD	-	-	500	μA
Supply Current (2)	I_0	*3	V_0	-	-	50	μA

Note1: VDD = +5.0V, V_0 = +14.5V, CPU no access stand-by mode.

Note2: VDD = +5.0V, V_0 = +14.5V, f_{CP} = 474.112KHz, f_M = 37.04Hz, No-load, E_I = VDD.
The input data is turned over by data taking clock (4-bit parallel input mode).

Note3: VDD = +5.0V, V_0 = +14.5V, f_{CP} = 474.112KHz, f_{LP} = 2.963KHz, f_M = 37.04KHz, without loading.
The input data is turned over by data taking clock (4-bit parallel input mode).

8.3.2. Common mode (VSS = 0V, VDD = +2.4V to +5.5V, V0 = +3V to +14.5V, TA = +25℃)

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Input Voltage	V_{IH}	-	DI_{3-0}, CP, LP, SHL, M, SCL, SDI, DISOFFB	0.8VDD	-	-	V
	V_{IL}	-		-	-	0.2VDD	V
Output Voltage	V_{OH}	I_{OH} = -0.4mA	EIO_1, EIO_2	VDD - 0.4	-	-	V
	V_{OL}	I_{OL} = +0.4mA		-	-	+0.4	V
Input Leakage Current	I_{LIH}	V_I = VDD	DI_{3-0}, CP, LP, SHL, M, SCL, SDI, DISOFFB	-	-	+1.0	μA
	I_{LIL}	V_I = VSS		-	-	-1.0	μA
Output Resistance	R_{ON}	$\|\triangle V_{ON}\|$ = 0.5V, V_0 = +14.5V	Y_{120-1}	-	1.0	2.0	KΩ
Stand-by Current	I_{STB}	*1	VSS	-	-	1	μA
Supply Current (1)	I_{DD}	*2	VDD	-	-	400	μA
Supply Current (2)	I_0	*2	V_0	-	-	50	μA

Note1: VDD = +5.0V, V_0 = +14.5V, CPU no access stand-by mode.

Note2: VDD = +5.0V, V_0 = +14.5V, f_{LP} = 3.288 KHz, f_M = 27.4 KHz in case of 1/120 duty operation, without loading.

8.4. AC Characteristics

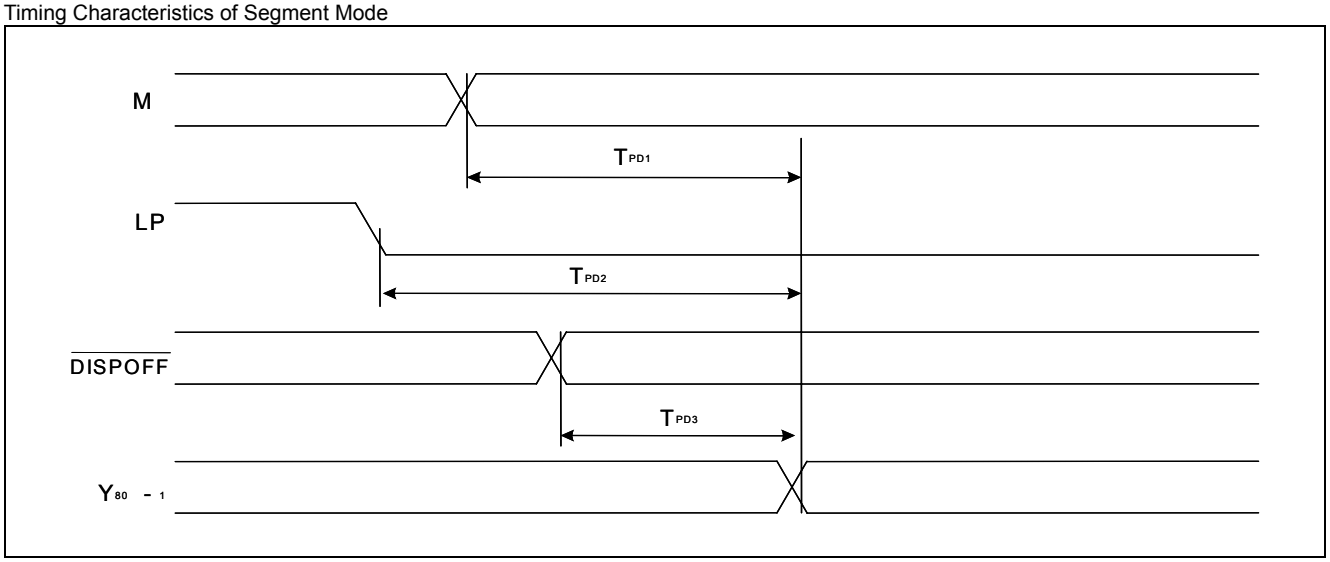
8.4.1. Segment side of mix mode 1 (VSS = 0V, VDD = +2.4V to +5.5V, V_0 = +3V to +14.5V, T_A = +25℃)

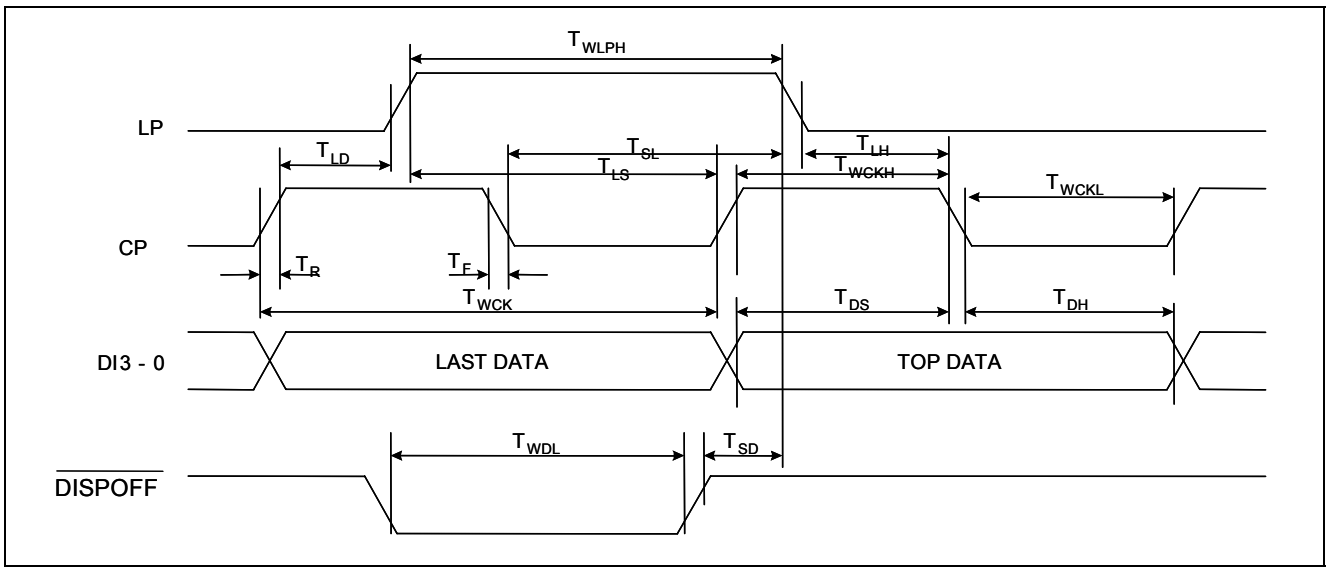
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift Clock Period *1	T_{WCK}	-	160	-	-	ns
Shift Clock “H” Pulse Width	T_{WCKH}	-	70	-	-	ns
Shift Clock “L” Pulse Width	T_{WCKL}	-	70	-	-	ns
Data Setup Time	T_{DS}	-	40	-	-	ns
Data Hold Time	T_{DH}	-	40	-	-	ns
Latch Pulse “H” Pulse Width	T_{WLPH}	-	70	-	-	ns
Shift Clock Rise to Latch Pulse Rise Time	T_{LD}	-	70	-	-	ns
Shift Clock Fall to Latch Pulse Fall Time	T_{SL}	-	70	-	-	ns
Latch Pulse Fall to Shift Clock Fall Time	T_{LH}	-	70	-	-	ns
Latch Pulse Rise to Shift Clock Rise Time	T_{LS}	-	70	-	-	ns
Input Signal Rise Time *2	T_R	-	-	-	20	ns
Input Signal Fall Time *2	T_F	-	-	-	20	ns
DISOFFB Removal Time	T_{SD}	-	100	-	-	ns
DISOFFB “L” Pulse Width	T_{WDL}	-	1.2	-	-	μs
Output Delay Time (1)	T_D	-	-	-	40	ns
Output Delay Time (2)	T_{PD1}, T_{PD2}	CL = 20pF	-	-	1.2	μs
Output Delay Time (3)	T_{PD3}	CL = 20pF	-	-	1.2	μs

Note1: Take the cascade connection into consideration.

Note2: (T_{WCK} - T_{WCKH} - T_{WCKL}) / 2 is maximum in the case of high speed operation.

Timing Characteristics of Segment Mode

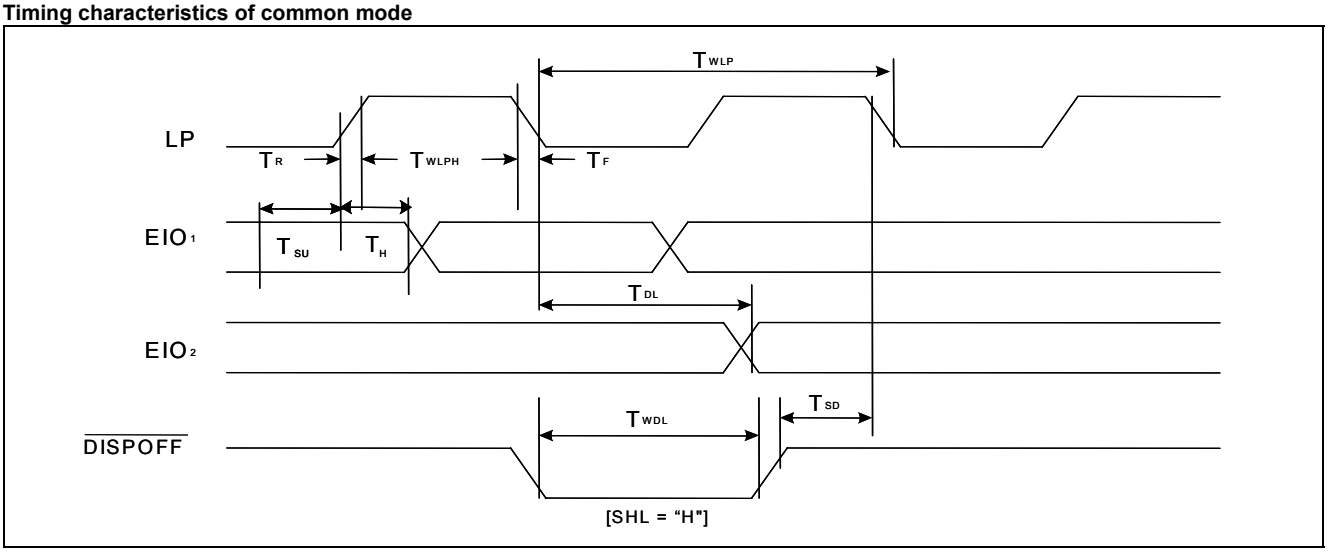


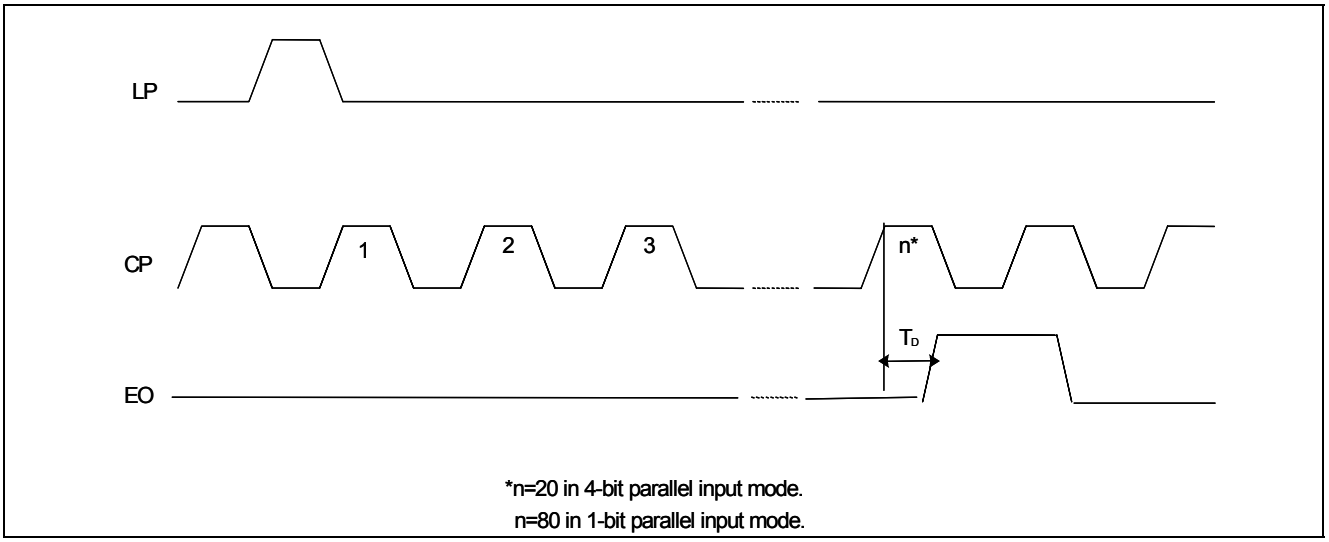


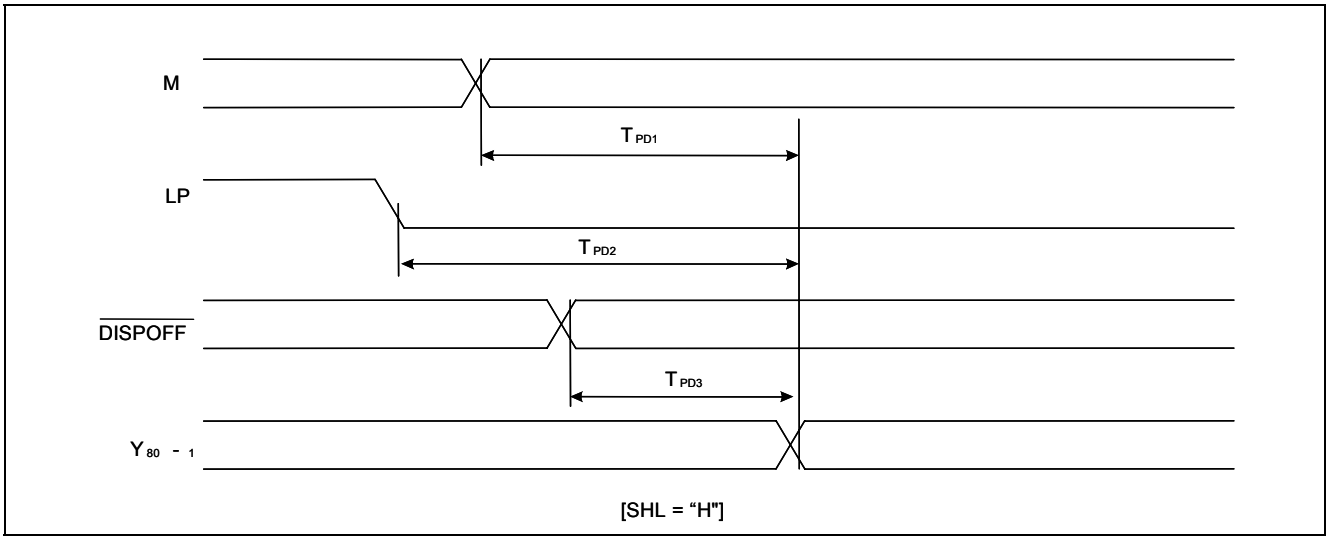
8.4.2. Common mode (VSS = 0V, VDD = +2.4V to +5.5V, V_0 = +3V to +14.5V, T_A = +25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift Clock Period	T_{WLP}	-	3.2	-	-	μs
Shift "H" Pulse Width	T_{WLPH}	VDD = +5.0V ± 10%	30	-	-	ns
		VDD = +2.4V ~ +4.5V	50	-	-	ns
Data Setup Time	T_{SU}	-	50	-	-	ns
Data Hold Time	T_H	-	50	-	-	ns
Input Signal Rise Time	T_R	-	-	-	25	ns
Input Signal Fall Time	T_F	-	-	-	25	ns
DISOFFB Removal Time	T_{SD}	-	100	-	-	ns
DISOFFB "L" Pulse Width	T_{WDL}	-	1.2	-	-	μs
Output Delay Time (1)	T_{DL}	C_L = 15pF	-	-	200	ns
Output Delay Time (2)	T_{PD1}, T_{PD2}	C_L = 15pF	-	-	1.2	μs
Output Delay Time (3)	T_{PD3}	C_L = 15pF	-	-	1.2	μs

Timing characteristics of common mode







9. APPLICATION CIRCUITS

The data transferred from GPLD1120D/GPLD2080A or GPLD1120D/GPLD2120A module will pass to last point.

Please refer to the example. We have an “E” letter (Fig) in computer and want to show it from computer to LCD panel, please see the following six sections, 9.1~9.6.

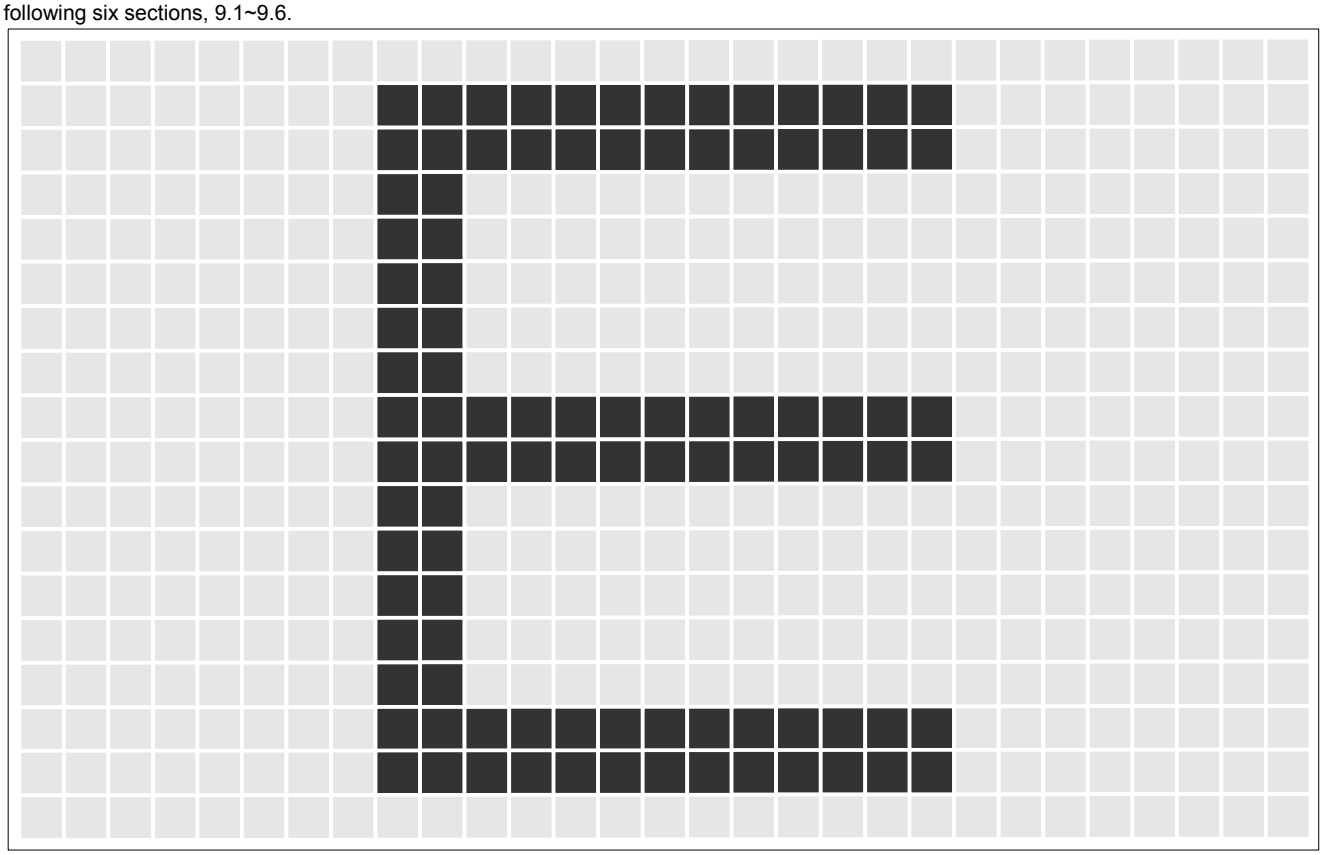
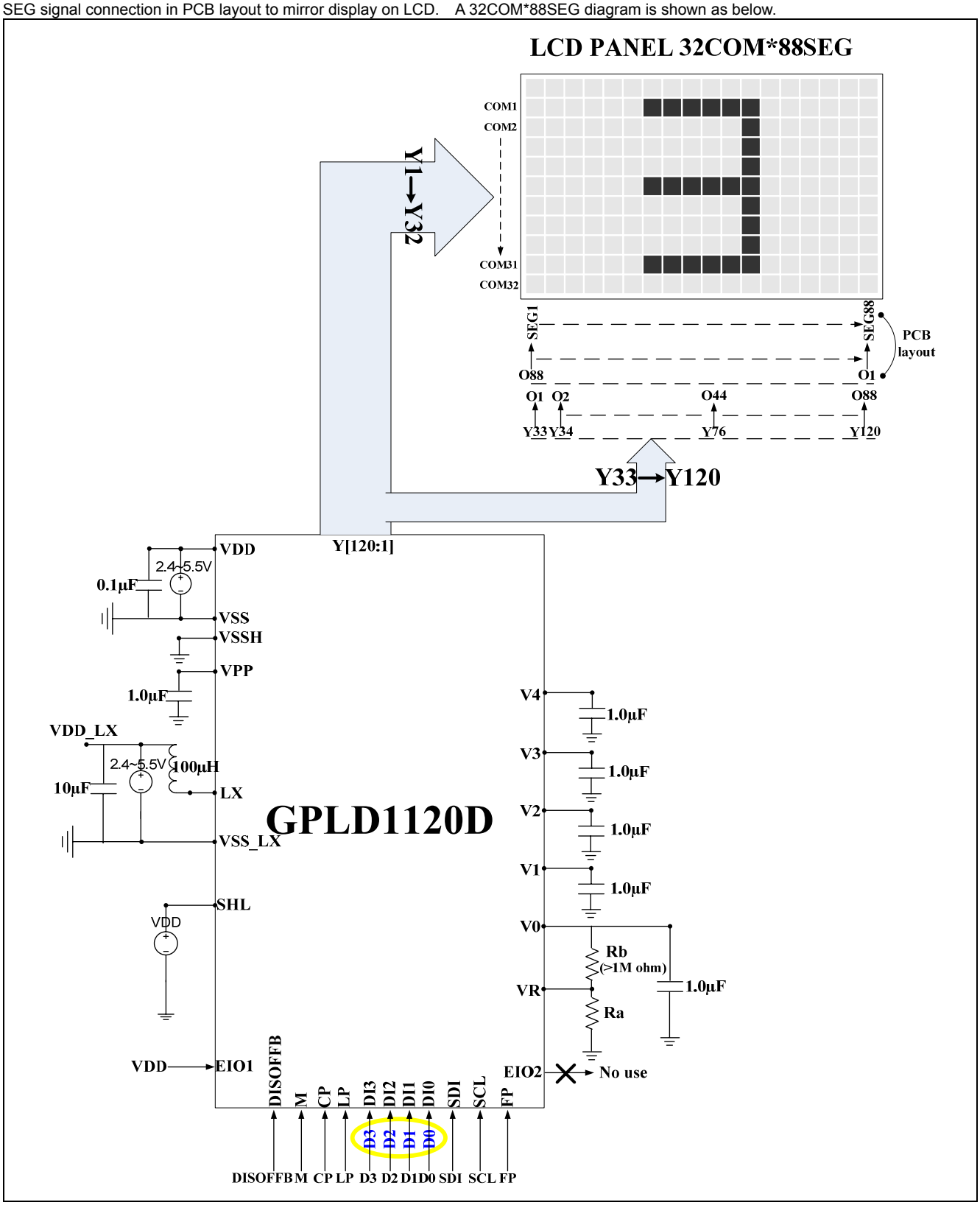


Fig. “E” letter in computer

9.1. (1) Only GPLD1120D Application with SHL=VDD to display 〝∃〞 letter in LCD Panel

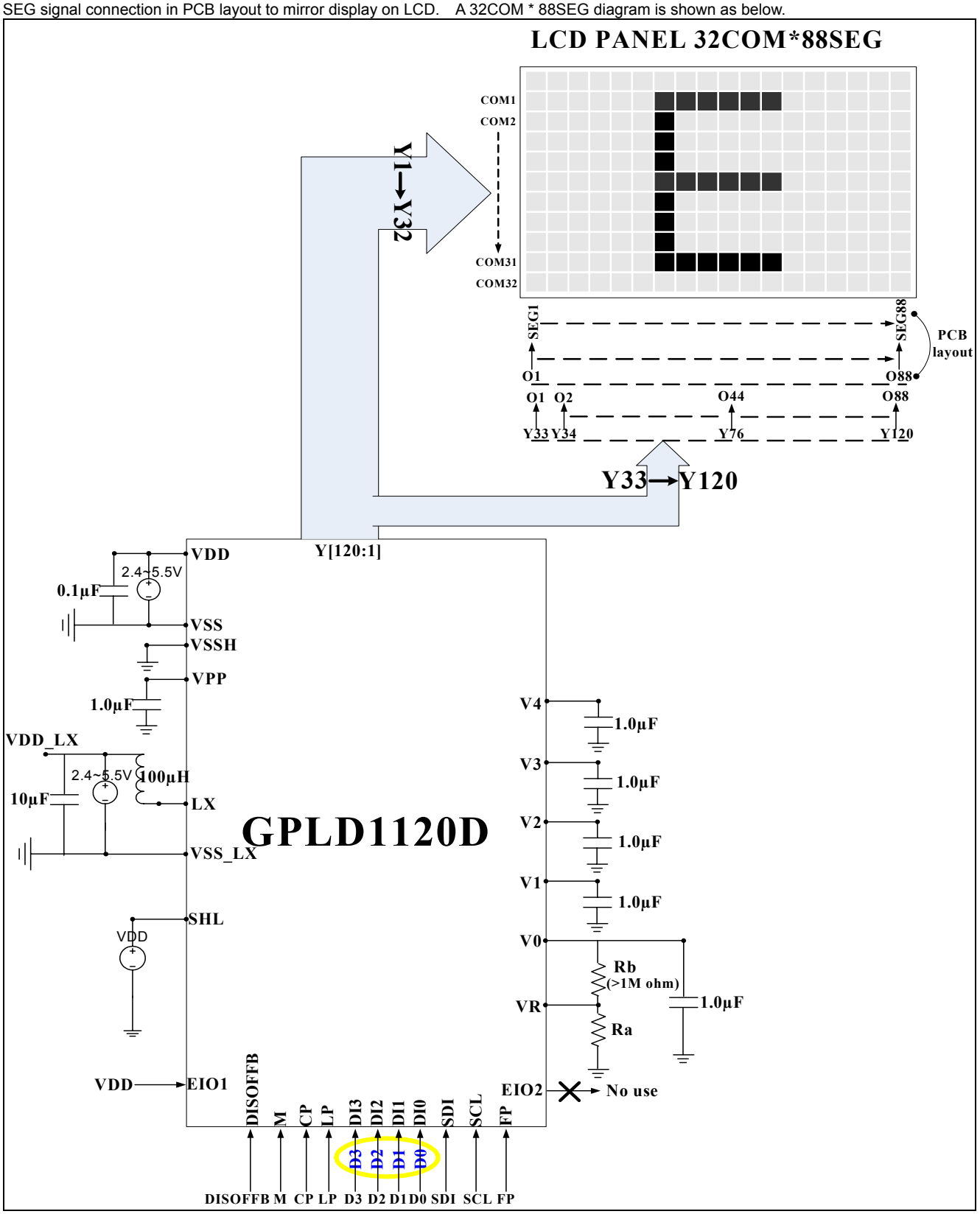
The SEG signal connected to O88→SEG1, O87→SEG2·····O2→SEG87, O1→SEG88 in PCB layout. You can also use reverse SEG signal connection in PCB layout to mirror display on LCD. A 32COM*88SEG diagram is shown as below.



Note1: VDD and VDD_LX power node are the same power supply voltage but different power path from external power.
Note2: The booster inductor value is recommended 100 μH for VDD=5.5V~3.3V and 220 μH for VDD=3.3V~2.4V.
Note3: In only GPLD1120D application, SHL and EIO1 both must be tied to VDD.

9.2. (2) Only GPLD1120D Application with SHL=VDD to display "E" letter in LCD Panel

The SEG signal connected to O1→SEG1, O2→SEG2·····O87→SEG87, O88→SEG88 in PCB layout. You can also use reverse SEG signal connection in PCB layout to mirror display on LCD. A 32COM * 88SEG diagram is shown as below.



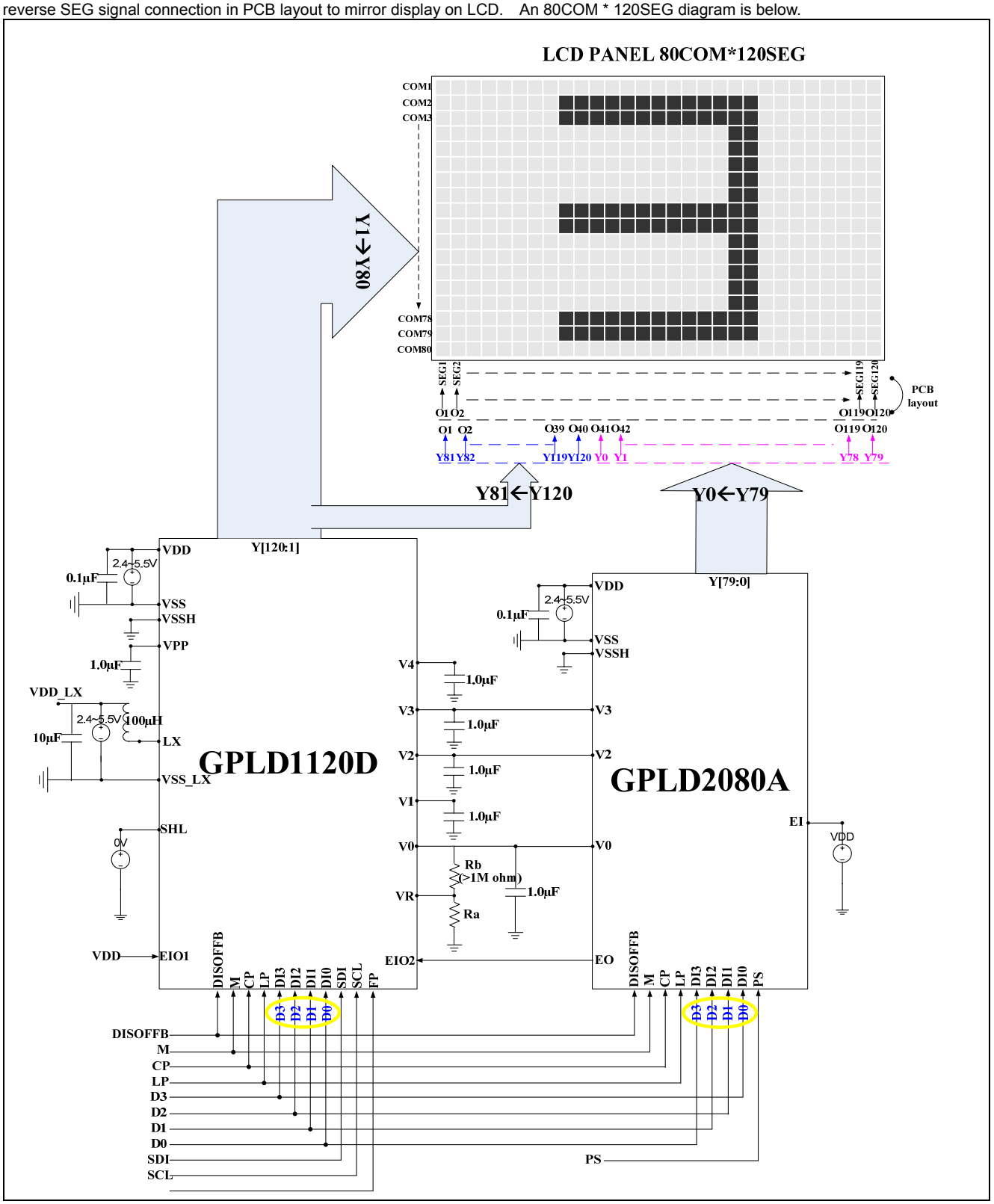
Note1: VDD and VDD_LX power node are the same power supply voltage but different power path from external power.

Note2: The booster inductor value is recommended 100 μH for VDD=5.5V~3.3V and 220 μH for VDD=3.3V~2.4V.

Note3: In only GPLD1120D application, SHL and EIO1 both must be tied to VDD.

9.3. (3) Application with GPLD2080A with SHL=0 to display 〝∃〞 letter in LCD Panel

The SEG signal connected to O1→SEG1, O2→SEG2·····O119→SEG119, O120→SEG120 in PCB layout. You also can use reverse SEG signal connection in PCB layout to mirror display on LCD. An 80COM * 120SEG diagram is below.



Note1: The segment data shifting direction from GPLD2080 to GPLD1120D is acceded only.

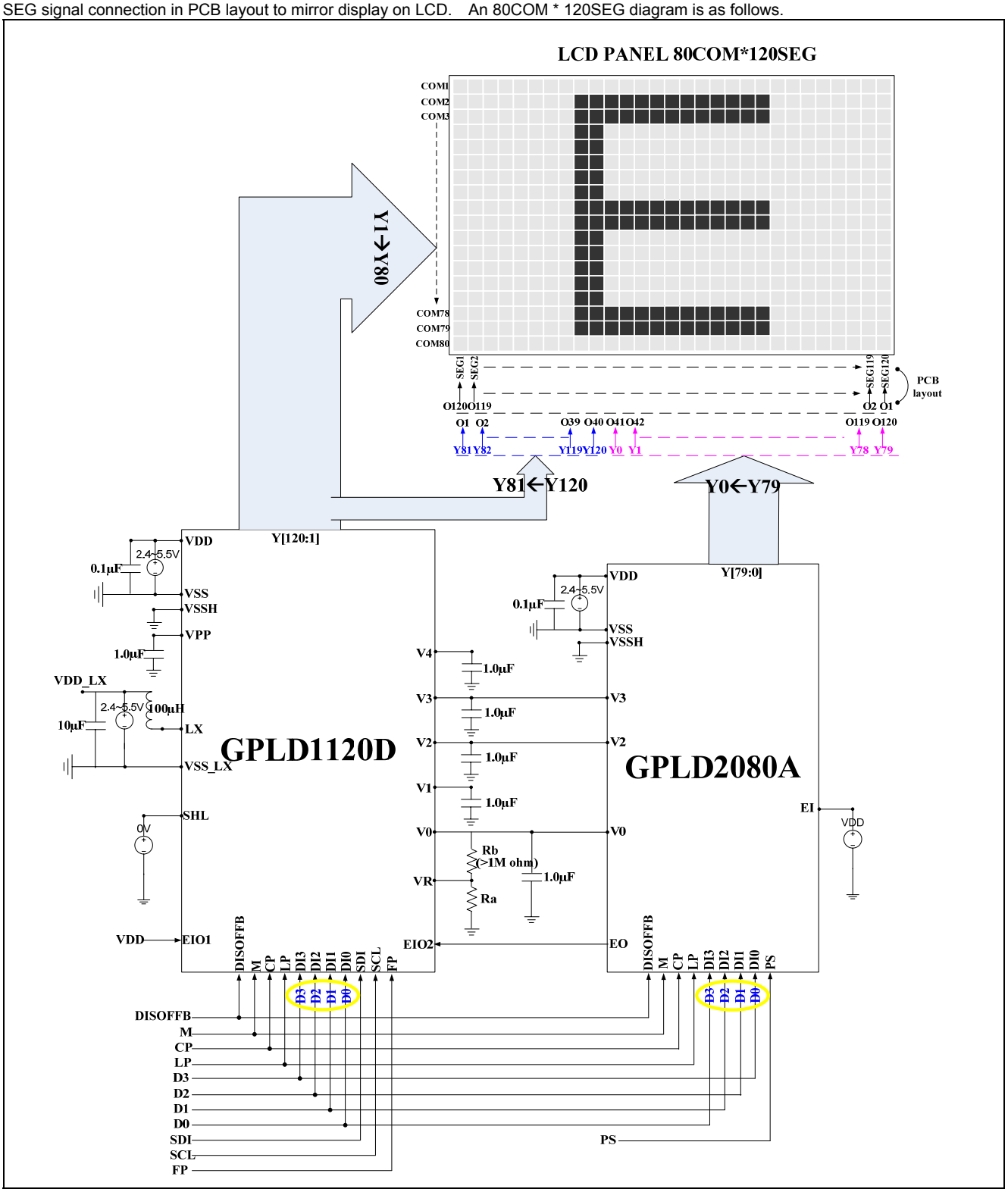
Note2: In the case of 80 COMs X 120 SEGs by GPLD1120D+GPLD2080, SHL can be connected to VSS only.

Note3: VDD and VDD_LX power node are the same power supply voltage but different power path from external power.

Note4: The booster inductor value is recommended 100 μH for VDD=5.5V~3.3V and 220 μH for VDD=3.3V~2.4V.

9.4. (4) Application with GPLD2080A with SHL=0 to display "E" letter in LCD Panel

The SEG signal connected to O120→SEG1, O119→SEG2····O2→SEG119, O1→SEG120 in PCB layout. You can also use reverse SEG signal connection in PCB layout to mirror display on LCD. An 80COM * 120SEG diagram is as follows.



Note1: The segment data shifting direction from GPLD2080 to GPLD1120D is acceded only.

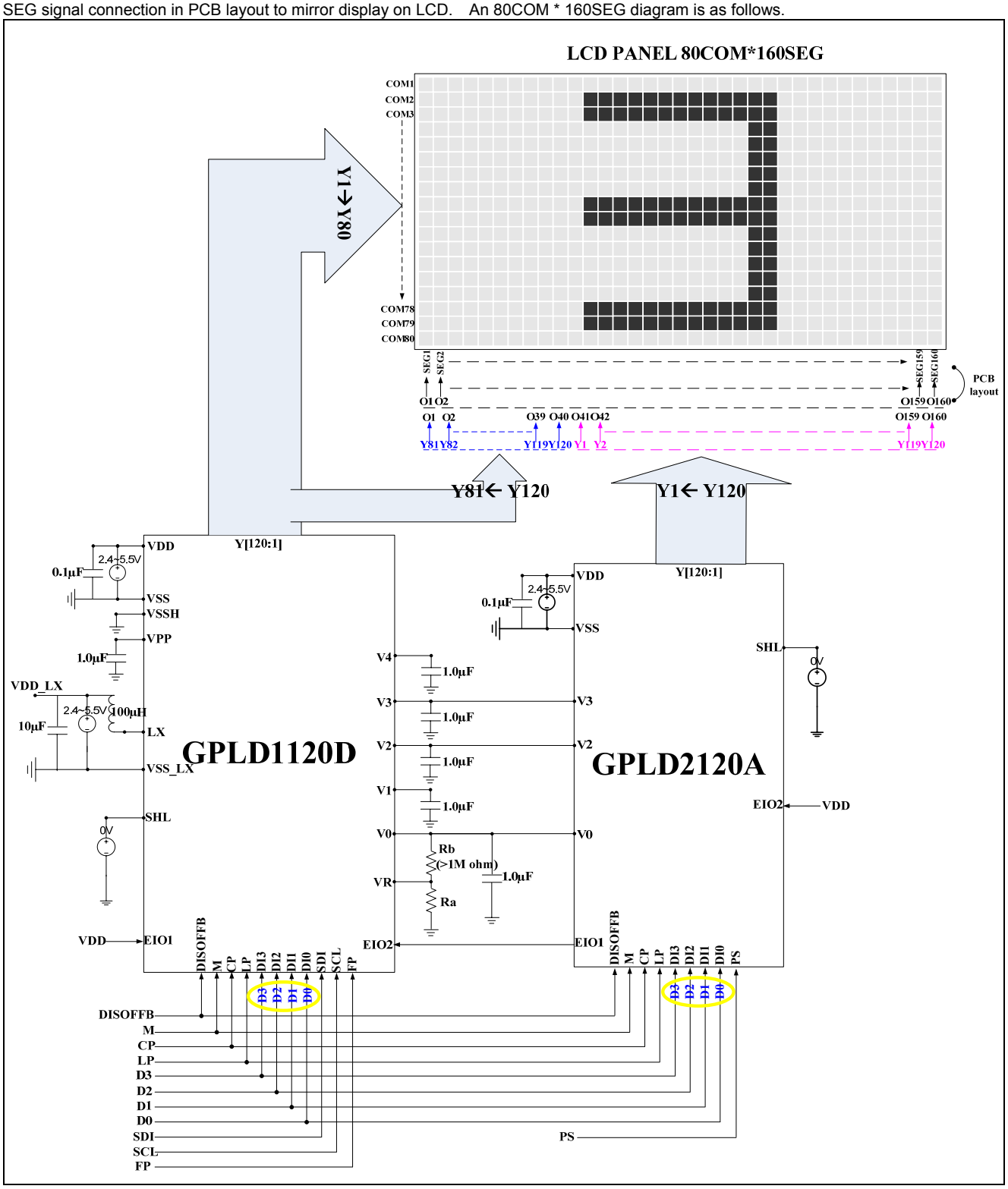
Note2: In the case of 80 COMs X 120 SEGs by GPLD1120D+GPLD2080, SHL can be connected to VSS only.

Note3: VDD and VDD_LX power node are the same power supply voltage but different power path from external power.

Note4: The booster inductor value is recommended 100 μH for VDD=5.5V~3.3V and 220 μH for VDD=3.3V~2.4V.

9.5. (5) Application with GPLD2120A with SHL=0 to display 〝∃〞 letter in LCD Panel

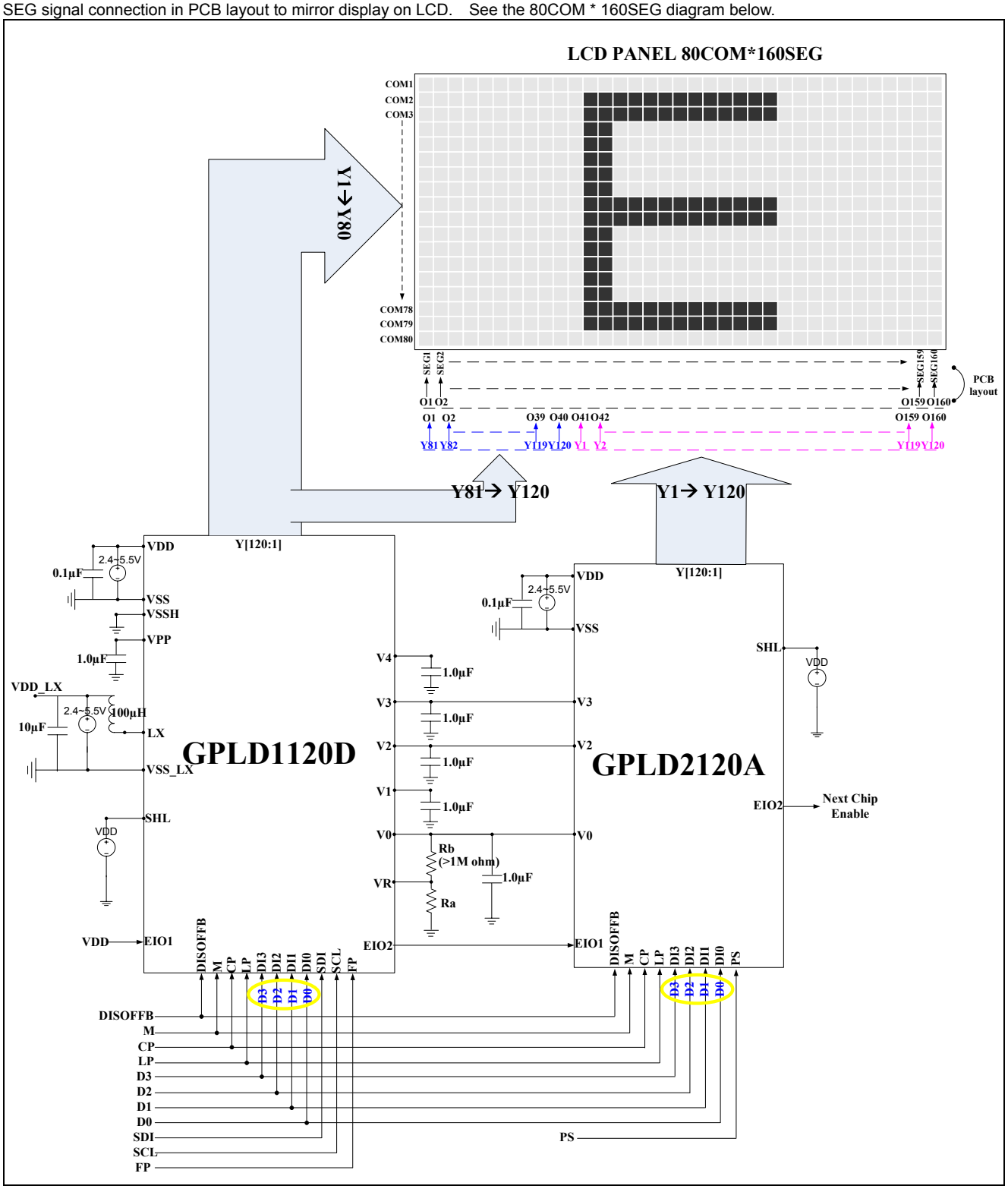
The SEG signal connected to O1→SEG1, O2→SEG2‧‧‧‧O159→SEG159, O160→SEG160 in PCB layout. You can also use reverse SEG signal connection in PCB layout to mirror display on LCD. An 80COM * 160SEG diagram is as follows.



Note1: VDD and VDD_LX power node are the same power supply voltage but different power path from external power.
Note2: The booster inductor value is recommended 100 μH for VDD=5.5V~3.3V and 220 μH for VDD=3.3V~2.4V.

9.6. (6) Application with GPLD2120A with SHL=VDD to display "E" letter in LCD Panel

The SEG signal connected to O1→SEG1, O2→SEG2·····O159→SEG159, O160→SEG160 in PCB layout. You can also use reverse SEG signal connection in PCB layout to mirror display on LCD. See the 80COM * 160SEG diagram below.



Note1: VDD and VDD_LX power node are the same power supply voltage but different power path from external power.
Note2: The booster inductor value is recommended 100 μH for VDD=5.5V~3.3V and 220 μH for VDD=3.3V~2.4V.

10. PACKAGE/PAD LOCATIONS

10.1. Ordering Information

Product Number	Package Type
GPLD1120D-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

11. DISCLAIMER

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12. REVISION HISTORY

Date	Revision #	Description	Page
Dec. 10, 2010	1.0	Officially Released Version	32
Oct. 19, 2010	0.1	Preliminary Version	32