DATA SHEET

凌通科技
Generalplus

# GPLD2120A

## 120 Channels SEGMENT STN LCD Driver

FEB. 08, 2006

Version 1.0

# Table of Contents

**PAGE**

**1. GENERAL DESCRIPTION ..... 3**
**2. FEATURES ..... 3**
**3. BLOCK DIAGRAM ..... 3**
3.1. INPUT/OUTPUT CIRCUITS ..... 4
**4. PIN DESCRIPTIONS ..... 5**
**5. FUNCTIONAL DESCRIPTIONS ..... 6**
5.1. FUNCTION OPERATIONS ..... 6
5.1.1. Truth table ..... 6
5.2. RELATIONSHIP BETWEEN THE DISPLAY DATA AND DRIVER OUTPUT PINS ..... 6
5.2.1. 4-bit parallel mode ..... 6
5.2.2. 1-bit serial mode ..... 6
5.2.3. Connection examples of plural segment drivers ..... 7
5.2.4. Timing characteristics of 4-device cascade connection of segment drivers ..... 8
**6. PRECAUTIONS ..... 9**
6.1. PRECAUTION WHEN OPERATING IN THE EXTERNAL POWER MODE ..... 9
**7. ELECTRICAL SPECIFICATIONS ..... 10**
7.1. ABSOLUTE MAXIMUM RATINGS ..... 10
7.2. RECOMMENDED OPERATING CONDITIONS ..... 10
7.3. DC CHARACTERISTICS ..... 10
7.3.1. Segment mode (VSS = 0V, VDD = +2.4V to +5.5V, V0 = +3V to +16V, TA = +25℃) ..... 10
7.4. AC CHARACTERISTICS ..... 11
7.4.1. Segment mode 1 (VSS = 0V, VDD = +4.5V to + +5.5V, V0 = +3V to +16V, TA = +25℃) ..... 11
7.4.2. Segment mode 2 (VSS = 0V, VDD = +2.4V to +4.5V, V0 = +3V to +16V, TA = +25℃) ..... 11
7.5. TIMING CHARACTERISTICS OF SEGMENT MODE ..... 12
**8. APPLICATION CIRCUIT ..... 13**
8.1. LCD PANEL SIZE: COM/SEG = 80/160 ..... 13
8.2. LCD PANEL SIZE: COM/SEG = 120/240 ..... 14
8.3. LCD PANEL SIZE: COM/SEG = 152/208 ..... 15
**9. PACKAGE/PAD LOCATIONS ..... 16**
9.1. PAD ASSIGNMENT AND LOCATIONS ..... 16
9.2. ORDERING INFORMATION ..... 16
**10. DISCLAIMER ..... 17**
**11. REVISION HISTORY ..... 18**

# 120 CHANNELS SEGMENT STN LCD DRIVER

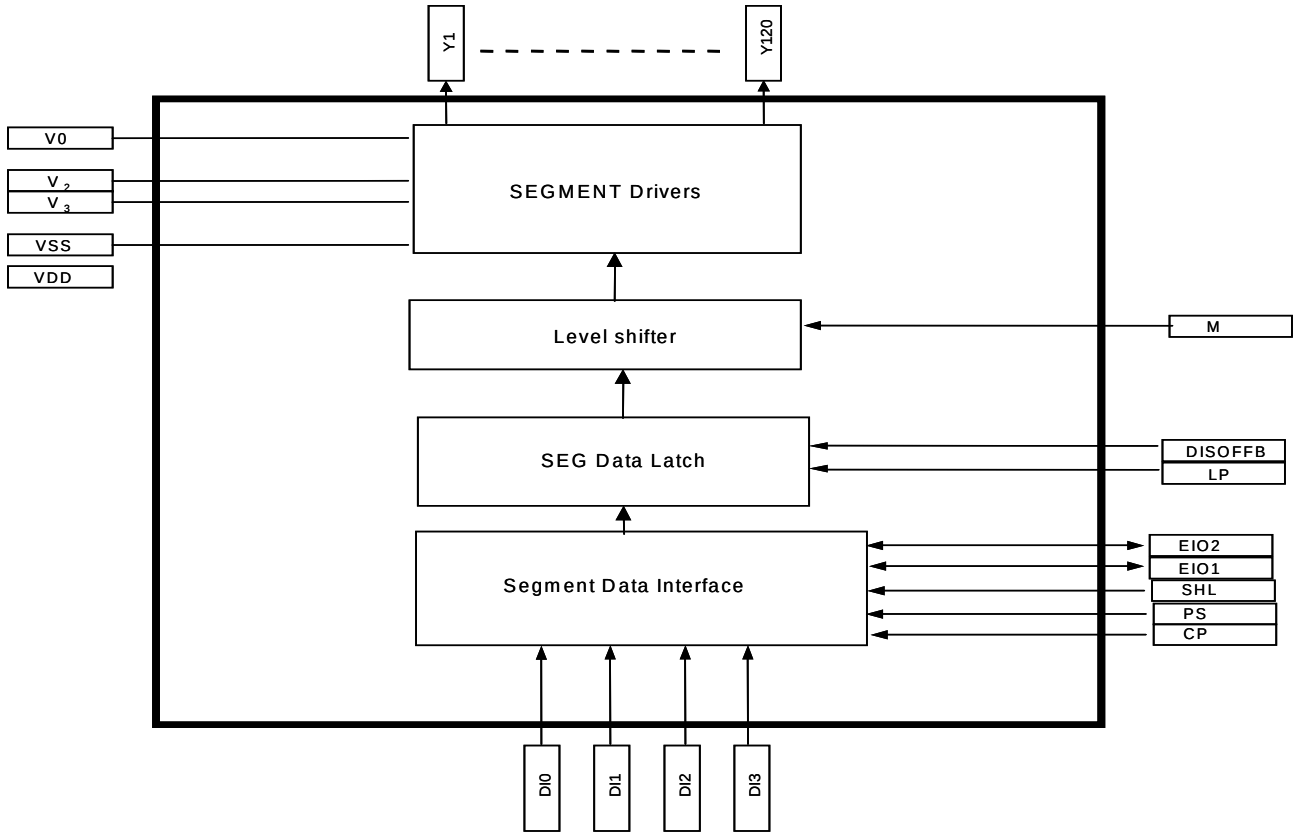
## 1. GENERAL DESCRIPTION

The GPLD2120A is a 120-channel segment driver IC and is suitable for driving small/medium scale dot matrix LCD panels. It is used in hand-hold game or electronic dictionary. The GPLD2120A is a segment driver and can display a STN-LCD panel with GPLD1120B.

## 2. FEATURES

- Number of LCD drive outputs: 120
- Supply voltage for LCD drive: 16V (max.)
- Supply voltage for logic system: 2.4V to 5.5V
- Adopts a data bus system
- 4-bits parallel /1-bit serial modes are selectable by PS pin.
- Bi-Directional display data shift.
- Automatic transfer function of enable signal (EIO1, EIO2)
- Chain function for different LCD resolution (EIO1, EIO2)
- Display off function
- Low power consumption
- Shift clock frequency
- 12.5 MHz (max.)

## 3. BLOCK DIAGRAM



### 3.1. Input/Output Circuits

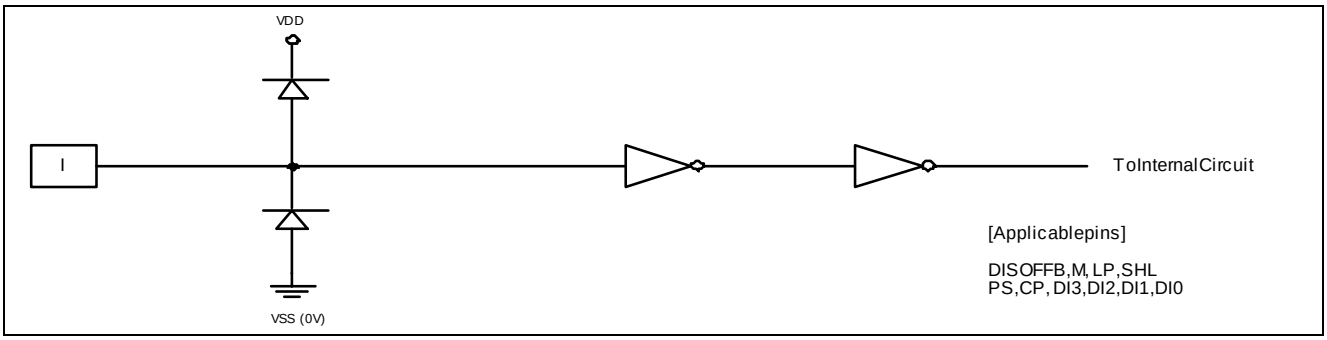



Figure 1: Input Circuit

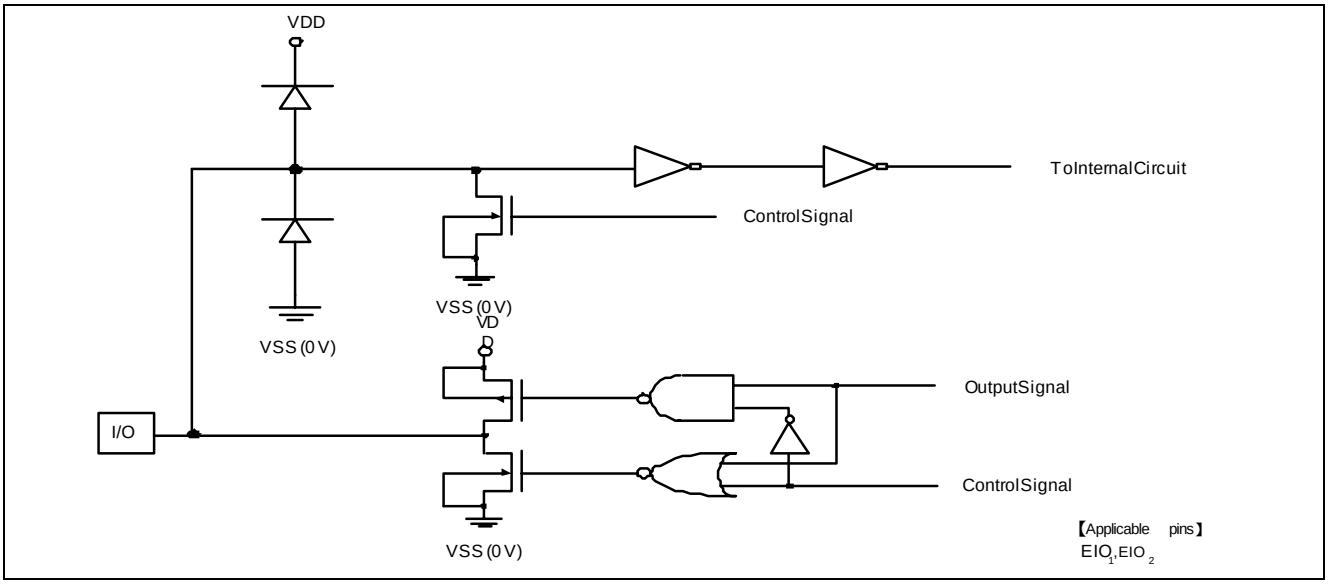



Figure 2: Input/Output Circuit

## 4. PIN DESCRIPTIONS

| Mnemonic | PIN No. | Type | Description |
|---|---|---|---|
| Y1 – Y120 | 17-136 | O | LCD driver output pins. |
| V0, V2, V3 | 9,8,7 | P | The bias voltages for LCD driving. Where V0>V2>V3>VSS. |
| SHL | 138 | I | Display data shift direction selection.<br>Input pin for selecting the reading direction of display data.<br>1). When set to VSS, data is read sequentially from Y120 to Y1.<br>2). When set to VDD, data is read sequentially from Y1 to Y120. |
| VDD | 10 | P | Power supply for logic system. (+2.4V to +5.5V) |
| EIO1, EIO2 | 2, 3 | I/O | Input/output pins for chip selection.<br>1). When SHL input is set to VSS, EIO1 is set for output and EIO2 is set for input.<br>2). When SHL input is set to VDD, EIO1 is set for input and EIO2 is set for output.<br>3). During output, it is set to “L”. After 120 bits of data have been read, it will be set to “H” for one cycle. After one cycle, it will return to “L”.<br>4). During input, the chip is selected while EI is set to “H” after the LP signal. The chip is non-selected after 120 bits of data have been read. |
| DI3 ~ DI0 | 15, 14,<br>13, 12 | I | Display data input at segment mode.<br>1). In 1-bit serial input mode (PS=”L”), input data into the pin DI3.<br>Connect DI2 - DI0 to VDD or VSS, avoid floating.<br>2). In 4-bit parallel input mode (PS=”H”), input data into the four pins, DI3 - DI0. |
| DISOFFB | 1 | I | Display Off control input pin, Control input pin for output non-select level.<br>When set to VSS, the LCD drive output pins (Y1 – Y120) are set to level VSS. |
| CP | 16 | I | Clock input for taking display data.<br>1). Data is read at the falling edge of the clock pulse. |
| LP | 4 | I | Latch pulse input for display data.<br>1). Data is latched at the falling edge of the clock pulse. |
| M | 5 | I | AC converting signal input for LCD drive waveform. |
| PS | 137 | I | Data input mode select pin.<br>1). When set to VSS, 1-bit serial input mode is set.<br>2). When set to VDD, 4-bit parallel input mode is set. |
| VSS | 6,11 | I | Ground (0V). Both two VSS pins should be connected to Ground. |

## 5. FUNCTIONAL DESCRIPTIONS

### 5.1. Function Operations

#### 5.1.1. Truth table

**Segment outputs**

| M | Latch data | DISOFFB | Driver output voltage level |
|---|---|---|---|
| L | L | H | V2 |
| L | H | H | V0 |
| H | L | H | V3 |
| H | H | H | VSS |
| X | X | L | VSS |

**Note1:** V0 > V2 > V3 > VSS, L: VSS (0V), H: VDD (+2.4V to +5.5V), X: Don't care.

**Note2:** "Don't care" should be fixed to "H" or "L", avoiding floating. There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supply regular voltage is assigned by specification for each power pin.

### 5.2. Relationship between the Display Data and Driver Output Pins

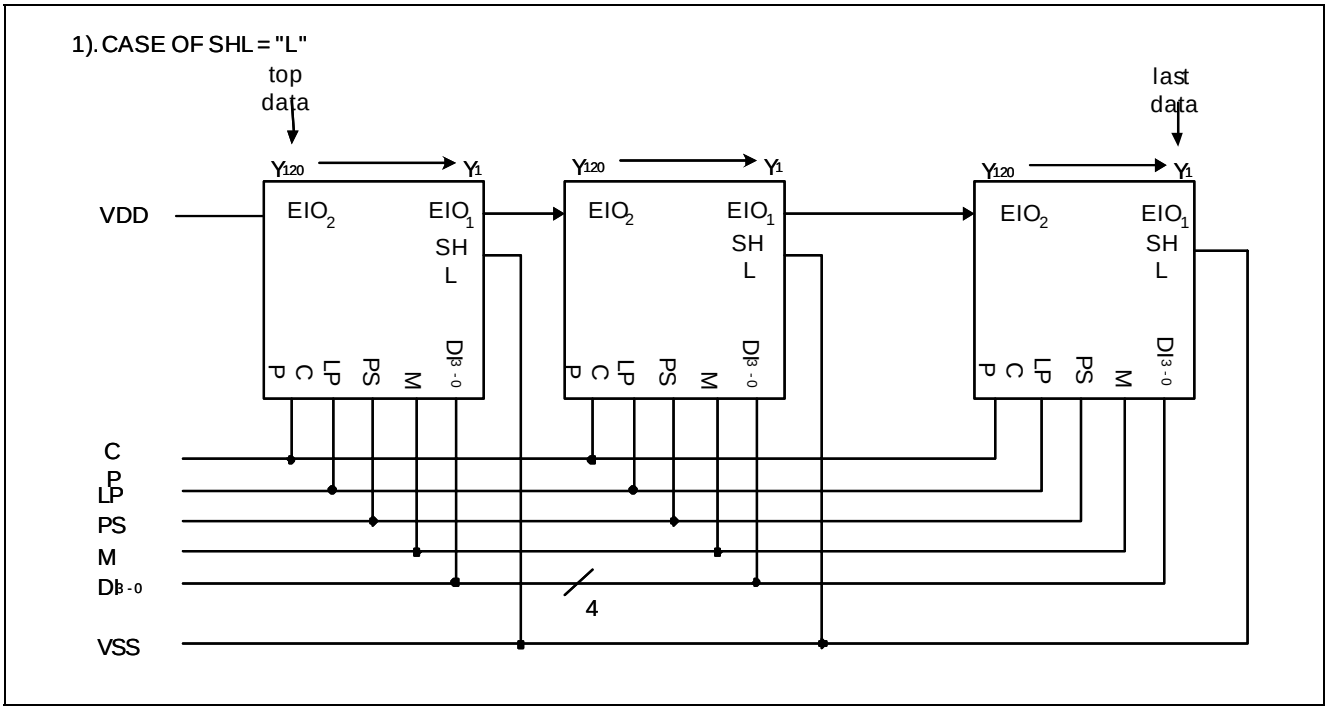
#### 5.2.1. 4-bit parallel mode

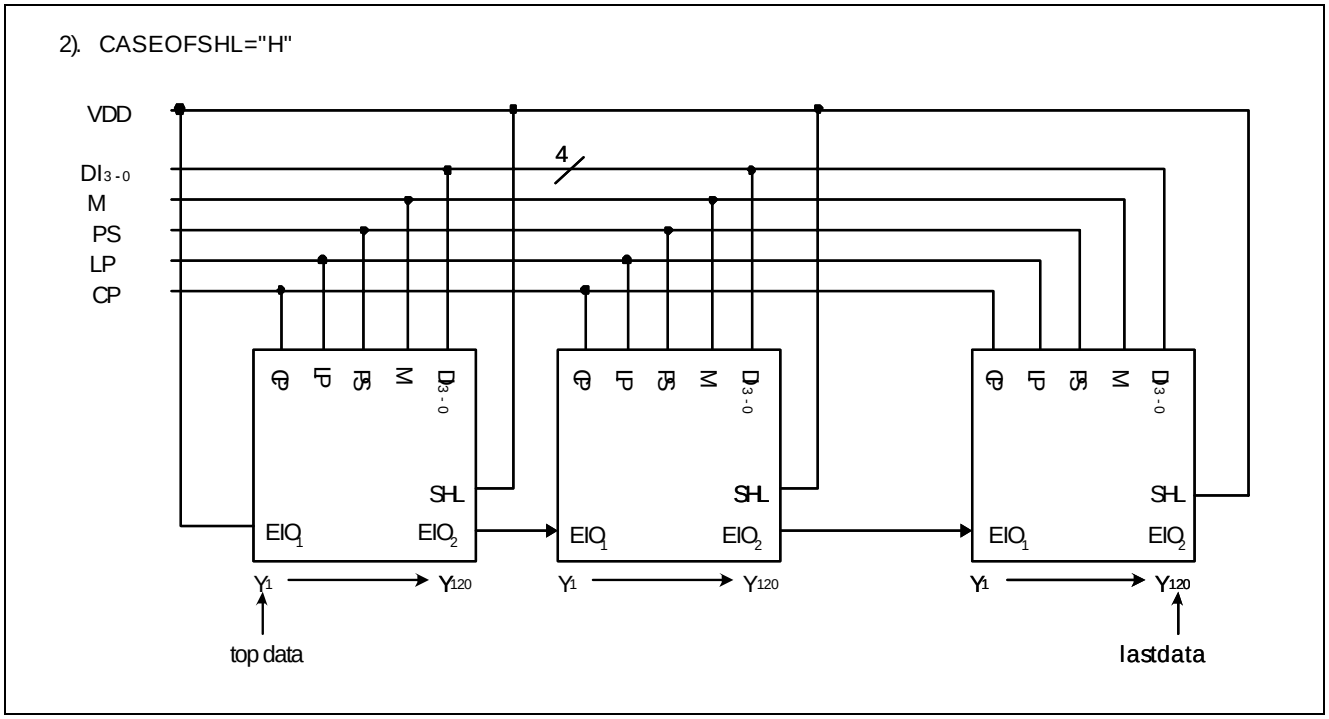
| SHL | EIO1 | EIO2 | Input Data | Figure of Clock | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 Clock | 2 Clock | 3 Clock | • • • | • • • | • • • | 28 Clock | 29 Clock | 30 Clock |
| L | Output | Input | DI3 | Y120 | Y116 | Y112 | • • • | • • • | • • • | Y12 | Y8 | Y4 |
| | | | DI2 | Y119 | Y115 | Y111 | • • • | • • • | • • • | Y11 | Y7 | Y3 |
| | | | DI1 | Y118 | Y114 | Y110 | • • • | • • • | • • • | Y10 | Y6 | Y2 |
| | | | DI0 | Y117 | Y113 | Y109 | • • • | • • • | • • • | Y9 | Y5 | Y1 |
| H | Input | Output | DI3 | Y1 | Y5 | Y9 | • • • | • • • | • • • | Y109 | Y113 | Y117 |
| | | | DI2 | Y2 | Y6 | Y10 | • • • | • • • | • • • | Y110 | Y114 | Y118 |
| | | | DI1 | Y3 | Y7 | Y11 | • • • | • • • | • • • | Y111 | Y115 | Y119 |
| | | | DI0 | Y4 | Y8 | Y12 | • • • | • • • | • • • | Y112 | Y116 | Y120 |

#### 5.2.2. 1-bit serial mode

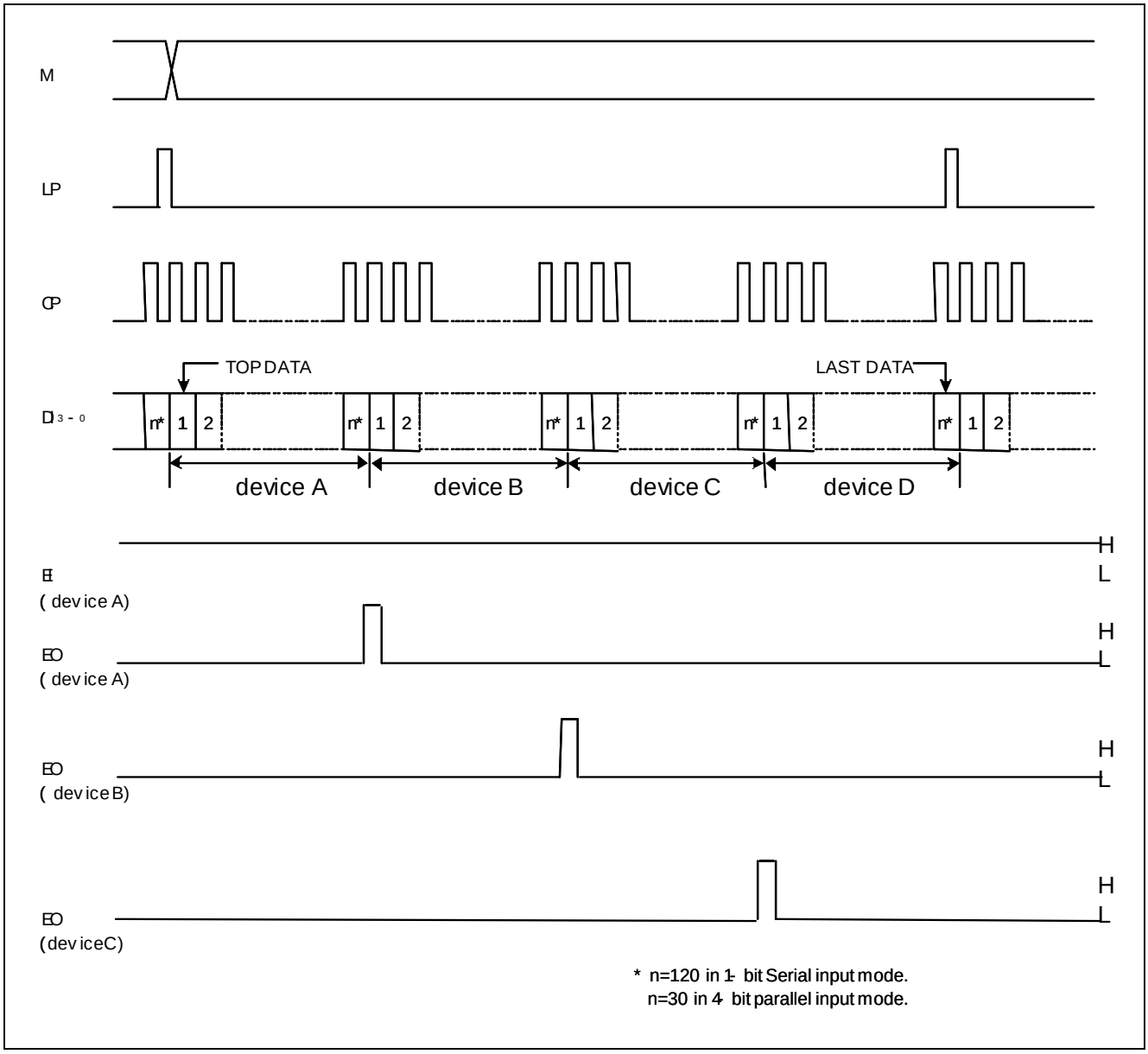
| SHL | EIO1 | EIO2 | Input Data | Figure of Clock | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 Clock | 2 Clock | 3 Clock | • • • | • • • | • • • | 118 Clock | 119 Clock | 120 Clock |
| L | Output | Input | DI3 | Y120 | Y119 | Y118 | • • • | • • • | • • • | Y3 | Y2 | Y1 |
| | | | DI2 | × | × | × | × | × | × | × | × | × |
| | | | DI1 | × | × | × | × | × | × | × | × | × |
| | | | DI0 | × | × | × | × | × | × | × | × | × |
| H | Input | Output | DI3 | Y1 | Y2 | Y3 | • • • | • • • | • • • | Y118 | Y119 | Y120 |
| | | | DI2 | × | × | × | × | × | × | × | × | × |
| | | | DI1 | × | × | × | × | × | × | × | × | × |
| | | | DI0 | × | × | × | × | × | × | × | × | × |

### 5.2.3. Connection examples of plural segment drivers



### 5.2.4. Timing characteristics of 4-device cascade connection of segment drivers



## 6. PRECAUTIONS

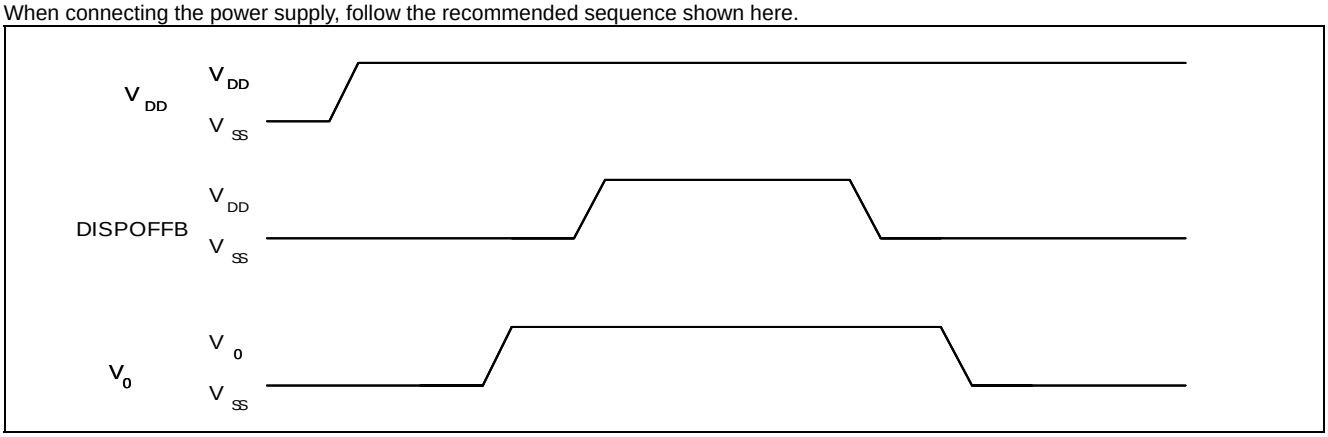
### 6.1. Precaution when operating in the external power mode

This GPLD2120A has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating.

When connecting to power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD driver power.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LCD driver power supply after resetting logic condition of this LSI inside on Displayoff function. After that, cancel the Displayoff function after the LCD driver power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level VSS on Displayoff function. After that, disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.



## 7. ELECTRICAL SPECIFICATIONS

### 7.1. Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Applicable Pins | Ratings | Unit |
|---|---|---|---|---|---|
| Supply voltage (1) | VDD | $T_A$ = +25℃ Referenced to VSS (0V) | VDD | -0.3 to +6.5 | V |
| Supply voltage (2) | V0 | | V0 | -0.3 to +18 | V |
| | V2 | | V2 | -0.3 to V0 + 0.3 | V |
| | V3 | | V3 | -0.3 to V0 + 0.3 | V |
| Input voltage | VI | | DI3 - DI0, CP, LP, SHL, M, PS, EIO1, EIO2, DISOFFB | -0.3 to VDD + 0.3 | V |
| Storage temperature | $T_{STG}$ | - | - | -45 to +125 | ℃ |

**Note1:** $T_A$ = +25℃

**Note2:** The maximum applicable voltage on any pin with respect to VSS (0V).

**Note3:** Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

### 7.2. Recommended Operating Conditions

| Parameter | Symbol | Conditions | Applicable Pins | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage (1) | VDD | Referenced to VSS (0V) | VDD | +2.4 | - | +5.5 | V |
| Supply voltage (2) | V0 | | V0 | +3 | - | +16 | V |
| Operating temperature | $T_{OPR}$ | - | - | -20 | - | +75 | ℃ |

**Note1:** The applicable voltage on any pin with respect to VSS (0V).

**Note2:** Ensure that voltage are set such that V0 > V2 > V3 > VSS.

### 7.3. DC Characteristics

#### 7.3.1. Segment mode (VSS = 0V, VDD = +2.4V to +5.5V, V0 = +3V to +16V, TA = +25℃)

| Parameter | Symbol | Conditions | Applicable Pins | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | - | DI3 - DI0, CP, LP, SHL, M, PS, DISOFFB | 0.8VDD | - | -- | V |
| | $V_{IL}$ | - | | - | - | 0.2VDD | V |
| Output voltage | $V_{OH}$ | $I_{OH}$ = -0.4mA | EIO1, EIO2 | VDD - 0.4 | - | - | V |
| | $V_{OL}$ | $I_{OL}$ = +0.4mA | | - | - | +0.4 | V |
| Input leakage current | $I_{LIH}$ | $V_I$ = VDD | DI3 - DI0, CP, LP, SHL, M, PS, DISOFFB, EIO1, EIO2 | - | - | +5 | μA |
| | $I_{LIL}$ | $V_I$ = VSS | | - | - | -5 | μA |
| Output resistance | $R_{ON}$ | V0 = +16V | Y1 - Y120 | - | 1.5 | 2.0 | KΩ |
| Stand-by current | $I_{STB}$ | *Note1 | VSS | - | - | 20 | μA |
| Supply current (1) | $I_{DD}$ | *Note2 | VDD | - | - | 50 | μA |
| Supply current (2) | $I_0$ | *Note2 | V0 | - | - | 10 | μA |

**Note1:** VDD = +5.5V, $V_0$ = +16V, CPU no access stand-by mode

**Note2:** VDD = +3.3V, $V_0$ = +16V, $f_M$ = 55Hz, $f_{LP}$ = 13.2KHz, $f_{CP}$ = 396KHz, EIO1=VDD, SHL=VDD, PS=VDD (4-bit Parallel input mode), DI[3:0]=1010, DISOFFB=VDD, No LCD Panel loading.

### 7.4. AC Characteristics

#### 7.4.1. Segment mode 1 (VSS = 0V, VDD = +4.5V to + +5.5V, V0 = +3V to +16V, TA = +25℃)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Shift clock period *1 | $T_{WCK}$ | *Note1/*Note2 | 80 | - | - | ns |
| Shift clock “H” pulse width | $T_{WCKH}$ | - | 35 | - | - | ns |
| Shift clock “L” pulse width | $T_{WCKL}$ | - | 35 | - | - | ns |
| Data setup time | $T_{DS}$ | - | 35 | - | - | ns |
| Data hold time | $T_{DH}$ | - | 35 | - | - | ns |
| Latch pulse “H” pulse width | $T_{WLPH}$ | - | 35 | - | - | ns |
| Shift clock rise to latch pulse rise time | $T_{LD}$ | - | 0 | - | - | ns |
| Shift clock fall to latch pulse fall time | $T_{SL}$ | - | 35 | - | - | ns |
| Latch pulse fall to shift clock fall time | $T_{LH}$ | - | 35 | - | - | ns |
| Latch pulse rise to shift clock rise time | $T_{LS}$ | - | 0 | - | - | ns |
| Input signal rise time *2 | $T_R$ | *Note2 | - | - | 25 | ns |
| Input signal fall time *2 | $T_F$ | *Note2 | - | - | 25 | ns |
| DISOFFB removal time | $T_{SD}$ | - | 100 | - | - | ns |
| DISOFFB “L” pulse width | $T_{WDL}$ | - | 1.2 | - | - | µs |
| Output delay time (1) | $T_D$ | CL = 15pF | - | - | 40 | ns |
| Output delay time (2) | $T_{PD1}$, $T_{PD2}$ | CL = 15pF | - | - | 1.2 | µs |
| Output delay time (3) | $T_{PD3}$ | CL = 15pF | - | - | 1.2 | µs |

**Note1:** Take the cascade connection into consideration.

**Note2:** ($T_{WCK}$ - $T_{WCKH}$ - $T_{WCKL}$) / 2 is maximum in the case of high speed operation.

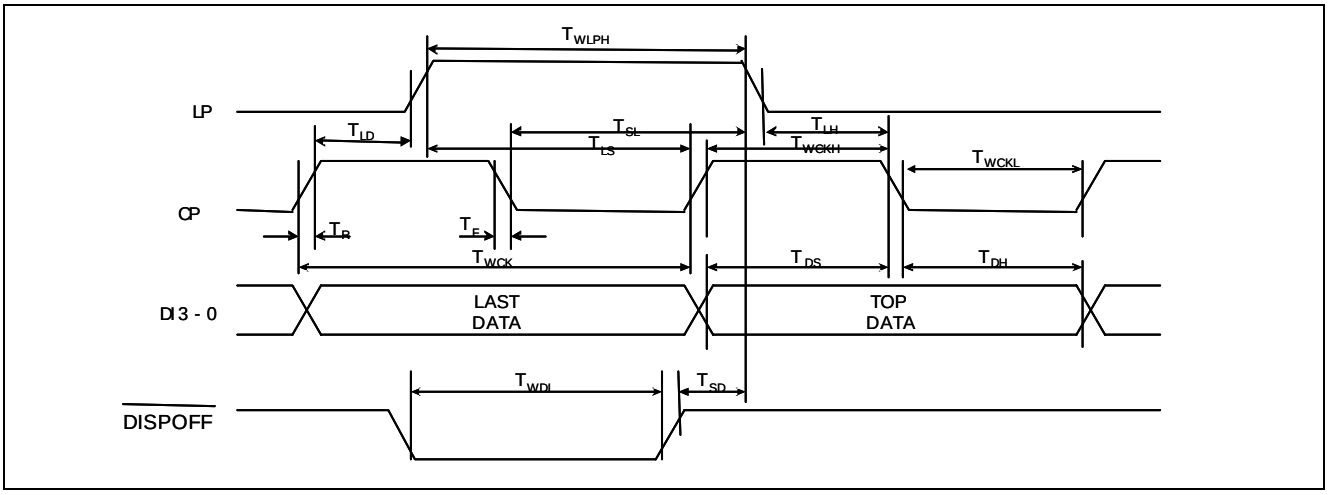
#### 7.4.2. Segment mode 2 (VSS = 0V, VDD = +2.4V to +4.5V, V0 = +3V to +16V, TA = +25℃)

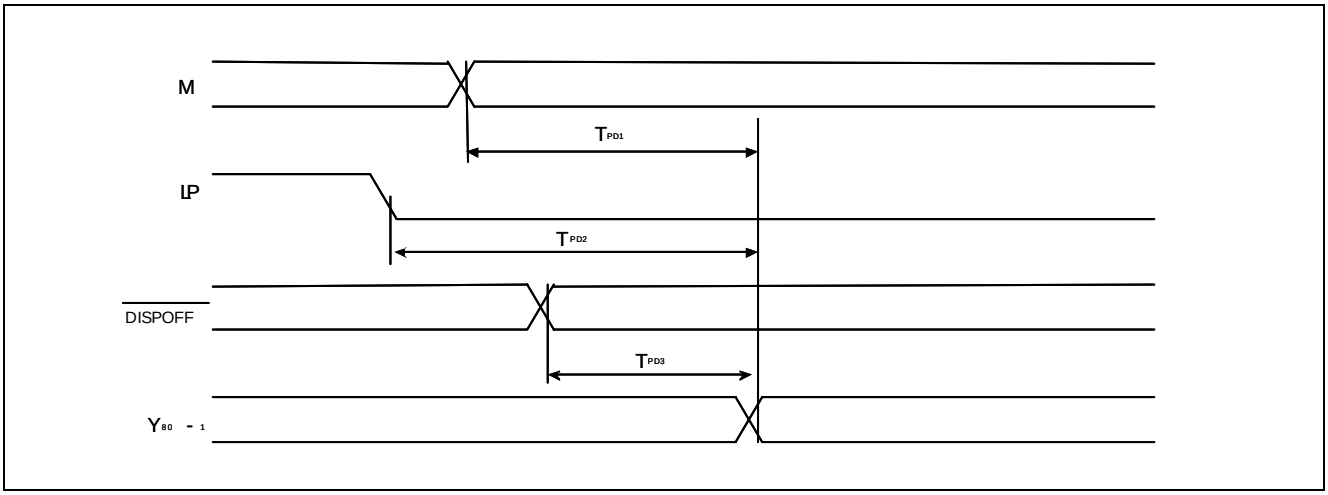
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Shift clock period *1 | $T_{WCK}$ | *Note1/*Note2 | 120 | - | - | ns |
| Shift clock “H” pulse width | $T_{WCKH}$ | - | 55 | - | - | ns |
| Shift clock “L” pulse width | $T_{WCKL}$ | - | 55 | - | - | ns |
| Data setup time | $T_{DS}$ | - | 55 | - | - | ns |
| Data hold time | $T_{DH}$ | - | 55 | - | - | ns |
| Latch pulse “H” pulse width | $T_{WLPH}$ | - | 55 | - | - | ns |
| Shift clock rise to latch pulse rise time | $T_{LD}$ | - | 0 | - | - | ns |
| Shift clock fall to latch pulse fall time | $T_{SL}$ | - | 55 | - | - | ns |
| Latch pulse fall to shift clock fall time | $T_{LH}$ | - | 55 | - | - | ns |
| Latch pulse rise to shift clock rise time | $T_{LS}$ | - | 0 | - | - | ns |
| Input signal rise time *2 | $T_R$ | *Note2 | - | - | 25 | ns |
| Input signal fall time *2 | $T_F$ | *Note2 | - | - | 25 | ns |
| DISOFFB removal time | $T_{SD}$ | - | 100 | - | - | ns |
| DISOFFB “L” pulse width | $T_{WDL}$ | - | 1.2 | - | - | µs |
| Output delay time (1) | $T_D$ | CL = 15pF | - | - | 75 | ns |
| Output delay time (2) | $T_{PD1}$, $T_{PD2}$ | CL = 15pF | - | - | 1.2 | µs |
| Output delay time (3) | $T_{PD3}$ | CL = 15pF | - | - | 1.2 | µs |

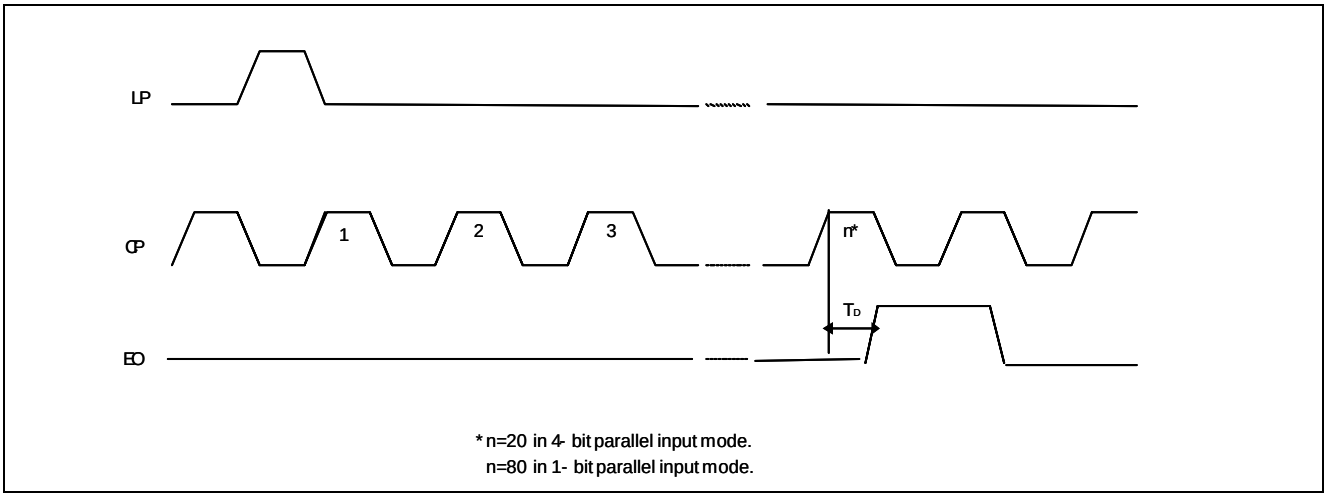
**Note1:** Take the cascade connection into consideration.

**Note2:** ($T_{WCK}$ - $T_{WCKH}$ - $T_{WCKL}$) / 2 is maximum in the case of high speed operation.

### 7.5. Timing Characteristics of Segment Mode



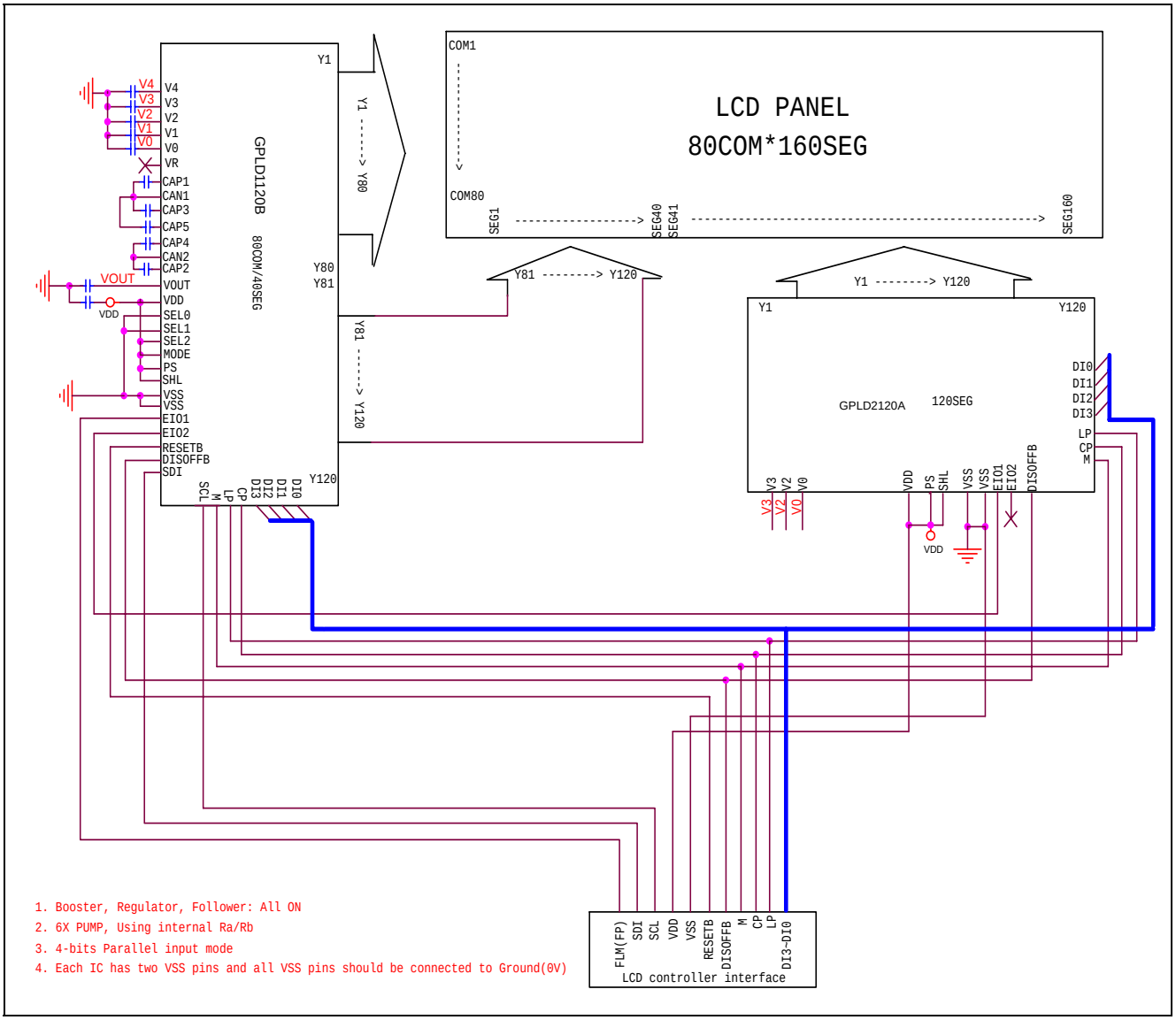



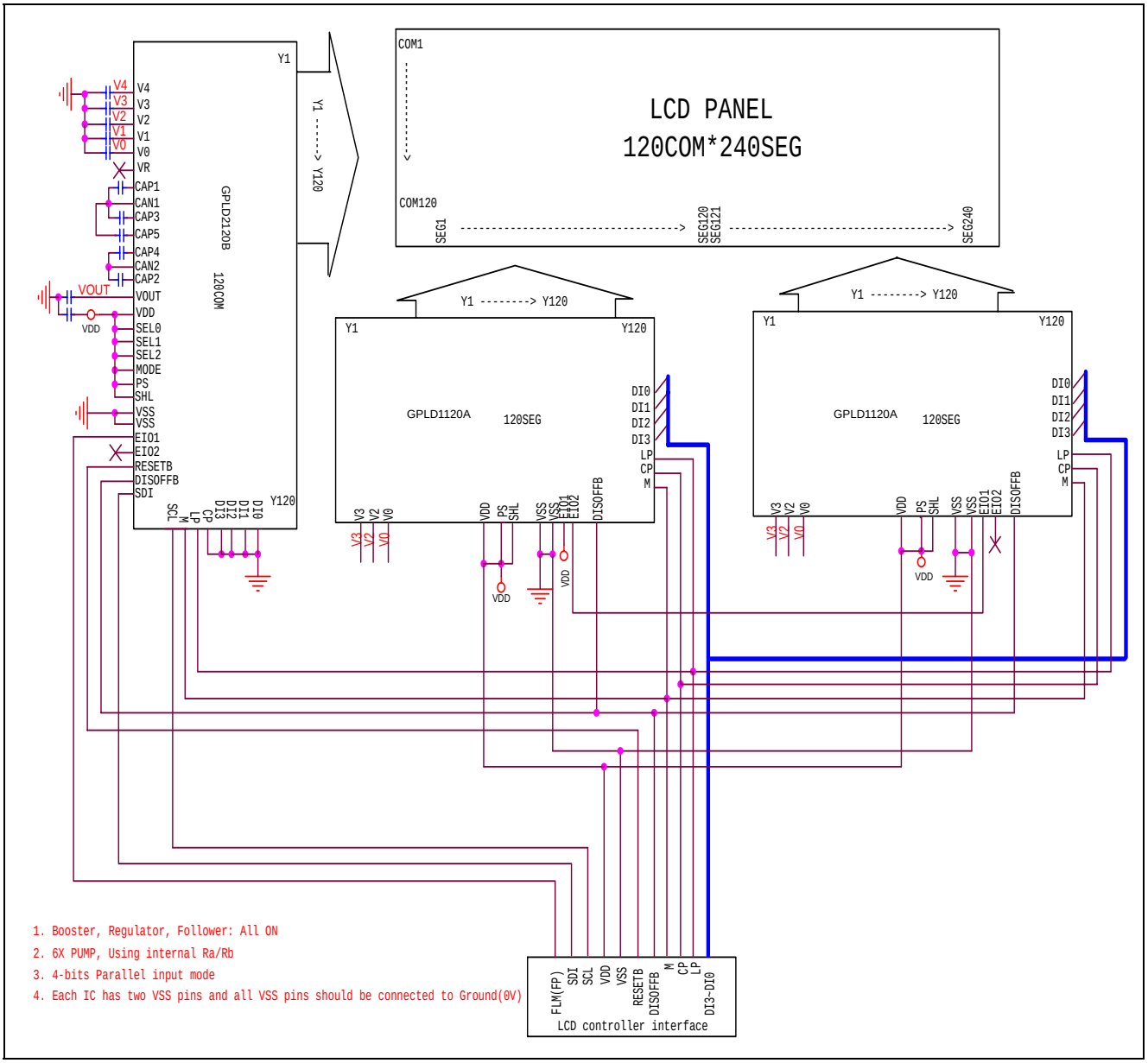

* n=20 in 4- bit parallel input mode.
n=80 in 1- bit parallel input mode.

## 8. APPLICATION CIRCUIT

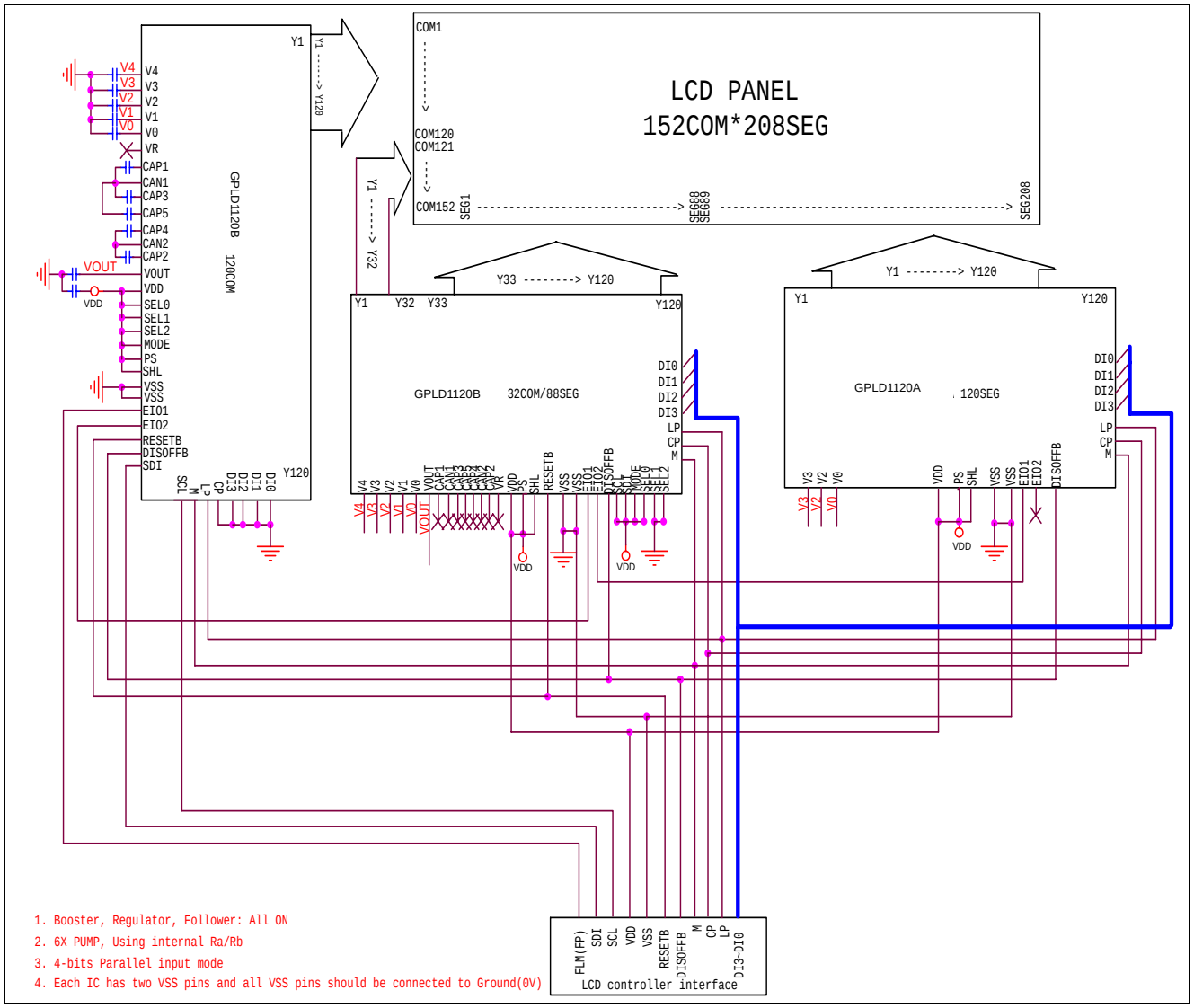
### 8.1. LCD Panel Size: COM/SEG = 80/160



### 8.2. LCD Panel Size: COM/SEG = 120/240

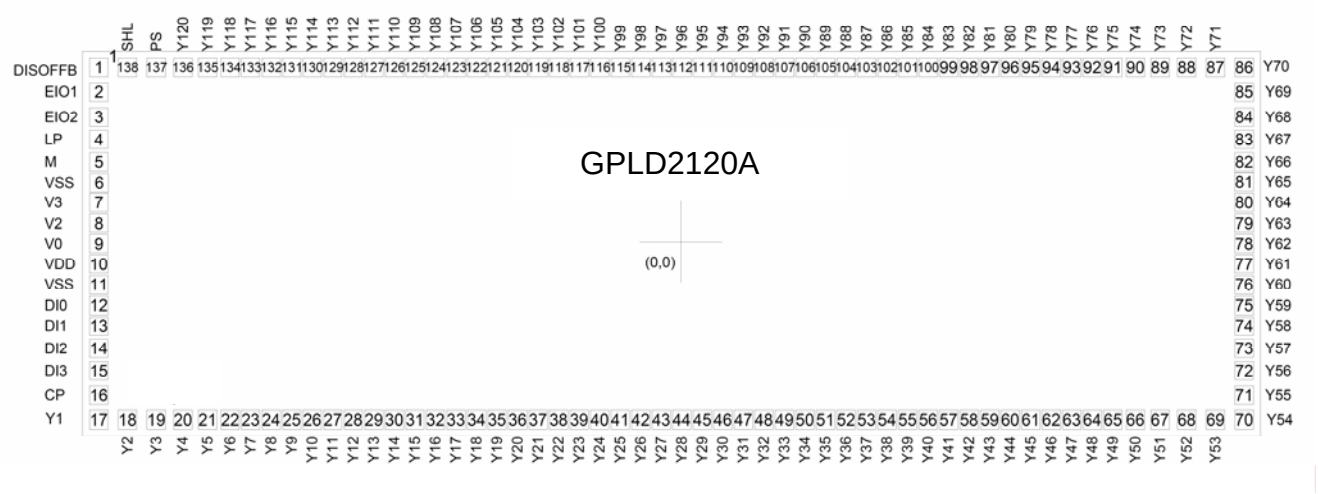


### 8.3. LCD Panel Size: COM/SEG = 152/208



## 9. PACKAGE/PAD LOCATIONS

### 9.1. PAD Assignment and Locations




The IC substrate should be connected to VSS

**Note1:** To ensure that the IC functions properly, please bond all of VDD and VSS pins.

**Note2:** The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

### 9.2. Ordering Information

| Product Number | Package Type |
|---|---|
| GPLD2120A - NnnV - C | Chip form |

**Note1:** Code number is assigned for customer.

**Note2:** Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

## 10. DISCLAIMER

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## 11. REVISION HISTORY

| Date | Revision # | Description | Page |
|---|---|---|---|
| FEB. 08, 2006 | 1.0 | Original<br>Note: The GPLD2120A data sheet v1.0 is a continued version of SPLD2120A data sheet v0.1. | 18 |