DATA SHEET

GPM6P1129A / GPM6C1067A
GPM6P1065A / GPM6P1033A
GPM6P1017A / GPM6P1015A

Learning Type Remote Controller

Preliminary

AUG. 17, 2010

Version 0.1

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Learning Type Remote Controller

1. GENERAL DESCRIPTION

This document contains device-specific information for the following devices:

- GPM6P1129A
- GPM6C1067A
- GPM6P1065A
- GPM6P1033A
- GPM6P1017A
- GPM6P1015A

The GPM6P1129A/C1067A/P1065A/P1033A/P1017A/P1015A are special chips for remote control with 256/512/192/192/512/256 bytes built-in SRAM. The GPM6P1129A/P1065A/P1033A/P1017A/P1015A have 128/64/32/16/16K bytes built-in OTP ROM. And GPM6C1067A has 64K bytes built-in Mask ROM. They include three Timers and up to 20/14/14/12/12/12 software selectable general I/Os and GPM6P1129A/C1067A/P1065A/P1033A have 6 Schmitt trigger pure input I/Os. Additionally, they provide one frequency programmable and duty selectable Pulse Width Modulation (PWM) output for remote control. And they provide built-in capture mode timer for input signal frequency detecting by Infrared learning function. They operate over a wide voltage range of 2.4V - 3.6V. All of them have a clock SLEEP mode for power saving. The power saving mode maintains the RAM contents, but stops the oscillator and causes all other chip functions to be inoperative. The SLEEP mode can be released by using external wakeup sources.

In addition, they provide a FREEZE mode for power saving and key board locking when power-supply voltage is detected lower than V_{LVR}. In FREEZE mode, CPU and peripheral were stopped, and all I/Os maintain floating with input function disabled. The FREEZE mode can not be released by any wakeup or interrupt sources. It is released only when a battery is removed and reinstalled, which must be with enough power or external reset occurs. Especially, they have a very accuracy internal OSC, which can match the spec (4MHz±1.5%(typ) @ 2.4V~3.6V) and can be used for most applications. Meanwhile, the built-in IR transfer module can make IR control and usage easier. Using GPM6P1129A/ C1067A/P1065A/P1033A/P1017A/P1015A do not only share the latest technology, but also enjoy the full commitment and technical support from Generalplus.

2. FEATURES

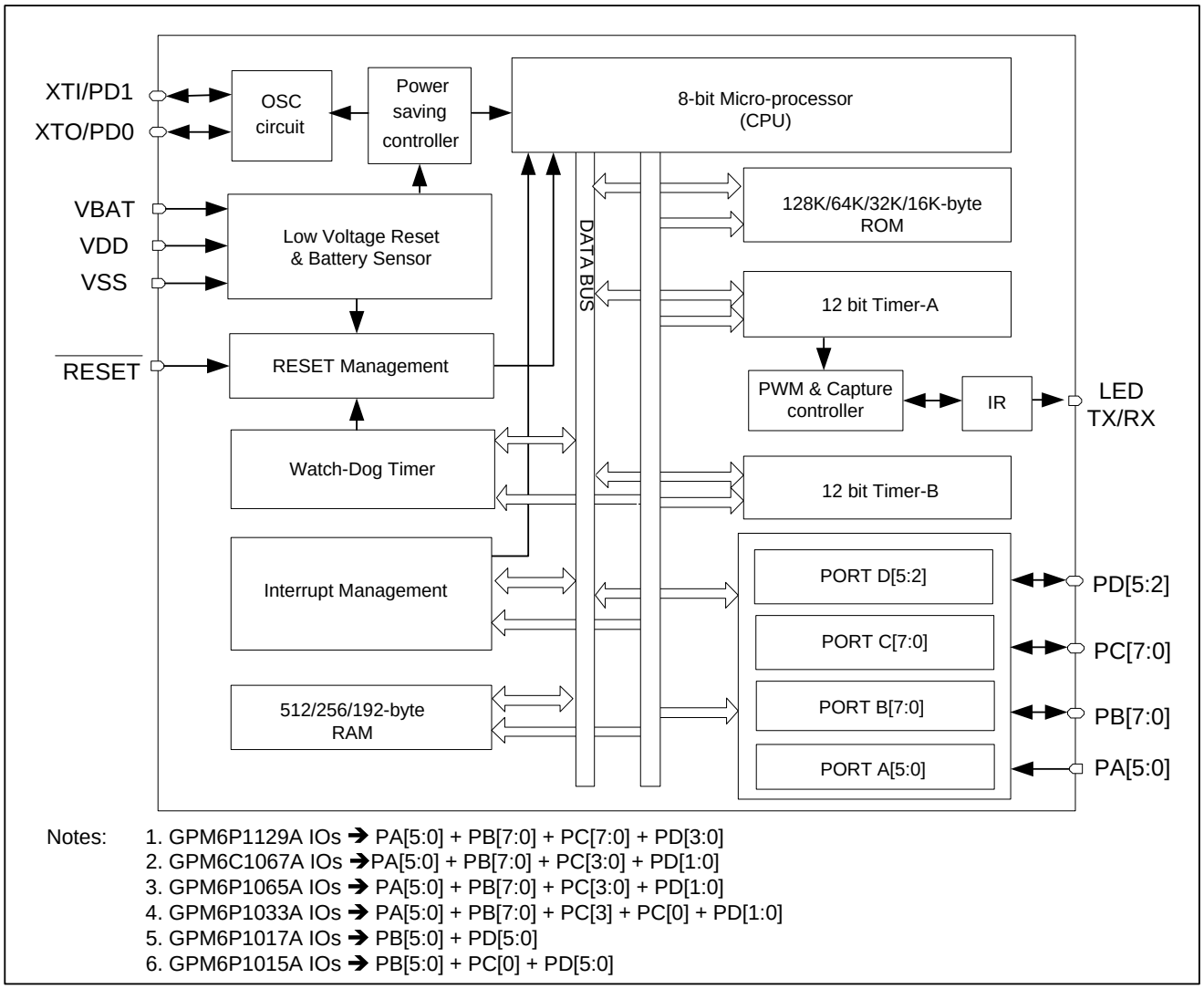
- **CPU**
  - 151 instructions
  - 13 addressing modes
  - Up to 8MHz clock operation
- **Memories**
  - GPM6P1129A
    - 128K bytes program memory (ROM)
    - 256 bytes RAM including stack area
  - GPM6C1067A
    - 64K bytes program memory (ROM)
    - 512 bytes RAM including stack area
  - GPM6P1065A
    - 64K bytes program memory (ROM)
    - 192 bytes RAM including stack area
  - GPM6P1033A
    - 32K bytes program memory (ROM)
    - 192 bytes RAM including stack area
  - GPM6P1017A
    - 16K bytes program memory (ROM)
    - 512 bytes RAM including stack area
  - GPM6P1015A
    - 16K bytes program memory (ROM)
    - 256 bytes RAM including stack area
- **Reset Management**
  - Enhanced reset system
  - Power On Reset (POR)
  - Low Voltage Reset (LVR)
  - Watchdog Reset (WDR)
  - External Reset (ERST)
- **Interrupt Management**
  - 8 internal interrupts
- **I/O Ports**
  - Max 20 (GPM6P1129A), max 14 (GPM6C1067A), max 14 (GPM6P1065A), max 12 (GPM6P1033A), max 12 (GPM6P1017A) and max 13 (GPM6P1015A) multifunction bi-directional I/Os
  - GPM6P1129A/C1067A/P1065A/P1033A have 6 Schmitt Trigger pure input I/Os
  - Each incorporate with pull-up resistor, pull-down resistor or floating input, depending on programmer's settings on the corresponding registers
  - Bi-directional I/O ports with LED driving capability
  - Bi-directional I/O ports with 16mA current sink

- **Clock Management**
  - Internal oscillator: 4MHz±1.5%(typ), @ 2.4V~3.6V
  - Crystal input: 4~ 8MHz @ 2.4V~3.6V
  - GPM6C1067A/P1017A/P1015A
    - Internal oscillator: 4MHz±1.5%(typ), @ 2.0V~3.6V; 8MHz±1.5%(typ), @ 2.4V~3.6V.
    - Crystal input: 4MHz @ 2.0V~3.6V; 8MHz @ 2.4V~3.6V.
- **Power Management**
  - 2 power saving modes: SLEEP, FREEZE mode
- **2 Analog Peripheral**
  - Battery Sensor for detecting the battery is connected or not
  - GPM6C1064A/1064A1 LVR: Low Voltage Reset (1.85V ± 0.15V)
  - GPM6C1032A/1024A LVR: Low Voltage Reset (1.85V ± 0.15V & 2.25V ± 0.15V selectable)
- **12-bit Timer (Timer A)**
  - Timer mode with clock source selectable
  - PWM output in carrier signal mode with duty and driver current programmable
  - GPM6P1129A/P1065A/P1033A current programmable
  - PWM output in no carrier signal mode with driver current programmable
  - Capture the input signal frequency
  - Detect the signal envelop
- **12-bit Timer (Timer B)**
  - Timer mode with clock source selectable
  - Timer A's carry signal can be its clock source
- **Watchdog Timer**
  - Frequency: 0.95Hz @8MHz(System Clock)
- **Key Wake up**
  - Key change wake-up from SLEEP mode
- **IR**
  - Built-in IR TX can drive IR LED with up to 200mA driving capability @ VBAT=3.0V & V_{LED}=3.0V
  - Built-in IR RX can provide capture function with sensitivity adjustable. (2uA, 5uA, 8uA, 11uA)

Table 2-1 GPM6P1129A/C1067A/P1065A/P1033A/P1017A/P1015A Configuration

Part NO.	ROM Type	Voltage (V)	Speed (HMz)	ROM (Byte)	RAM (Byte)	IR Tx/Rx	CCP			CPU OSC.		IO No.	PKG
							CAP	CNT	PWM	INT	XTAL		
GPM6P1129A	OTP	2.4~3.6	8/4	128K	256	Tx/Rx	1	1	1	•	•	26	LQFP44
GPM6C1067A	Mask	2.4~3.6	8	64K	512	Tx/Rx	1	1	1	•	•	20	SOP28
		2.0~3.6	4										
GPM6P1065A	OTP	2.4~3.6	8/4	64K	192	Tx/Rx	1	1	1	•	•	20	SOP28
GPM6P1033A	OTP	2.4~3.6	8/4	32K	192	Tx/Rx	1	1	1	•	•	18	SOP24
GPM6P1017A	OTP	2.4~3.6	8	16K	512	Tx/Rx	1	1	1	•	•	12	SOP16
		2.0~3.6	4										
GPM6P1015A	OTP	2.4~3.6	8	16K	256	Tx/Rx	1	1	1	•	•	13	SOP16
		2.0~3.6	4										

3. BLOCK DIAGRAM



Notes:
1. GPM6P1129A IOs ➔ PA[5:0] + PB[7:0] + PC[7:0] + PD[3:0]
2. GPM6C1067A IOs ➔PA[5:0] + PB[7:0] + PC[3:0] + PD[1:0]
3. GPM6P1065A IOs ➔ PA[5:0] + PB[7:0] + PC[3:0] + PD[1:0]
4. GPM6P1033A IOs ➔ PA[5:0] + PB[7:0] + PC[3] + PC[0] + PD[1:0]
5. GPM6P1017A IOs ➔ PB[5:0] + PD[5:0]
6. GPM6P1015A IOs ➔ PB[5:0] + PC[0] + PD[5:0]

Figure 3-1 The block diagram of GPM6P1129A/C1067A/P1065A/P1033A/P1017A/P1015A

4. SIGNAL DESCRIPTIONS

4.1. Pin Description

Type: I = Input, O = Output, S = Supply

Pin Name	GPM6P1129A LQFP44	GPM6C1067A/ GPM6P1065A SOP28	GPM6P1033A SOP24	GPM6P1017A SOP16	GPM6P1015A SOP16	Type	Main Function	Alternate Function
XTI / PD1	28	15	13	6	6	I/O	**Crystal Input**: It will be connected with external crystal for a crystal oscillation circuitry in crystal mode. **PortD[1]**: Bi-directional programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor or floating input, open-drain PMOS output, or CMOS output. The sink current (I_{OL}) of this I/O can reach 16mA (VDD = 3.0V, V_{OL} = 0.2*VDD) enough for driving LED. For **GPM6P1017A/P1015A PortD[1]** can be Key scan wakeup source, if key change is detected, chip wakeup from sleep mode.	
XTO /PD0	29	16	14	5	5	I/O	**Crystal Output**: It will be connected with external crystal for a crystal oscillation circuitry in crystal mode. **PortD[0]**: Bi-directional programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor or floating input, open-drain PMOS output, or CMOS output. The sink current (I_{OL}) of this I/O can reach 16mA (VDD = 3.0V, V_{OL} = 0.2*VDD) enough for driving LED. For **GPM6P1017A/P1015A PortD[0]** can be Key scan wakeup source, if key change is detected, chip wakeup from sleep mode.	
VPP /PD5	---	---	---	10	10	S/I/O	**VPP Power Supply**: **GPM6P1017A/ P1015A** OTP Program power supply. **PortD[5]**: Bi-directional programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor or floating input, open-drain NMOS output. The sink current (I_{OL}) of this I/O can reach 16 mA (VDD = 3.0V, V_{OL} = 0.2*VDD) enough to drive LED. For **GPM6P1017A/P1015A PortD[5]** can be Key scan wakeup source, if key change is detected, chip wakeup from sleep mode.	

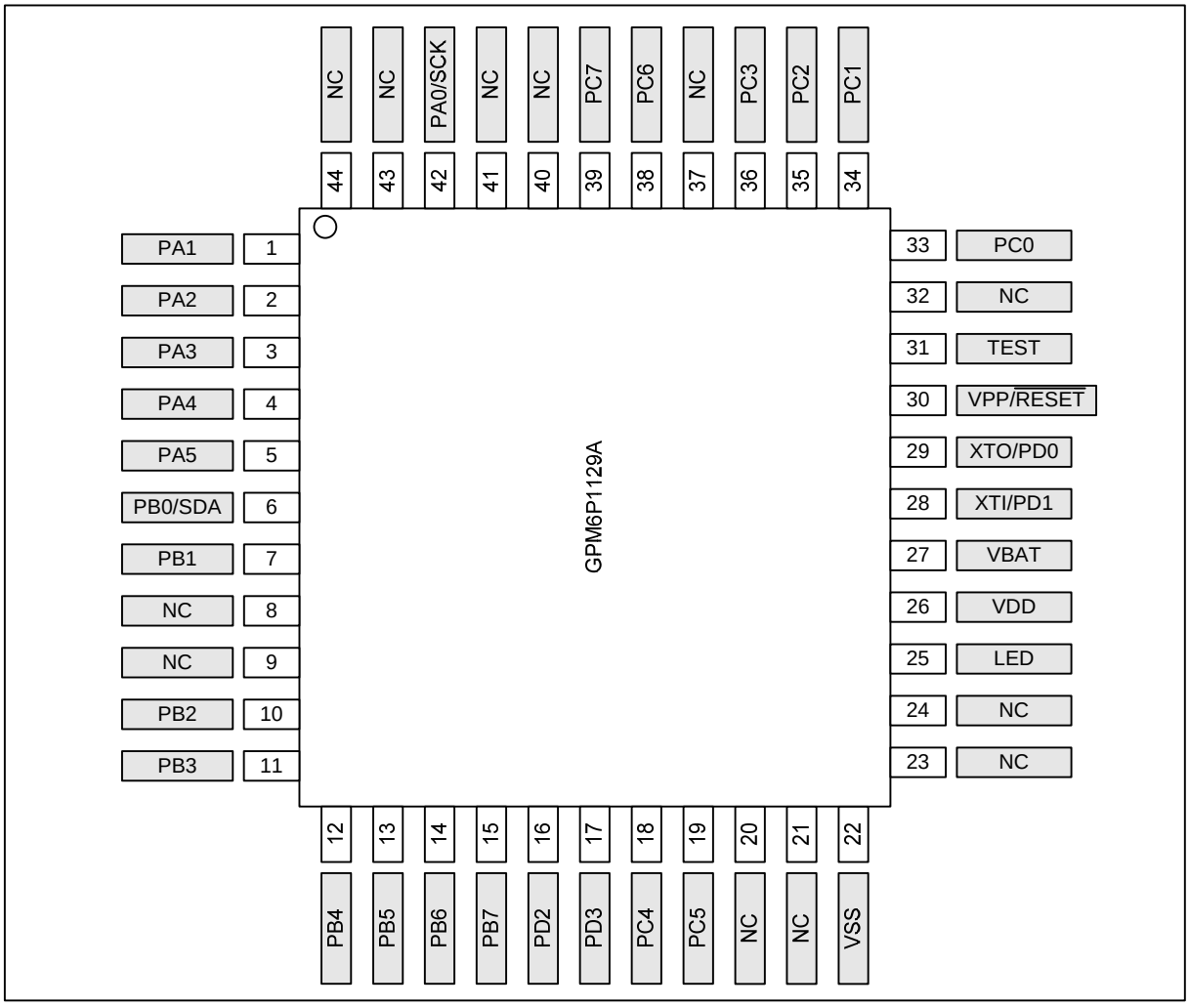
Pin Name	GPM6P1129A LQFP44	GPM6C1067A/ GPM6P1065A SOP28	GPM6P1033A SOP24	GPM6P1017A SOP16	GPM6P1015A SOP16	Type	Main Function	Alternate Function
PD4/SDA	---	---	---	9	9	I/O	**SDA: GPM6P1017A/ P1015A** OTP Program data input/output pin. **PortD[4]**: Bi-directional programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor or floating input, open-drain NMOS output. The sink current (I_{OL}) of this I/O can reach 16 mA (VDD = 3.0V, V_{OL} = 0.2*VDD) enough to drive LED. For **GPM6P1017A/P1015A PortD[4]** can be Key scan wakeup source, if key change is detected, chip wakeup from sleep mode.	
PD3/SCK	17	---	---	8	8	I/O	**SCK: GPM6P1017A/ P1015A** OTP Program clock input pin. **PortD[3]**: Bi-directional programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor or floating input, open-drain NMOS output. The sink current (I_{OL}) of this I/O can reach 16 mA (VDD = 3.0V, V_{OL} = 0.2*VDD) enough to drive LED. For **GPM6P1017A/P1015A PortD[3]** can be Key scan wakeup source, if key change is detected, chip wakeup from sleep mode.	
PD2	16	---	---	7	7	I/O	**PortD[2]**: Bi-directional programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor or floating input, open-drain PMOS output, or CMOS output. The sink current (I_{OL}) of this I/O can reach 16mA (VDD = 3.0V, V_{OL} = 0.2*VDD) enough for driving LED. For **GPM6P1017A/P1015A PortD[2]** can be Key scan wakeup source, if key change is detected, chip wakeup from sleep mode.	
PA5	5	28	24	---	---	I	**PortA[5:1]**: Schmitt Trigger pure input. It can be configured as pull-up resistor, pull-down resistor or floating input. This port is special for key input in IR controller application. (Key Change Wake-up).	
PA4	4	27	23	---	---	I		
PA3	3	26	22	---	---	I		
PA2	2	25	21	---	---	I		
PA1	1	24	20	---	---	I		

Pin Name	GPM6P1129A LQFP44	GPM6C1067A/ GPM6P1065A SOP28	GPM6P1033A SOP24	GPM6P1017A SOP16	GPM6P1015A SOP16	Type	Main Function	Alternate Function
PA0/SCK	42	23	19	---	---	I	**SCK: GPM6P11129A/P1065A/P1033A** OTP Program clock input pin. **PortA[0]**: Schmitt Trigger pure input. It can be configured as pull-up resistor, pull-down resistor or floating input. This port is special for key input in IR controller application. (Key Change Wake-up).	
PB7	15	8	8	---	---	I/O	**PortB[7:1]**: Bi-directional programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor or floating input, open-drain PMOS output, or CMOS output. The sink current (I_{OL}) of this I/O can reach 16mA (VDD = 3.0V, V_{OL} = 0.2*VDD) enough for driving LED. For **GPM6P1017A/P1015A PortB[5:1]** is special for key input in IR controller application. (Key Change Wake-up). And this port can be Key scan wakeup source, if key change is detected, chip wakeup from sleep mode.	
PB6	14	7	7	---	---	I/O		
PB5	13	6	6	4	4	I/O		
PB4	12	5	5	3	3	I/O		
PB3	11	4	4	2	2	I/O		
PB2	10	3	3	1	1	I/O		
PB1	7	2	2	16	16	I/O		
PB0/SDA	6	1	1	15	15	I/O	**SDA:GPM6P11129A/P1065A/P1033A** OTP Program data input/output pin. **PortB[0]**:Bi-directional programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor or floating input, open-drain PMOS output, or CMOS output. The sink current (I_{OL}) of this I/O can reach 16mA (VDD = 3.0V, V_{OL} = 0.2*VDD) enough for driving LED. For **GPM6P1017A/P1015A PortB[0]** is special for key input in IR controller application. (Key Change Wake-up). And This port can be Key scan wakeup source, if key change is detected, chip wakeup from sleep mode.	
PC7	39	---	---	---	---	I/O	**PortC[7:0]**: Bi-directional programmable Input/Output port. It can be configured as pull-up resistor, pull-down resistor or floating input, open-drain PMOS output, or CMOS output. The sink current (I_{OL}) of this I/O can reach 16mA (VDD = 3.0V, V_{OL} = 0.2*VDD) enough for driving LED.	
PC6	38	---	---	---	---	I/O		
PC5	19	---	---	---	---	I/O		
PC4	18	---	---	---	---	I/O		
PC3	36	22	18	---	---	I/O		
PC2	35	21	---	---	---	I/O		
PC1	34	20	---	---	---	I/O		

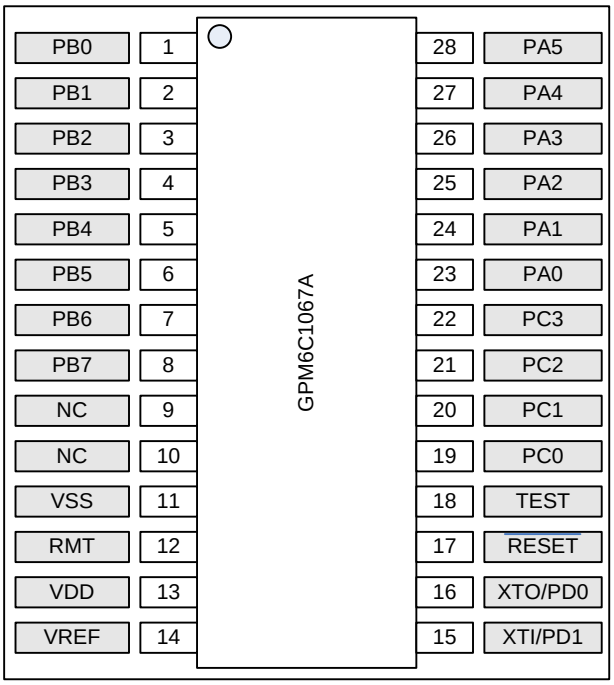
Pin Name	GPM6P1129A LQFP44	GPM6C1067A/ GPM6P1065A SOP28	GPM6P1033A SOP24	GPM6P1017A SOP16	GPM6P1015A SOP16	Type	Main Function	Alternate Function
PC0	33	19	17	---	14	I/O	For **GPM6P1015A PortC[0]** can be Key scan wakeup source, if key change is detected, chip wakeup from sleep mode.	
LED	25	12	10	11	11	O	IR controller signal transmit or receive pin.	
VBAT	27	14	12	12	12	S	Battery supply	
VDD	26	13	11	14	---	S	Power supply	
VSS	22	11	9	13	13	S	Ground	
VPP/ $\overline{\text{RESET}}$	30	17	15	---	---	I	**VPP Power Supply**: **GPM6P1129A/ P1065A/P1033A** OTP Program power supply. **RESET:** This pin is an active low reset for the chip.	
TEST	31	18	16	---	---	I	Test pin, high active.	

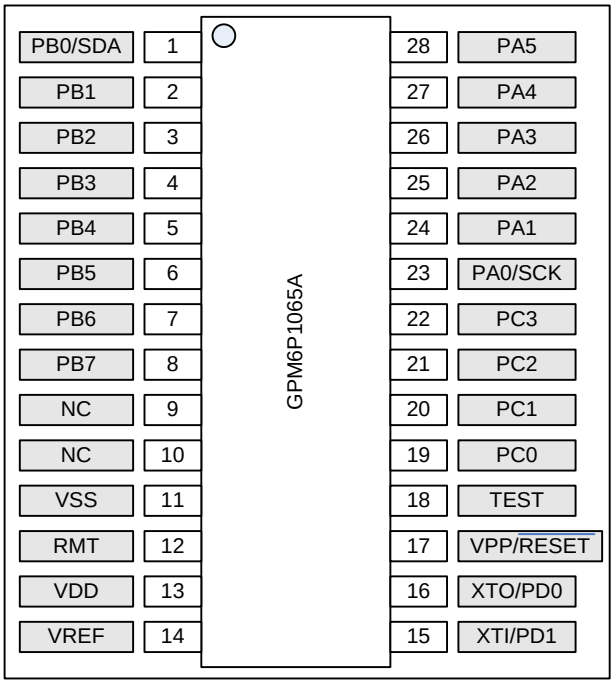
4.2. PIN Assignment (Top View)

4.2.1. LQFP44 Package

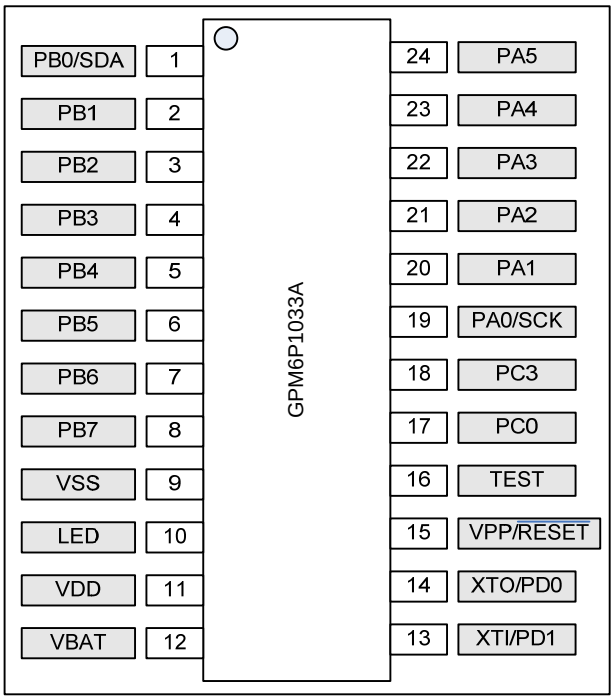


4.2.2. SOP28 Package

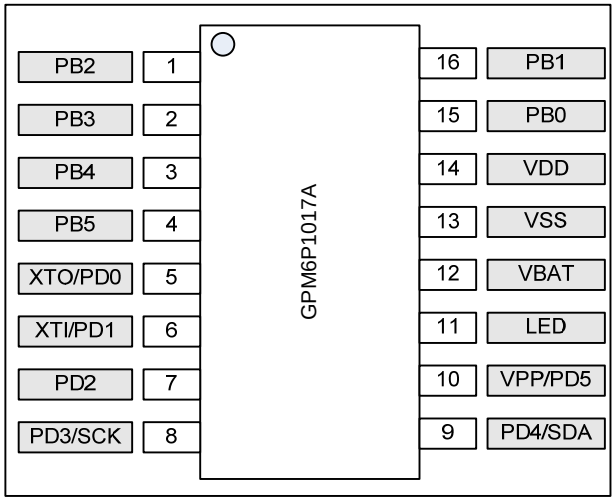


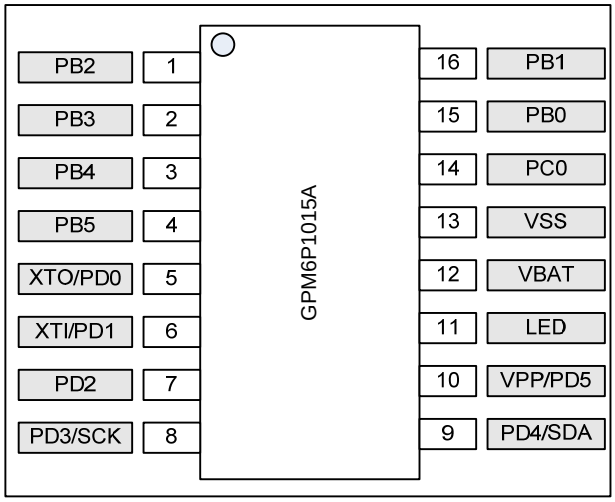


4.2.3. SOP24 Package



4.2.4. SOP16 Package





5. FUNCTIONAL DESCRIPTIONS

5.1. Central Processing Unit

5.1.1. CPU Introduction

The microprocessors of GPM6P1129A/C1067A/P1065A/P1033A/ P1017A/P1015A are high performance processors equipped with 6 internal registers: accumulator, program counter, X register, Y register, stack pointer, and processor status register. This CPU is a fully static CMOS design. The oscillation frequency could be varied up to 8.0MHz depending on the application.

5.1.2. CPU Register

The CPU has six registers that are the Program Counter (PC), an Accumulator (A), two Index Registers (X, Y), the Stack Pointer (SP), and the Status register (P). The program counter consists of 16-bit register.

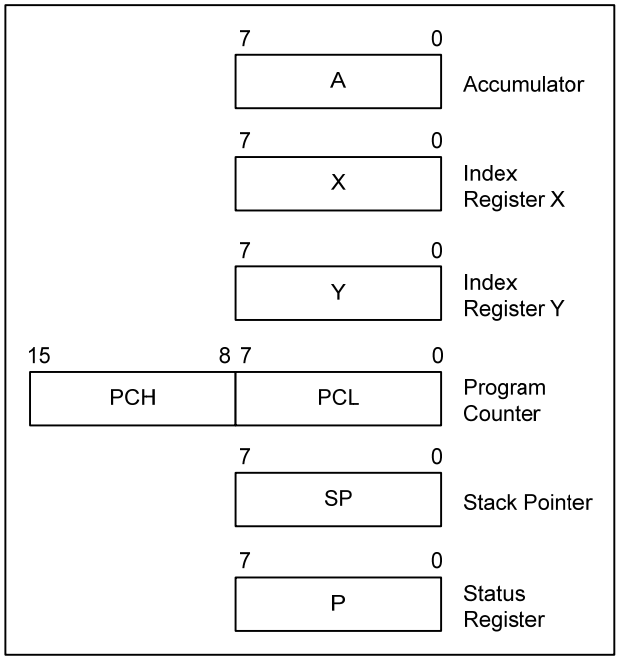


Figure 5-1 System registers

X, Y Register

In address mode, X and Y registers can be used as index registers or buffer registers. These register contents are added to the specified address, which becomes the actual address. Some operations such as increment, decrement, comparison and data transfer function can be used in X and Y registers.

Accumulator

The Accumulation is the 8-bit general-purpose register, which can be operated with transfer, temporary saving, condition judgment, etc.

Stack Pointer

The CPU has an 8-bit-wide register indicating the location in the stack to be accessed (push or pop) when a subroutine call or interrupt occurs.

When subroutine call is executed or an interrupt occurrence is accepted, the value of stack point is updated automatically.

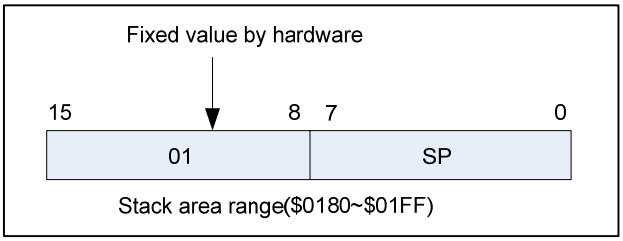


Figure 5-2 Stack point register

[Example] 5-1 Initialized stack point value

```
LDX   #C_STACK_BOTTOM    ; Initial stack pointer at $1FF
TXS                      ;Transfer to stack point
```

Program Counter (PC)

The program counter is a 16-bit wide register. It consists of two 8-bit registers which are PCH and PCL. This register indicates the address of next instruction to be executed. In Reset state, the content of program counter is stored with $FFFC.

Status Register (P)

The 8-bit status register contains the interrupt mask and 6 flags representative of the result of the instruction just executed. This register can also be handled by the PHP and PLP instructions. These bits can be individually controlled by specific instructions. The detailed description is shown in following description.

Note: Not all instructions affect status register. A detailed instruction description will be discussed in 6502 instruction manual.

❑ **Negative Flag Bit**

This flag indicated the bit7 status of the result of a data or arithmetic operation. Programmer can use this bit to do some operations, e.g. branch condition or bit operation.

❑ **Overflow Flag Bit**

This flag indicates whether the overflow has occurred in arithmetic operation. When the result of an addition or subtraction is over +127 or less than –128, this overflow bit is set to '1'.

❑ **Decimal Mode Flag**

This flag indicates what mode is operated by arithmetic operation. The CPU has two operation modes, binary mode and decimal mode for arithmetic operation. Programmer can use the instruction to alternate them.

❑ **Interrupt Disable Flag**

This bit can enable or disable all interrupts except NMI interrupt source. If this bit is set to '1', CPU will ignore interrupt signal. On the contrary, if this bit is set to '0', CPU will accept interrupt signal.

❑ **Zero Flag**

This flag indicated the result of a data or arithmetic operation. If the result is equal to zero, the zero flag is set to '1'. Contrary, this bit is set to '0' by other values.

❑ **Carry Flag**

This bit is set to '1 if the result of addition operation generates a carry, or if the result of subtraction doesn't generate a borrowing. In addition, some shift instructions or rotate instructions also change this bit.

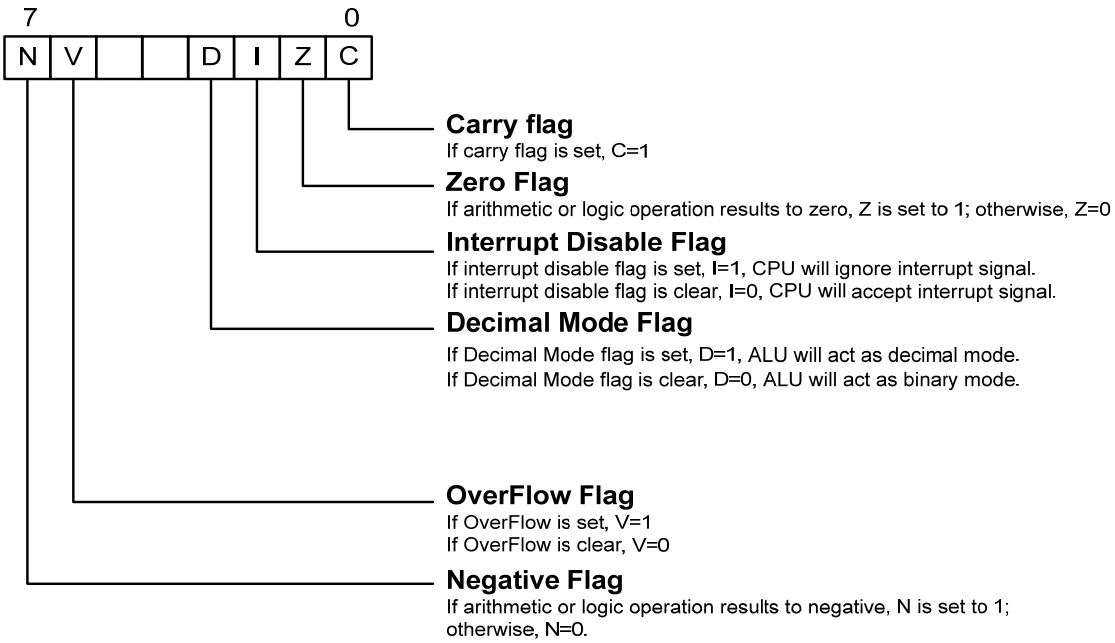


Figure 5-3 Status register

5.2. Memory Organization

5.2.1. Introduction

The GPM6P1129A/C1067A/P1065A/P1033A/P1017A/P1015A have separated address spaces for program memory and data memory. Program memory can be read only. GPM6P1129A contains up to 128K bytes of program memory. Data memory contains 256 bytes of RAM including stack area, which can be read and written. GPM6C1067A contains up to 64K bytes of program memory. Data memory contains 512 bytes of RAM including stack area, which can be read and written. GPM6P1065A contains up to 64K bytes of program memory. Data memory contains 192 bytes of RAM including stack area, which can be read and written. GPM6P1033A contains up to 32K bytes of program memory. Data memory contains 192 bytes of RAM including stack area, which can be read and written. GPM6P1017A contains up to 16K bytes of program memory. Data memory contains 512 bytes of RAM including stack area, which can be read and written. GPM6P1015A contains up to 16K bytes of program memory. Data memory contains 256 bytes of RAM including stack area, which can be read and written.

5.2.2. Memory Space

Memory address allocations on the GPM6P1129A/C1067A/ P1065A/P1033A/P1017A/P1015A are divided into several parts. The first 128 addresses are allocated for special function registers, including function control registers and I/O control registers, which allow programmer to use the first page instruction in setting this register and help for program size reduction.

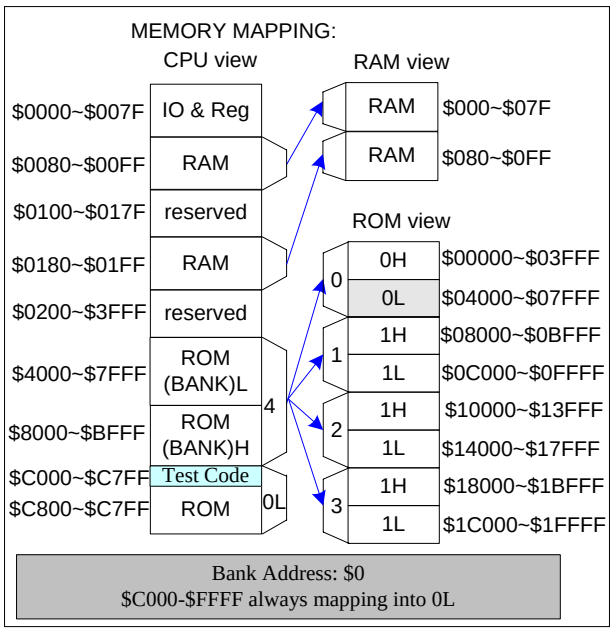


Figure 5-4 shows GPM6P1129A memory map.

GPM6P1129A's RAM consists of 256 bytes (including Stack). In CPU view, the RAM locations are from $080 ~ $FF and from $180 ~ $1FF. They are mapped to RAM $000~$07F and $080~$0FF respectively in RAM view.

GPM6P1129A supports 128K bytes of ROM. In CPU view, it has four banks, which are BANK0~3. Each bank includes high bank and low bank. The address for the four ROM bank is located on $4000 ~ $BFFF. And the ROM area, $C000~$FFFF, is always mapped to the LOW area $00000 ~ $1FFFF of BANK0.

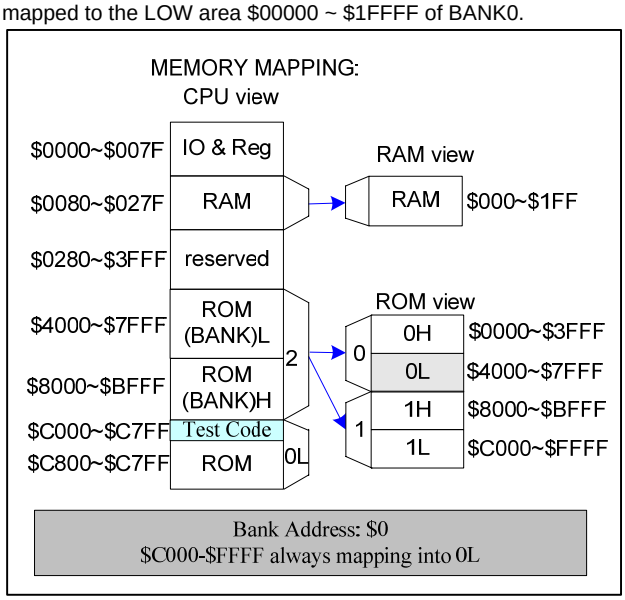


Figure 5-5 shows GPM6C1067A memory map.

GPM6C1067A's RAM consists of 512 bytes (including Stack). In CPU view, the RAM locations are from $080 ~ $27F. They are mapped to RAM $000~$1FF respectively in RAM view.

GPM6C1067A supports 64K bytes of ROM. In CPU view, it has two banks, which are BANK0~1. Each bank includes high bank and low bank. The address for the two ROM bank is located on $4000 ~ $BFFF. And the ROM area, $C000~$FFFF, is always mapped to the LOW area $00000 to $0FFFF of BANK0.

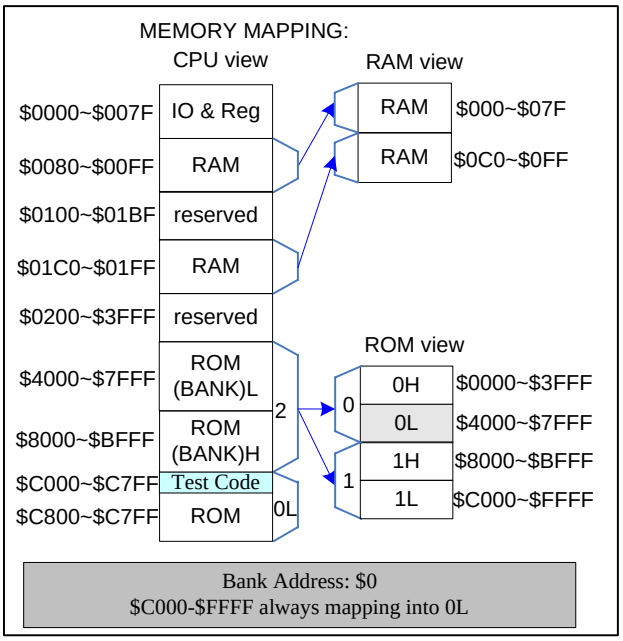


Figure 5-6 shows GPM6P1065A memory map

GPM6P1065A 's RAM consists of 192 bytes (including Stack). In CPU view, the RAM locations are from $080 through $FF and from $1C0 to $1FF. They are mapped to $000~$07F and $0C0~$0FF respectively in RAM view.

GPM6P1065A supports 64K bytes of ROM. In CPU view, it has two banks, which are BANK0~1. Each bank includes high bank and low bank. The address for the two ROM bank is located on $4000 ~ $BFFF. And the ROM area, $C000~$FFFF, is always mapped to the LOW area $00000 to $0FFFF of BANK0.

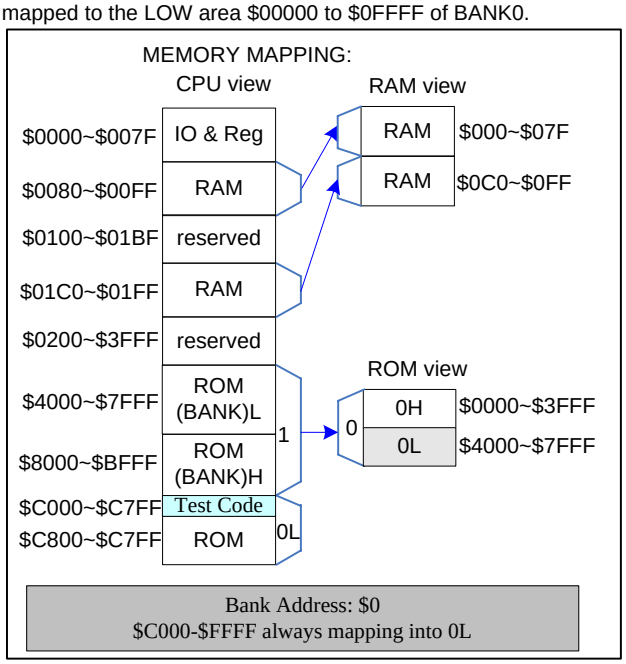


Figure 5-7 shows GPM6P1033A memory map.

GPM6P1033A's RAM consists of 192 bytes (including Stack). In CPU view, the RAM locations are from $080 through $FF and from $1C0 to $1FF. They are mapped to $000~$07F and $0C0~$0FF respectively in RAM view.

GPM6P1033A supports 32K bytes of ROM. In CPU view, it has only one bank, which is BANK0. The bank includes high bank and low bank. The address for the ROM bank is located on $4000 ~ $BFFF. And the ROM area, $C000~$FFFF, is always mapped to the LOW area $00000 ~ $07FFF of BANK0.

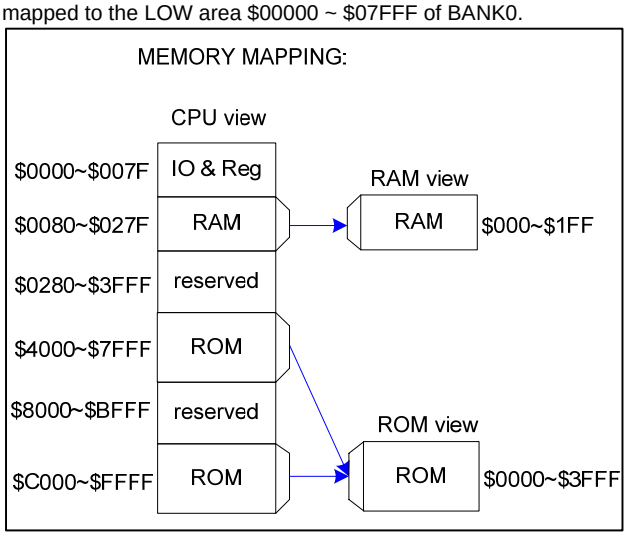


Figure 5-8 shows GPM6P1017A memory map

GPM6P1017A's RAM consists of 512 bytes (including Stack). In CPU view, the RAM locations are from $080 through $27F. It is mapped to RAM $000~1FF respectively in RAM view.

GPM6P1017A supports 16K bytes of ROM. In CPU view, the address for the ROM is located on $4000 ~ $7FFF. And the ROM area, $C000~$FFFF, is double mapped to the area $00000 ~ $03FFF.

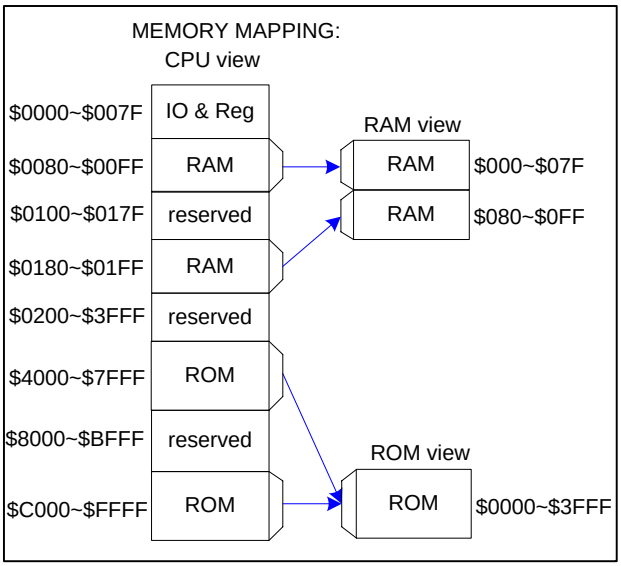


Figure 5-9 shows GPM6P1015A memory map.

GPM6P1015A 's RAM consists of 256 bytes (including Stack). In CPU view, the RAM locations are from $080 through $FF and from $180 to $1FF. They are mapped to $000~$07F and $080~$0FF respectively in RAM view.

GPM6P1015A supports 16K bytes of ROM. In CPU view, the address for the ROM is located on $4000 ~ $7FFF. And the ROM area, $C000~$FFFF, is always double mapped to the area $00000 to $03FFF.

The address of NMI, $\overline{\text{RESET}}$ and IRQ exception vectors are located from $FFFA to $FFFF. The exception vectors should be specified in the program to have proper operation.

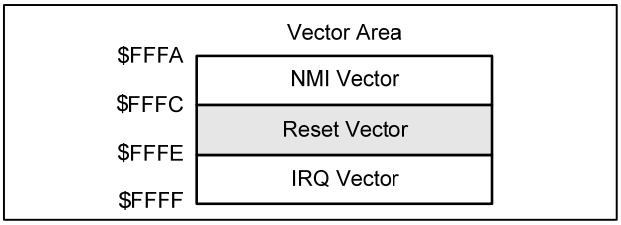


Figure 5-10 Interrupt vector area

[Example] 5-2 Interrupt vector table in software

```
VECTOR:     .SECTION
            DW      V_NMI
            DW      V_Reset
            DW      V_IRQ
```

5.2.3. Configuration Option Register

The configuration option register is used to setup the operation condition. And its CPU view address is $FFF8. It is mapped to the special reserved ROM address $7FF8.

The GPM6P1129A/C1067A/P1065A/P1033A/P1017A/P1015A have the following configuration options.

- Crystal resonator or internal oscillator clock source option.
- LVR enable or disable option.
- Watch dog enable or disable option.

Device Configuration Register (OPCODE0, $FFF8)

BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	**OPTCHK3**	**OPTCHK2**	**OPTCHK1**	**OPTCHK0**	**Reserved**	**WDTENB**	**LVRENB**	**SYSCLKS**
Access	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Default	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Bit [7:4] **OPTCHK [3:1]:** Configuration Option Check bits must be filled in 101.
OPTCHK0: disable/enable security protection. Can or not read data from OTPROM
1: Security disable
0: Security enable

Bit [3] Reserved

Bit [2] **WDTENB:** disable/enable watchdog
0= WDT is enabled
1= WDT is disabled

Bit [1] **LVRENB:** disable/enable LVR
0= LVR is enabled
1= LVR is disabled

Bit [0] **SYSCLKS:** IOSC (internal) / Crystal selection
0= IOSC
1= Crystal

The GPM6C1067A has the following additional configuration options.

- It supports LVR trigger level select option.
- It supports IOSC frequency select option.

Device Configuration Register for GPM6C1067A(OPCODE1, $FFF9)

BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	-	-	-	-	-	-	LVRHTS	IOSCPS
Access	-	-	-	-	-	-	R	R
Default	-	-	-	-	-	-	1	1

Bit [7:2] Reserved

Bit [1] **LVRHTS:** LVR trigger level selection

0= 1.8V
1= 2.2V

Bit [0] **SYSCLKS:** IOSC (internal) frequency selection

0= 4MHz

1= 8MHz

Users can refer to the Device Configuration Register and set it in [Project/ Setting/ Mask Option] of Fortis IDE as Figure 5-11.

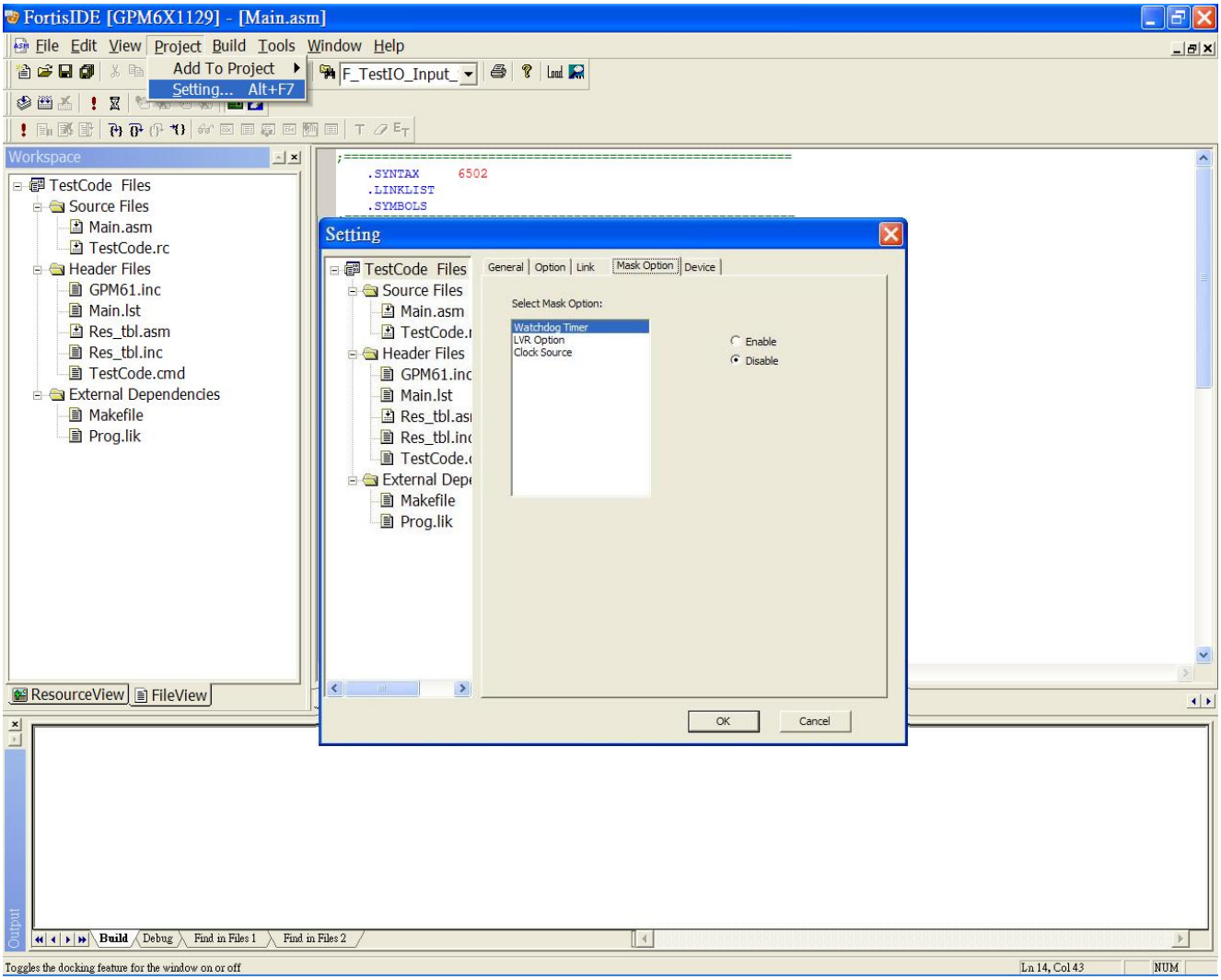


Figure 5-11 Device Configuration Register set in Fortis IDE

5.2.4. Special Function Registers

GPM6P1129A/C1067A/P1065A/P1033A/P1017A/P1015A devices have many control registers. All of the control registers are used by MCU and peripheral function block for controlling the desired operation of the device. Some of the control registers contain control and statue bits for peripheral module such as Timer unit, interrupt control unit, etc. Note that the reserved addresses are not implemented on the chip. Some of bits in control register are read only. When writing to them, there are no any effects on the corresponding bits. The following table shows the summary of the control registers. The detailed information of each control registers are explained in each peripheral section.

GPM6P1129A Special Function Registers Description

$0000~$000A: I/O port

Address	Register	Reset Value	R/W	Bit7	Bit6$	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$00	P_IOB_DIR	00h	R/W	Port B Direction control							
$01	P_IOC_DIR	00h	R/W	Port C Direction control							
$02	P_IOD_DIR	00h	R/W	-	-	-	-	Port D Direction control			
$03	P_IOA_PULL	00h	R/W	-	-	Port A input control					
$04	P_IOB_ATT	00h	R/W	Port B attribute register							
$05	P_IOC_ ATT	00h	R/W	Port C attribute register							
$06	P_IOD_ ATT	00h	R/W	-	-	-	-	Port D attribute register			
$07	P_IOA_DAT	00h	R/W	R/0	R/0	Write data into the Port A data register and read data from the I/O pad.					
$08	P_IOB_DAT	00h	R/W	Write data into the Port B data register and read data from the I/O pad.							
$09	P_IOC_DAT	00h	R/W	Write data into the Port C data register and read data from the I/O pad.							
$0A	P_IOD_DAT	00h	R/W	R/0	R/0	R/0	R/0	Write data into the Port D data register and read data from the I/O pad.			

$0010~$0016: INT Flag & other special register

Address	Register	Reset Value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$10	P_BANK_CTRL	00h	R/W	-	-	-	-	-	-	BANK1	BANK0
$11	P_PWM_DRV	00h	W	-	-	-	PWMDRV1	PWMDRV0	-	-	-
	P_RX_SEN	00h	W	-	-	-	-	-	TMACAPS	SENSE1	SENSE0
$12	P_SYS_SLEEP	00h	W	C_SYS_SLEEP= AAH (Write other data system to reset.)							
$13	P_INT_CTRL	00h	R/W	TMADTE	TMAOIE	CAPIE	TMBOIE	F1KIE	F4KIE	F32KIE	F2MIE
$14	P_INT_FLAG	00h	R/W	TMADTF	TMAOIF	CAPIF	TMBOIF	F1KIF	F4KIF	F32KIF	F2MIF
$16	P_INT_FLAGC	00h	R/W	ENVDET	-	-	-	-	-	-	-

$0020~0026: Timer control

Address	Register	Reset Value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$20	P_WDT_CTRL	00h	W	C_WDT_CLR= AAH (Write other data system to reset.)							
$21	P_TMA_CTRL	00h	R/W	TMAES	CAPEG	TMACLK1	TMACLK0	TMADUT1	TMADUT0	TMAMOD1	TMAMOD0
$22	P_TMB_CTRL	00h	R/W	TMBES	-	TMBCLK1	TMBCLK0	-	-	-	-
$23	P_TMA_CNTL	00h	R/W	TMA Counter Low Byte 8-bit Pre-value.							
	P_TMA_PWML			TMA PWM Low Byte 8-bit Period Value.							
	P_TMA_CAPL			TMA CAPTURE Low Byte 8-bit Width value.							
$24	P_TMA_CNTH	00h	R/W	-	-	-	-	TMA Counter High Byte 4-bit Pre-value.			
	P_TMA_PWMH			-	-	-	-	TMA PWM High Byte 4-bit Period Value.			
	P_TMA_CAPH			-	-	-	-	TMA CAPTURE High Byte 4-bit Width value.			
$25	P_TMB_CNTL	00h	R	TMB Counter Low Byte 8-bit Pre-value.							
	P_TMB_REGL		W	TMB Low Byte 8-bit Register							
$26	P_TMB_CNTH	00h	R	-	-	-	-	TMB Counter High Byte 4-bit Pre-value.			
	P_TMB_REGH		W	-	-	-	-	TMB High Byte 4-bit Register			

GPM6C1067A/GPM6P1065A Special Function Registers Description

$0000~$000A: I/O port

Address	Register	Reset Value	R/W	Bit7	Bit6$	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$00	P_IOB_DIR	00h	R/W	Port B Direction control							
$01	P_IOC_DIR	00h	R/W	-	-	-	-	Port C Direction control			
$02	P_IOD_DIR	00h	R/W	-	-	-	-	-	-	Port D Direction control	
$03	P_IOA_PULL	00h	R/W	-	-	Port A input control					
$04	P_IOB_ATT	00h	R/W	Port B attribute register							
$05	P_IOC_ ATT	00h	R/W	-	-	-	-	Port C attribute register			
$06	P_IOD_ ATT	00h	R/W	-	-	-	-	-	-	Port D attribute register	
$07	P_IOA_DAT	00h	R/W	R/0	R/0	Write data into the Port A data register and read data from the I/O pad.					
$08	P_IOB_DAT	00h	R/W	Write data into the Port B data register and read data from the I/O pad.							
$09	P_IOC_DAT	00h	R/W	R/0	R/0	R/0	R/0	Write data into the Port C data register and read data from the I/O pad.			
$0A	P_IOD_DAT	00h	R/W	R/0	R/0	R/0	R/0	R/0	R/0	Write data into the Port D data register and read data from the I/O pad.	

$0010~$0016: INT Flag & other special register

Address	Register	Reset Value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$10	P_BANK_CTRL	00h	R/W	-	-	-	-	-	-	-	BANK0
$11	P_PWM_DRV	00h	W	-	-	-	PWMDRV1	PWMDRV0	-	-	-
	P_RX_SEN	00h	W	-	-	-	-	-	TMACAPS	SENSE1	SENSE0
$12	P_SYS_SLEEP	00h	W	C_SYS_SLEEP= AAH (Write other data system to reset.)							
$13	P_INT_CTRL	00h	R/W	TMADTE	TMAOIE	CAPIE	TMBOIE	F1KIE	F4KIE	F32KIE	F2MIE
$14	P_INT_FLAG	00h	R/W	TMADTF	TMAOIF	CAPIF	TMBOIF	F1KIF	F4KIF	F32KIF	F2MIF
$16	P_INT_FLAGC	00h	R/W	ENVDET	-	-	-	-	-	-	-

$0020~0026: Timer control

Address	Register	Reset Value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$20	P_WDT_CTRL	00h	W	C_WDT_CLR= AAH (Write other data system to reset.)							
$21	P_TMA_CTRL	00h	R/W	TMAES	CAPEG	TMACLK1	TMACLK0	TMADUT1	TMADUT0	TMAMOD1	TMAMOD0
$22	P_TMB_CTRL	00h	R/W	TMBES	-	TMBCLK1	TMBCLK0	-	-	-	-
$23	P_TMA_CNTL	00h	R/W	TMA Counter Low Byte 8-bit Pre-value.							
	P_TMA_PWML			TMA PWM Low Byte 8-bit Period Value.							
	P_TMA_CAPL			TMA CAPTURE Low Byte 8-bit Width value.							
$24	P_TMA_CNTH	00h	R/W	-	-	-	-	TMA Counter High Byte 4-bit Pre-value.			
	P_TMA_PWMH			-	-	-	-	TMA PWM High Byte 4-bit Period Value.			
	P_TMA_CAPH			-	-	-	-	TMA CAPTURE High Byte 4-bit Width value.			
$25	P_TMB_CNTL	00h	R	TMB Counter Low Byte 8-bit Pre-value.							
	P_TMB_REGL		W	TMB Low Byte 8-bit Register							
$26	P_TMB_CNTH	00h	R	-	-	-	-	TMB Counter High Byte 4-bit Pre-value.			
	P_TMB_REGH		W	-	-	-	-	TMB High Byte 4-bit Register			

GPM6P1033A Special Function Registers Description

$0000~$000A: I/O port

Address	Register	Reset Value	R/W	Bit7	Bit6$	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$00	P_IOB_DIR	00h	R/W	Port B Direction control							
$01	P_IOC_DIR	00h	R/W	-	-	-	-	Port C Direction control	-	-	Port C Direction control
$02	P_IOD_DIR	00h	R/W	-	-	-	-	-	-	Port D Direction control	
$03	P_IOA_PULL	00h	R/W	-	-	Port A input control					
$04	P_IOB_ATT	00h	R/W	Port B attribute register							
$05	P_IOC_ ATT	00h	R/W	-	-	-	-	Port C attribute register	-	-	Port C attribute register
$06	P_IOD_ ATT	00h	R/W	-	-	-	-	-	-	Port D attribute register	
$07	P_IOA_DAT	00h	R/W	R/0	R/0	Write data into the Port A data register and read data from the I/O pad.					
$08	P_IOB_DAT	00h	R/W	Write data into the Port B data register and read data from the I/O pad.							
$09	P_IOC_DAT	00h	R/W	R/0	R/0	R/0	R/0	Write data into the PortC data register and read data from the I/O pad.	R/0	R/0	Write data into the PortC data register and read data from the I/O pad.
$0A	P_IOD_DAT	00h	R/W	R/0	R/0	R/0	R/0	R/0	R/0	Write data into the Port D data register and read data from the I/O pad.	

$0010~$0016：INT Flag & other special register

Address	Register	Reset Value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$11	P_PWM_DRV	00h	W	-	-	-	PWMDRV1	PWMDRV0	-	-	-
	P_RX_SEN	00h	W	-	-	-	-	-	TMACAPS	SENSE1	SENSE0
$12	P_SYS_SLEEP	00h	W	C_SYS_SLEEP= AAH (Write other data system to reset.)							
$13	P_INT_CTRL	00h	R/W	TMADTE	TMAOIE	CAPIE	TMBOIE	F1KIE	F4KIE	F32KIE	F2MIE
$14	P_INT_FLAG	00h	R/W	TMADTF	TMAOIF	CAPIF	TMBOIF	F1KIF	F4KIF	F32KIF	F2MIF
$16	P_INT_FLAGC	00h	R/W	ENVDET	-	-	-	-	-	-	-

$0020~0026: Timer control

Address	Register	Reset Value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$20	P_WDT_CTRL	00h	W	C_WDT_CLR= AAH (Write other data system to reset.)							
$21	P_TMA_CTRL	00h	R/W	TMAES	CAPEG	TMACLK1	TMACLK0	TMADUT1	TMADUT0	TMAMOD1	TMAMOD0
$22	P_TMB_CTRL	00h	R/W	TMBES	-	TMBCLK1	TMBCLK0	-	-	-	-
$23	P_TMA_CNTL	00h	R/W	TMA Counter Low Byte 8-bit Pre-value.							
	P_TMA_PWML			TMA PWM Low Byte 8-bit Period Value.							
	P_TMA_CAPL			TMA CAPTURE Low Byte 8-bit Width value.							
$24	P_TMA_CNTH	00h	R/W	-	-	-	-	TMA Counter High Byte 4-bit Pre-value.			
	P_TMA_PWMH			-	-	-	-	TMA PWM High Byte 4-bit Period Value.			
	P_TMA_CAPH							TMA CAPTURE High Byte 4-bit Width value.			
$25	P_TMB_CNTL	00h	R	TMB Counter Low Byte 8-bit Pre-value.							

	P_TMB_REGL		W	TMB Low Byte 8-bit Register				
$26	P_TMB_CNTH	00h	R	-	-	-	-	TMB Counter High Byte 4-bit Pre-value.
	P_TMB_REGH		W	-	-	-	-	TMB High Byte 4-bit Register

GPM6P1017A Special Function Registers Description

$0000~$000A: I/O port

Address	Register	Reset Value	R/W	Bit7	Bit6$	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$00	P_IOB_DIR	00h	R/W	R/0	R/0	Port B Direction control					
$02	P_IOD_DIR	00h	R/W	R/0	R/0	Port D Direction control					
$04	P_IOB_ATT	00h	R/W	R/0	R/0	Port B attribute register					
$06	P_IOD_ ATT	00h	R/W	R/0	R/0	Port D attribute register					
$08	P_IOB_DAT	00h	R/W	R/0	R/0	Write data into the Port B data register and read data from the I/O pad.					
$0A	P_IOD_DAT	00h	R/W	R/0	R/0	Write data into the Port D data register and read data from the I/O pad.					

$0011~$001D: INT Flag & other special register

Address	Register	Reset Value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$11	P_PWM_DRV	00h	W	-	R/0	R/0	R/0	PWMDRV0	-	-	-
	P_RX_SEN	00h	W	-	R/0	R/0	R/0	-	TMACAPS	SENSE1	SENSE0
$12	P_SYS_SLEEP	00h	W	C_SYS_SLEEP= AAH (Write other data system to reset.)							
$13	P_INT_CTRL	00h	R/W	TMADTE	TMAOIE	CAPIE	TMBOIE	F1KIE	F4KIE	F32KIE	F2MIE
$14	P_INT_FLAG	00h	R/W	TMADTF	TMAOIF	CAPIF	TMBOIF	F1KIF	F4KIF	F32KIF	F2MIF
$16	P_INT_FLAGC	00h	R/W	ENVDET	R/0	R/0	R/0	R/0	R/0	R/0	R/0
$1B	P_SC_IOB	00h	R/W	R/0	R/0	PB5SE	PB4SE	PB3SE	PB2SE	PB1SE	PB0SE
$1D	P_SC_IOD	00h	R/W	R/0	R/0	PD5SE	PD4SE	PD3SE	PD2SE	PD1SE	PD0SE

$0020~0026: Timer control

Address	Register	Reset Value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$20	P_WDT_CTRL	00h	W	C_WDT_CLR= AAH (Write other data system to reset.)							
$21	P_TMA_CTRL	00h	R/W	TMAES	CAPEG	TMACLK1	TMACLK0	TMADUT1	TMADUT0	TMAMOD1	TMAMOD0
$22	P_TMB_CTRL	00h	R/W	TMBES	R/0	TMBCLK1	TMBCLK0	R/0	R/0	R/0	R/0
$23	P_TMA_CNTL	xxh	R	Timer A Counter Low Byte 8-bit Pre-value for COUNTER mode.							
	P_TMA_PWML		W	Timer A PWM carrier signal Low Byte 8-bit Period Value for PWM mode.							
	P_TMA_CAPL		R	Timer A received carrier signal Low Byte 8-bit Period Width value for CAPTURE mode.							
	P_TMA_ENVL		W	Timer A received carrier signal Low Byte 8-bit Period Width pre-value for ENVELOPE mode.							
$24	P_TMA_CNTH	xxh	R	R/0	R/0	R/0	R/0	Timer A Counter High Byte 4-bit Pre-value for COUNTER mode.			
	P_TMA_PWMH		W	-	-	-	-	Timer A PWM carrier signal High Byte 4-bit Period Value for PWM mode.			
	P_TMA_CAPH		R	R/0	R/0	R/0	R/0	Timer A received carrier signal High Byte 4-bit Period Width value for CAPTURE mode.			
	P_TMA_ENVH		W	-	-	-	-	Timer A received carrier signal High Byte 4-bit Period Width pre-value for ENVELOPE mode.			
$25	P_TMB_CNTL	xxh	R	Timer B Counter Low Byte 8-bit Pre-value.							

	P_TMB_REGL		W	Timer B Low Byte 8-bit Register.				
$26	P_TMB_CNTH	xxh	R	R/0	R/0	R/0	R/0	Timer B Counter High Byte 4-bit Pre-value.
	P_TMB_REGH		W	-	-	-	-	Timer B High Byte 4-bit Register

GPM6P1015A Special Function Registers Description

$0000~$000A: I/O port

Address	Register	Reset Value	R/W	Bit7	Bit6$	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$00	P_IOB_DIR	00h	R/W	R/0	R/0	Port B Direction control					
$01	P_IOC_DIR	00h	R/W	R/0	R/0	R/0	R/0	R/0	R/0	R/0	Port C Direction control
$02	P_IOD_DIR	00h	R/W	R/0	R/0	Port D Direction control					
$04	P_IOB_ATT	00h	R/W	R/0	R/0	Port B attribute register					
$05	P_IOC_ATT	00h	R/W	R/0	R/0	R/0	R/0	R/0	R/0	R/0	Port C attribute register
$06	P_IOD_ ATT	00h	R/W	R/0	R/0	Port D attribute register					
$08	P_IOB_DAT	00h	R/W	R/0	R/0	Write data into the Port B data register and read data from the I/O pad.					
$09	P_IOC_DAT	00h	R/W	R/0	R/0	R/0	R/0	R/0	R/0	R/0	Write data into the Port C data register and read data from the I/O pad.
$0A	P_IOD_DAT	00h	R/W	R/0	R/0	Write data into the Port D data register and read data from the I/O pad.					

$0011~$001D: INT Flag & other special register

Address	Register	Reset Value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$11	P_PWM_DRV	00h	W	-	R/0	R/0	R/0	PWMDRV0	-	-	-
	P_RX_SEN	00h	W	-	R/0	R/0	R/0	-	TMACAPS	SENSE1	SENSE0
$12	P_SYS_SLEEP	00h	W	C_SYS_SLEEP= AAH (Write other data system to reset.)							
$13	P_INT_CTRL	00h	R/W	TMADTE	TMAOIE	CAPIE	TMBOIE	F1KIE	F4KIE	F32KIE	F2MIE
$14	P_INT_FLAG	00h	R/W	TMADTF	TMAOIF	CAPIF	TMBOIF	F1KIF	F4KIF	F32KIF	F2MIF
$16	P_INT_FLAGC	00h	R/W	ENVDET	R/0	R/0	R/0	R/0	R/0	R/0	R/0
$1B	P_SC_IOB	00h	R/W	R/0	R/0	PB5SE	PB4SE	PB3SE	PB2SE	PB1SE	PB0SE
$1C	P_SC_IOC	00h	R/W	R/0	R/0	R/0	R/0	R/0	R/0	R/0	PC0SE
$1D	P_SC_IOD	00h	R/W	R/0	R/0	PD5SE	PD4SE	PD3SE	PD2SE	PD1SE	PD0SE

$0020~0026: Timer control

Address	Register	Reset Value	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$20	P_WDT_CTRL	00h	W	C_WDT_CLR= AAH (Write other data system to reset.)							
$21	P_TMA_CTRL	00h	R/W	TMAES	CAPEG	TMACLK1	TMACLK0	TMADUT1	TMADUT0	TMAMOD1	TMAMOD0
$22	P_TMB_CTRL	00h	R/W	TMBES	-	TMBCLK1	TMBCLK0	-	-	-	-
$23	P_TMA_CNTL	xxh	R	Timer A Counter Low Byte 8-bit Pre-value for COUNTER mode.							
	P_TMA_PWML		W	Timer A PWM carrier signal Low Byte 8-bit Period Value for PWM mode.							
	P_TMA_CAPL		R	Timer A received carrier signal Low Byte 8-bit Period Width value for CAPTURE mode.							
	P_TMA_ENVL		W	Timer A received carrier signal Low Byte 8-bit Period Width pre-value for ENVELOPE mode.							
$24	P_TMA_CNTH	xxh	R	R/0	R/0	R/0	R/0	Timer A Counter High Byte 4-bit Pre-value for COUNTER mode.			

	P_TMA_PWMH		W	-	-	-	R/0	Timer A PWM carrier signal High Byte 4-bit Period Value for PWM mode.
	P_TMA_CAPH		R	R/0	R/0	R/0	R/0	Timer A received carrier signal High Byte 4-bit Period Width value for CAPTURE mode.
	P_TMA_ENVH		W	-	-	-	R/0	Timer A received carrier signal High Byte 4-bit Period Width pre-value for ENVELOPE mode.
$25	P_TMB_CNTL	xxh	R	Timer B Counter Low Byte 8-bit Pre-value.				
	P_TMB_REGL		W	Timer B Low Byte 8-bit Register.				
$26	P_TMB_CNTH	xxh	R	R/0	R/0	R/0	R/0	Timer B Counter High Byte 4-bit Pre-value.
	P_TMB_REGH		W	-	-	-	-	Timer B High Byte 4-bit Register

5.2.5. BANK Control

GPM6P1129A supports 4 banks OTP ROM: each bank has 32K address space. GPM6C1067A supports 2 banks Mask ROM: each bank has 32K address space. GPM6P1065A supports 2 banks OTP ROM: each bank has 32K address space. GPM6P1033A/p1017A/P1015A supports 1 bank OTP ROM. Bank control register can control bank switch. It is shown as below.

Bank Control Register (P_BANK_CTRL, $0010)

BIT	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	-	-	-	-	-	-	BANK1	BANK0
Access	-	-	-	-	-	-	R/W	R/W
Default	-	-	-	-	-	-	**0**	**0**

GPM6P1129A

Bit [7:2] Reserved

Bit [1:0] **BANK[1:0]:** Bank number set.
00 = Bank number 0 (C_BANK_00)
01 = Bank number 1 (C_BANK_01)
10 = Bank number 2 (C_BANK_10)
11 = Bank number 3 (C_BANK_11)

GPM6C1067A/GPM6P1065A

Bit [7:1] Reserved

Bit [0] **BANK[0]:** Bank number set.
0 = Bank number 0 (C_BANK_00)
1 = Bank number 1 (C_BANK_01)

5.3. Clock Source

GPM6P1129A/C1067A/P1065A/P1033A/P1017A/P1015A support Crystal / Ceramic or Internal oscillator, as shown in the following diagram, Figure 5-12. They can be selected by device configuration option at address ($FFF8.0) and be set in Fortis IDE as Figure 5-11.

The detailed configuration option setting of device has been given in *Section 0 Configuration Option Registe.*

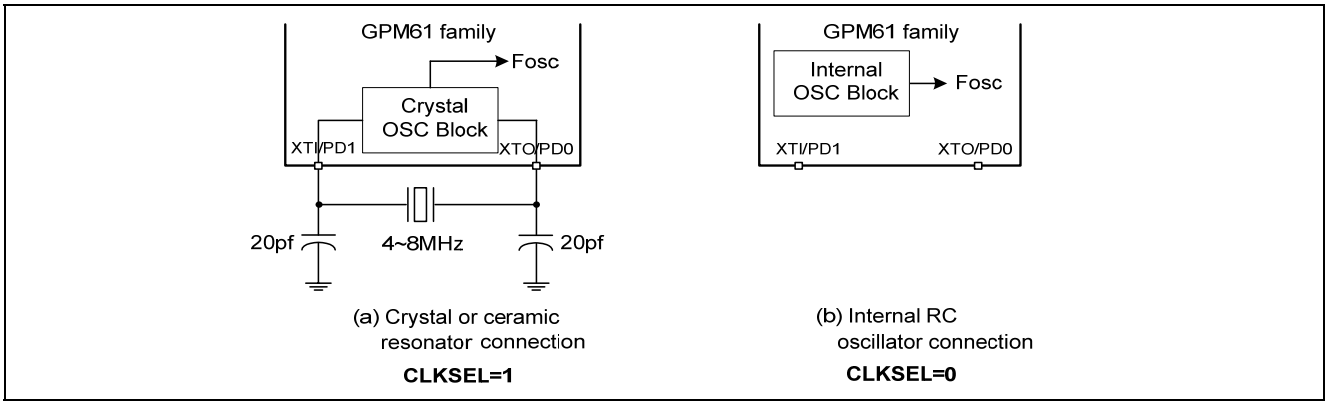


Figure 5-12 Two types of clock sources

5.4. Power Saving Mode

5.4.1. Introduction

To reduce the current consumption when system does not need to be active, SLEEP mode and FREEZE mode can be utilized. These two modes are able to reduce power consumption and save power. They also feature different wakeup time. User must write corresponding value to SLEEP Control Register to enter SLEEP mode. And system will enter FREEZE mode automatically when power supply is lower than a special value or power down. For more information about SLEEP and FREEZE modes, please see Figure 5-13 and they will be depicted in the next two sections.

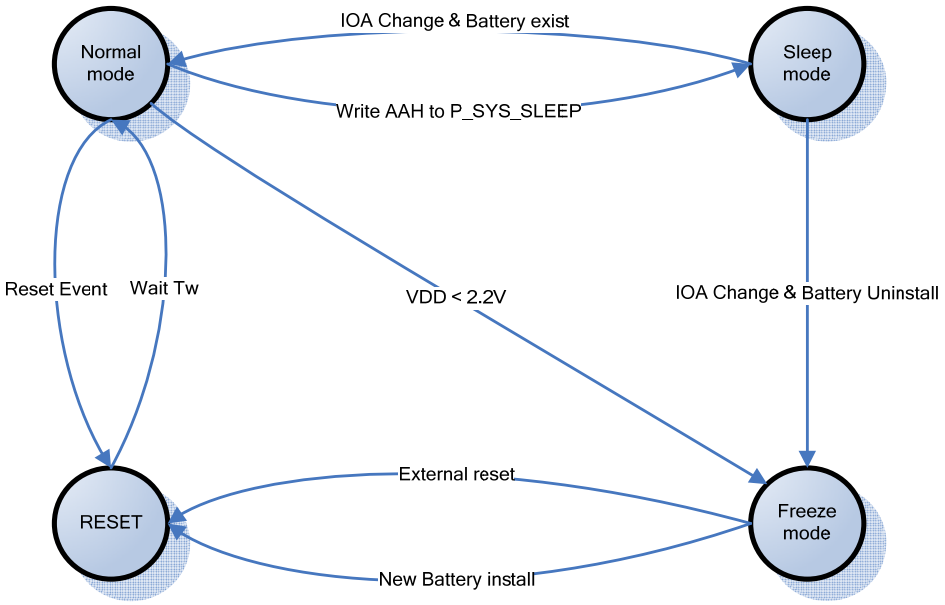


Figure 5-13 Power saving mode operation

5.4.2. SLEEP Mode

The SLEEP mode function will disable all system clocks, including the clock generation circuit. Once the system enters the SLEEP mode, LVR function is disabled, RAM and I/Os will remain in their previous states until being awakened. The system will be waked up by any change on port A. After the GPM6P1129A/C1067A/P1065A/P1033A/P1017A/P1015A are awakened, the internal CPU will remain in previous state until Tw ≧ 65536 x T1 (Tw = waiting time & T1 = system clock cycle); and then continue processing the program. (See Figure 5-14).

$$T1 = 1 / (F_{CPU}),\ Tw \geqq 65536 \times T1$$

To enter SLEEP mode, programmer must write #C_SYS_SLEEP ($AA) to SLEEP control register (P_SYS_SLEEP).

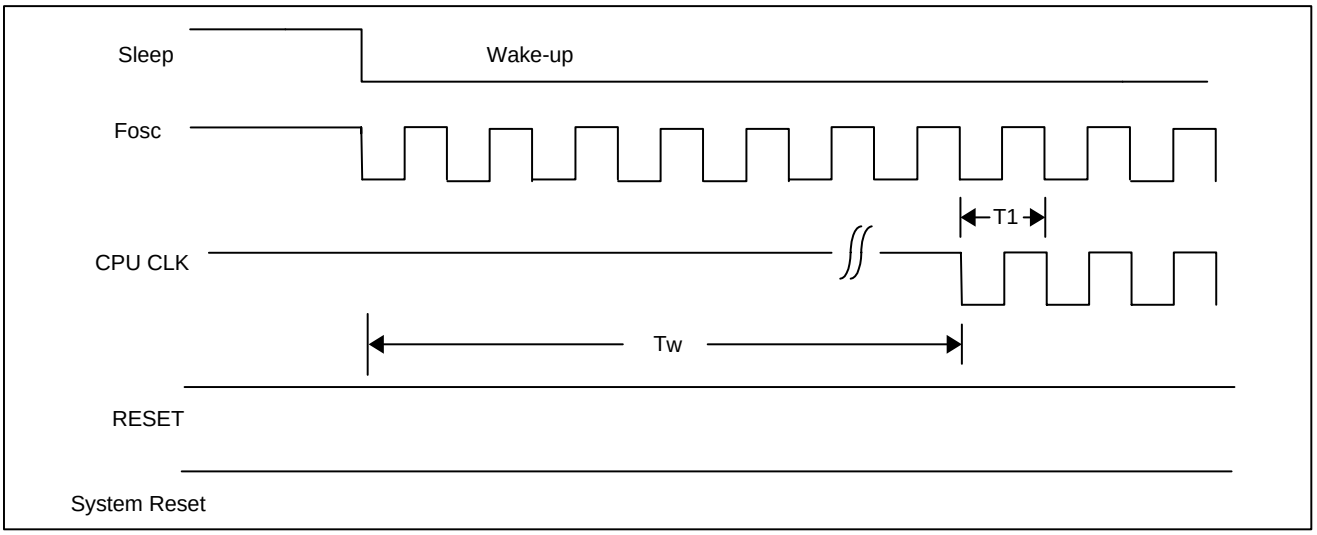


Figure 5-14 SLEEP mode

5.4.3. FREEZE Mode

If the power-supply voltage drops below 2.2V (See Figure 5-15), system will go into FREEZE mode. Low Voltage Reset (LVR) will reset all functions into the initial operational (stable) state. In FREEZE mode, system clock and CPU is stopped; RAM remains in the previous states; all I/Os are floating with input function disabled; LVR function is disabled. The FREEZE mode would not be released by any external interrupts unless the battery is removed and reinstalled, which voltage is higher than 2.2V or external reset occurrence. The system watch dog action is not occurred in FREEZE mode.

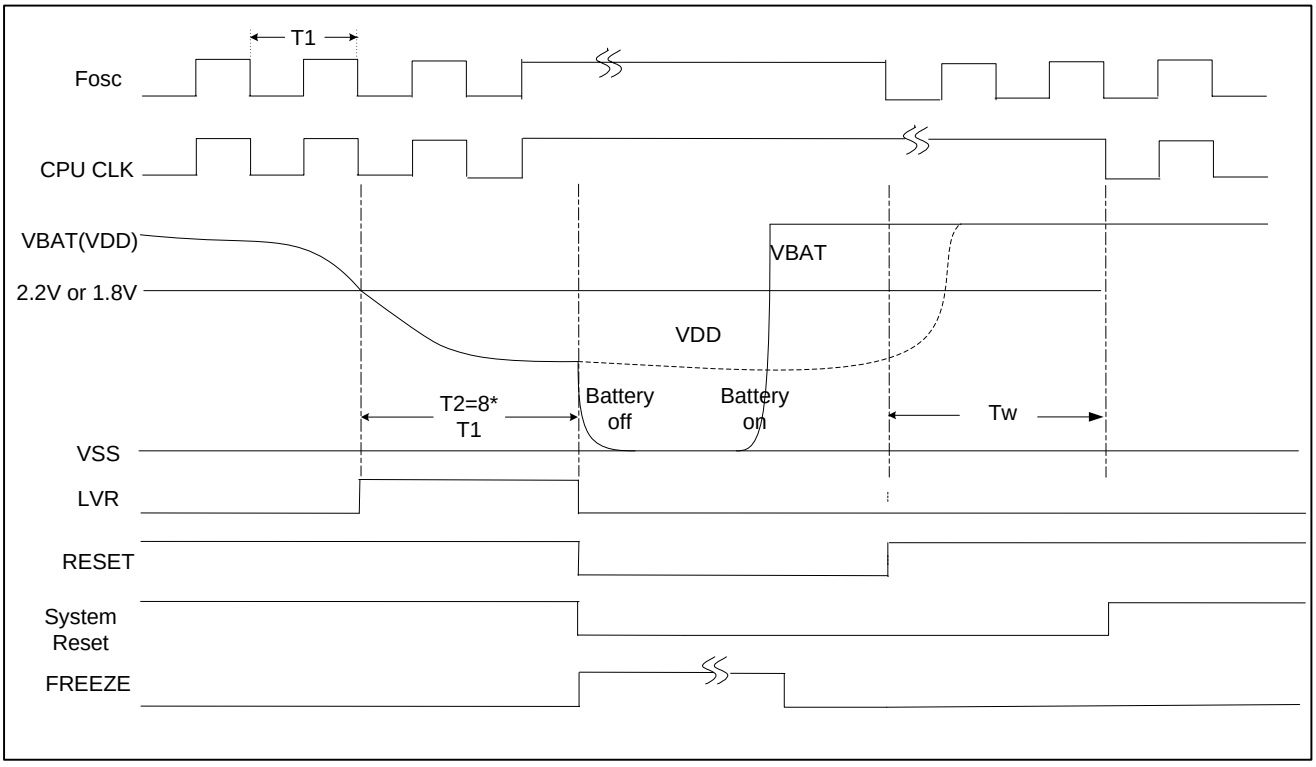


Figure 5-15 FREEZE mode

SLEEP Control Register (P_SYS_SLEEP, $0012)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	SLEEPCTRL7	SLEEPCTRL6	SLEEPCTRL5	SLEEPCTRL4	SLEEPCTRL3	SLEEPCTRL2	SLEEPCTRL1	SLEEPCTRL0
ACCESS	W	W	W	W	W	W	W	W

Bit [7:0] **SLEEPCTRL** [7:0]: Operation mode control.
$AA = write to enter SLEEP mode (C_SYS_SLEEP)
Other data = reset system

[Example] 5-3 Let MCU enter SLEEP mode

```
LDA     P_IOA_DAT                ; latch PortA
LDA     #C_SYS_SLEEP             ; SLEEP command $AA
STA     P_SYS_ SLEEP             ; go to sleep mode
```

5.5. Interrupt

5.5.1. Introduction

The GPM6P1129A/C1067A/P1065A/P1033A/P1017A/P1015A provide eight types of interrupt sources with the same normal interrupt level. The eight types of interrupt sources are Timer A envelope detect interrupt, Timer A capture interrupt, Timer A overflow interrupt, Timer B overflow interrupt, time Fosc/1024 interrupt, time Fosc/4096 interrupt, time Fosc/32768 interrupt, time Fosc/2097152 interrupt.

These interrupts have individual status (occurred or not) and control (enable or not) registers. In general, once an interrupt event occurs, the corresponding flag bit will be set. If the related interrupt control bit is set to enable interrupt, an interrupt request signal will be generated and then CPU executes the interrupt service routine. If the related interrupt control bit is disabled, programmer still can observe the corresponding flag bit, but no interrupt request signal will be generated. The interrupt flag bits must be cleared in the interrupt service routine to prevent program from deadlock. With any instruction, interrupts pending during the previous instruction is served.

Before entering interrupt service routine, the system saves the current PC address into bottom of the stack such as address $1FF and $1FE in Figure 5-16. And abstract the interrupt service routine first address from $FFFE and $FFFF. In a corresponding way, the system abstracts the returned PC address from the bottom of the stack when finishing the interrupt service (See Figure 5-17).

These interrupt sources are listed as **[Table] 5-1** and will be described in corresponding section.

[Table] 5-1 Interrupt Source List

Source	Interrupt Flag Register	Interrupt Control Register	Source	Interrupt Flag Register	Interrupt Control Register
Envelope Detect Interrupt	TMADTF($0014.7)	TMADTE($0013.7)	Time Fosc/1024	F1KIF($0014.3)	F1KIE($0013.3)
Timer A Overflow	TMAOIF($0014.6)	TMAOIE($0013.6)	Time Fosc/4096	F4KIF($0014.2)	F4KIE($0013.2)
Capture Interrupt	CAPIF($0014.5)	CAPIE($0013.5)	Time Fosc/32768	F32KIF($0014.1)	F32KIE($0013.1)
Timer B Overflow	TMBOIF($0014.4)	TMBOIE($0013.4)	Time Fosc/2097152	F2MIF($0014.0)	F2MIE($0013.0)

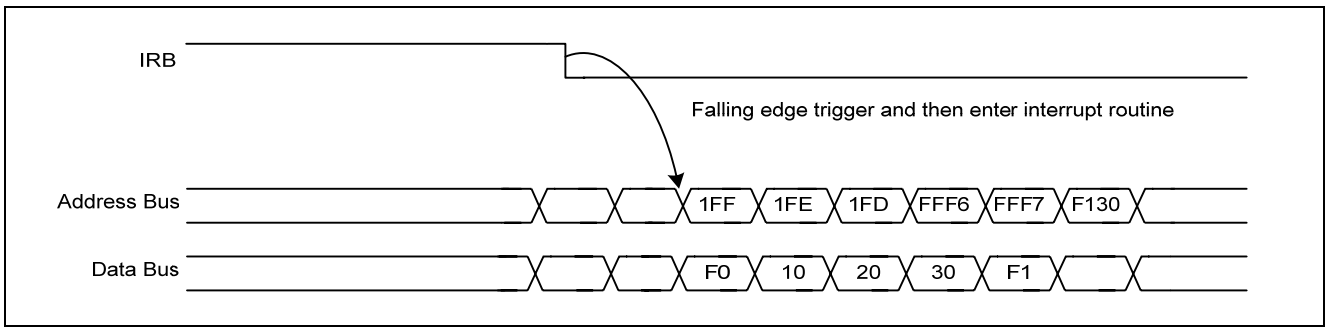


Figure 5-16 Interrupt triggered by IRB

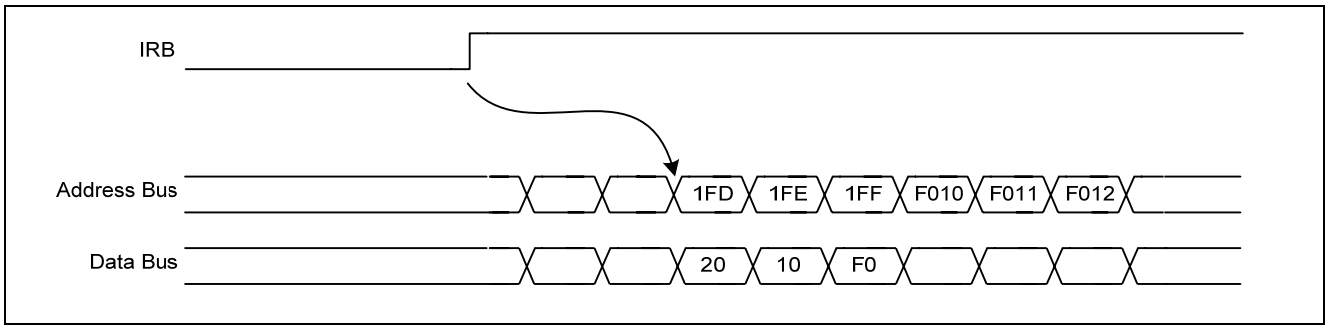


Figure 5-17 Leave interrupt routine

5.5.2. Interrupt register

Interrupt Flag Register (P_INT_FLAG, $0014)

BIT	7	6	5	4	3	2	1	0
Name	TMADTF	TMAOIF	CAPIF	TMBOIF	FD1KIF	FD4KIF	FD32KIF	FD2MIF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

This flag is cleared by writing the corresponding bit by “1”.

Bit 7 **TMADTF**: Timer A envelope detect interrupt flag
0 = no event
1 = event has occurred

Bit 6 **TMAOIF**: Timer A overflow interrupt flag
0 = no event
1 = event has occurred

Bit 5 **CAPIF**: Timer A capture interrupt flag
0 = no event
1 = event has occurred

Bit 4 **TMBOIF**: Timer B overflow interrupt flag
0 = no event
1 = event has occurred

Bit 3 **FD1KIF**: Time Fosc/1024 interrupt flag
0 = no event
1 = event has occurred

Bit 2 **FD4KIF**: Time Fosc/4096 interrupt flag
0 = no event
1 = event has occurred

Bit 1 **FD32KIF**: Time Fosc/32768 interrupt flag
0 = no event
1 = event has occurred

Bit 0 **FD2MIF**: Time Fosc/2097152 interrupt flag
0 = no event
1 = event has occurred

Interrupt Control Register (P_INT_CTRL, $0013)

BIT	7	6	5	4	3	2	1	0
Name	TMADTE	TMAOIE	CAPIE	TMBOIE	FD1KIE	FD4KIE	FD32KIE	FD2MIE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 **TMADTF**: Timer A envelope detect interrupt enable bit
0 = interrupt disable
1 = interrupt enable

Bit 6 **TMAOIE**: Timer A overflow interrupt enable bit
0 = interrupt disable
1 = interrupt enable

Bit 5 **CAPIF**: Timer A capture interrupt enable bit
0 = interrupt disable
1 = interrupt enable

Bit 4 **TMBOIE**: Timer B overflow interrupt enable bit
0 = interrupt disable
1 = interrupt enable

Bit 3 **FD1KIE**: Time Fosc/1024 interrupt enable bit
0 = interrupt disable
1 = interrupt enable

Bit 2 **FD4KIE**: Time Fosc/4096 interrupt enable bit
0 = interrupt disable
1 = interrupt enable

Bit 1 **FD32KIE**: Time Fosc/32768 interrupt enable bit
0 = interrupt disable
1 = interrupt enable

Bit 0 **FD2MIE**: Time Fosc/2097152 interrupt enable bit
0 = interrupt disable
1 = interrupt enable

Envelop Detect Register (P_INT_FLAGC, $0016)

BIT	7	6	5	4	3	2	1	0
Name	ENVDET	-	-	-	-	-	-	-
Access	R	-	-	-	-	-	-	-
Default	0	-	-	-	-	-	-	-

Bit 7 **ENVDET**: Envelope flag showing whether envelope exist or not.
0 = no envelope exist
1 = envelope exist

Bit [6:0] Reversed

[Example] 5-4 Enable Timer A overflow interrupt

```
;=========================;
; main loop routine
;=========================;
LDA     #C_INT_TMAOIE
STA     P_INT_CTRL                      ; enable Timer A overflow INT
CLI                                     ; enable INT
;=========================;
;IRQ interrupt service routine
;=========================;
LDA     #C_INT_TMAOIF
STA     P_INT_FLAG                      ; clear INT request flag
STA     P_INT_CTRL                      ; enable Timer A overflow INT
```

5.6. Reset Sources

5.6.1. Introduction

There are four types of reset sources for the system, Power-On Reset (POR), External Reset (ERST), Low Voltage Reset (LVR), Watchdog Timer Reset (WDR). These reset sources can be concluded as external events and internal events. The external events come from power line or external trigger event. The internal events come from the program execution. Figure 5-18 shows the affected region for each reset source.

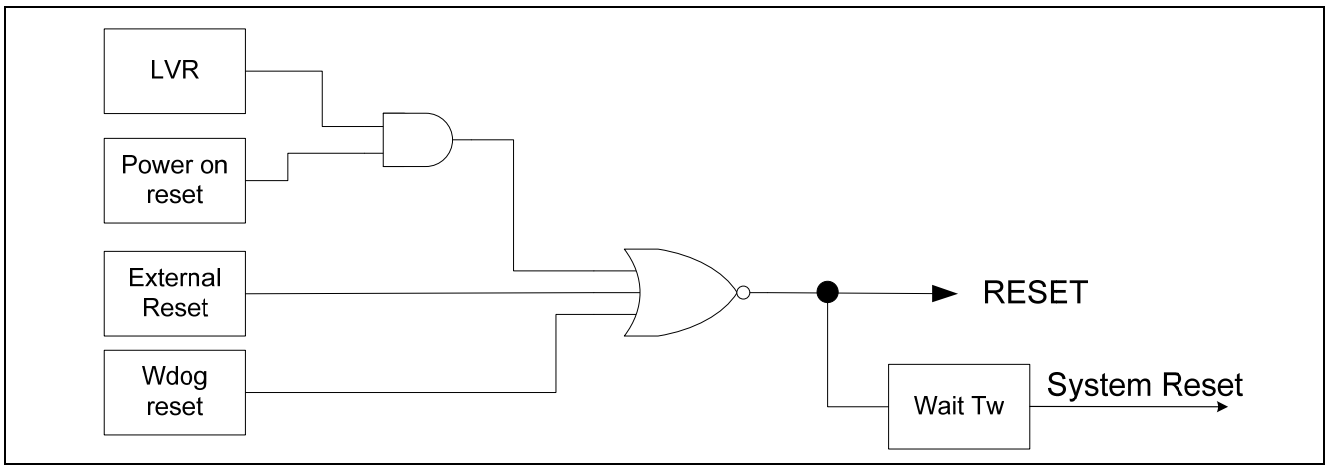


Figure 5-18 Reset sources

5.6.2. Power-On Reset (POR)

A POR is generated when VDD is rising from 0v. When VDD rises to an acceptable level (~1.45V), the power on reset circuit will start a power-on sequence. After that, the system will operate in target speed and start to activate.

5.6.3. External Reset (ERST)

The GPM6P1129A/C1067A/P1065A/P1033A provide an external reset pin to force the system returning to the initial status. The External Reset circuit is shown in Figure 5-19. This pin is a low active signal. When the $\overline{\text{RESET}}$ pin falls below 0.3 x VDD, the system will be forced to enter reset state.

The external reset pulse width must be larger than 1000ns at least. Any pulse shorter than 1000ns will be filtered and taken no effect n the system. If a reset pulse that is long enough to take effect, the reset will be extended to 16ms.

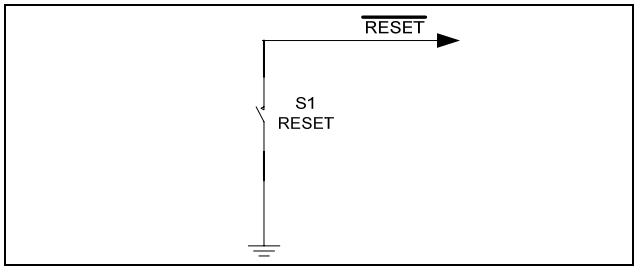


Figure 5-19 External Reset circuit

5.6.4. Low Voltage Reset (LVR)

The on-chip Low Voltage Reset (LVR) circuitry forces the system entering FREEZE mode when the MCU voltage falls below the specific LVR trigger voltage. This function prevents MCU from working at an invalid operating voltage range.

A device configuration option bit $FFF8.1(can be set in Fortis IDE as Figure 5-11) is used to enable or disable this function. If this function is enabled, the LVR circuit will monitor power level while chip is operating. If the power is lower than the specific level for a specific period, the system will enter FREEZE mode and all I/Os will be locked.

5.6.5. Watchdog Timer Reset (WDR)

On-chip watchdog circuitry makes the device entering reset when MCU goes into an unknown state without watchdog clearing information. This function prevents the MCU from an abnormal condition. The Watchdog Timer (WDT) can be disabled or enabled through configuration option bit $FFF8.2 (can be set in Fortis IDE as Figure 5-11). The Watchdog Timer Reset will be generated by a time-out event of the WDT automatically when watchdog is enabled.

The Watchdog Timer Reset will reset the CPU and restart the program. To avoid a WDT time-out reset, user should write # C_WDT_CLR (=$AA) to P_WDT_CTRL periodically. If a reset signal is generated, it will also clear the WDT counter and restart the WDT.

Different Reset Sequences are as the following figures:

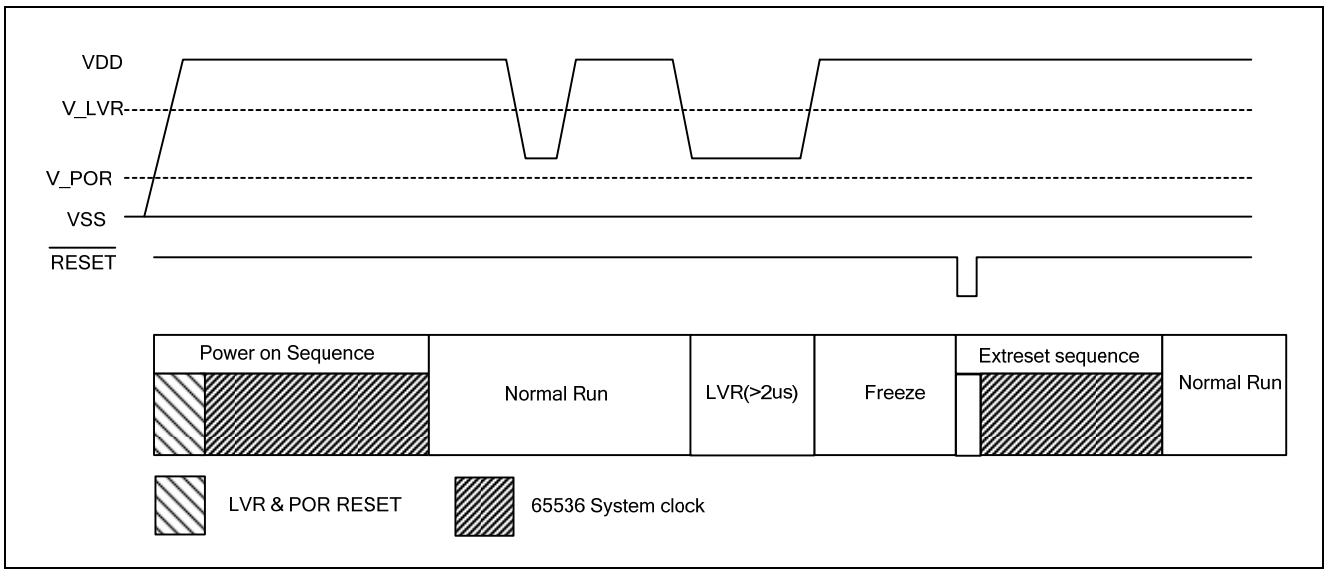


Figure 5-20 Reset Sequence

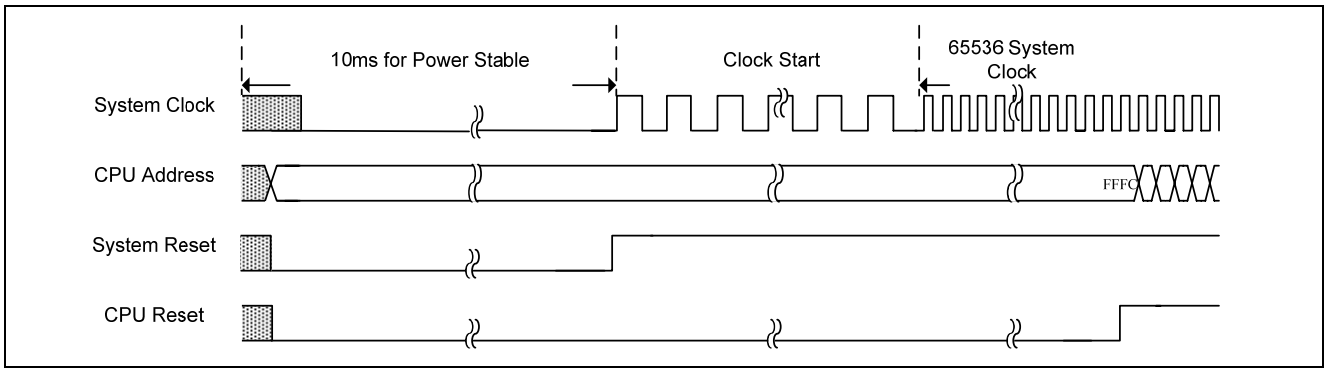


Figure 5-21 Power-On Reset Sequence

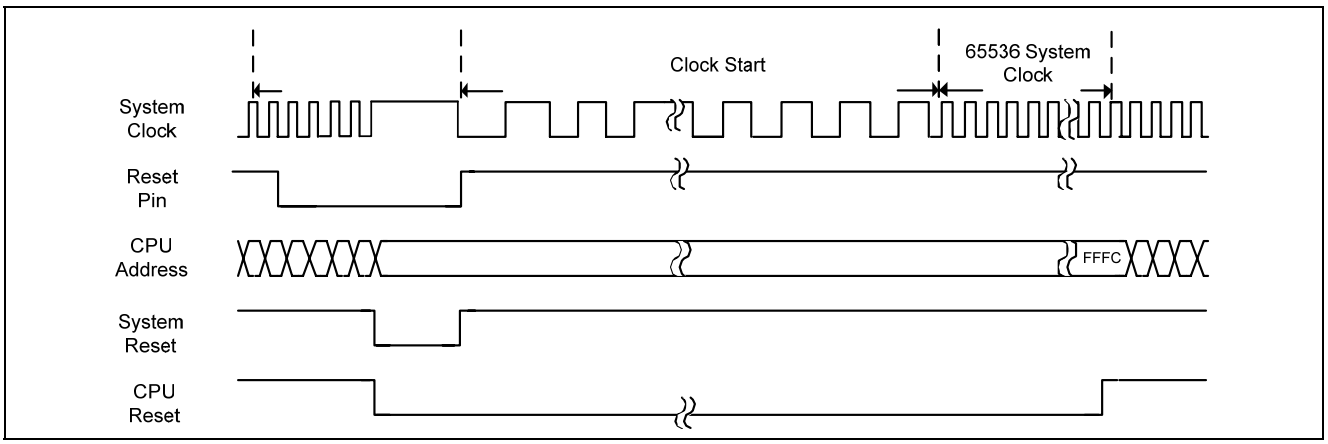


Figure 5-22 External Reset Sequence

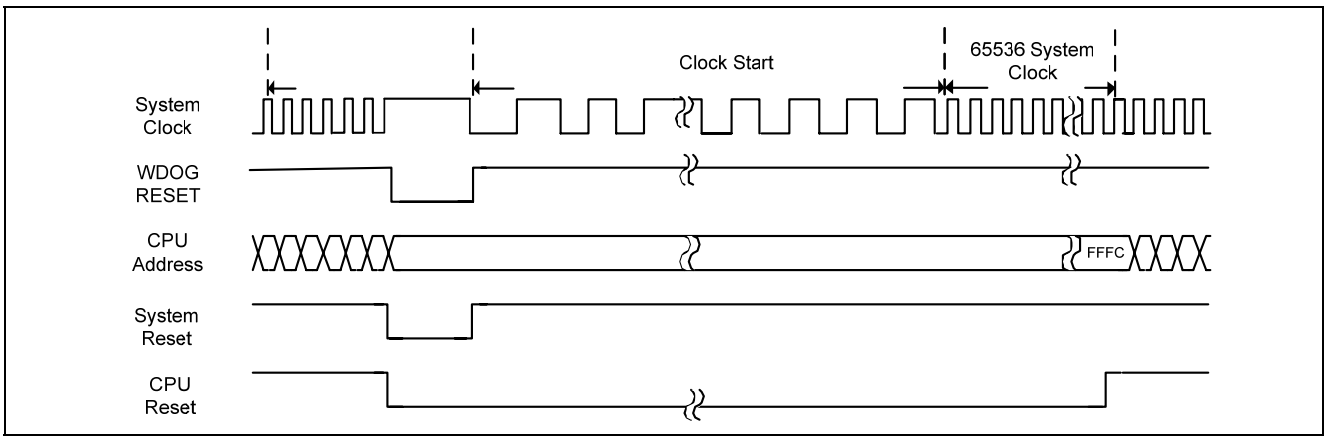


Figure 5-23 Watch-Dog Reset Sequence

Watchdog Control Register (P_WDT_CTRL, $0020)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	WDTCTRL7	WDTCTRL6	WDTCTRL5	WDTCTRL4	WDTCTRL3	WDTCTRL2	WDTCTRL1	WDTCTRL0
ACCESS	W	W	W	W	W	W	W	W

Bit [7:0] **WDTCTRL [7:0]:** Operation mode control register
$AA = write to clear watchdog CNT (C_WDT_CLR)
Other data = reset system

[Example] 5-5 Clear watch dog counter

```
LDA     # C_WDT_CLR                    ; Clear watch dog command $AA
STA     P_WDT_ CTRL
```

5.7. I/O PORTS

5.7.1. Introduction

GPM6P1129A/C1067A/P1065A/P1033A have four ports: Port A, Port B, Port C and Port D. GPM6P1017A/ P1015A have two ports: Port B and Port D. These port pins may be multiplexed with an alternate function for the peripheral features on the device. In general, when an initial reset state occurs, all ports are used as a general purpose input port. There are two parts in Port A IO structures: data and pull registers, and three parts in the others' IO structures: data, direction and attribution registers. Each corresponding bit in these ports should be given a value.

GPM6P1129A/C1067A/P1065A/P1033A can use in M-Type keyboard application, Port A should be configured as input ports, and in sleep mode any change occurred in these ports will cause system wakeup. GPM6P1017A/P1015A can use in M-Type keyboard application, Port B should be configured as input ports, and in sleep mode any change occurred in these ports will cause system wakeup. GPM6P1017A/P1015A also can use in T-Type keyboard application, each port of Port B and Port D can be selected as scan key independently by configuring register P_SC_IOX. If the port is configured as scan key, it worked as input with pull-high resistor and output fixed frequency low pulse in sleep mode. Any of the keys touch would cause system wakeup.

The setting rules are as follows:

- The direction setting determines whether this pin is an input or an output.
- The data register is used to read the value on the port, which can be different when programmer sets the port to different configuration (input pull-high/pull-low).
- The pull registers for IOA setting affect if the pure input pin with or without a pull resistor.

Please refer to the
[Table] 5-1 for IOA's and **[Table] 5-2**, **[Table] 5-23** for IOB, IOC, IOD's setting.

[Table] 5-1 I/O configurations (for IOA)

Pull (P_IOA_PULL)	Data (P_IOA_DAT)	Function	Description
0	0	Floating	Input with float
0	1	Floating	Input with float
1	0	Pull Low	Input with pull-low
1	1	Pull High	Input with pull-high

[Table] 5-2 I/O configurations (for IOB, IOC and IOD)

Attribution (P_IOX_ATT)	Direction (P_IOX_DIR)	Data (P_IOX_DAT)	Function	Description
0	0	0	Floating	Input with float
0	0	1	Pull low	Input with pull-low
0	1	0	Driving low	Output Data
0	1	1	Driving High	Output Data
1	0	0	Floating	Input with float
1	0	1	Pull high	Input with pull-high
1	1	0	Driving High	Output Data
1	1	1	Driving low	Output Data

[Table] 5-3 I/O configurations (for IOD[5])

Attribution (P_IOX_ATT)	Direction (P_IOX_DIR)	Data (P_IOX_DAT)	Function	Description
0	0	0	Floating	Input with float
0	0	1	Pull low	Input with pull-low
0	1	0	Driving low	Output Data
0	1	1	Floating	float
1	0	0	Floating	Input with float
1	0	1	Pull high	Input with pull-high
1	1	0	Floating	float
1	1	1	Driving low	Output Data

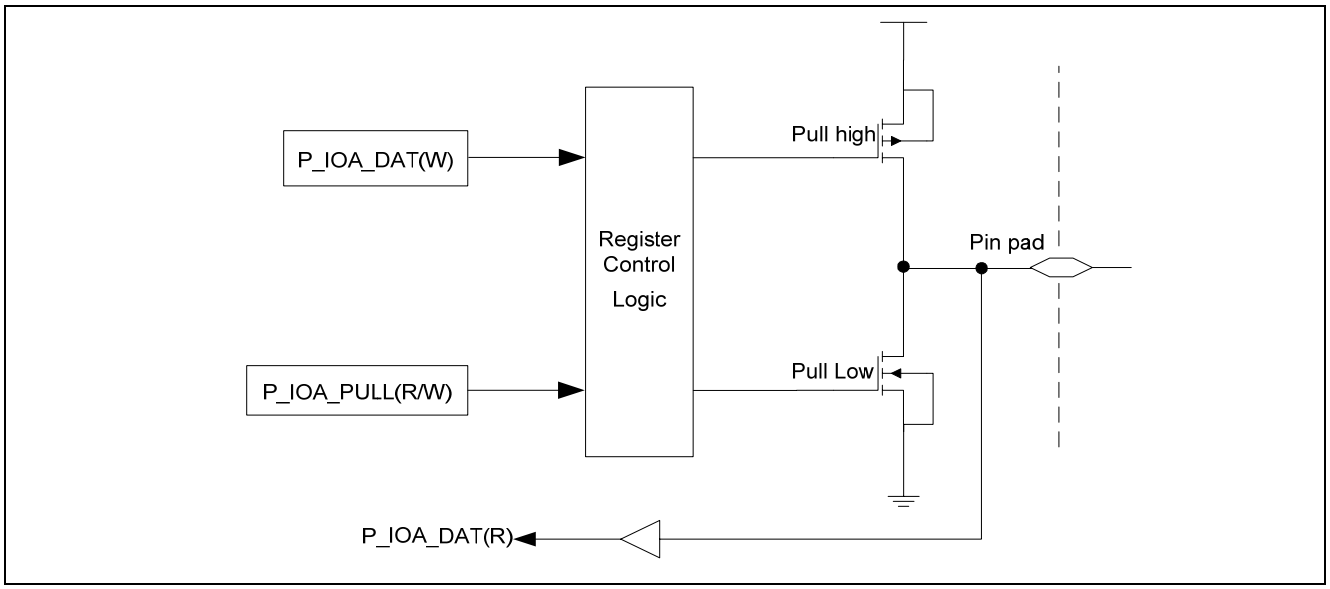


Figure 5-24 Block diagram of I/O port (IOA)

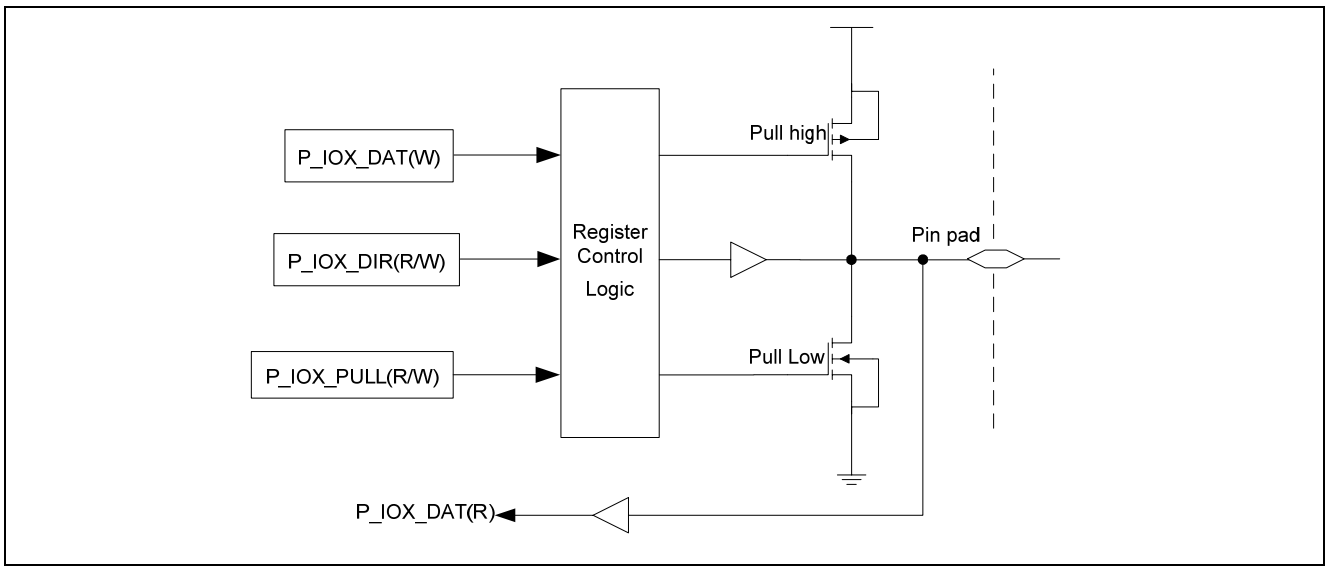


Figure 5-25 Block diagram of I/O port (IOB, IOC and IOD)

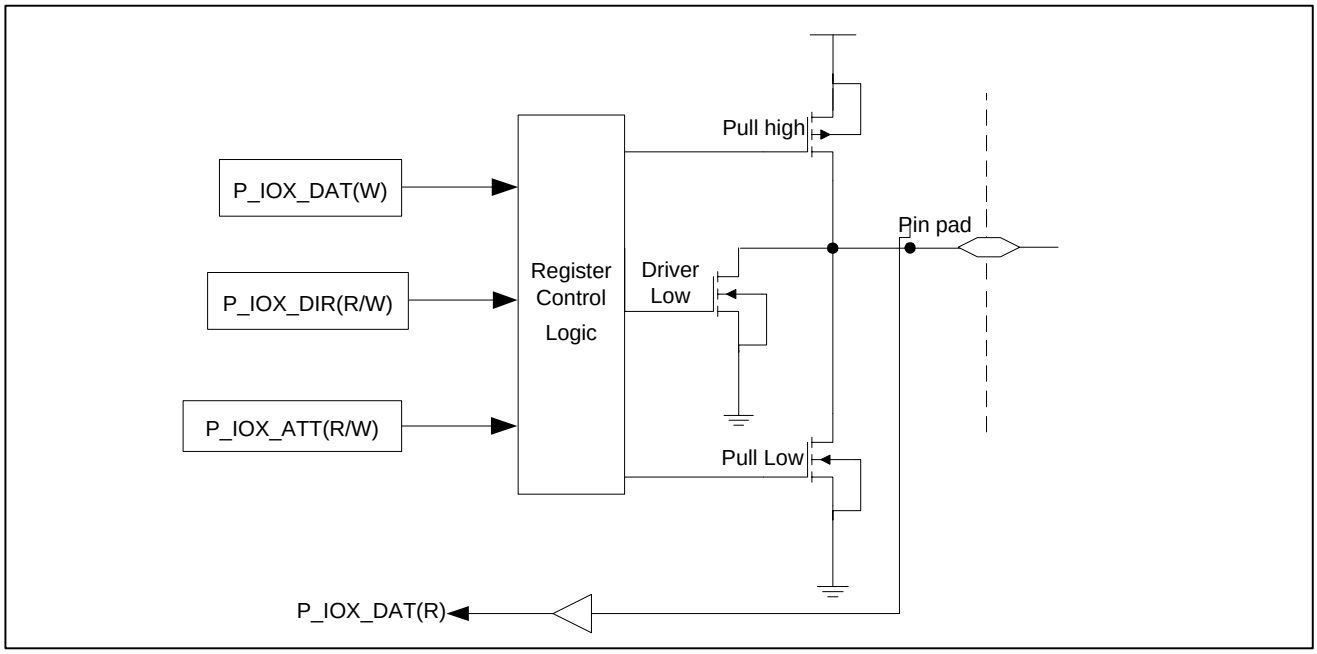


Figure 5-26 Block diagram of I/O port (PD[5])

5.7.2. Port A

Port A is a 6-bit pure input port. The Port is controlled by data register P_IOA_DAT, and pull control register P_IOA_PULL. P_IOA_PULL is used to disable or enable pull resistor. P_IOA_DAT is used to control the input pin with pull-low or pull-high resistor. To read the real IO value, user should read P_IOA_DAT.

Port A Pull Register (P_IOA_PULL $0003)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	-	-	P_IOA_PULL					
ACCESS	-	-	R/W					
DEFAULT	-	-	00h					

GPM6P1129A/C1067A/P1065A/P1033A

Bit [7:6] Reserved

Bit [5:0] **P_IOA_PULL**: Writing to disable or enable pull resistor.

0 = disable pull resistor

1 = enable pull resistor

Port A Data Register (P_IOA_DAT, $0007)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	-	-	P_IOA_DAT					
ACCESS	-	-	R/W					
DEFAULT	-	-	00h					

GPM6P1129A/C1067A/P1065A/P1033A

Bit [7:6] Reserved

Bit [5:0] **P_IOA_DAT:** Port A Data value.

Read to get Port A value

Write to configure input with pull low or pull high resistor if the corresponding P_IOA_PULL register bit is set as “1”.

0= input with pull low resistor

1= input with pull high resistor

[Example] 5-6 Set Port A [5:0] as input with pull low resistor.

```
LDA     #$3F                    ; STORE ACCUMULATOR WITH $3F
STA     P_IOA_PULL              ; ENABLE PULL RESISTOR
LDA     #$00                    ; STORE ACCUMULATOR WITH $00
STA     P_IOA_DAT               ; SET IOA AS INPUT WITH PULL LOW RESISTOR
```

[Example] 5-7 Set Port A [5:0] as Input with pull high resistor.

```
LDA     #$3F                    ; store accumulator with $3F
STA     P_IOA_PULL              ; Enable pull resistor
STA     P_IOA_DAT               ; set IOA as input with pull high resistor
```

5.7.3. Port B

Port B is an 8-bit programmable bi-directional port. The Port is controlled by direction control register P_IOB_DIR, and attribution register P_IOB_ATT. Reading P_IOB_DAT will get the real IO value.

Port B Direction Register (P_IOB_DIR, $0000)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	P_IOB_DIR							
ACCESS	R/W							
DEFAULT	00h							

GPM6P1129A/C1067A/P1065A/P1033A

Bit [7:0] **P_IOB_DIR:** Port B direction register.

0 = input

1 = output

GPM6P1017A/ P1015A

Bit [7:6] Reserved

Bit [5:0] **P_IOB_DIR:** Port B direction register.

0 = input

1 = output

Port B Attribution Register (P_IOB_ATT, $0004)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	P_IOB_ATT							
ACCESS	R/W							
DEFAULT	00h							

GPM6P1129A/C1067A/P1065A/P1033A

Bit [7:0] **P_IOB_ATT:** Port B attribution register

GPM6P1017A/ P1015A

Bit [7:6] Reserved

Bit [5:0] **P_IOB_ATT:** Port B attribution register

Port B Data Register (P_IOB_ DAT, $0008)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	P_IOB_ DAT							
ACCESS	R/W							
DEFAULT	00h							

GPM6P1129A/C1067A/P1065A/P1033A

Bit [7:0] **P_IOB_ DAT:** Port B Data value.
Read to get Port B value
Write to configure input with pull low or pull high resistor

GPM6P1017A/ P1015A

Bit [7:6] Reserved

Bit [5:0] **P_IOB_ DAT:** Port B Data value.
Read to get Port B value
Write to configure input with pull low or pull high resistor

[Example] 5-8 Set Port B [3:0] as output with low data and Port B [7:4] as input with pulling high.

```
LDA     #$0F                    ; store accumulator with $0F
STA     P_IOB_DIR               ; set direction
LDA     #$00                    ; store accumulator with $00
STA     P_IOB_ATT               ; set attribute
LDA     #$F0                    ; store accumulator with $F0
STA     P_IOB_DAT               ; set Port Data
```

[Example] 5-9 Set Port B [7:0] as input with float.

```
LDA     #$00                    ; store accumulator with $00
STA     P_IOB_ATT               ; set direction
STA     P_IOB_DIR               ; set attribute
STA     P_IOB_DAT               ; set Port Data
```

The GPM6P1017A/P1015A's Port B can be configured as scan key or not by key scan selectable register.

GPM6P1017A/P1015A's Port B Key Scan Selectable Register (P_SC_IOB, $001B)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	-	-	PB5SE	PB4SE	PB3SE	PB2SE	PB1SE	PB0SE
ACCESS	-	-	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	00h							

Bit [7:6] Reserved

Bit [5:0] **P_SC_IOB:** Port B Key scan select register.
0: no key scan function
1: with key scan function.

[Example] 5-10 Set PB[3:0] as key scan port.

```
LDA     #$0F
STA     P_SC_IOB                        ; set PB[3:0] as key scan port
```

5.7.4. Port C

Port C is a 8-bit programmable bi-directional port. The port is controlled by direction control register P_IOC_DIR, and attribution register P_IOC_ATT. Reading P_IOC_DAT will get the real IO value.

Port C Direction Register (P_IOC_DIR, $0001)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	P_IOC_DIR							
ACCESS	R/W							
DEFAULT	00h							

GPM6P1129A

Bit [7:0] **P_IOC_DIR:** Port C direction register.
0 = input
1 = output

GPM6C1067A/P1065A

Bit [7:4] Reserved

Bit [3:0] **P_IOC_DIR:** Port C direction register.
0 = input
1 = output

GPM6P1033A

Bit [7:4] Reserved

Bit [3],[0] **P_IOC_DIR:** Port C direction register.
0 = input
1 = output

Bit [1:0] Reserved

GPM6P1015A

Bit [7:1] Reserved

Bit [0] **P_IOC_DIR:** Port C direction register.
0 = input
1 = output

Port C Attribution Register (P_IOC_ATT, $0005)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	P_IOC_ATT							
ACCESS	R/W							
DEFAULT	00h							

GPM6P1129A

Bit [7:0] **P_IOC_ATT:** Port C attribution register

GPM6C1067A/P1065A

Bit [7:4] Reserved

Bit [3:0] **P_IOC_ATT:** Port C attribution register

GPM6P1033A

Bit [7:4] Reserved

Bit [3],[0] **P_IOC_ATT:** Port C attribution register

Bit [1:0] Reserved

GPM6P1015A

Bit [7:1] Reserved

Bit [0] **P_IOC_ATT:** Port C attribution register

Port C Data Register (P_IOC_ DAT, $0009)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	P_IOC_ DAT							
ACCESS	R/W							
DEFAULT	00h							

GPM6P1129A

Bit [7:0] **P_IOC_ DAT:** Port C Data value.
Read to get Port C value
Write to configure input with pull low or pull high resistor

GPM6C1067A/P1065A

Bit [7:4] Reserved

Bit [3:0] **P_IOC_ DAT:** Port C Data value.
Read to get Port C value
Write to configure input with pull low or pull high resistor

GPM6P1033A

Bit [7:4] Reserved

Bit [3],[0] **P_IOC_ DAT:** Port C Data value.
Read to get Port C value
Write to configure input with pull low or pull high resistor

Bit [2:1] Reserved

GPM6P1015A

Bit [7:1] Reserved

Bit [0] **P_IOC_ DAT:** Port C Data value.
Read to get Port C value
Write to configure input with pull low or pull high resistor

[Example] 5-11 Set Port C [1:0] as output with high data and Port C [3:2] as input with pulling high.

```
LDA     #$03                    ; store accumulator with $03
STA     P_IOC_DIR               ; set direction
LDA     #$0F                    ; store accumulator with $0F
STA     P_IOC_ATT               ; set attribute
LDA     #$0B                    ; store accumulator with $0B
STA     P_IOC_DAT               ; set Port Data
```

[Example] 5-12 Set Port C [3:0] as input with pulling low.

```
LDA     #$00                    ; store accumulator with $00
STA     P_IOC_DIR               ; set direction
STA     P_IOC_ATT               ; set attribute
LDA     #$0F                    ; store accumulator with $0F
STA     P_IOC_DAT               ; set Port Data
```

The GPM6P1015A's Port C can be configured as scan key or not by key scan selectable register.

GPM6P1015A's Port C Key Scan Select Register (P_SC_IOC, $001C)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	-	-	-	-	-	-	-	PC0SE
ACCESS	-	-	-	-	-	-	-	R/W
DEFAULT	00h							

Bit [7:1] Reserved

Bit [0] **P_SC_IOC:** Port C Key scan select register.
0: no key scan function
1: with key scan function.

[Example] 5-13 Set PC[0] as key scan port.

```
LDA     #$01
STA     P_SC_IOC                ; set PC[0] as key scan port
```

5.7.5. Port D

Port D is a 6-bit programmable bi-directional port. The Port is controlled by direction control register P_IOD_DIR, and attribution register P_IOD_ATT. Reading P_IOD_DAT will get the real IO value. In addition, Port D is multiplexed with various special functions. After reset, the default setting for Port D is used as general I/O ports.

[Table] 5-4 Port D Function List

Port D Pin	BIT	Shared function
PD0	Bit0	Crystal output (XTO)
PD1	Bit1	Crystal input (XTI)
PD5	Bit5	GPM6P1017A/P1015A OTP program power supply (VPP)

Port D Direction Register (P_IOD_DIR, $0002)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	-	-	P_IOD_DIR					
ACCESS	-	-	R/W					
DEFAULT	00h							

GPM6P1129A

Bit [7:4] Reserved

Bit [3:0] **P_IOD_DIR**: Port D direction register.

0 = input

1 = output

GPM6P1017A/P1015A

Bit [7:6] Reserved

Bit [5:0] **P_IOD_DIR**: Port D direction register.

0 = input

1 = output

GPM6C1067A/P1065A/P1033A

Bit [7:2] Reserved

Bit [1:0] **P_IOD_DIR**: Port D direction register.

0 = input

1 = output

Port D Attribution Register (P_IOD_ATT, $0006)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	-	-	P_IOD_ATT					
ACCESS	-	-	R/W					
DEFAULT	00h							

GPM6P1129A

Bit [7:4] Reserved

Bit [3:0] **P_IOD_ATT**: Port D attribution register

GPM6P1017A/P1015A

Bit [7:6] Reserved

Bit [5:0] **P_IOD_ATT**: Port D attribution register

GPM6C1067A/P1065A/P1033A

Bit [7:2] Reserved

Bit [1:0] **P_IOD_ATT**: Port D attribution register

Port D Data Register (P_IOD_ DAT, $000A)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	-	-	P_IOD_ DAT					
ACCESS	-	-	R/W					
DEFAULT	00h							

GPM6P1129A

Bit [7:4] Reserved

Bit [3:0] **P_IOD_ DAT**: Port D Data value.
Read to get Port D value
Write to configure input with pull low or pull high resistor

GPM6C1067A/P1065A/P1033A

Bit [7:2] Reserved

Bit [1:0] **P_IOD_ DAT**: Port D Data value.
Read to get Port D value
Write to configure input with pull low or pull high resistor

GPM6P1017A/P1015A

Bit [7:6] Reserved

Bit [5:0] **P_IOD_ DAT**: Port D Data value.
Read to get Port D value
Write to configure input with pull low or pull high resistor

[Example] 5-14 Set Port D[1:0] as output with low data.

```
LDA     #$03                    ; store accumulator with $03
STA     P_IOD_DIR               ; set direction
LDA     #$00                    ; store accumulator with $00
STA     P_IOD_ATT               ; set attribute
STA     P_IOD_DAT               ; set port data
```

The GPM6P1017A/P1015A's Port D can be configured as scan key or not by key scan selectable register.

GPM6P1017A/P1015A's Port D Key Scan Select Register (P_SC_IOD, $001D)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	-	-	PD5SE	PD4SE	PD3SE	PD2SE	PD1SE	PD0SE
ACCESS	-	-	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	00h							

Bit [7:6] Reserved

Bit [5:0] **P_SC_IOD:** Port D Key scan select register.
0: no key scan function
1: with key scan function.

[Example] 5-15 Set PD[5:0] as key scan port.

```
LDA     #$3F
STA     P_SC_IOD                ; set PD[5:0] as key scan port
```

5.8. Timer Module

5.8.1. Introduction

GPM6P1129A/C1067A/P1065A/1033A/P1017A/P1015A has two 12-bit timers, Timer A and Timer B respectively. They are up-count timers. Timer A contains one powerful PWM function and is controlled by corresponding control registers. This function can be easily configured. And Timer A also has a capture function; it can capture the frequency of input signal. Each timer's function summary is shown as [Table] 5-5.

[Table] 5-5 Summary of timer function for GPM6P1129A

	Timer Counter	PWM	CAPTURE
Timer A	YES	YES	YES
Timer B	YES	None	None

5.9. Timer A

Timer A is special for generating carrier signal in IR control application. The 12-bit timer is an up counter with input clock selectable (Fosc/1, Fosc/4, Fosc/16), which can be configured by control register P_TMA_CTRL[5:4]. Timer A provides with two PWM modes, and the PWM signal is sent to IR TX (LED) pin. The driver current of these two kinds of PWM are programmable by configuring TX PWM driving current control source register (P_PWM_DRV [4:3]).

Timer A module has the following features:

- Readable and writable
- Clock source selectable
- Interrupt-on-overflow from #$FFF to #$000
- Supports PWM with carrier signal mode
- Supports PWM without carrier signal mode

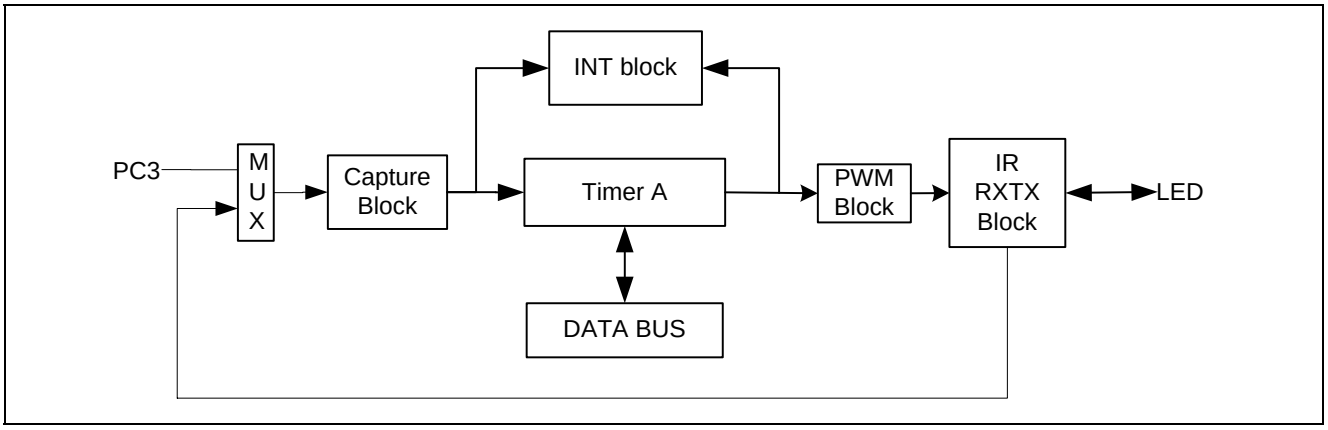


Figure 5-27 Timer A block diagram

5.9.1. PWM with Carrier Signal Mode

Timer A can be configured as PWM mode for generating carrier signal. In PWM with carrier signal mode, the 12-bit timer is an up counter with input clock selectable (Fosc/1, Fosc/4, Fosc/16). When Timer A is started, the value of 4-bit high-byte (low-nibble) register and 8-bit low-byte register would firstly be loaded into the 12-bit counter and then the counter starts count up from the loaded value. If an overflow occurs, the value of high-byte (low-nibble) register (P_TMA_CNTH) and low-byte register (P_TMA_CNTL) would be reloaded into the counter automatically and the counter starts count up again. So the carrier signal with frequency programmable can be generated by this PWM mode via configuring these two registers. Also users can select PWM duty cycle (1/3, 1/4, 1/5, 1/2) via configuring the corresponding bits of the control register (P_TMA_CTRL[3:2]). The carrier signal's enabled or disabled bit can be controlled by two methods depended on which clock source is selected by Timer B. If Timer B is selected one of the first three clock source (Fosc, Fosc/4 or Fosc/64) by P_TMB_CTRL [5:4] (TMBCLK [1:0]), the timer A's carrier signal on/ off is controlled by Timer A's enable/ disable control bit (TMAES) directly.

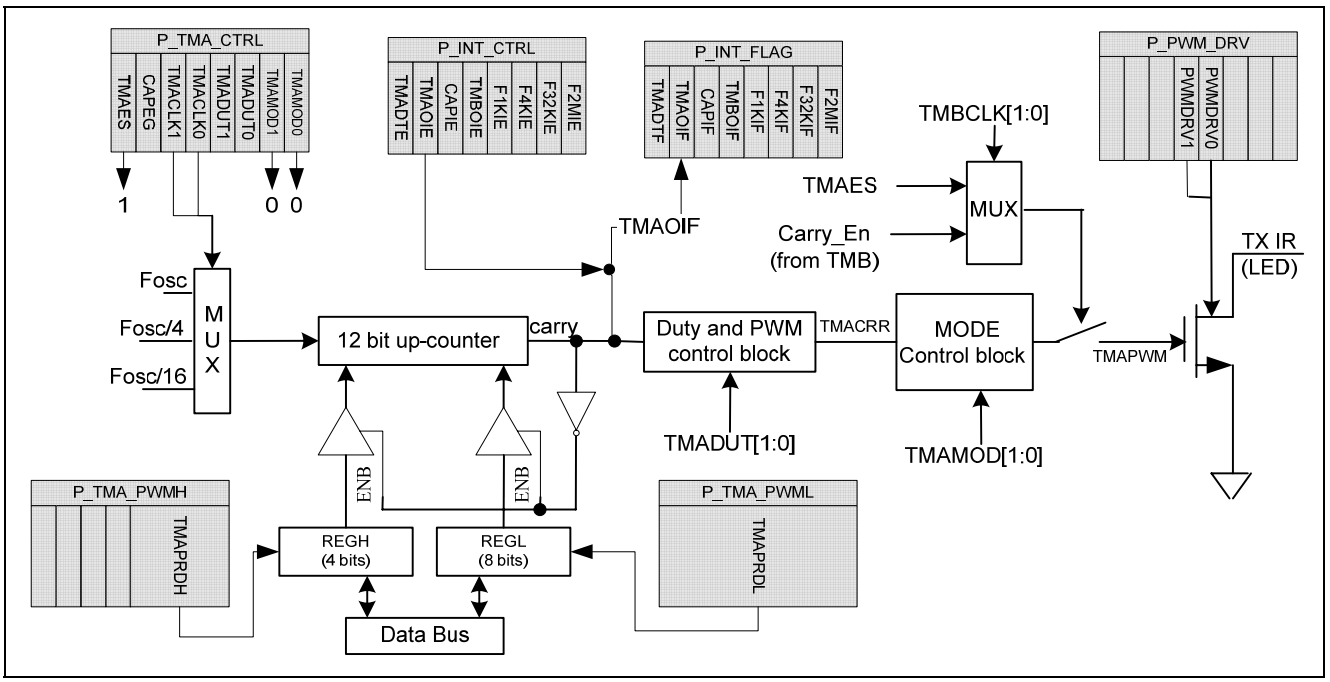


Figure 5-28 Timer A PWM mode diagram

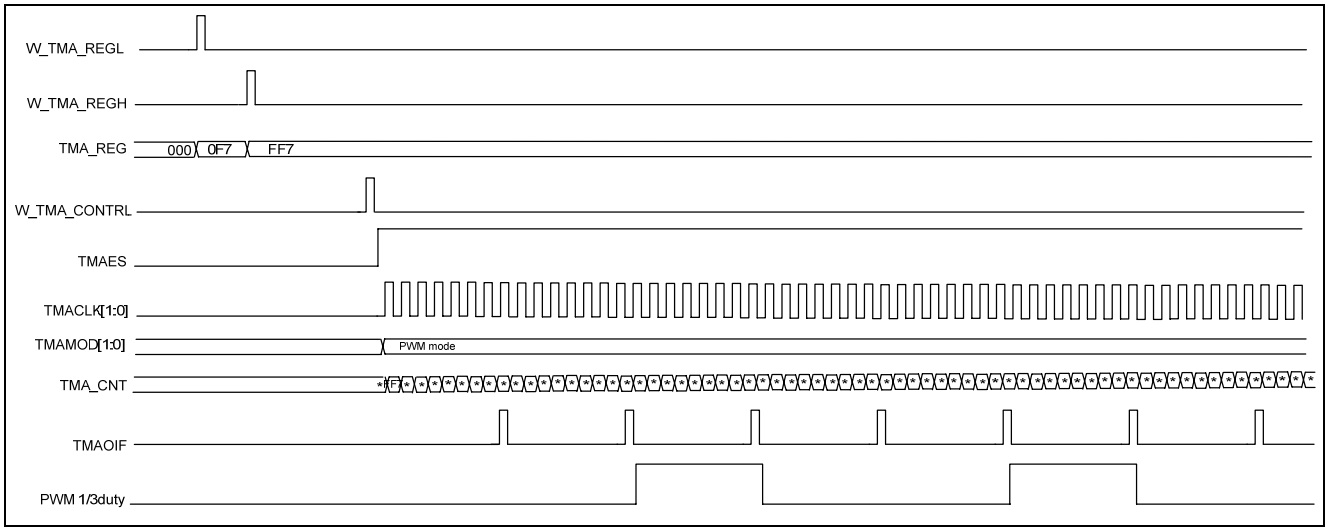


Figure 5-29 Normal PWM generation without envelop

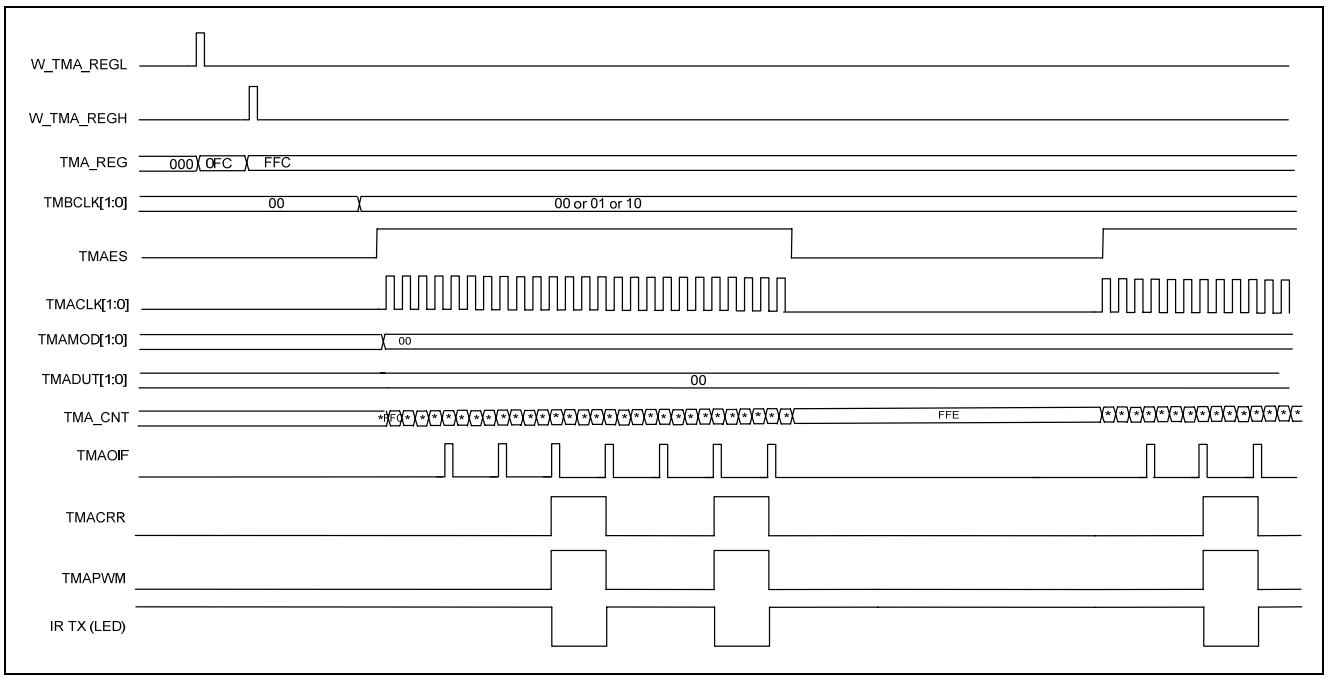
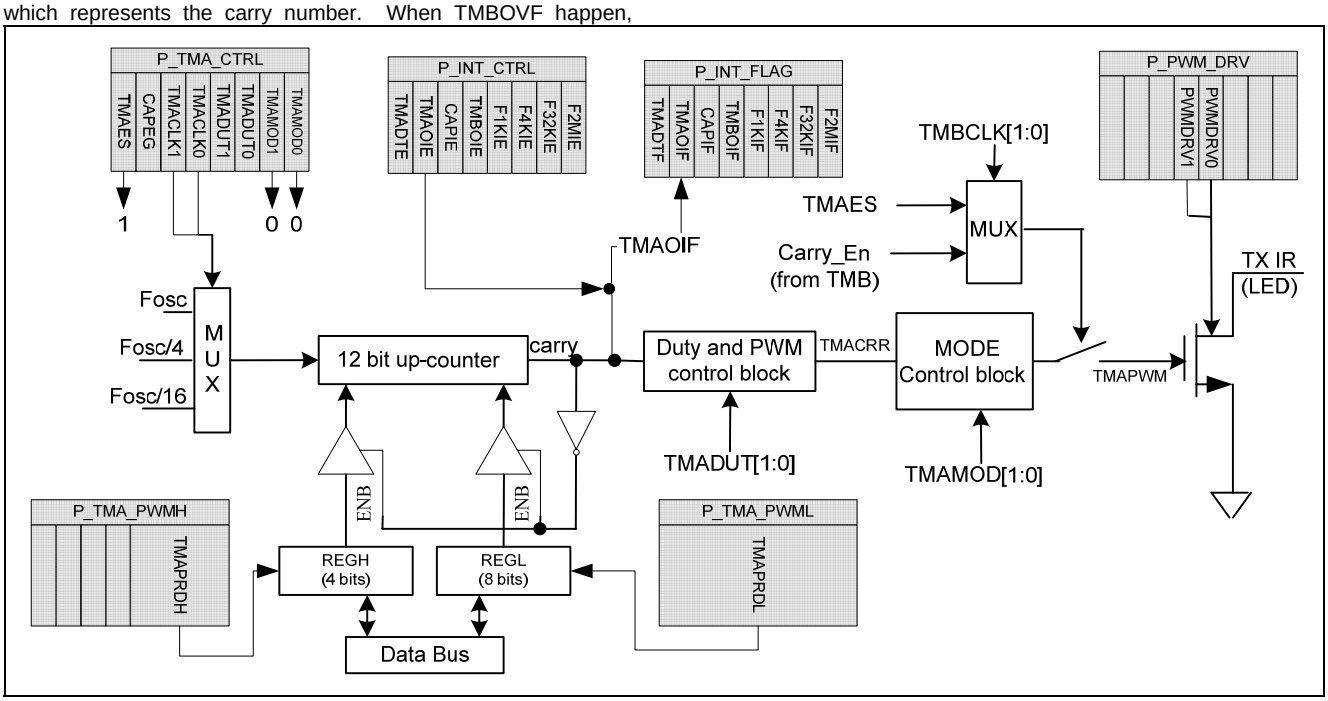


Figure 5-30 The Waveform of PWM with carrier signal mode (1/3 duty, on/off control by TMAES)

Another method to generate envelope PWM signal is that Timer A and Timer B must be used together. Timer A must generate carry clock at first, which is same as normal PWM generation. Then enable Timer B and select Timer A carrier signal as its input clock. And Timer B register must be written in the right data, which represents the carry number. When TMBOVF happen, another value must be written into Timer B register, which represents the no carry clock number. Envelop with carrier is on or off only when Timer B overflow events occur one by one. Then, the envelop PWM signal will be generated on LED port at last.



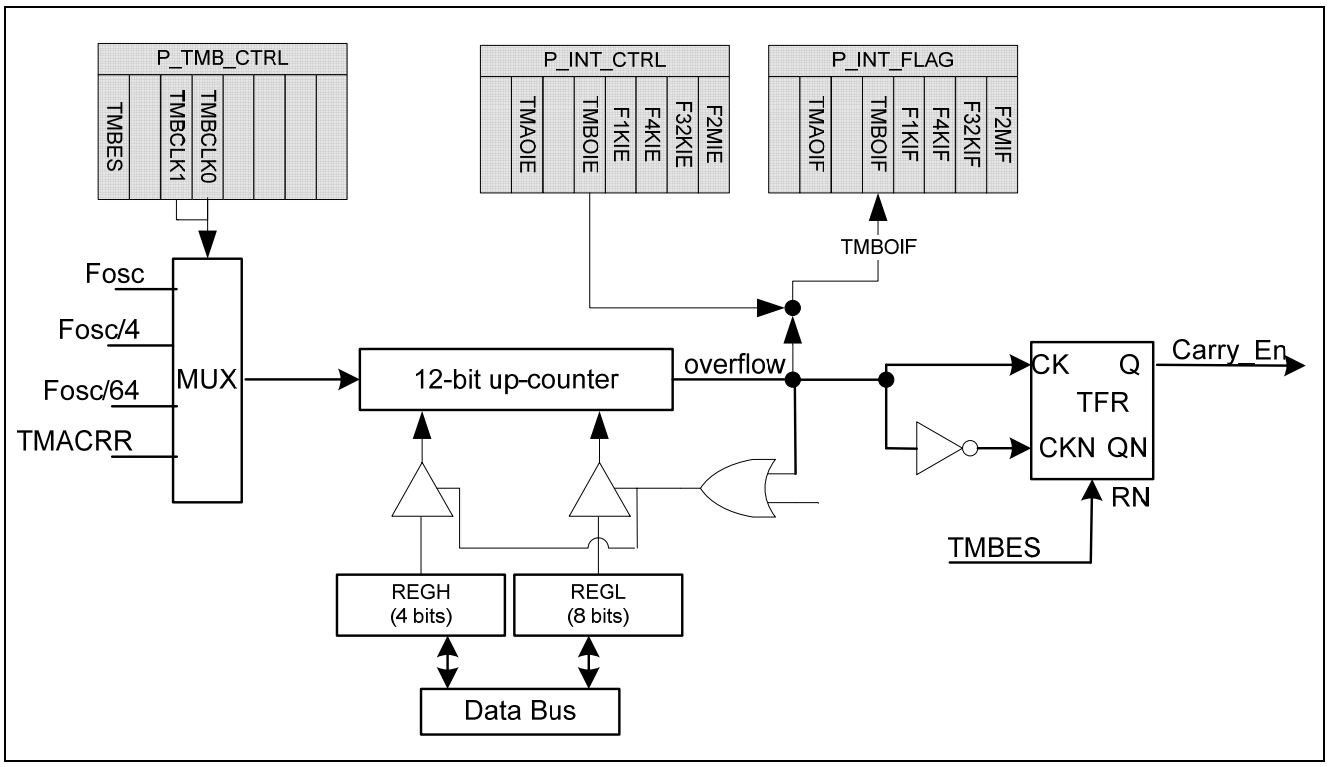


Figure 5-31 Envelope PWM Generated by Timer A & Timer B diagram

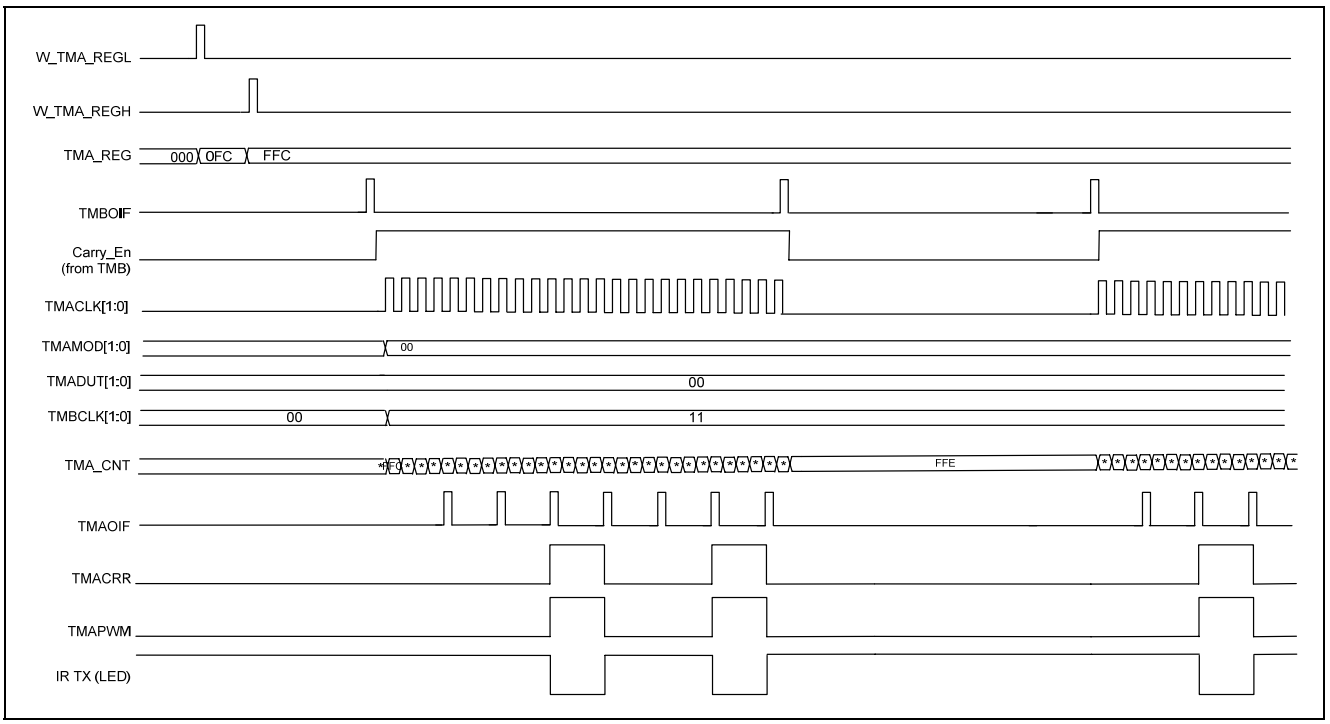


Figure 5-32 The Waveform of PWM with carrier signal mode (1/3 duty, on/off control by Timer B overflow events)

5.9.2. PWM without Carrier Signal Mode

PWM without carrier signal mode is used to generate envelop PWM signal without carrier signal. In this mode, IR TX (LED) pin just output high or low, and is controlled by Timer A's enable or disable control bit or Timer B's overflow events in turn. The same as PWM with carrier signal mode, the 12-bit timer is an up counter with input clock selectable (Fosc/1, Fosc/4, Fosc/16). When the

Timer A is started, the value of high-byte (low-nibble) Register and low-byte Register would firstly be loaded into the 12-bit counter and then the counter starts to count up from the loaded value. If an overflow occurs, the value of high-byte (low-nibble) register and low-byte register would be reloaded into the counter automatically and the counter starts to count up again. The internal carrier signal is generated but not be sent to IR TX pin.

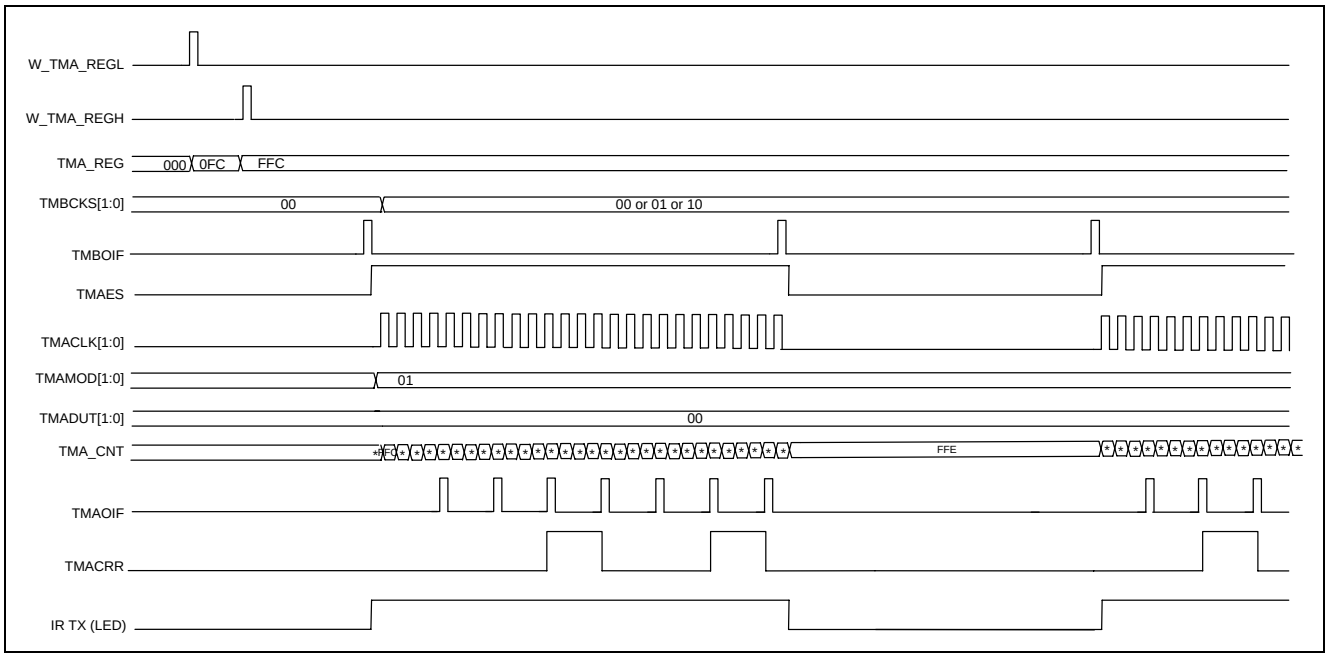


Figure 5-33 The Waveform of PWM without carrier signal mode (on/off control by TMAES)

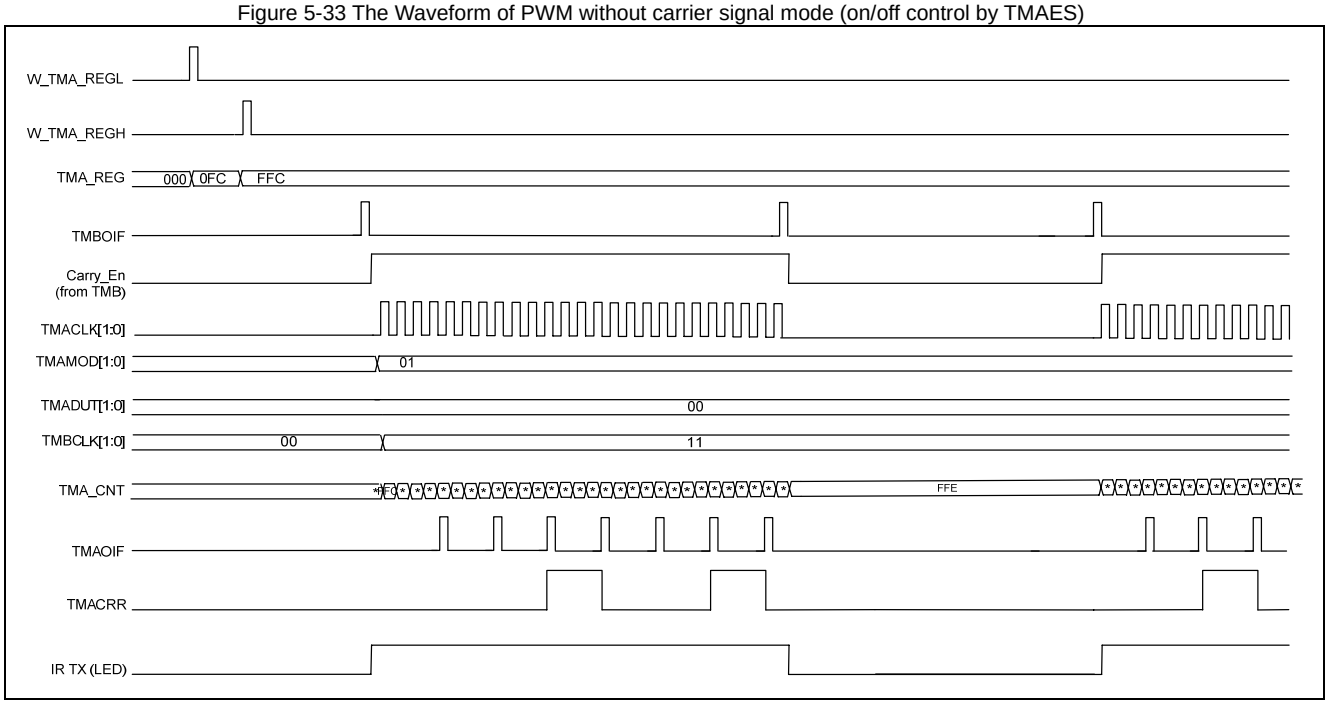


Figure 5-34 The Waveform of PWM without carrier signal mode (on/off control by Timer B overflow events)

5.9.3. Capture & Envelope Detect Mode

In IR learning function application, Timer A should be configured as capture mode for measuring the frequency of input signal from RX pin. In capture mode, the 12 bit timer is an up counter which counts from 00H with input clock selectable (Fosc/1, Fosc/4, Fosc/16). When rising or falling (selectable via P_TMA_CTRL) edge of RX is captured, the high-byte (low-nibble) value of the

counter would be loaded into register high and the low byte value of counter would be loaded into register low, at the same time, it generates an interrupt (CAPIF) and then the counter is cleared to 00H. When the timer overflows, the overflow interrupt (TMAOIF) occurs. The input carrier signal cycle time is recorded in register low (P_TMA_CAPL) and register high (P_TMA_CAPL). Of course, if the time data recorded is bigger than the biggest data, these two registers can be loaded, the overflows of the Timer A should be count inclusively.

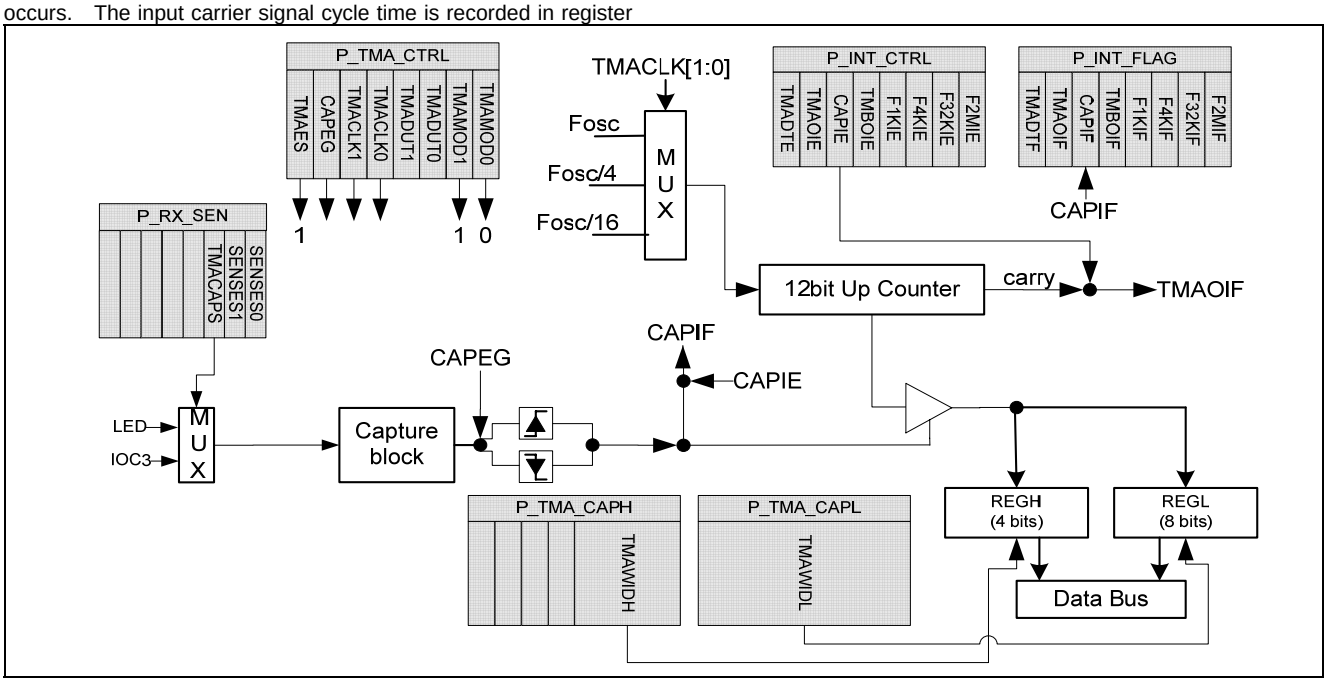


Figure 5-35 Timer A block diagram (Capture Mode)

After capture the carrier frequency, Timer A should be configured as envelope detect mode for measuring the envelope of input signal from RX pin. In order to detect the envelope, enter capture mode at first, and get the carrier frequency (named F_{CRR}). Then load the value (0xFFF-1.5* F_{CRR}) to Timer A counter register and enter envelope detect mode. If the first rising or falling-edge of carry wave arrives, envelope interrupt occurs (TMADTF=1) and ENVDET ($16.7) is set to '1', and the value (0xFFF-1.5* F_{CRR}) is loaded to counter automatically, and the counter starts to count. If next rising or falling-edge arrives, the value (0xFFF-1.5* F_{CRR}) will be reloaded into the counter, and ENVDET ($16.7) not changes its status (still equal '1'). However, if the next carry wave does not arrive on time (that's over 1.5* F_{CRR}), the Timer A overflow happens resulting in envelope interrupt occurrence, and make ENVDET ($16.7) change to "0". So checking ENVDET bit can know whether envelope exist or not.

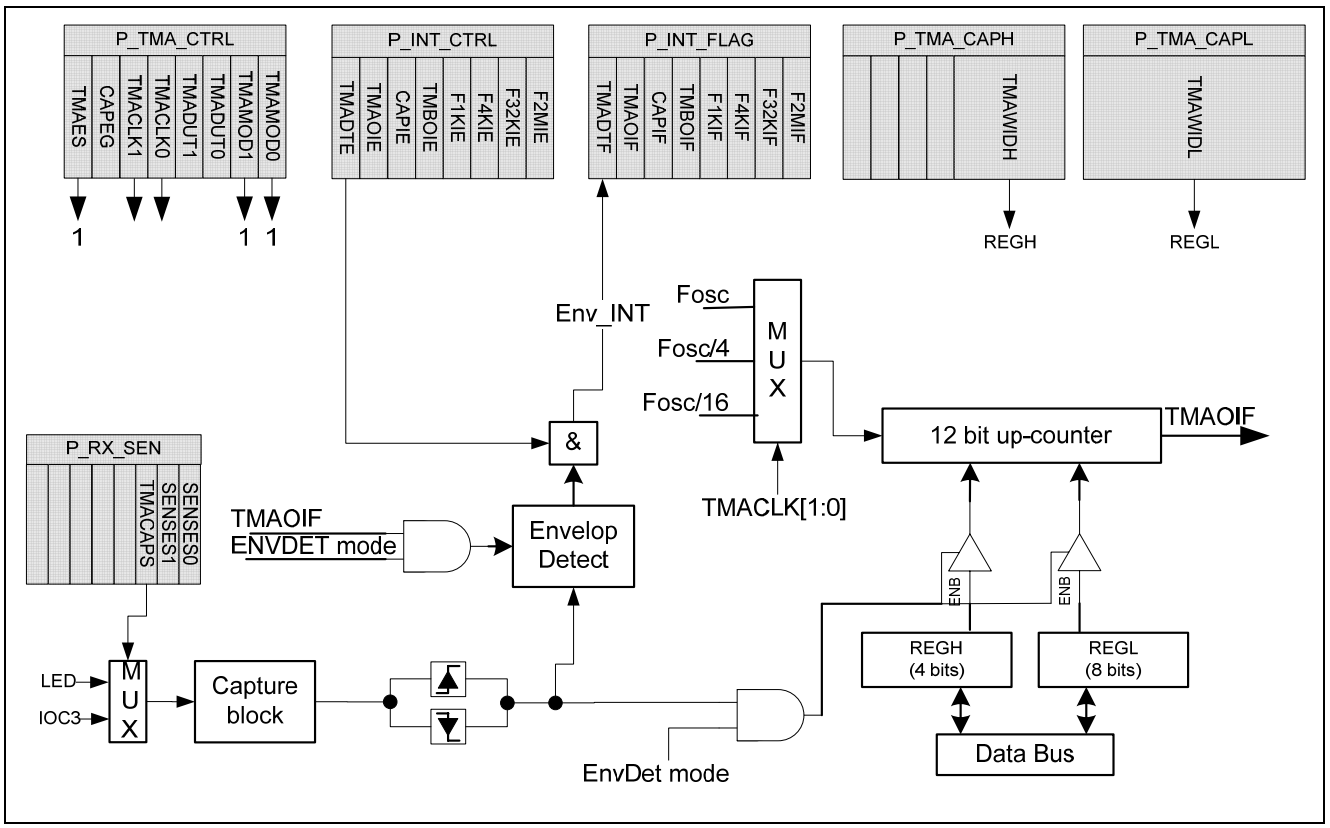


Figure 5-36 Timer A block diagram (Envelope detect Mode)

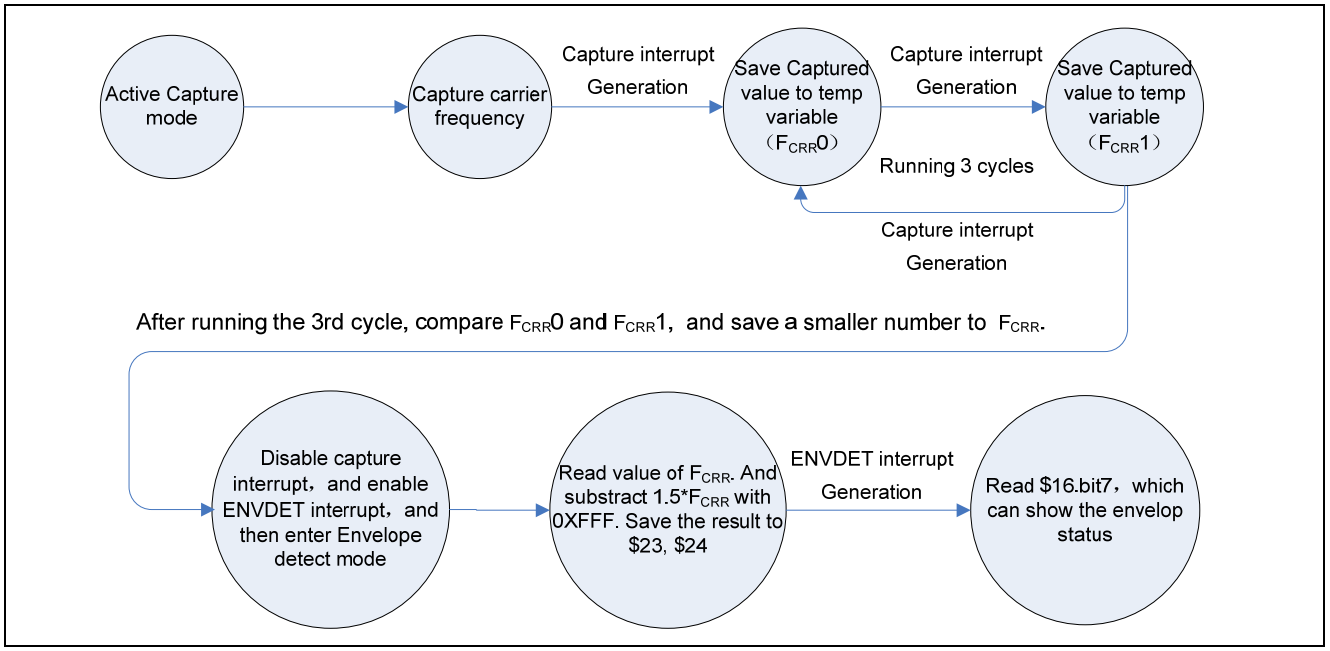


Figure 5-37 Timer A envelope detect flow

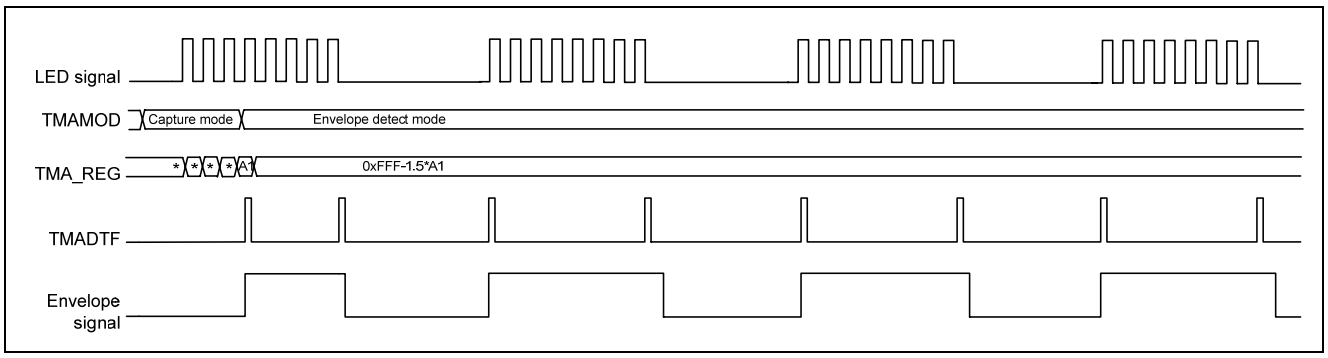


Figure 5-38 The waveform of envelope detect

Timer A Control Register (P_TMA_CTRL, $0021)

BIT	7	6	5	4	3	2	1	0
Name	TMAES	CAPEG	TMACLK1	TMACLK0	TMADUT1	TMADUT0	TMAMOD1	TMAMOD0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7 **TMAES:** Timer A enable/disable control.
0, disable; (C_TMAES_DIS)
1, enable. (C_TMAES_EN)

Bit 6 **CAPEG:** Timer A capture edge selection.
0, Rising; (C_TMACAP_RISE)
1, Falling. (C_TMACAP_FALL)

Bit [5:4] **TMACLK[1:0]:** Timer A clock source select bits
11 = Fosc/16 (C_TMACLK_16)
10 = Fosc/4 (C_TMACLK_4)
01 = Fosc (C_TMACLK_1)
00 = Fosc (C_TMACLK_1)

Bit [3:2] **TMADUT[1:0]:** Timer A PWM duty selection
00: 1/3 (C_TMADUT_3)
01: 1/4 (C_TMADUT_4)
10: 1/5 (C_TMADUT_5)
11: 1/6 (C_TMADUT_6)

Bit [1:0] **TMAMOD[1:0]:** Timer A mode setting
00: PWM (C_TMAMOD_WTC)
01: PWM1 (enter the mode, PWM out always high) (C_TMAMOD_WOC)
10: Capture (C_TMAMOD_CAP)
11: Envelop detect (C_TMAMOD_ENDE)

Timer A Count Low Byte Register (P_TMA_CNTL, $23) (R/W)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	TMACNTL7	TMACNTL6	TMACNTL5	TMACNTL4	TMACNTL3	TMACNTL2	TMACNTL1	TMACNTL0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [7:0] **TMACNTL**[7：0]: Timer A low byte 8-bit pre-value for the counter.
Read: Timer A Count Low Byte Value(R)
Write: Timer A Pre-Load Count Low Byte Value (W)

Timer A PWM Low Byte Period Register (P_TMA_PWML, $23) (R/W)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	TMAPRDL7	TMAPRDL6	TMAPRDL5	TMAPRDL4	TMAPRDL3	TMAPRDL2	TMAPRDL1	TMAPRDL0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [7:0] **TMAPRDL**[7：0]: Timer A low byte 8-bit period value for the PWM.
Read: Timer A Period Low Byte Value(R)
Write: Timer A Pre-Load Period Low Byte Value (W)

Timer A Capture Low Byte Width Register (P_TMA_CAPL, $23) (R/W)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	TMAWIDL7	TMAWIDL6	TMAWIDL5	TMAWIDL4	TMAWIDL3	TMAWIDL2	TMAWIDL1	TMAWIDL0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [7:0] **TMAWIDL**[7：0]: Timer A low byte 8-bit width value for the CAPTURE.

Read: Timer A Width Low Byte Value(R)

Write: Timer A Width Low Byte Value (W)

Timer A Count High Byte Register (P_TMA_CNTH, $24) (R/W)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	-	-	-	-	TMACNTH3	TMACNTH2	TMACNTH1	TMACNTH0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [7:4] Reserved

Bit [3:0] **TMACNTH**[3：0]: Timer A high byte 4-bit pre-value for the counter.

Read: Timer A Count High Byte Value (R)

Write: Timer A Pre-Load Count High Byte Value (W)

Timer A PWM High Byte Period Register (P_TMA_PWMH, $24) (R/W)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	-	-	-	-	TMAPRDH3	TMAPRDH2	TMAPRDH1	TMAPRDH0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [7:4] Reserved

Bit [3:0] **TMAPRDH**[3：0]: Timer A high byte 4-bit period value for the PWM.

Read: Timer A Period High Byte Value (R)

Write: Timer A Pre-Load Period High Byte Value (W)

Timer A Capture High Byte Width Register (P_TMA_CAPH, $24) (R/W)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	-	-	-	-	TMAWIDH3	TMAWIDH2	TMAWIDH1	TMAWIDH0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit [7:4] Reserved

Bit [3:0] **TMAWIDH**[3：0]: Timer A high byte 4-bit period value for the CAPTURE.

Read: Timer A Width High Byte Value (R)

Write: Timer A Width High Byte Value (W)

[Example] 5-16 Set Timer A as PWM with carrier signal mode.

```
LDA     #$FC                                    ; Before starting timer, set Timer A counter initial value first
STA     P_TMA_PWML                               ; set low 8-bit pre-value
LDA     #$0F
STA     P_TMA_PWMH                               ;set high 4-bit pre-value
LDA     #C_TMAES_EN + #C_TMACLK _4 +#C_TMADUT_3 + #C_TMAMOD_WTC
STA     P_TMA_CTRL                              ;Set clock source Fosc/4, 1/3duty, PWM with carrier signal mode
```

5.9.4. PWM Carrier Signal Algorithm

The frequency of PWM carrier signal (F_{PWM}) generated by Timer A depends on three factors.

- The initial value (V_{REG}=12-bit Preload PREIOD) is filled into high-byte (low-nibble) register (P_TMA_PWMH [3:0]) and low-byte register (P_TMA_PWML [7:0])
- The duty of the carrier signal (DUT= PWM DUTY).
- The frequency of timer A clock source (F_{timer})

V_{REG} = P_TMA_PWMH[4:0]+P_TMA_PWML[7:0]
DUT = one of (1/3, 1/4, 1/5, 1/6), defined by P_TMA_CTRL[3:2]
If
$F_{timer} = F_{osc}/1$, defined by P_TMA_CTRL[5:4]
Then
$V_{REG} = 4097 - F_{timer} / F_{PWM} * DUT$

For example, if user needs to generate 38 KHz 1/3 duty PWM carrier frequency and TIMER clock source is 4MHz/1 (system clock is 4MHz).

Condition: F_{PWM} = 38 KHz, F_{timer} =4MHz, DUT=1/3
V_{REG} = 4097 – (4M/38K)*1/3 = 4062 =FDEH

Then the result FDEH can be written into the PWM high/low register, and the 38 KHz PWM signal is generated.

V_{REG} = P_TMA_PWMH[4:0]+P_TMA_PWML[7:0]
DUT = one of (1/3, 1/4, 1/5, 1/6), defined by P_TMA_CTRL[3:2]
If
$F_{timer} = F_{osc}/4$, $F_{osc}/16$, defined by P_TMA_CTRL[5:4]
Then
$V_{REG} = 4096 - F_{timer} / F_{PWM} * DUT$

For example, if user need to generate 38 KHz 1/3 duty PWM carrier frequency, and system frequency is 4MHz. and $F_{OSC}/4$ is selected as timer clock.

Condition: F_{PWM} = 38 KHz, F_{timer} = 4MHz/4, DUT=1/3
V_{REG} = 4096 – (1M/38K)*1/3 = 4087 =FF7H

Then the result FF7H can be written into the PWM high/low register, and the 38 KHz PWM signal is generated.

[Example] 5-17 Set Timer A as PWM with carrier signal mode and the carrier frequency is 38 KHz with 1/3 duty (clock source=Fosc/1).

```
LDA     #$DE                                        ; Before starting timer, set Timer A counter initial value first
STA     P_TMA_ PWML                                 ; set low 8-bit pre-value
LDA     #$0F
STA     P_TMA_ PWMH                                 ;set high 4-bit pre-value
LDA     #C_TMAES_EN + #C_TMACLK _1 +#C_TMADUT_3 + #C_TMAMOD_WTC
STA     P_TMA_CTRL                                  ;Set clock source Fosc/1, 1/3duty, PWM with carrier signal mode
```

[Example] 5-18 Set Timer A as PWM with carrier signal mode and the carrier frequency is 38 KHz with 1/3 duty (clock source=Fosc/4).

```
LDA     #$F7                                        ; Before starting timer, set Timer A counter initial value first
STA     P_TMA_ PWML                                 ; set low 8-bit pre-value
LDA     #$0F
STA     P_TMA_ PWMH                                 ;set high 4-bit pre-value
LDA     #C_TMAES_EN + #C_TMACLK _4 +#C_TMADUT_3 + #C_TMAMOD_WTC
STA     P_TMA_CTRL                                  ;Set clock source Fosc/4, 1/3 duty, PWM with carrier signal mode
```

5.10. Timer B

The Timer B is special for envelope signal generation in IR controller application. The 12-bit timer is an up counter with input clock selectable (Fosc/1, Fosc/4, Fosc/64, TMACAR) via configuring the control register P_TMB_CTRL [5:4] (TMBCLK [1:0]). And the value of low-byte register (P_TMB_CNTL) and high-byte (low-nibble) register (P_TMB_CNTH) would be reloaded into the 12-bit up counter and an interrupt (TMBOIF) would be generated whenever an overflow occurs. The interrupt frequency can be freely selected by choosing different clock source and configuring the low-byte register and high-byte (low-nibble) register with different values.

The Timer B module has the following features:

- Readable and writable
- Clock source selectable
- Interrupt-on-overflow from #$FFF to #$000

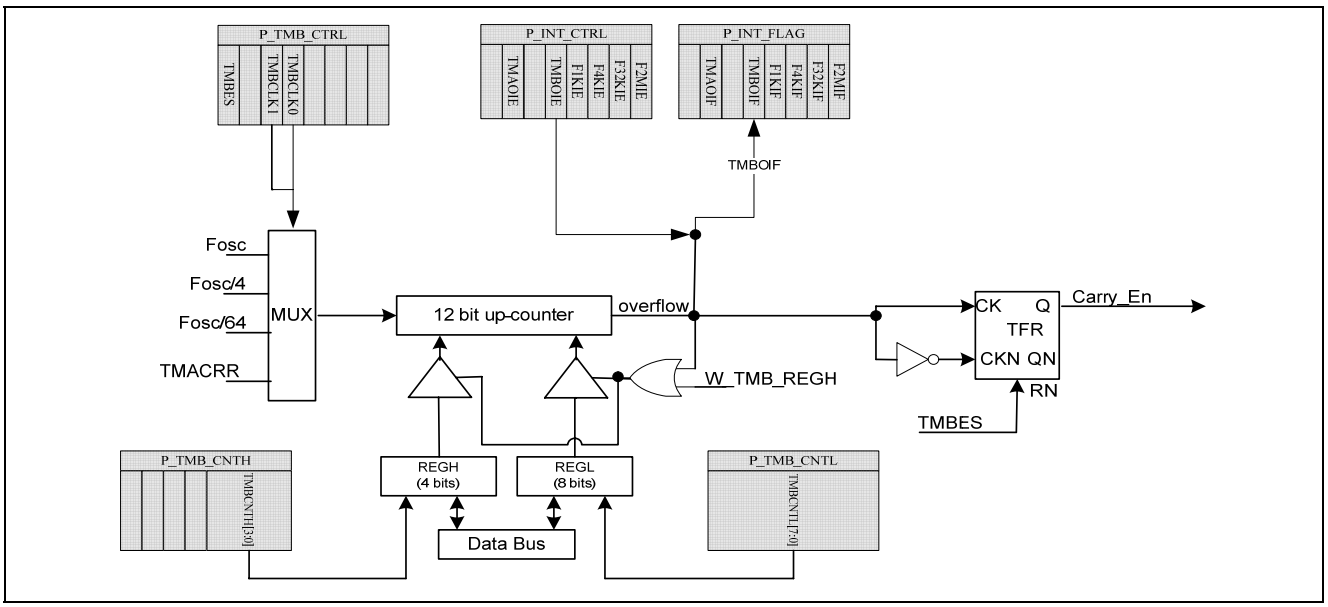


Figure 5-39 Timer B block diagram

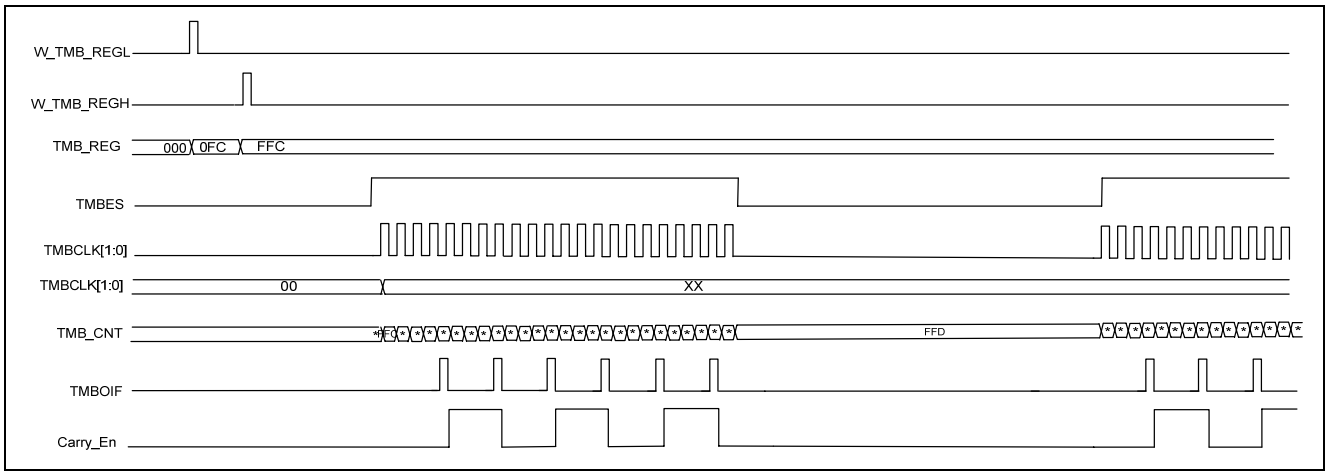


Figure 5-40 The Waveform of Timer B

Timer B Control Register (P_TMB_CTRL, $0022)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	TMBES	-	TMBCLK1	TMBCLK0	-	-	-	-
ACCESS	R/W	-	R/W	R/W	-	-	-	-
DEFAULT	0	-	0	0	-	-	-	-

Bit [7] **TMBES**: Timer B enable/disable control selected bit.

0 = disable (C_TMBES_DIS)

1 = enable (C_TMBES_EN)

Bit [6] Reserved

Bit [5:4] **TMBCLK[1：0]**: Timer B clock source selected bits

00 = Fosc (C_TMBCLK_1)

01 = Fosc/4 (C_TMBCLK_4)

10 = Fosc/64 (C_TMBCLK_64)

11 = TMACRR (C_TMBCLK_TMACRR)

Bit [3:0] Reserved

Timer B Low 8-bit Data Register (P_TMB_CNTL, $0025)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	TMBCNTL7	TMBCNTL6	TMBCNTL5	TMBCNTL4	TMBCNTL3	TMBCNTL2	TMBCNTL1	TMBCNTL0
ACCESS	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

Bit [7:0] **TMBCNTL**[7：0]: Timer B low byte 8-bit pre-value for the counter.

Read: Timer B Count Low Byte Value (R)

Write: Timer B Pre-Load Count Low Byte Value (W)

Timer B High 4-bit Data Register (P_TMB_CNTH, $0026)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NAME	-	-	-	-	TMBCNTH3	TMBCNTH2	TMBCNTH1	TMBCNTH0
ACCESS	-	-	-	-	R/W	R/W	R/W	R/W
DEFAULT	-	-	-	-	0	0	0	0

Bit [7:4] Reserved

Bit [3:0] **TMBCNTH**[3：0]: Timer B High byte 4-bit pre-value for the counter.

Read: Timer B Count High Byte Value (R)

Write: Timer B Pre-Load Count High Byte Value (W)

[Example] 5-19 Set Timer B selects timer A carrier signal as counter clock.

```
LDA     #$FC                            ; Before starting timer, set Timer B counter initial value first
STA     P_TMB_CNTL                      ; set low 8-bit pre-value
LDA     #$0F
STA     P_TMB_CNTH                      ; set high 4-bit pre-value
LDA     #C_TMBES_EN + #C_TMBCLK_TMACRR
STA     P_TMB_CTRL                      ;Set clock source for TMA_Carrier
```

5.11. IR Transfer/Receiver Module

RXTX is an analog block of GPM6P1129A/C1067A/P1065A/ P1033A/P1017A/P1015A, which can drive LED by TX, and can translate the IR LED sense current to digital signal. RX_SEN register can control this block. User can adjust PWM output driving capability by setting value of PWMDRV [1:0], and adjust the sensitivity of Rx block by SENSE [1:0]. Meanwhile, by setting the value of TACAPS to '1', capture signal can be input from PC3 pin.

TMAPWM signal (as showed in Figure 5-41) controls LED driver MOS. When in PWM mode, Timer A can generate PWM signal, and the PWM duty, frequency, on/off switch can be accuracy controlled by Timer A. The Envelope PWM signal can be generated by Timer A & Timer B. And it has been illustrated in timer instruction. RX block translates sense current to digital signal RXOUT, and RXOUT is sent to Timer A block, which can get the carrier frequency in capture mode and get envelope waveform in envelope detect mode.

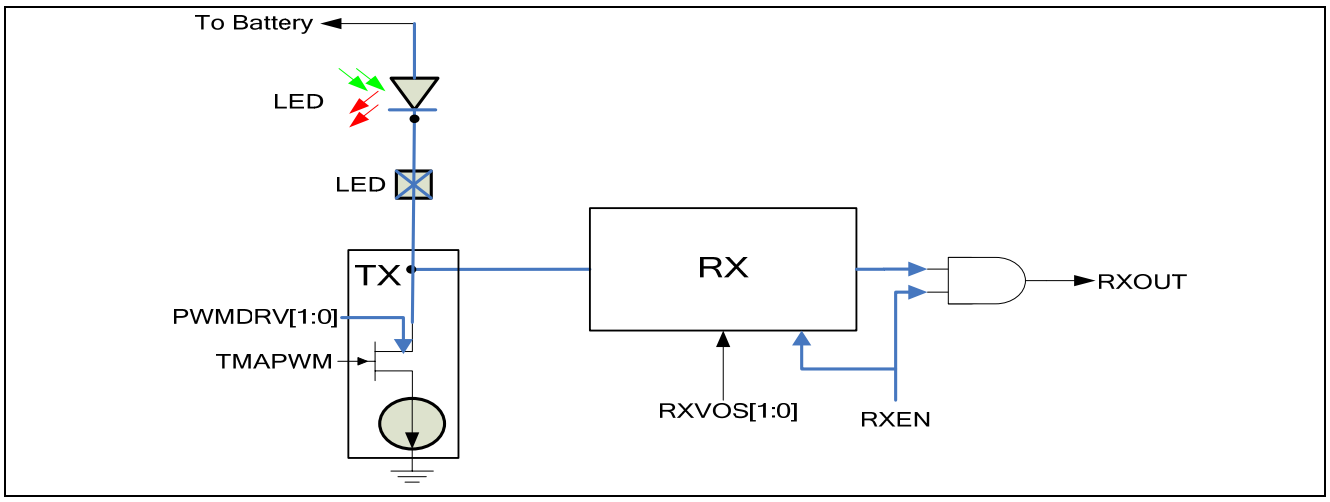


Figure 5-41 RXTX module diagram

Timer A PWM Drive Register (P_PWM_DRV, $11) (W)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	-	-	-	PWMDRVS1	PWMDRVS0	-	-	-
Access	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

GPM6P1129A/C1067A/P1065A/P1033A

Bit [7:5] Reserved

Bit [4:3] **PWMDRVS[1:0] :** PWM driving current selected bits.

00 = PWM 1/4 driving current (C_PWMDRV_1)

01 = PWM 2/4 driving current (C_PWMDRV_2)

10 = PWM 3/4 driving current (C_PWMDRV_3)

11 = PWM full driving current (C_PWMDRV_4)

Bit [2:0] Please refer to P_RX_SEN register.

GPM6P1017A /P1015A

Bit [7:4] Reserved

Bit [3] **PWMDRVS[0] :** PWM driving current selected bits.

0 = PWM 1/1 driving current (C_PWMDRV_1)

1 = PWM 2/2 driving current (C_PWMDRV_2)

Bit [2:0] Please refer to P_RX_SEN register.

Timer A Sense Control Register (P_RX_SEN, $11) (W)

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	-	-	-	-	-	TMACAPS	SENSES1	SENSES0
Access	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

Bit [7:5] Reserved

Bit [4:3] Please refer to P_PWM_DRV register.

Bit [2] **TMACAPS:** Timer A capture input selected bit.

0 = LED PAD (C_RX_CAP)

1 = IOC3 (C_RX_IOC3)

Bit [1:0] **SENSES[1:0]:** RX SENSE selected bits.

00 → 01 → 10 → 11 sensitivity MAX → Min

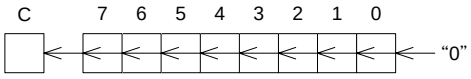
00 = RX SENSE Level 1 (C_RX_SENSE_1)
sense current >=2uA

01 = RX SENSE Level 2 (C_RX_SENSE_2)
sense current >=5uA

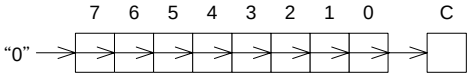
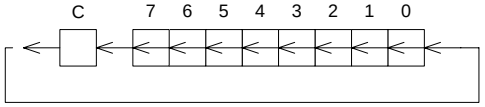
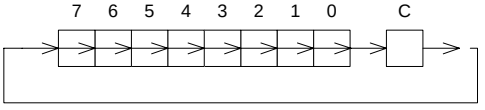
10 = RX SENSE Level 3 (C_RX_SENSE_3)
sense current >=8uA

11 = RX SENSE Level 4 (C_RX_SENSE_4)
sense current >=11uA

5.12. Alphabetical List of Instruction Set

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NV-BDIZC
1.	ADC #dd	69	2	2	Add to accumulator with carry. A ← (A) + (M) + C If D-flag set to 1, the ADC performs decimal operation.	NV--D-ZC
2.	ADC aa	65	2	3		
3.	ADC aa, X	75	2	4		
4.	ADC aaaa	6D	3	4		
5.	ADC aaaa,X	7D	3	4(A)		
6.	ADC aaaa,Y	79	3	4(A)		
7.	ADC (aa,X)	61	2	6		
8.	ADC (aa), Y	71	2	5(A)		
9.	AND #dd	29	2	2	And memory data with accumulator. A ← (A) ^ (M)	N-----Z-
10.	AND aa	25	2	3		
11.	AND aa, X	35	2	4		
12.	AND aaaa	2D	3	4		
13.	AND aaaa,X	3D	3	4(A)		
14.	AND aaaa,Y	39	3	4(A)		
15.	AND (aa,X)	21	2	6		
16.	AND (aa), Y	31	2	5(A)		
17.	ASL A	0A	1	2	Arithmetic Shift Left 	N-----ZC
18.	ASL aa	06	2	5		
19.	ASL aa,X	16	2	6		
20.	ASL aaaa	0E	3	6		
21.	ASL aaaa,X	1E	3	6(A)		
22.	BCC aa	90	2	2(C)	Branch if carry bit clear If (C) = 0, then pc ← (pc) + ??	--------
23.	BCS aa	B0	2	2(C)	Branch if carry bit set If (C) = 1, then pc ← (pc) + ??	--------
24.	BEQ aa	F0	2	2(C)	Branch if equal If (Z) = 1, then pc ← (pc) + ??	--------
25.	BIT aa	24	2	3	Test bit in memory with accumulator Z ← (A) ^ (M), N ← (M_7), V ← (M_6)	NV----Z-
26.	BIT aaaa	2C	3	4		
27.	BMI aa	30	2	2(C)	Branch if minus If (N) = 1, then pc ← (pc) + ??	--------
28.	BNE aa	D0	2	2(C)	Branch if not equal If (Z) = 0, then pc ← (pc) + ??	--------
29.	BPL aa	10	2	2(C)	Branch if plus If (N) = 0, then pc ← (pc) + ??	--------
30.	BRK	00	1	7	Software interrupt If (B) = 1, then pc ← (pc) + 1	---B-I--
31.	BVC aa	50	2	2(C)	Branch if overflow bit clear If (V) = 0, then pc ← (pc) + ??	--------
32.	BVS aa	70	2	2(C)	Branch if overflow bit set If (V) = 1, then pc ← (pc) + ??	--------
33.	CLC	18	1	2	Clear C-flag：C ← "0"	-------0
34.	CLD	D8	1	2	Clear D-flag：D ← "0"	----0---

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NV-BDIZC
35.	CLI	58	1	2	Clear I-flag: I ← "0"	-----0--
36.	CLV	B8	1	2	Clear V-flag: V ← "0"	-0------
37.	CMP #dd	C9	2	2	Compare memory data with accumulator,	N-----ZC
38.	CMP aa	C5	2	3	(A) – (M)	
39.	CMP aa, X	D5	2	4		
40.	CMP aaaa	CD	3	4		
41.	CMP aaaa,X	DD	3	4(A)		
42.	CMP aaaa,Y	D9	3	4(A)		
43.	CMP (aa,X)	C1	2	6		
44.	CMP (aa), Y	D1	2	5(A)		
45.	CPX #dd	E0	2	2	Compare memory data with X-register,	N-----ZC
46.	CPX aa	E4	2	3	(X) – (M)	
47.	CPX aaaa	EC	3	4		
48.	CPY #dd	C0	2	2	Compare memory data with Y-register,	N-----ZC
49.	CPY aa	C4	2	3	(Y) – (M)	
50.	CPY aaaa	CC	3	4		
51.	DEC aa	C6	2	5	Decrement	N-----Z-
52.	DEC aa, X	D6	2	6	M ← (M) - 1	
53.	DEC aaaa	CE	3	6		
54.	DEC aaaa,X	DE	3	7		
55.	DEX	CA	1	2		
56.	DEY	88	1	2		
57.	EOR #dd	49	2	2	Exclusive OR	N-----Z-
58.	EOR aa	45	2	3	A ← (A) ⊕ (M)	
59.	EOR aa, X	55	2	4		
60.	EOR aaaa	4D	3	4		
61.	EOR aaaa,X	5D	3	4(A)		
62.	EOR aaaa,Y	59	3	4(A)		
63.	EOR (aa,X)	41	2	6		
64.	EOR (aa), Y	51	2	5(A)		
65.	INC aa	E6	2	5	Increment	N-----Z-
66.	INC aa, X	F6	2	6	M ← (M) + 1	
67.	INC aaaa	EE	3	6		
68.	INC aaaa,X	FE	3	7		
69.	INX	E8	1	2	X ← X + 1	N-----Z-
70.	INY	C8	1	2	Y ← Y + 1	N-----Z-
71.	JMP aaaa	4C	3	3	Unconditional jump	--------
72.	JMP (aaaa)	6C	3	6	Pc ← jump address	
73.	JSR aaaa	20	3	6	Jump to subroutine (sp) ← (pc_H), sp ← sp – 1, (sp) ← (pc_L), sp ← sp – 1, pc ← aaaa	--------
74.	LDA #dd	A9	2	2	Load accumulator	N-----Z-
75.	LDA aa	A5	2	3	A ← (M)	

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NV-BDIZC
76.	LDA aa, X	B5	2	4		
77.	LDA aaaa	AD	3	4		
78.	LDA aaaa,X	BD	3	4(A)		
79.	LDA aaaa,Y	B9	3	4(A)		
80.	LDA (aa,X)	A1	2	6		
81.	LDA (aa), Y	B1	2	5(A)		
82.	LDX #dd	A2	2	2	Load X-register X ← (M)	N-----Z-
83.	LDX aa	A6	2	3		
84.	LDX aa, Y	B6	2	4		
85.	LDX aaaa	AE	3	4		
86.	LDX aaaa,Y	BE	3	4(A)		
87.	LDY #dd	A0	2	2	Load Y-register Y ← (M)	N-----Z-
88.	LDY aa	A4	2	3		
89.	LDY aa, X	B4	2	4		
90.	LDY aaaa	AC	3	4		
91.	LDY aaaa,X	BC	3	4(A)		
92.	LSR A	4A	1	2	Logical shift right 	N-----ZC
93.	LSR aa	46	2	5		
94.	LSR aa, X	56	2	6		
95.	LSR aaaa	4E	3	6		
96.	LSR aaaa,X	5E	3	6(A)		
97.	NOP	EA	1	2	No operation	--------
98.	ORA #dd	09	2	2	Logical OR A ← (A) v (M)	N-----Z-
99.	ORA aa	05	2	3		
100.	ORA aa, X	15	2	4		
101.	ORA aaaa	0D	3	4		
102.	ORA aaaa,X	1D	3	4(A)		
103.	ORA aaaa,Y	19	3	4(A)		
104.	ORA (aa,X)	01	2	6		
105.	ORA (aa), Y	11	2	5(A)		
106.	PHA	48	1	3	(sp) ← A, sp ← sp - 1	--------
107.	PHP	08	1	3	(sp) ← P status, sp ← sp -1	
108.	PLA	68	1	4	sp ← sp +1, A ← (sp)	--------
109.	PLP	28	1	4	Sp ← sp +1, P status ← (sp)	restored
110.	ROL A	2A	1	2	Rotate left through carry 	N-----ZC
111.	ROL aa	26	2	5		
112.	ROL aa, X	36	2	6		
113.	ROL aaaa	2E	3	6		
114.	ROL aaaa,X	3E	3	6(A)		
115.	ROR A	6A	1	2	Rotate right through carry 	N-----ZC
116.	ROR aa	66	2	5		
117.	ROR aa, X	76	2	6		
118.	ROR aaaa	6E	3	6		

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NV-BDIZC
119.	ROR aaaa,X	7E	3	6(A)		
120.	RTI	40	1	6	Return from interrupt Sp ← sp + 1, P status ← (sp), sp ← sp + 1, pc_L ← (sp), sp ← sp +1, pc_H ← (sp)	restored
121.	RTS	60	1	6	Return from subroutine Sp ← sp + 1, pc_L ← (sp), sp ← sp +1, pc_H ← (sp)	--------
122.	SBC #dd	E9	2	2	Subtract with carry A ← (A) – (M) - ~(C)	NV----ZC
123.	SBC aa	E5	2	3		
124.	SBC aa, X	F5	2	4		
125.	SBC aaaa	ED	3	4		
126.	SBC aaaa,X	FD	3	4(A)		
127.	SBC aaaa,Y	F9	3	4(A)		
128.	SBC (aa,X)	E1	2	6		
129.	SBC (aa), Y	F1	2	5(A)		
130.	SEC	38	1	2	Set C-flag: C ← “1”	-------1
131.	SED	F8	1	2	Set D-flag: D ← “1”	----1---
132.	SEI	78	1	2	Set I-flag: I ← “1”	-----1--
133.	STA aa	85	2	3	Store accumulator in memory (M) ← A	--------
134.	STA aa, X	95	2	4		
135.	STA aaaa	8D	3	4		
136.	STA aaaa,X	9D	3	5		
137.	STA aaaa,Y	99	3	5		
138.	STA (aa,X)	81	2	6		
139.	STA (aa), Y	91	2	6		
140.	STX aa	86	2	3	Store X-register in memory (M) ← X	--------
141.	STX aa, Y	96	2	4		
142.	STX aaaa	8E	3	4		
143.	STY aa	84	2	3	Store Y-register in memory (M) ← Y	--------
144.	STY aa, X	94	2	4		
145.	STY aaaa	8C	3	4		
146.	TAX	AA	1	2	Transfer accumulator to X-register: X ← A	N-----Z-
147.	TAY	A8	1	2	Transfer accumulator to Y-register: Y ← A	N-----Z-
148.	TSX	BA	1	2	Transfer sp to X-register: X ← sp	N-----Z-
149.	TXA	8A	1	2	Transfer X-register to accumulator: A ← X	N-----Z-
150.	TXS	9A	1	2	Transfer X-register to sp: sp ← X	N-----Z-
151.	TYA	98	1	2	Transfer Y-register to accumulator: A ← Y	N-----Z-

Notes:

1. Cycle (A): Cycle+1 when cross a boundary.
2. Cycle(C): Cycle+1 if the branch condition is true; Cycle+2 if the branch condition is true and cross a boundary.

6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 5.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-50℃ to +150℃
Average PWM MAX Driving Current	I_{LEDM}	150mA
VDD Total MAX Current	I_{VDDM}	100mA
VSS Total MAX Current	I_{VSSM}	120mA

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. AC Characteristics (T_A = 25℃)

Characteristics	Limit			Unit	Test Condition
	Min.	Typ.	Max.		
OSC Accuracy @ Freq=4MHz					
OSC Variation	-3.0	±1.5	3.0	%	VDD = 2.2V - 3.6V, T_A =25°C

6.3. GPM6P1129A/P1065A/P1033A DC Characteristics (VDD = 3.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	4.0	8.0	mA	F_{CPU} = 8.0MHz @ 3.6V, no load
Standby Current	I_{STBY}	-	-	1.0	uA	VDD = 3.6V
Input High Level	V_{IH}	0.7VDD	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.3VDD	V	VDD = 3.0V
Output High Level PB, PC, PD	V_{OH}	0.8VDD	-	-	V	VDD = 3.0V I_{OH} = -6mA
Output Low Level PB, PC, PD	V_{OL}	-	-	0.2VDD	V	VDD = 3.0V I_{OL} = 16mA
Input Pull High Resistor PA, PB, PC, PD	R_H	120	160	200	Kohm	Pull High VDD = 3.0V
Input Pull Low Resistor PA, PB, PC, PD	R_L	120	160	200	Kohm	Pull Low VDD = 3.0V
PWM Driver Current (driver MOS all on for LED pin)	I_{PWM}	200	-	-	mA	VDD = 3.0V, V_{LED} =3.0V
LVR Active Voltage	V_{LVR}	2.1	2.25	2.4	V	-

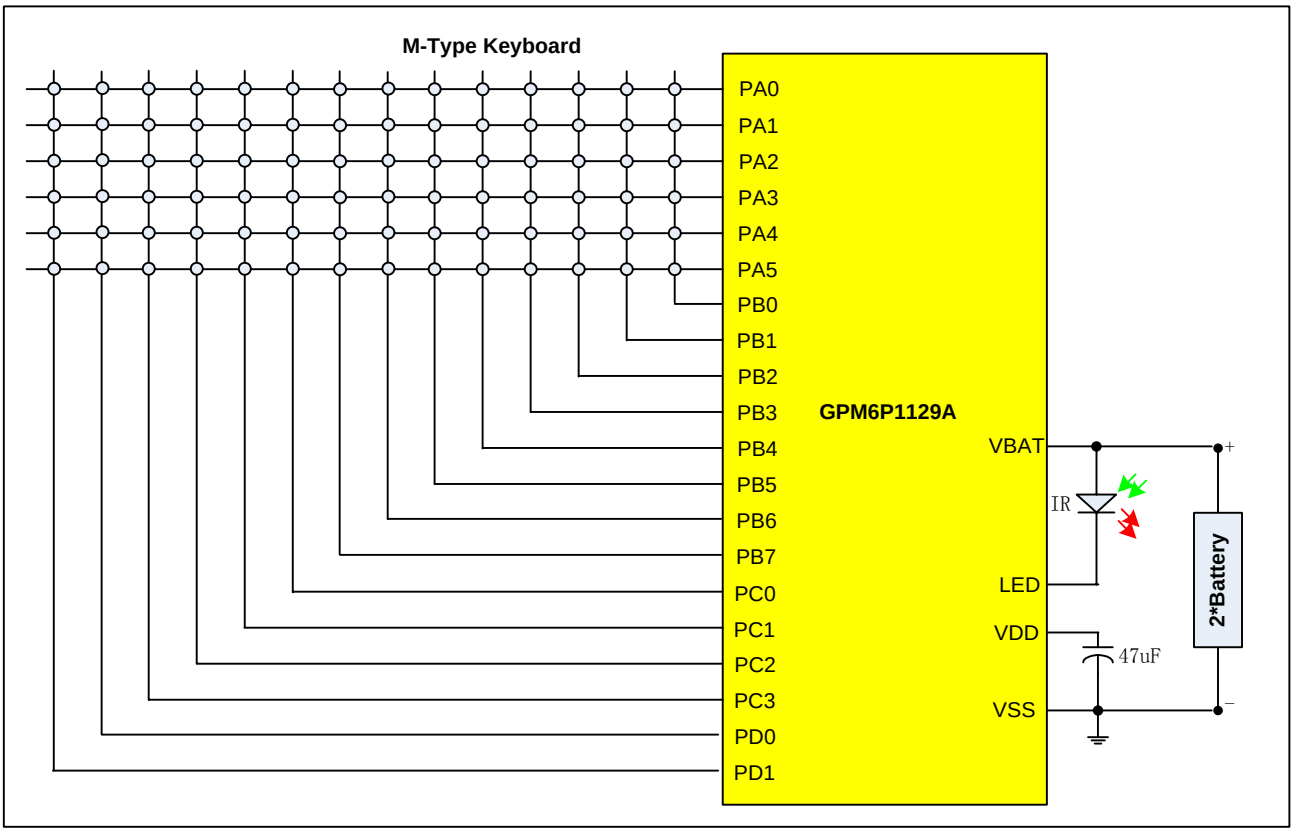
6.4. GPM6C1067A/P1017A/P1015A DC Characteristics (VDD = 3.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage1	VDD	2.0	-	3.6	V	F_{CPU} = 4.0MHz, For 2-battery
Operating Voltage1	VDD	2.4	-	3.6	V	F_{CPU} = 8.0MHz, For 2-battery
Operating Current	I_{OP}	-	4.0	8.0	mA	F_{CPU} = 8.0MHz @ 3.6V, no load

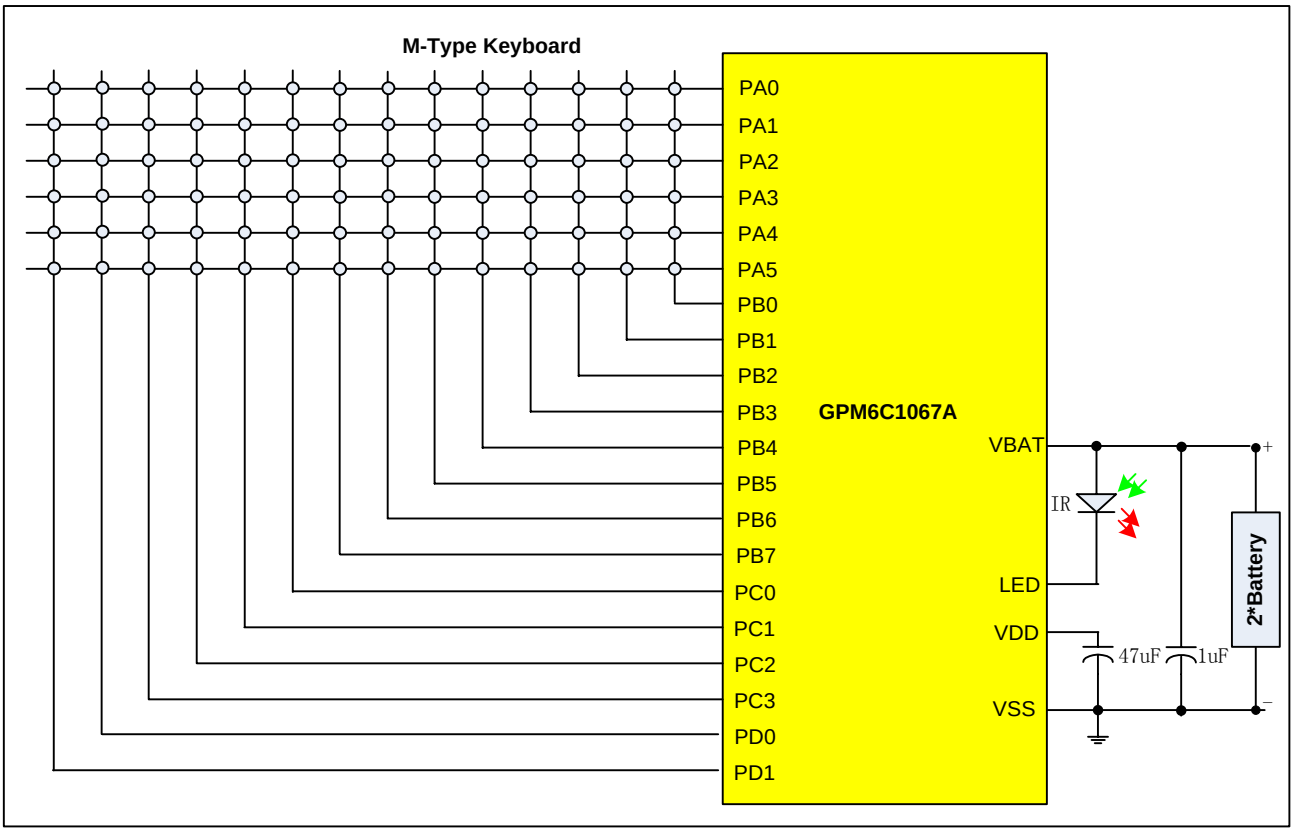
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
M-Type Key Standby Current	I_{MSTBY}	-	-	1.0	uA	VDD = 3.6V
T-Type Key Standby Current	I_{TSTBY}	-	-	2.0	uA	VDD = 3.6V, Key loading≤ 50pF
Input High Level	V_{IH}	0.7VDD	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.3VDD	V	VDD = 3.0V
Output High Level PB, PC, PD	V_{OH}	0.8VDD	-	-	V	VDD = 3.0V I_{OH} = -6mA
Output Low Level PB, PC, PD	V_{OL}	-	-	0.2VDD	V	VDD = 3.0V I_{OL} = 16mA
Input Pull High Resistor PA, PB, PC, PD	R_H	30	50	70	Kohm	Pull High VDD = 3.0V
Input Pull Low Resistor PA, PB, PC, PD	R_L	30	50	70	Kohm	Pull Low VDD = 3.0V
Max PWM Driving Current	I_{PWM}	200	-	-	mA	VDD = 3.0V,V_{RMT} =3.0V PWMDRV0=1
LVR Active Voltage (by option)	V_{LVR}	1.7	1.85	2.0	V	LVRVSEL=0
		2.1	2.25	2.4	V	LVRVSEL=1

7. APPLICATION CIRCUITS

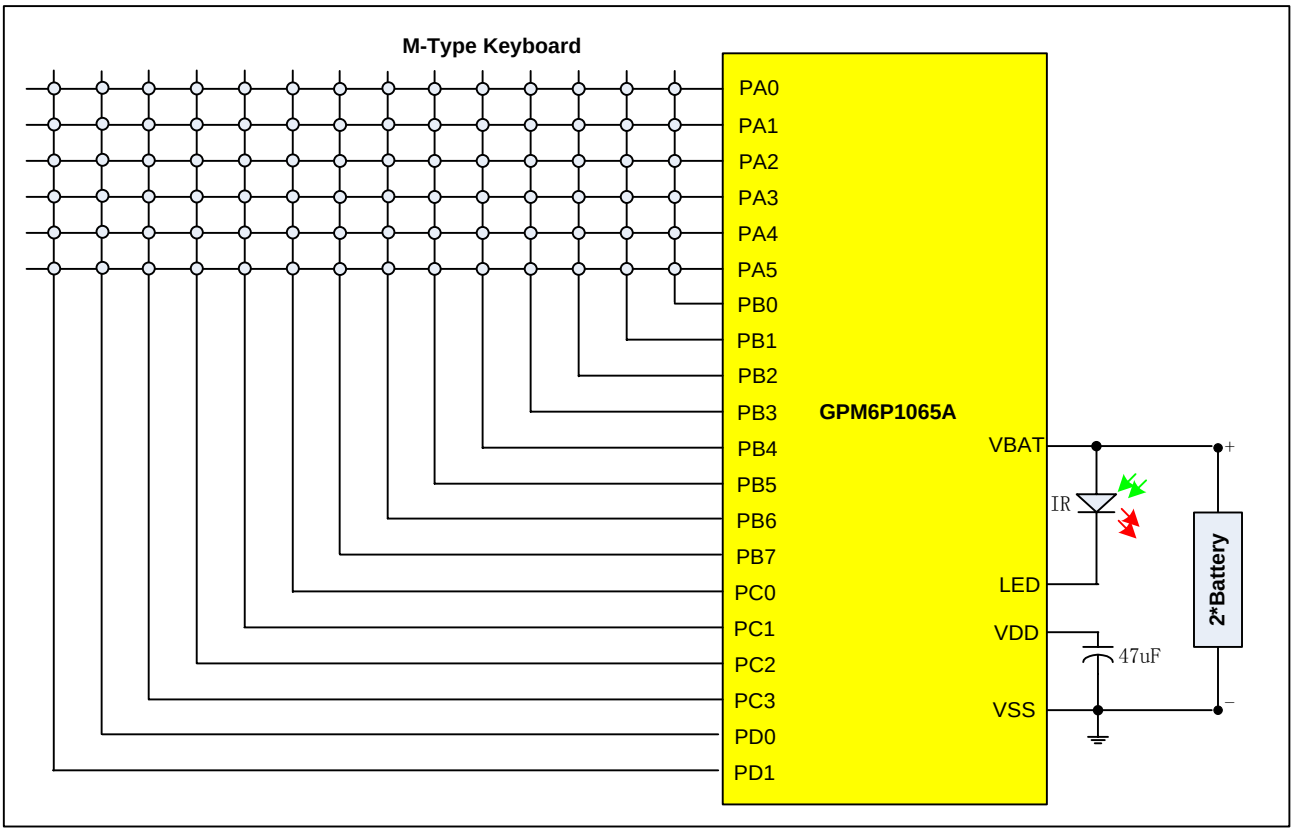
7.1. GPM6P1129A Application Circuit



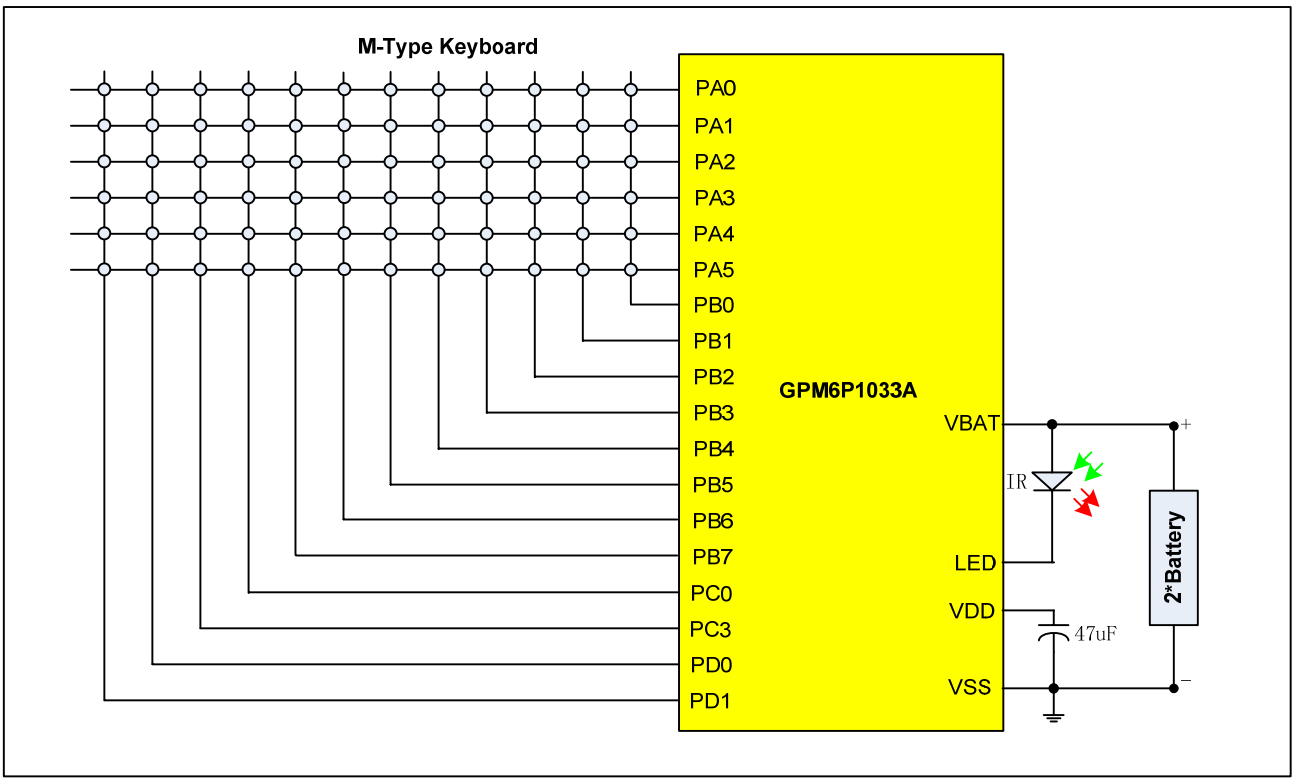
7.2. GPM6C1067A Application Circuit



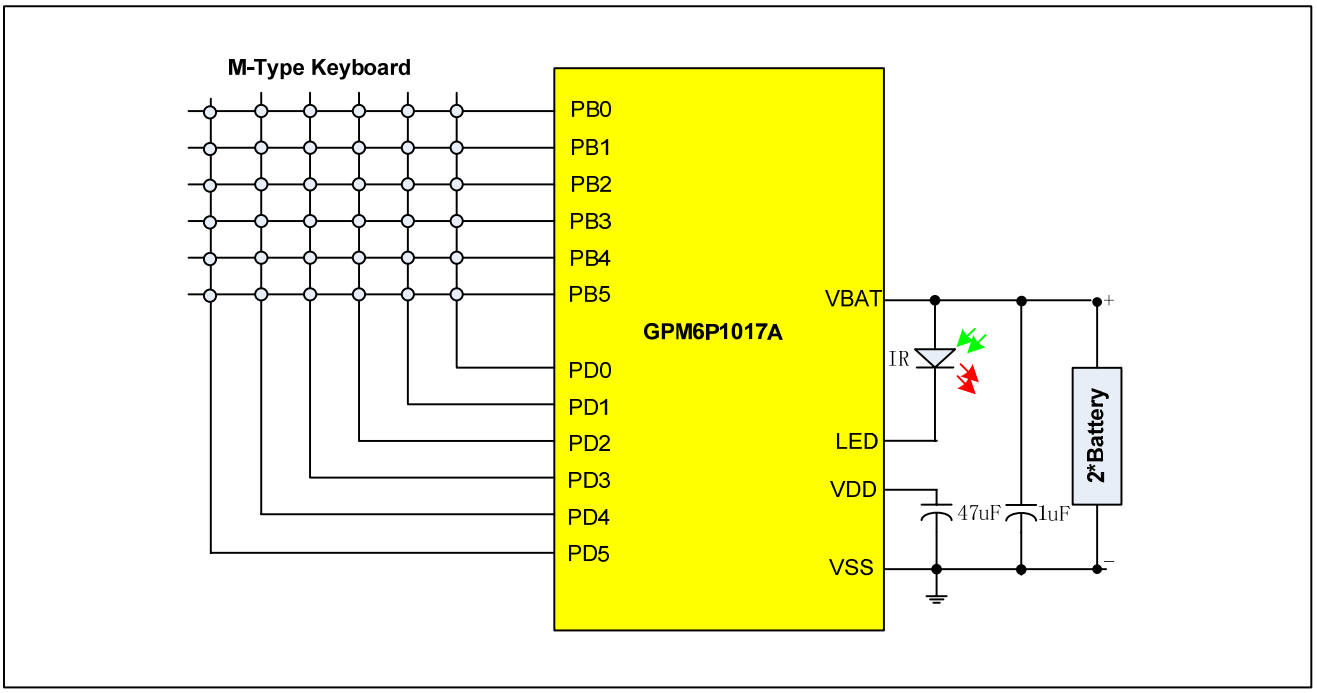
7.3. GPM6P1065A Application Circuit

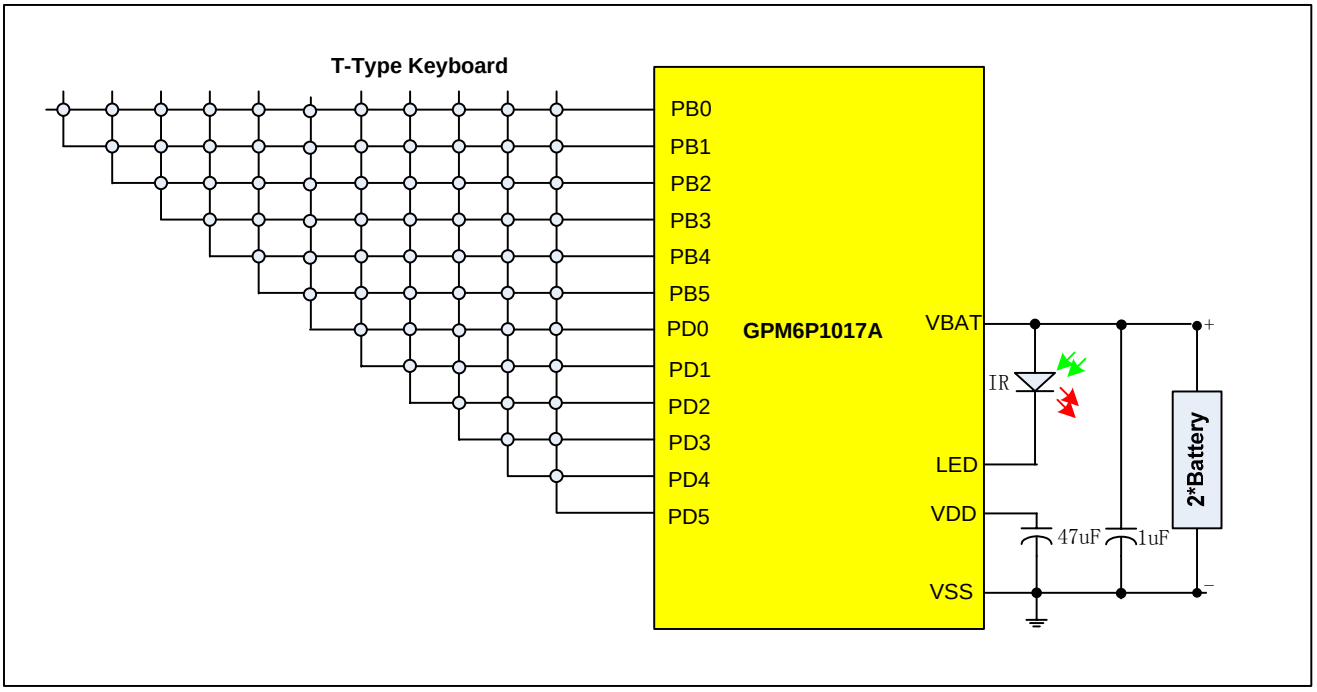


7.4. GPM6P1033A Application Circuit

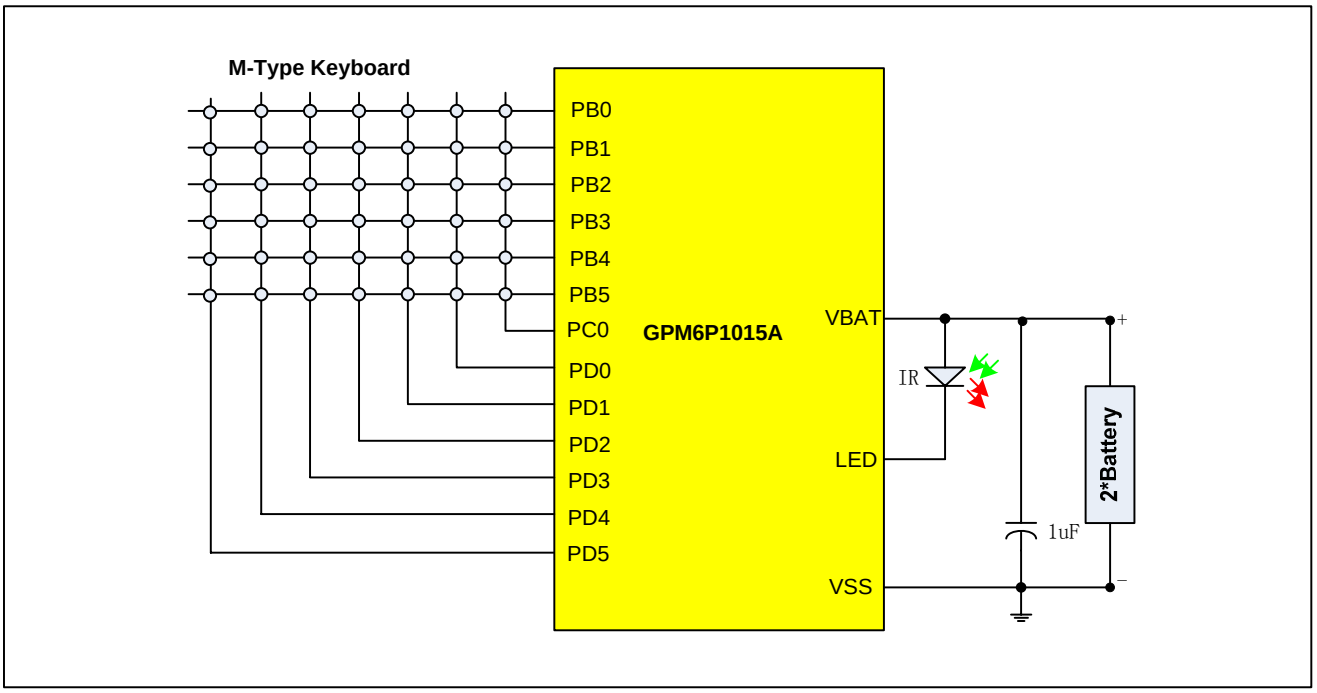


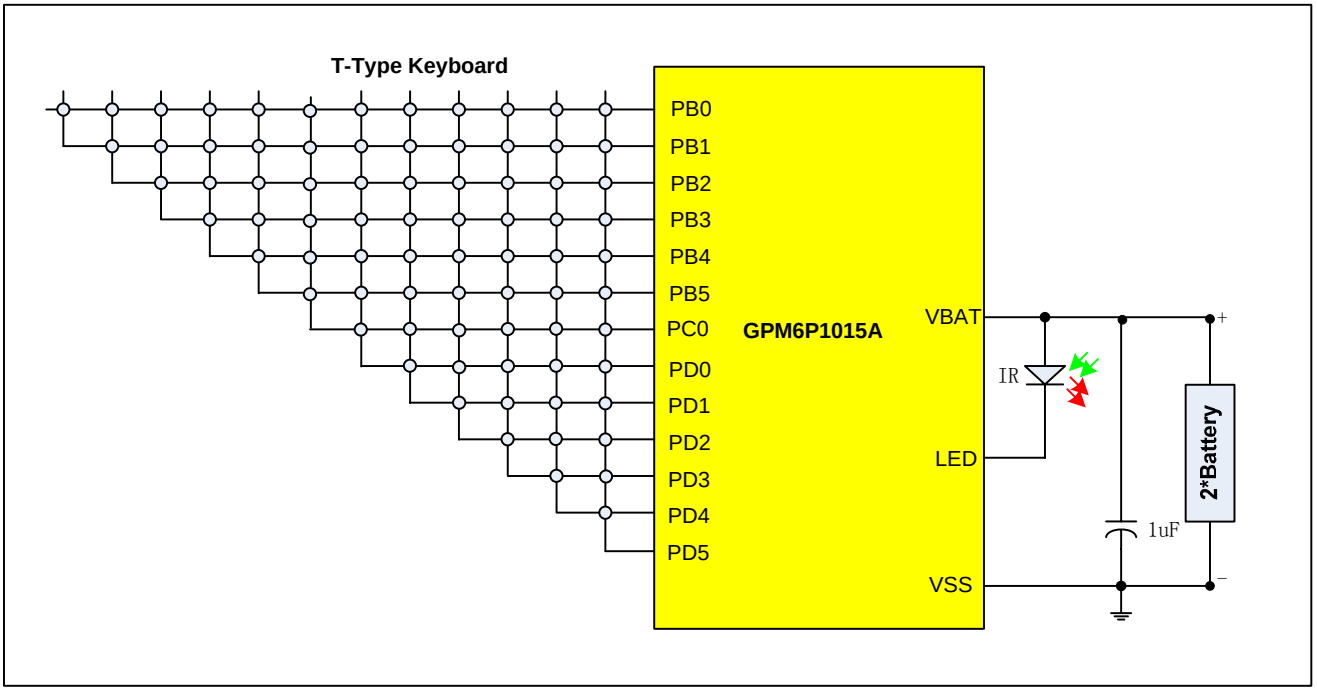
7.5. GPM6P1017A Application Circuit



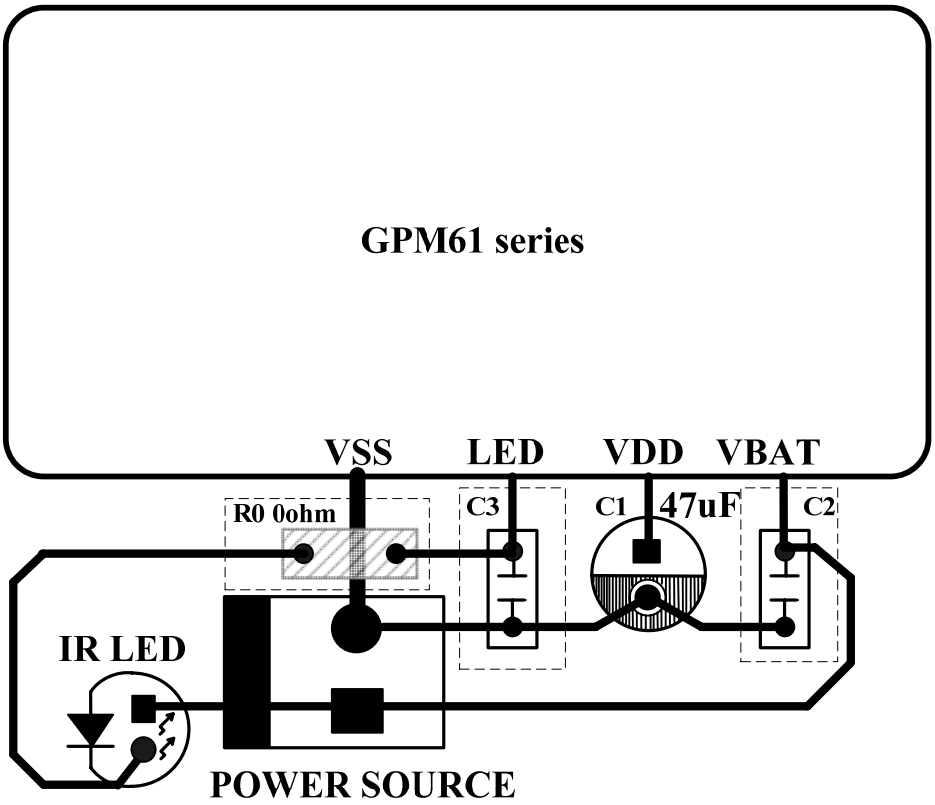


7.6. GPM6P1015A Application Circuit





7.7. PCB Layout Guideline



To avoid the unexpected noises to cause abnormal CPU operations, the following notes must be exercised while doing the PCB Layout:

1. Forbidden insert jump 0ohm resistor in the connect line between VSS pin and power source, this line should be as short as possible, and its width keep wider than 3mm is better.
2. The GND line of all these voltage stabilize intention capacitors should be pull from power source separately divided from chip GND line.
3. C1 placed between VDD and VSS must be as closed as possible to IC itself, it is necessary for all GPM61 series application circuits for power stabilization and power down data protection.
4. C2 must be as closed as possible to IC itself too, it is necessary for body GPM6C1067A/GPM6P1071A/GPM6P1015A; and it must be remove for body GPM6P1129A/GPM6P1065A/ GPM6P10133A.
5. C3 only is placed in some special application for IR LED power stabilization, its GND must be as closed as possible to power source GND.
6. The power and GND connect lines between these device should be short and wide as possible, the width keeping more than 1mm is better.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPM6P1129A-NnnV-C	Chip form
GPM6C1067A-NnnV-C	Chip form
GPM6P1065A-NnnV-C	Chip form
GPM6P1033A-NnnV-C	Chip form
GPM6P1017A-NnnV-C	Chip form
GPM6P1015A-NnnV-C	Chip form
GPM6P1129A-NnnV-QL01x	Halogen Free Package
GPM6C1067A-NnnV-QS05x	Halogen Free Package
GPM6P1065A-NnnV-QS05x	Halogen Free Package
GPM6P1033A-NnnV-QS10x	Halogen Free Package
GPM6P1017A-NnnV-QS03x	Halogen Free Package
GPM6P1015A-NnnV-QS03x	Halogen Free Package

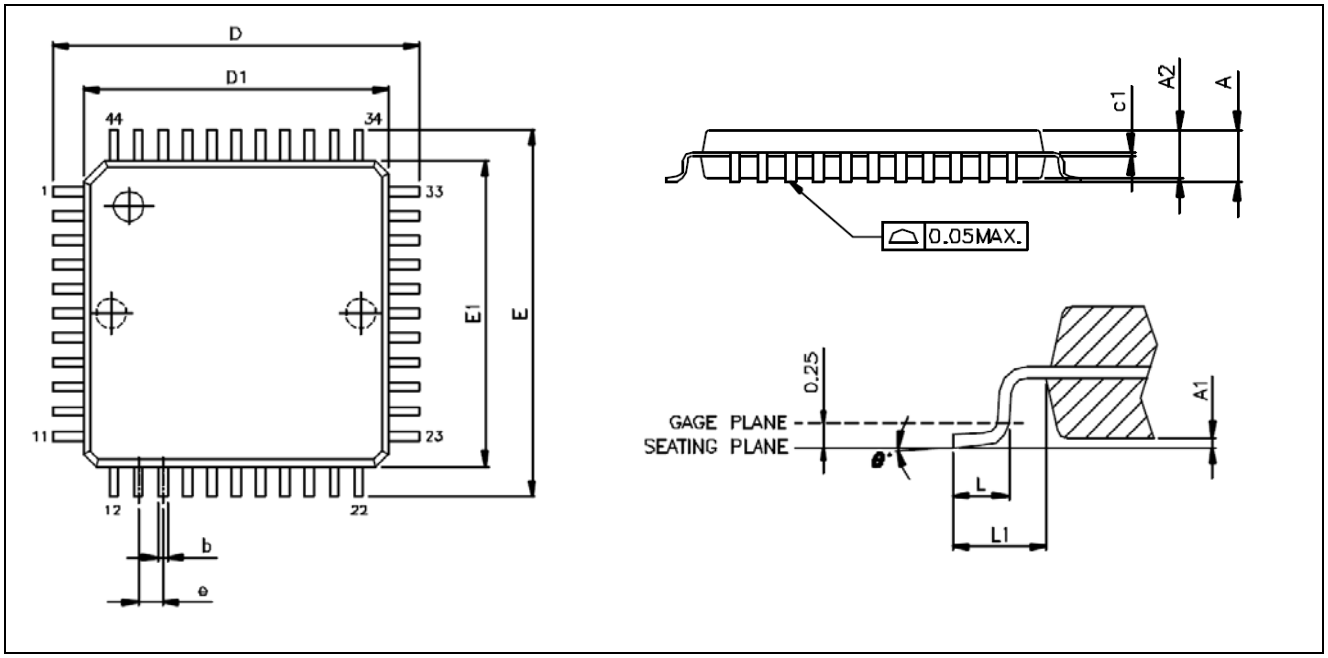
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

8.2. Package Information

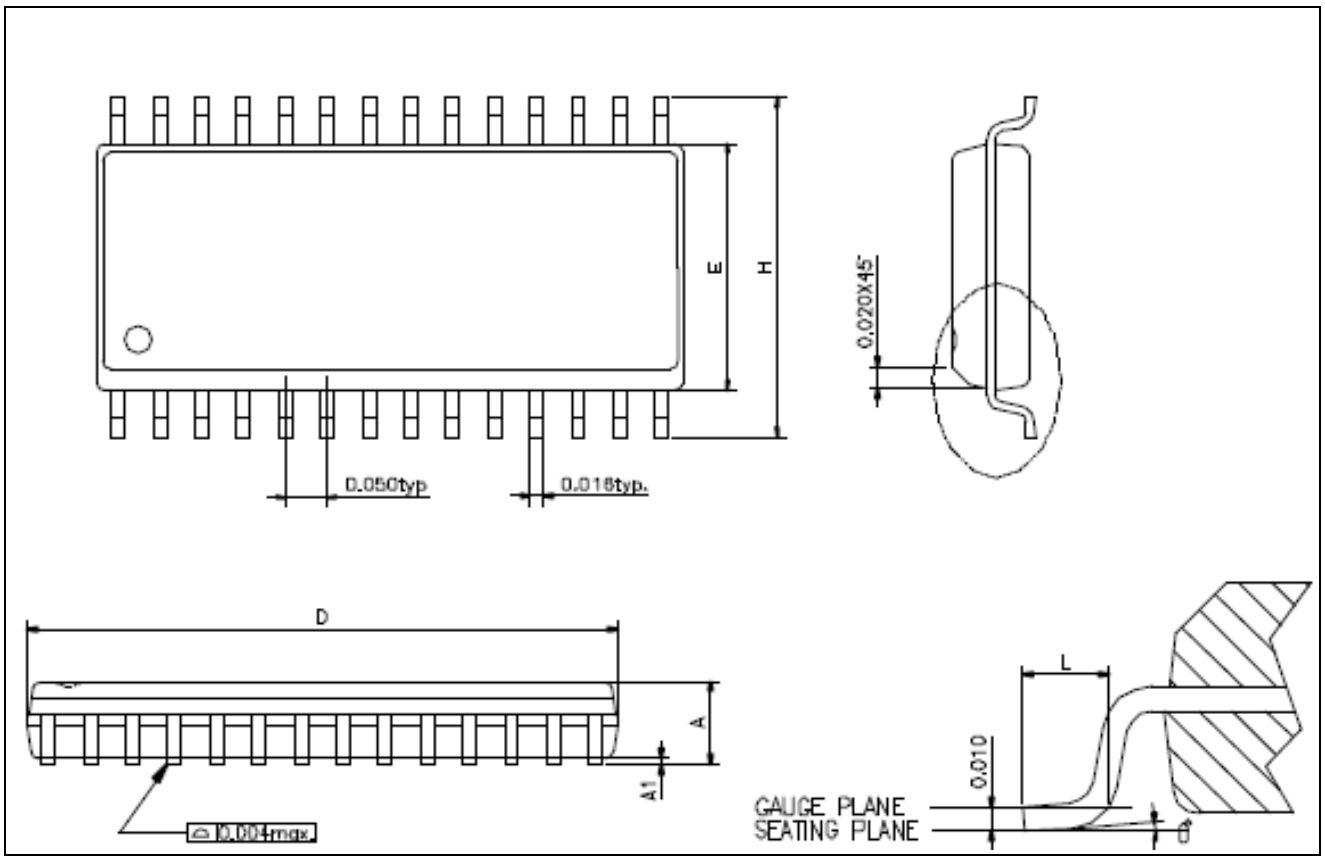
8.2.1. GPM6P1129A LQFP44



Symbols	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
c1	0.09	-	0.16
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.80 BSC		
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1	1.00 REF		
θ°	0°	3.5°	7°

Variations (All dimensions show in mm).

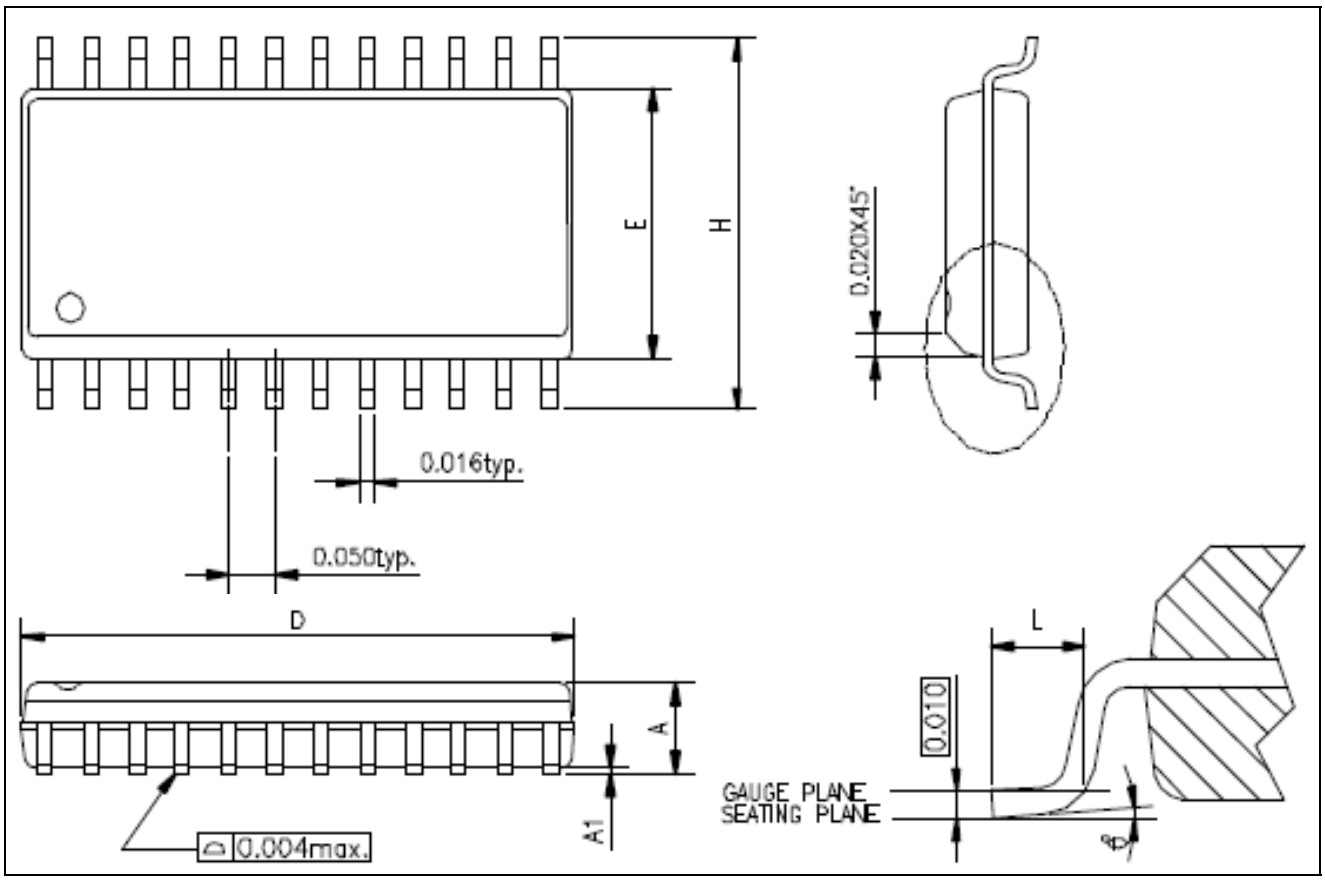
8.2.2. GPM6C1067A / GPM6P1065A SOP28



Symbol	Min.	Max.
A	0.093	0.104
A1	0.004	0.012
D	0.697	0.713
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

UNIT: INCH

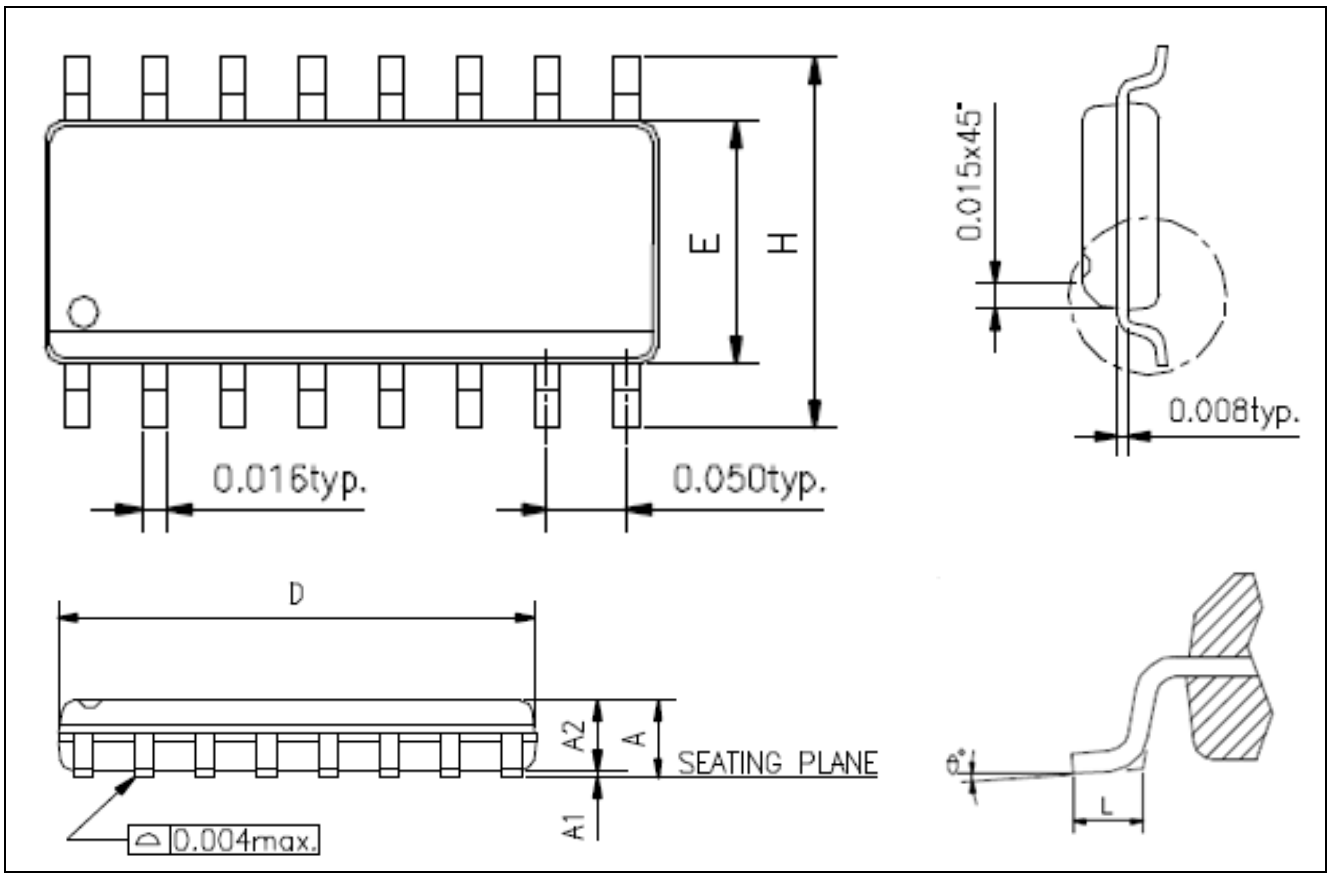
8.2.3. GPM6P1033A SOP24



Symbol	Min.	Nom.	Max.
A	0.093	0.099	0.104
A1	0.004	-	0.012
D	0.599	0.600	0.614
E	0.291	0.295	0.299
H	0.394	0.406	0.419
L	0.016	0.035	0.050
θ°	0	-	8

UNIT: INCH

8.2.4. GPM6P1017A / GPM6P1015A SOP16



Symbols	Min.	Max.
A	0.053	0.069
A1	0.004	0.010
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT: INCH

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
AUG. 17, 2010	0.1	Original	73