DATA SHEET

GPM8F2702A

16-pin 8-bit Microcontroller with 2KB EEPROM

Preliminary

Dec. 16, 2011

Version 0.2

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16-PIN 8-BIT MICROCONTROLLER WITH 2KB EEPROM

1. GENERAL DESCRIPTION

The GPM8F2702A is a highly integrated microcontroller. Besides integrating a pipelined 1T 8051 CPU, 128 Byte IDM SRAM and 2K Byte program EEPROM, it also includes 14 programmable multi-functional I/Os, Timer0/1/2, UART, and two comparators and one up to 6+1 channel (6 channel external ADC input + 1 channel internal 1.23v) of 12-bit ADC for general-purpose application. It operates over a wide voltage range of 2.0V - 5.5V with different clock sources. It has two modes in power management unit. The detail are described in the following sections.

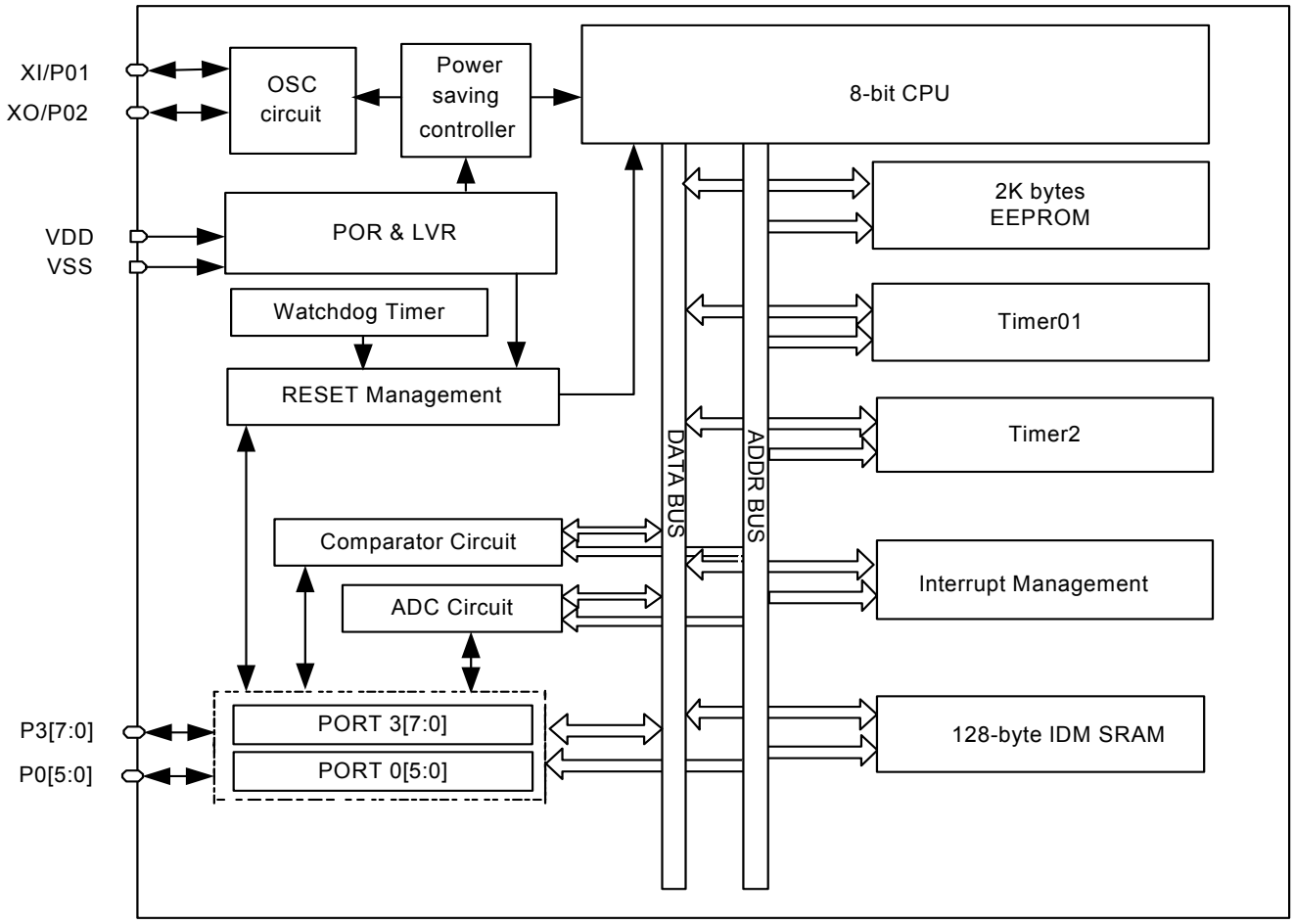
2. FEATURES

- **CPU**
  - High speed, high performance 1T 8051
    - 100% software compatible with industry standard 8051
    - Pipeline RISC architecture makes instruction execution 10 times faster than standard 8051
  - Up to 16MHz clock operation, @4.5~5.5
  - Up to 8MHz clock operation, @ 2.7~5.5
  - Up to 4MHz clock operation, @ 2.0~5.5
- **Memories**
  - 128 Bytes internal Data Memory (IDM) SRAM
  - 2K Bytes EEPROM with high endurance
    - Minimum 100,000 program/erase cycles
    - Minimum 10 years data retention
  - Programming lock level for software security
- **Clock Management**
  - Internal oscillator: 16MHz±2%, @ 2.0V~5.5V
  - Crystal input with 4MHz~16MHz
- **Power Management**
  - 1 STOP mode for power saving
  - 1 IDLE mode for only peripheral operation
- **Interrupt Management**
  - Up to 9 interrupt sources
  - Up to 3 external interrupt sources
- **Reset Management**
  - Power On Reset (POR)
  - Low Voltage Reset (LVR)
    - Three trigger level (1.92V/2.61V/4.25V)
  - Pad Reset (PAD_RST)
  - Watchdog Reset (WDT_RST)
  - Software Reset (SW_RST)
  - Stop mode Reset (STOP_RST)
  - Miss Clock Reset (MISS_CLK_RST)
  - Flash Related Error Reset (FLASH_ERR_RST)
- **Programmable Watchdog Timer**
  - A time-base generator
  - An event timer
  - System supervisor
- **I/O Ports**
  - Max 13 multifunction bi-directional I/Os
    - Each incorporate with pull-up resistor, pull-down resistor, output high, output low or floating input, depending on programmer's settings on the corresponding registers
    - I/O ports with 20mA current sink
    - I/O ports with 8mA current drive
  - One single output low I/O
    - with pull-up resistor, pull-down resistor, output low or floating input, depending on programmer's settings on the corresponding registers
    - I/O ports with 20mA current sink
- **Two 16-bit Timer/Counter (Timer 0/1)**
  - Timer mode with clock source selectable
  - Auto reload 8 bit timers
  - Externally gated event counters
- **One Powerful Timer2 with 16-bit Compare/Capture Unit**
  - Timer mode with clock source selectable
  - Auto reload 16 bit timers
  - Externally gated event counters
  - Event capturing
  - Digital signals generator
  - Pulse width modulation and measurement
- **UART0**
  - One synchronous mode
  - Three asynchronous modes
- **A/D Converter**
  - One 6+1 channel 12-bit resolution ADC
  - Max conversion clock : 2MHz (F_{OSC} /8) @16MHz
- **Built-in Comparators**
  - Two comparators with input offset < 10mV
  - Internal 4-bit reference voltage generator

***Note:**

The lowest operating voltage (4.5/2.7/2.0) is defined by the selection of LVR trigger level.

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

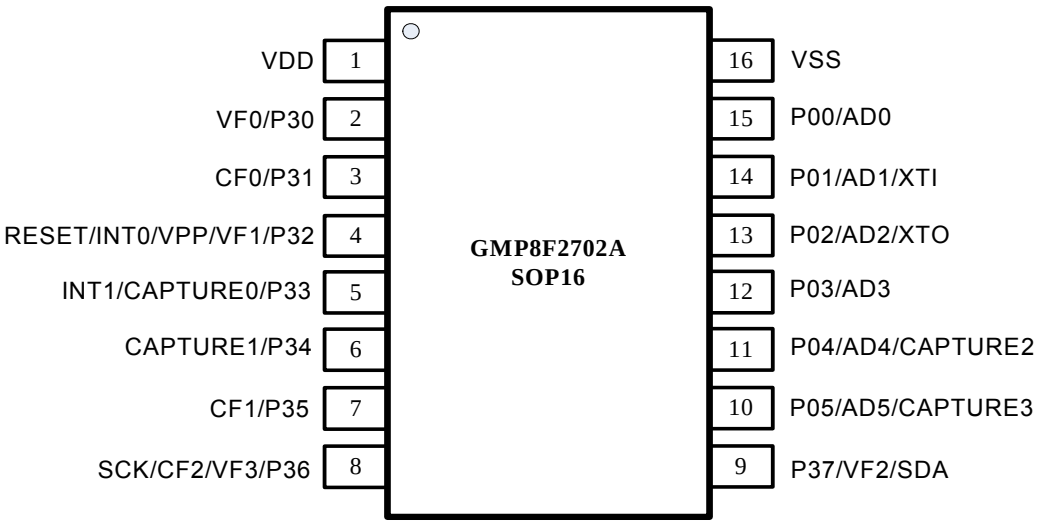
4.1. Pin Descriptions

Type：I = Input, O = Output, S = Supply

Pin Name	SOP16	Type	Description
VDD	1	S	VDD
P30	2	I/O	Port 3 bit 0 / RXD0 / VF0
P31	3	I/O	Port 3 bit 1 / TXD0 / CF0
P32	4	I/O	Port 3 bit 2 / VF1 / INT0 / VPP/ RESET
P33	5	I/O	Port 3 bit 3 / INT1 / CAPTURE0
P34	6	I/O	Port 3 bit 4 / T0 / CAPTURE1
P35	7	I/O	Port 3 bit 5 / CF1 / T1
P36	8	I/O	Port 3 bit 6 / CF2 / VF3 / GATE0 / SCK (2 wire serial bus clock input line)
P37	9	I/O	Port 3 bit 7 / VF2 / GATE1 / SDA (2 wire serial bus data input/output line)
P05	10	I/O	Port 0 bit 5 / AD5 / CAPTURE3
P04	11	I/O	Port 0 bit 4 / AD4 / CAPTURE2
P03	12	I/O	Port 0 bit 3 / AD3
P02	13	I/O	Port 0 bit 2 / AD2 / XTO
P01	14	I/O	Port 0 bit 1 / AD1 / XTI
P00	15	I/O	Port 0 bit 0 / AD0
VSS	16	S	Ground

4.2. PIN Map

SOP16



5. FUNCTIONAL DESCRIPTIONS

5.1. Central Processing Unit

5.1.1. CPU Introduction

The CPU is an ultra high performance, high speed embedded microcontroller. It is designed with a special concern about performance to power consumption. Pipelined architecture enables the CPU 10 timers faster compared to standard architecture. This performance can also be exploited to great advantage in low power application where the core can be clocked over ten times slower than original implementation for no performance penalty.

5.1.2. CPU Features

- ❑ 100 % software compatible with industry 8051
- ❑ 24 times faster multiplication
- ❑ 12 times faster addition

The CPU is fully compatible with industry standard 8051 microcontroller, maintaining all instruction mnemonics and binary compatibility. It incorporates some great architectural enhancements, allowing the CPU execution of instructions with high performance and high speed. The arithmetic section of the processor performs extensive data manipulation and is comprised of the 8-bit arithmetic logic unit (ALU), an ACC(0xE0) register, B(0xF0) register and PSW(0xD0) register.

5.1.3. Arithmetic Logic Unit (ALU)

The ALU performs the arithmetic and logic operations during execution of an instruction. Typical arithmetic operations are addition, subtraction, multiplication and division. Additional operations are such as increment, decrement, BCD-decimal-add-adjust and compare. Within logic unit, operation such as AND, OR, Exclusive OR, complement and rotation are performed. The Boolean processor performs the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry.

5.1.4. Accumulator A Register

The accumulation is the 8-bit general-purpose register, which can be operated with data transfer, temporary saving, condition judgment, etc.

5.1.5. B Register

The B register is used during multiply and divide operations. In other cases, it may be used as normal SFR.

5.1.6. Program Status Word (PSW)

The PSW contains several bits that reflect the current state of the CPU which is similar to the flag-register of general CPU.

5.1.7. Program Counter (PC)

The program counter is a 16-bit wide register. It consists of two 8-bit registers which registers are PCH and PCL. This register indicates the address of next instruction to be executed. In Reset state, the content of program counter is stored with 0x0000.

ACC			**Address: 0xE0**		**Accumulator A Register**			
Bit	7	6	5	4	3	2	1	0
Function	ACC[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	**Function**	**Type**	**Description**	**Condition**
7:0	ACC[7:0]	R/W	Accumulator A register	

Table 5-1 The ACC register

B			**Address: 0xF0**		**B Register**			
Bit	7	6	5	4	3	2	1	0
Function	B[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	**Function**	**Type**	**Description**	**Condition**
7:0	B[7:0]	R/W	B register	

Table 5-2 The B register

PSW			Address: 0xD0		Program Status Word Register			
Bit	7	6	5	4	3	2	1	0
Function	CY	AC	F0	RS1	RS0	OV	F1	P
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CY	R/W	Carry flag	
6	AC	R/W	Auxiliary carry flag	
5	F0	R/W	General purpose flag 0	
4:3	RS[1:0]	R/W	Register bank select bits RS[1:0] Function description 00 Bank 0, data address 0x00-0x07 01 Bank 1, data address 0x08-0x0F 10 Bank 2, data address 0x10-0x17 11 Bank 3, data address 0x18-0x1F	
2	OV	R/W	Overflow flag	
1	F1	R/W	General purpose flag 1	
0	P	R/W	Parity flag	

Table 5-3 The PSW register

5.2. Memory Organization

5.2.1. Introduction

The GPM8F2702A has three separated address spaces for program memory and data memory. The program memory is on-chip, re-programmable EEPROM memory and contains up to 2K bytes spaces. The data memory is divided into 128 bytes of internal data memory (IDM) and 128 bytes special function register (SFR). The IDM and SFR use the different access address. The SFR space can be accessed by using the direct addressing instructions only. The detailed description of IDM and SFR are shown is described in 5.2.3.

5.2.2. Program Memory Allocation

The GPM8F2702A implements 2KB memory size. It begins at address 0x000 and ends on address 0x7FF. The last address 0x7FF is used for CONFIG_BYTE whose definition of each bit is described in Table 5-4. User can lock the whole chip by CODE_LOCK bit of CONFIG_BYTE. If CODE_LOCK is programmed to be '0', the program memory is protected and any program by two wire serial interface is not allowed. The only one thing user can do is to whole chip erase. Figure 5-1 shows the program memory map of 2KB EEPROM. The RSTPIN_ENB bit of CONFIG_BYTE is used to set the P32 as GPIO or dedicated reset pin. If the P32 is set as external reset pin, P32_PU bit of P3_PU and P32_PD bit of P3_PD are force to "0" and "1" respectively. User also can select GPIO as pull low or pull high after reset status by setting the PUEN bit of CONFIG_BYTE.

After each reset, the CPU starts execution in the program memory at location 0x0000. Each interrupt has its own start address for service routine. The EEPROM memory can be programmed in-system, through the SCK/SDA interface or by software using the MOVX instruction when PWE= 1. The EEPROM can be written as SRAM without erasing first. The program operations executed using PSIDLE (Pseudo-idle) mode to be automatically timed by hardware without needing data polling to determine the end of the program operation. The WTST (0x92) register is used to setting the access time of program memory. Users must set the content of WTST[2:0] $\geqq$ 3'b100 before write data to program memory.

For software security consideration, user can set the programmable Flash level by FL_LEVEL (0xED) register to limit the code area to avoid inadvertently erase or write by software and the protect region is called READONLY_PAGE.

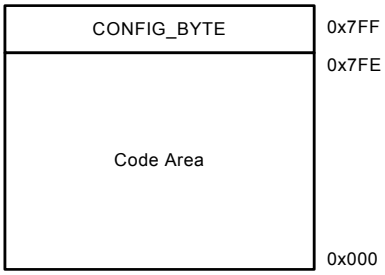


Figure 5-1 Program memory organization

CONFIG_BYTE	Address: 0x7FF (Program Memory)			CONFIG_BYTE Register				
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	PUEN	--	RSTPIN_ENB	--	CODE_LOCK
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:5	--	R	Reserved	
4	PUEN	R/W	GPIO IO pull up or low select bit 0: set all GPIO as pull low after reset status 1: set all GPIO as pull high after reset status	
3	--	R	Reserved	
2	RSTPIN_ENB	R/W	External reset pin enable bit 0: set P32 as external reset pin 1: set P32 as GPIO	
1	--	R	Reserved	
0	CODE_LOCK	R/W	Program memory protection enable bit 0 : CODE is locked 1 : CODE is unlocked	

Table 5-4 The CONFIG_BYTE register

P3_PU	Address: 0xA2			Port3 pull up configuration Register				
Bit	7	6	5	4	3	2	1	0
Function	P37_PU	P36_PU	P35_PU	P34_PU	P33_PU	P32_PU	P31_PU	P30_PU
Default	Note1	Note1	Note1	Note1	Note1	Note1	Note1	Note1

Bit	Function	Type	Description	Condition
7:0	P3_PU[7:0]	R/W	Port3 pull up control bits 0 : floating 1 : pull up	

Table 5-5 P3_PU register

P3_PD	Address: 0xA3			Port3 pull down configuration Register				
Bit	7	6	5	4	3	2	1	0
Function	P37_PD	P36_PD	P35_PD	P34_PD	P33_PD	P32_PD	P31_PD	P30_PD
Default	Note1	Note1	Note1	Note1	Note1	Note2	Note1	Note1

Bit	Function	Type	Description	Condition
7:0	P3_PD[7:0]	R/W	Port3 pull down control bits 0 : floating 1 : pull down	

Note1: If P3_PU and P3_PD are setting to '1' simultaneously, P3 will be output mode

Note2: P30_PU~P37_PU/ P30_PD~P31_PD and P33_PD~P37_PD are all "0" during reset status, and they can be set or clear by setting the PUEN bit of CONFIG_BYTE after reset status.

Note3: P32_PD is "1" during reset status, and it can be set or clear by setting the PUEN bit of CONFIG_BYTE after reset status. If the P32 is set as external reset pin (RSTPIN_ENB bit of CONFIG_BYTE is set to "0"), P32_PU and P32_PD are force to "0" and "1" respectively.

Table 5-6 P3_PD register

WTST			Address: 0x92		Program Memory Wait States Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	WTST[2:0]		
Default	0	0	0	0	0	1	0	0

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2:0	WTST[2:0]	R/W	Program memory access time 000 : 1CLK 001 : 2CLK 010 : 3CLK 011 : 4CLK 100 : 5CLK 101 : 6CLK 110 : 7CLK 111 : 8CLK	

Table 5-7 The WTST register

FL_LEVEL			Address: 0xED		Flash Level Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	FLASH_LEVEL[2:0]		
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2:0	FLASH_LEVEL[2:0]	R/W	Flash level select bits FLASH_LEVEL (Locked page) — Note 0 — address < 0x100 is read only 1 — address < 0x200 is read only 2 — address < 0x300 is read only 3 — address < 0x400 is read only 4 — address < 0x500 is read only 5 — address < 0x600 is read only 6 — address < 0x700 is read only 7 — All pages are read only	

Table 5-8 The FL_LEVEL register

5.2.3. Data Memory Allocation

Data memory address allocations on the GPM8F2702A are divided into two parts. The first part is 128 bytes of IDM and the second one is 128 byte SFR shown in Figure 5-2. The lowest internal data memory (IDM) consists of four register banks with eight registers each. A bit addressable segment with 128 bits (16 bytes) begins at 0x20. The address from 0x30 to 0x7F is not defined and can be utilized freely by user. With the direct addressing mode, the SFR addressing from 0x80 to 0xFF is accessed. The SFR memory map is shown in Table 5-9.

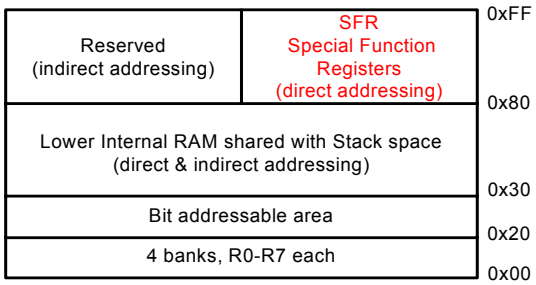


Figure 5-2 Data memory organization

Note: Black: standard 8051 register; gray: additional register;

0xF8		IOSCCON	IOSCT0	IOSCT1				
0xF0	B	ADCON	ADCFG	ADAEN	ADOL	ADOH	ADLB	ADUB
0xE8	EIE			TA	FLASHCON	FL_LEVEL		
0xE0	ACC							
0xD8	WDCON							
0xD0	PSW							
0xC8	T2CON	T2IF	CRCL	CRCH	TL2	TH2	CCEN	
0xC0	CCL0	CCH0	CCL1	CCH1	CCL2	CCH2	CCL3	CCH3
0xB8	IP	BIP	CMPICON	CMPAEN	VCMPCON	CCMPCON		
0xB0	P3						WKUEN	
0xA8	IE						SYSCON	
0xA0			P3_PU	P3_PD			FLASHERRF	
0x98	SCON0	SBUF0	P0_PU	P0_PD				
0x90		EIF	WTST		RSTSTS			
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	RSTCON
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F

Table 5-9 SFR memory map

5.2.4. Memory Related SFR

The following sub-sections describe program, external and internal memories related SFRs of 8051 core and their functionality. For other information about standard SFRs, please refer to appropriate peripheral section.

5.2.4.1. Program Write Enable Bit

The Program Write Enable (PWE) bit, located in PCON register bit 4, is used during MOVX instructions. When PWE bit is set to logic 1, the MOVX @DPTR, A instruction writes data located in accumulator register into program memory addressed by DPTR register. Program memory can be read by MOVC only regardless of PWE bit.

5.2.4.2. Program Wait State Register

Wait States register holds the information about program memory access time. It allows the 8051 core operation with fast and slow program memories. The default value of WTST[2:0] is 3'b100.

5.2.4.3. Data Pointer Registers

Dual data pointer registers are implemented to speed up data block copying. DPTR0 and DPTR1 are located in four SFR addresses. Active DPTR register is selected by SEL bit (DPS[0]). If SEL=0 then DPTR0 is selected otherwise DPTR1.

5.2.4.4. Stack Pointer

The 8051 has 7-bit stack pointer called SP (0x81) located in the internal RAM space. It is incremented before data is stored during PUSH and CALL execution and decremented after data is popped during POP, RET and RETI execution. In the other words, it always points to the last valid stack byte. The SP is accessed as any other SFRs. Figure 5-3 shows an example when PUSH A is executed and Figure 5-4 shows an example when POP PSW is executed.

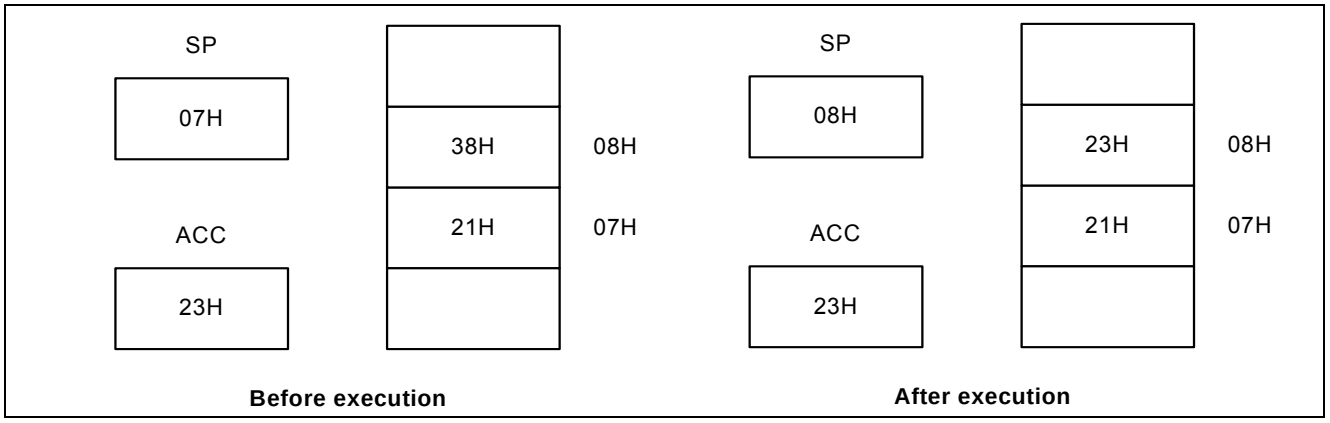


Figure 5-3 Stack byte order for PUSH A instruction

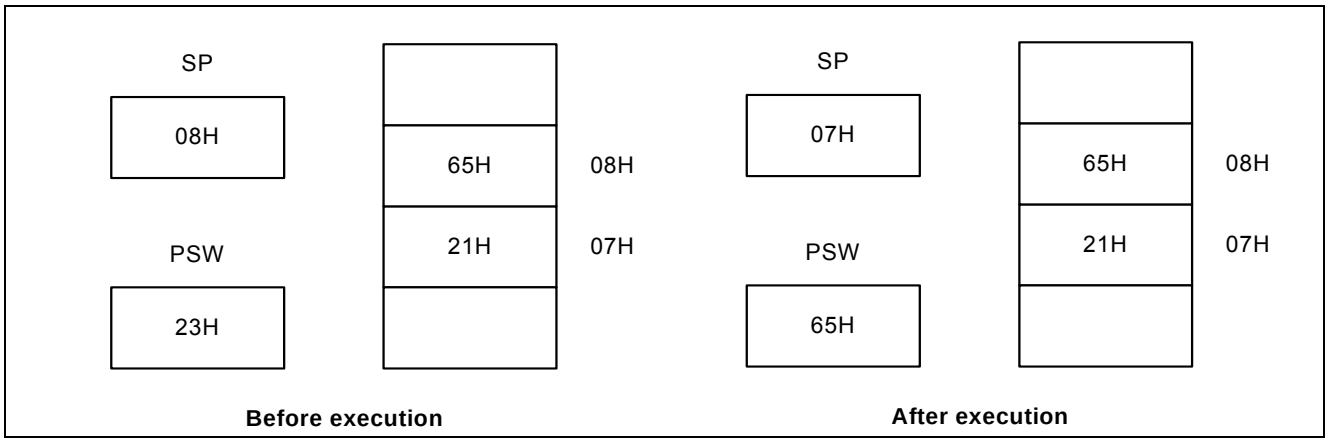


Figure 5-4 Stack byte order for POP PSW instruction

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	--	CPU_IDLE	PWE	STOP_RST_EN	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	--	R/W	Reserved	
5	CPU_IDLE	R/W	IDLE mode enable bit 0: IDLE mode disabled ; 1: IDLE mode entered	

Bit	Function	Type	Description	Condition
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3	STOP_RST_EN	R/W	Wakeup state selection bit 0: Next instruction state after wakeup 1: Reset state afer wakeup	
2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-10 The PCON register

WTST			Address: 0x92		Program Memory Wait States Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	WTST[2:0]		
Default	0	0	0	0	0	1	0	0

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2:0	WTST[2:0]	R/W	Program memory access time 000 : 1CLK 001 : 2CLK 010 : 3CLK 011 : 4CLK 100 : 5CLK 101 : 6CLK 110 : 7CLK 111 : 8CLK	

Table 5-11 The WTST register

DPH0			Address: 0x83		Data Pointer Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[15:8]	R/W	Data pointer register DPTR0 - high byte	

Table 5-12 The DPH0 register

DPL0			Address: 0x82		Data Pointer Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[7:0]	R/W	Data pointer register DPTR0 - low byte	

Table 5-13 The DPL0 register

DPH1			Address: 0x85		Data Pointer 1 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR1[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[15:8]	R/W	Data pointer 1 register DPTR1 - high byte	

Table 5-14 The DPH1 register

DPL1			Address: 0x84		Data Pointer 1 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[7:0]	R/W	Data pointer 1 register DPTR1 - low byte	

Table 5-15 The DPL1 register

DPS			Address: 0x86		Data Pointer Select Register			
Bit	7	6	5	4	3	2	1	0
Function	ID1	ID0	TSL	-	-	-	-	SEL
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	ID[1:0]	R/W	Increment/decrement function select. See Table 5-17	
5	TSL	R/W	Toggle select enable bit 0 : DPTR related instructions do not affect state of SEL bit 1 : DPTR related instructions to toggle the SEL bit	
4:1	--	R/W	Reserved	
0	SEL	R/W	Active data pointer select bit See Table 5-17	

Table 5-16 The DPS register

ID1	ID0	SEL=0	SEL=1
0	0	INC DPTR0	INC DPTR1
0	1	DEC DPTR0	INC DPTR1
1	0	INC DPTR0	DEC DPTR1
1	1	DEC DPTR0	DEC DPTR1

Table 5-17 DPTR0/DPTR1 operations

SP			Address: 0x81		Stack Pointer Register			
Bit	7	6	5	4	3	2	1	0
Function	--	SP[6:0]						
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6:0	SP[6:0]	R/W	Stack pointer	

Table 5-18 The SP register

5.3. Special Function Registers (SFR)

GPM8F2702A has up to 69 control registers for special function registers. All of the SFRs are used by MCU and peripheral function block for controlling the desired operation. Some of the SFRs contain control and status bits for peripheral module such as Timer unit, Interrupt control unit, etc. Some of bits in SFRs are read only, so write to those bits don't have any effect on corresponding bits. Some SFRs have key code design that TA (0xEB) register must be written with correct key codes, in sequence, before writing a value to it for software security. The following table shows the summary of the SFRs. The detailed information of each SFRs are explained in each peripheral section.

Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0x80	P0		0xFF	--	--	P05	P04	P03	P02	P01	P00
0x81	SP		0x07	--	Stack Pointer[6:0]						
0x82	DPL0		0x00	Data pointer register DPTR0 - low byte							
0x83	DPH0		0x00	Data pointer register DPTR0 - high byte							
0x84	DPL1		0x00	Data pointer register DPTR1 - low byte							
0x85	DPH1		0x00	Data pointer register DPTR1 - high byte							
0x86	DPS		0x00	ID1	ID0	TSL	-	-	-	-	SEL
0x87	PCON		0x00	SMOD0	--	CPU_IDLE	PWE	STOP_ RST_EN	--	STOP	--
0x88	TCON		0x00	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
0x89	TMOD		0x00	GATE1	CT1	M11	M10	GATE0	CT0	M01	M00
0x8A	TL0		0x00	Timer 0 Load value – low byte							
0x8B	TL1		0x00	Timer 1 Load value – low byte							
0x8C	TH0		0x00	Timer 0 Load value – high byte							
0x8D	TH1		0x00	Timer 1 Load value – high byte							
0x8E	CKCON		0x01	WD1	WD0	--	T1M	T0M	--	--	--
0x8F	RSTCON	0x4F, 0x72, 0x7A	0x00	CB_P_ ENB	--	FLASH_ FLOW_ ENB	ERR_ XROM_ENB	--	--	MISS_CLK_ ENB	FLASH_ ERR_ ENB
0x91	EIF		0x00	INTKEYF	--	--	--	--	--	--	--
0x92	WTST		0x04	--	--	--	--	--	WTST[2:0]		
0x94	RSTSTS		0x00	--	MISS_ CLK_RST	STOP_ RST	FLASH_ ERR_RST	SW_RST	WDT_RST	LVR_RST	PAD_RST
0x98	SCON0		0x00	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
0x99	SBUF0		0x00	UART 0 buffer							
0x9A	P0_PU		Note0	--	--	P05_PU	P04_PU	P03_PU	P02_PU	P01_PU	P00_PU
0x9B	P0_PD		Note0	--	--	P05_PD	P04_PD	P03_PD	P02_PD	P01_PD	P00_PD

Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0xA2	P3_PU		Note1	P37_PU	P36_PU	P35_PU	P34_PU	P33_PU	P32_PU	P31_PU	P30_PU
0xA3	P3_PD		Note2	P37_PD	P36_PD	P35_PD	P34_PD	P33_PD	P32_PD	P31_PD	P30_PD
0xA6	FLASHERRF		0x00	CB_P_F	--	FLASH_ FLOW_F	ERR_ XROM_F	--	--	--	--
0xA8	IE		0x00	EA	--	ET2	ES0	ET1	EX1	ET0	EX0
0xAE	SYSCON	0xFF,0x00	0x00	LVRENB	--	--	--	--	--	LVRSEL1	LVRSEL0
0xB0	P3		0xFF	P37	P36	P35	P34	P33	P32	P31	P30
0XB6	WKUEN	0xAF,0x50	0x83	INTKEY_ WKUEN	--	--	--	--	--	INT1_ WKUEN	INT0_ WKUEN
0xB8	IP		0x00	--	--	PT2	PS0	PT1	PX1	PT0	PX0
0xB9	BIP		0x00	--	--	--	--	--	--	P_CMP_KEY	P_ADC
0xBA	CMPICON		0x00	--	--	--	--	CCMPIF	VCMPIF	CCMPIE	VCMPIE
0xBB	CMPAEN		0x00	--	--	P37_AEN	P36_AEN	P35_AEN	P32_AEN	P31_AEN	P30_AEN
0xBC	VCMPCON		0x00	VFOUT	VCMP_SEL3	VCMP_SEL2	VCMP_SEL1	VCMP_SEL0	VFSEL1	VFSEL0	VCPEN
0xBD	CCMPCON		0x00	CFOUT	CCMP_SEL3	CCMP_SEL2	CCMP_SEL1	CCMP_SEL0	CFSEL1	CFSEL0	CCPEN
0xC0	CCL0		0x00	Timer2cc compare/capture 0 low byte							
0xC1	CCH0		0x00	Timer2cc compare/capture 0 high byte							
0xC2	CCL1		0x00	Timer2cc compare/capture 1 low byte							
0xC3	CCH1		0x00	Timer2cc compare/capture 1 high byte							
0xC4	CCL2		0x00	Timer2cc compare/capture 2 low byte							
0xC5	CCH2		0x00	Timer2cc compare/capture 2 high byte							
0xC6	CCL3		0x00	Timer2cc compare/capture 3 low byte							
0xC7	CCH3		0x00	Timer2cc compare/capture 3 high byte							
0xC8	T2CON		0x00	T2PS	I3FR	T2CM1	T2R	--	T2CM0	--	T2I
0xC9	T2IF		0x00	--	--	--	--	--	--	--	TF2
0xCA	CRCL		0x00	CRC register – Low byte							
0xCB	CRCH		0x00	CRC register – High Byte							
0xCC	TL2		0x00	Timer 2 Load value – low byte							
0xCD	TH2		0x00	Timer 2 Load value – high byte							
0xCE	CCEN		0x00	CMH3	CML3	CMH2	CML2	CMH1	CML1	CMH0	CML0
0xD0	PSW		0x00	CY	AC	F0	RS1	RS0	OV	F1	P
0xD8	WDCON	0xAA ,0x55	0x00	--	--	--	--	--	--	EWT	RWT
0xE0	ACC		0x00	ACC register							
0xE8	EIE		0x00	EKEYI	--	--	--	--	--	--	--
0xEB	TA		0x00	Timed Access protection register							
0xEC	FLASHCON		0x00	--	--	--	--	--	--	--	PROG
0xED	FL_LEVEL		0x07	--	--	--	--	--	FLASH_LEVEL[2:0]		
0xF0	B		0x00	B register							
0xF1	ADCON		0x00	WINF	READYF	WIN_SEL	WINIE	ADIE	--	PSIDLE	START
0xF2	ADCFG		0x00	--	CH_SEL[2:0]			SHCLK[1:0]		ADCLK[1:0]	
0xF3	ADAEN		0x00	--	--	P05_AEN	P04_AEN	P03_AEN	P02_AEN	P01_AEN	P00_AEN
0xF4	ADOL		0x00	ADO[3:0]				--	--	--	--
0xF5	ADOH		0x80	ADO[11:4]							
0xF6	ADLB		0x00	ADLB[7:0]							

Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0xF7	ADUB		0x00	ADUB[7:0]							
0xF9	IOSCCON		0x02	--	--	XTAL_PAD_EN	XTAL_EN		CLKDIV[2:0]		
0xFA	IOSCT0		0x00	--	--	--	--	--	--	--	XFCN
0xFB	IOSCT1		0x6F	OSC_TRIM[2:0]			OSC_TUNE[4:0]				

Note1: P00_PU ~ P05_PU/P00_PD~P05_PD are all "0" during reset status, and they can be set or clear by PUEN bit of CONFIG_BYTE after reset status.
Note2: P30_PU~P37_PU/ P30_PD~P31_PD and P33_PD~P37_PD are all "0" during reset status, and they can be set or clear by setting the PUEN bit of CONFIG_BYTE after reset status.
Note3: P32_PD is "1" during reset status, and it can be set or clear by setting the PUEN bit of CONFIG_BYTE after reset status. If the P32 is set as external reset pin (RSTPIN_ENB bit of CONFIG_BYTE is set to "0"), P32_PU and P32_PD are force to "0" and "1" respectively.

5.4. Clock Source

GPM8F2702A has two clock sources including internal oscillator (16MHz) and external crystal. These two clocks are chosen to be system clock source by controlling XTAL_EN bit of IOSCCON register. In addition, a clock divisor for the system clock source is contained to obtain different frequencies. There are eight selection totally and can be controlled by CLKDIV[2:0] bits of IOSCCON register. The block diagram of clock source and detailed description of IOSCCON register are shown in Figure 5-5 and Table 5-19 respectively.

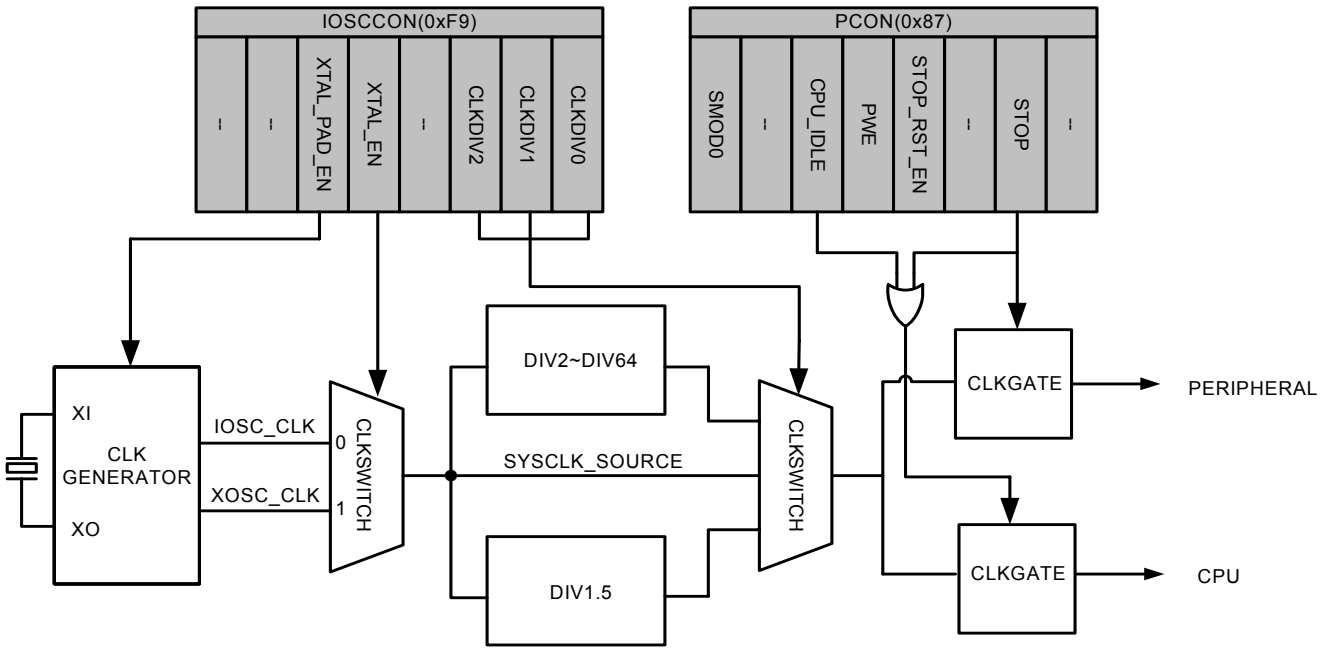


Figure 5-5 The block diagram of clock sources

If crystal mode is utilized, different frequencies can be selected by IOSCT0[0] as tabled in Table 5-20 and software should delay period of time according to different crystals for clock stable time. In order to enter stop mode, XTAL_PAD_EN should be turned off before PCON[1] is set to '1'. If internal oscillator mode is utilized, tuning frequencies is possible through IOSCT1[7:0]. If IOSCT1[7:5] is used for trimming bit, each step of frequency is 10%. If IOSCT1[4:0] is used for trimming bit, each step of frequency is 1% for fine-tuning. The IOSCT1 register is shown in Table 5-21.

IOSCCON			Address: 0xF9		IOSC Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	XTAL_PAD_EN	XTAL_EN	--	CLKDIV[2:0]		
Default	0	0	0	0	0	0	1	0

Bit	Function	Type	Description
7:6	--	R/W	Reserved
5	XTAL_PAD_EN	R/W	If using XTAL, XTAL_PAD_EN should be set to "1" XTI and XTO can be analog PAD.
4	XTAL_EN	R/W	External crystal select bit 0: ROSC 1: XTAL
3	--	R/W	Reserved
2:0	CLK_DIV	R/W	System clock source divider CLK_DIV Clock control 000 SYSCLK_SOURCE 001 SYSCLK_SOURCE/2 010 SYSCLK_SOURCE/4 011 SYSCLK_SOURCE/8 100 SYSCLK_SOURCE/16 101 SYSCLK_SOURCE/32 110 SYSCLK_SOURCE/64 111 SYSCLK_SOURCE/1.5

Table 5-19 The IOSCCON register

IOSCT0			Address: 0xFA		IOSC Timing 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	--	XFCN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	--	R/W	Reserved	
0	XFCN	R/W	External crystal frequency control bit (XTAL_PAD_EN need to be set to 1) XFCN XTAL(HZ) 0 4MHz<F<8MHz 1 8MHz<F<16MHz	

Table 5-20 The IOSCT0 register

IOSCT1			Address: 0xFB		IOSC Control Timing 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	OSC_TRIM[2:0]			OSC_TUNE[4:0]				
Default	0	1	1	0	1	1	1	1

Bit	Function	Type	Description	Condition
7:5	OSC_TRIM[2:0]	R/W	Internal OSC frequency trimming bit, 10% each step	

Bit	Function	Type	Description	Condition
4:0	OSC_TUNE[4:0]	R/W	Internal OSC frequency trimming bit, 1% each step	

Table 5-21 The IOSCT1 register

5.5. Power Saving Mode

5.5.1. Introduction

Although GPM8F2702A is a high-speed microcontrollers designed for maximum performance, it also provide Power Management Unit (PMU) with two advanced power conservation modes. These modes are IDLE mode, and STOP mode. In order to reduce the current consumption when system does not need to be active, STOP mode can be utilized. For more information about these two modes, please see the following two sections.

5.5.2. IDLE Mode

The IDLE Mode reduces power consumption by turning off the clock provided to the microcontroller, causing MCU to stop to execute following instruction. IDLE mode is entered by setting the CPU_IDLE bit (PCON[5]). In this mode, peripheral clock is not turned off, so peripheral device can still work normally.

5.5.3. STOP Mode

STOP mode is the lowest power states that the microcontroller can enter. It is achieved by cutting-off frequency provided to SYSCLK, resulting in a fully static condition. No processing is possible, timers are stopped, and no serial communication is executed. Processor operation will be postponed on the instruction that sets the STOP bit. STOP mode can be exited in the following ways:

i. When the RSTPIN_ENB bit of CONFIG_BYTE is set to “0” and RESET pin (P32) equals to VDD.
ii. A non-clocked interrupt such as the external interrupts INT0~INT1 and P0 key change interrupt can be used.

Clocked interrupts such as the watchdog timer, internal timers, and serial ports do not operate in STOP mode. Processor operation will resume with the fetching of the interrupt vector associated with the interrupt that caused the exit from STOP mode. When the interrupt service routine is completed, RETI returns the program to the instruction immediately following the one that invoked the STOP mode. When INT0~INT1 and P0 key change interrupt are used for wakeup source, WKUEN register must be set which tabled in Table 5-24. There are two selections of the place of instruction execution after wakeup when entering STOP mode and the control bit is in POCN[3]. If STOP_RST_EN is set to ‘1’, reset state will take place after wakeup, otherwise, next instruction will be executed. Table 5-22 shows the three modes in GPM8F2702A.

	System Clock	Peripheral Clock	After Wakeup
RUN Mode	Register setting	Register setting	--
IDLE Mode	OFF	ON	Next instruction state
STOP Mode	OFF	OFF	Reset state or next instruction state base on PCON[3]

Table 5-22 The three operation modes for GPM8F2702A

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	--	CPU_IDLE	PWE	STOP_RST_EN	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	--	R/W	Reserved	
5	CPU_IDLE	R/W	IDLE mode enable bit 0: IDLE mode disabled ; 1: IDLE mode entered	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction	

Bit	Function	Type	Description	Condition
			1: Enable Flash write activity during MOVX instruction	
3	STOP_RST_EN	R/W	Wakeup state selection bit 0: Next instruction state after wakeup 1: Reset state afer wakeup	
2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-23 The PCON register

WKUEN				Address: 0xB6	Wake Up Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	INTKEY_WKUEN	--	--	--	--	--	INT1_WKUEN	INT0_WKUEN
Default	1	0	0	0	0	0	1	1
Key Code	0xAF, 0x50							

Bit	Function	Type	Description	Condition
7	INTKEY_WKUEN	R/W	P0 key change wake up enable control	
6:2	--	R/W	Reserved	
1	INT1_WKUEN	R/W	INT1 PAD wake up enable control, active high	
0	INT0_WKUEN	R/W	INT0 PAD wake up enable control, active high	

Table 5-24 The WKUEN register

5.6. Interrupt System

5.6.1. Introduction

The GPM8F2702A provides 9 types of interrupt sources (including 6 interrupt sources of standard 8051 and additional 3 interrupt sources) with two levels interrupt priority control which tabled in Table 5-25. For standard 8051 interrupt sources, each interrupt can be in high or low level priority group by setting or clearing a bit in the IP(0xB8) registers. INT0 has the top priority in default state and user can choose the related interrupt source to be the top priority by IP register. For additional interrupt sources, high or low level priority group is set or cleared a bit in the BIP(0xB9). Interrupt requests are sampled each system clock at the rising edge of clock control. Each interrupt vector can be individually enabled or disabled by setting or clearing a corresponding bit in the IE(0xA8), EIE(0xE8). The IE contains global interrupt system disable(0) / enable(1) bit called EA. In general, once an interrupt event occurs, the corresponding flag bit will be set. The related registers of interrupt flag are described as below. If the related interrupt control bit is set to enable interrupt, an interrupt request signal will be generated and then CPU executes service routine. If the related interrupt control bit is disabled, programmer still can observe the corresponding flag bit, but no interrupt request signal will be generated. The interrupt flag bits must be cleared in the interrupt service routine to prevent program from deadlock in interrupt service routine. With any instruction, interrupts pending during the previous instruction is served. Before entering interrupt service routine, the system saves the current PC address into top of stack pointer and jumps to corresponding vector to execute the interrupt service. After finishing the interrupt service, the system abstract the return PC address from the top of the stack to execute the following instruction.

As to additional three interrupt sources, each interrupt vector can be individually enabled or disabled by setting or clearing a corresponding bit in the ADCON(0xF1), CMPICON(0xBA) and EIE(0xE8). The corresponding flag can be found in ADCON(0xF1), CMPICON(0xBA) and EIF(0x91). For detail description, please refer to related block.

Interrupt Flag	Function	Active Level/Edge	Flag Resets	Vector	Vector Number	Priority
IE0	Device pin INT 0	Low/Falling	Hardware	0x03	0	1
TF0	Internal Timer 0	-	Hardware	0x0B	1	2
IE1	Device pin INT 1	Low/Falling	Hardware	0x13	2	3
TF1	Internal Timer 1	-	Hardware	0x1B	3	4
TI0 & RI0	Internal UART0	-	Software(cleared by 0)	0x23	4	5
TF2	Internal Timer2	-	Software(cleared by 0)	0x2B	5	6
WINF & READYF	ADC interrupt	-	Software(cleared by 0)	0x33	6	7
CCMPIF & VCMPIF INTKEYF	Comparator interrupt P0 key change interrupt	-	Software (cleared by 0)	0x3B	7	8

Note1: INT0 and INT1 interrupt pins are activated at low level or by a falling edge

Note2: P0 key change interrupt is activated at any transition on P0. User should read P0 for latching P0 status before setting EKEYI bit of EIE(0xE8).

Table 5-25 Summaries of all interrupt sources

IP			Address: 0xB8		Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	-	--	PT2	PS0	PT1	PX1	PT0	PX0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	PT2	R/W	Timer 2 priority level control (1: high level)	
4	PS0	R/W	UART0 priority level control (1: high level)	
3	PT1	R/W	Timer 1 priority level control (1: high level)	
2	PX1	R/W	INT1 priority level control (1: high level)	
1	PT0	R/W	Timer 0 priority level control (1: high level)	
0	PX0	R/W	INT0 priority level control (1: high level)	

Table 5-26 IP register

BIP			Address: 0xB9		Additional Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	P_CMP_KEY	P_ADC
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:2	--	R/W	Reserved	
1	P_CMP_KEY	R/W	Comparator interrupt and P0 key change interrupt priority level control (1: high level)	
0	P_ADC	R/W	ADC interrupt priority level control (1: high level)	

Table 5-27 BIP register

IE			Address: 0xA8		Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	EA	--	ET2	ES0	ET1	EX1	ET0	EX0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EA	R/W	Enable global interrupts	
6	--	R/W	Reserved	

Bit	Function	Type	Description	Condition
5	ET2	R/W	Enable Timer 2 interrupt	
4	ES0	R/W	Enable UART0 interrupt	
3	ET1	R/W	Enable Timer 1 interrupt	
2	EX1	R/W	Enable INT1 interrupt	
1	ET0	R/W	Enable Timer 0 interrupt	
0	EX0	R/W	Enable INT0 interrupt	

Table 5-28 IE register

EIE			Address: 0xE8		Extended Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	EKEYI	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EKEYI	R/W	Enable P0 key change interrupt	
6:0	--	R/W	Reserved	

Table 5-29 EIE register

TCON			Address: 0x88		Timer0/1 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TF1	R/W	Timer 1 interrupt (overflow) flag	
6	TR1	R/W	Timer 1 run control bit 0: disabled ; 1: enabled	
5	TF0	R/W	Timer 0 interrupt (overflow) flag	
4	TR0	R/W	Timer 0 run control bit 0: disabled ; 1: enabled	
3	IE1	R/W	INT1 interrupt flag	
2	IT1	R/W	INT1 level (at 0)/ edge (at 1) sensitivity	
1	IE0	R/W	INT0 interrupt flag	
0	IT0	R/W	INT0 level (at 0)/ edge (at 1) sensitivity	

Table 5-30 TCON register

T2IF			Address: 0xC9		Timer 2 Interrupt Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	--	TF2
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	--	R/W	Reserved	
0	TF2	R/W	Timer 2 overflow flag Cleared by the software	

Table 5-31 T2IF register

SCON0			Address: 0x98		UART0 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SM00	--	SM02	REN0	TB08	RB08	TI0	RI0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	SM0[1:0]	R/W	Mode and baud rate setting	
5	SM02	R/W	Enables a multiprocessor communication feature	
4	REN0	R/W	Enable serial reception.	
3	TB08	R/W	The 9th transmitted data bit in Modes 2 and Mode 3	
2	RB08	R/W	In Mode 0 this bit is not used In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 2 and Mode 3, it is the 9th data bit received	
1	TI0	R/W	UART0 transmitter interrupt flag	
0	RI0	R/W	UART0 receiver interrupt flag	

Table 5-32 SCON0 register

EIF			Address: 0x91		Extended Interrupt Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	INTKEYF	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	INTKEYF	R/W	P0 key change interrupt flag	
6:0	--	R/W	Reserved	

Table 5-33 EIF register

5.7. Reset Sources

5.7.1. Introduction

There are eight types of reset sources for the GPM8F2702A including Power-On Reset (POR), Low Voltage Reset (LVR), Pad Reset (PAD_RST), Watchdog Timer Reset (WDT_RST), Software Reset (SW_RST), STOP mode Reset (STOP_RST), Flash Error Reset (FLASH_ERR_RST), and missing system clock Reset (MISS_CLK_RST). Figure 5 6 shows the block diagram of each reset source.

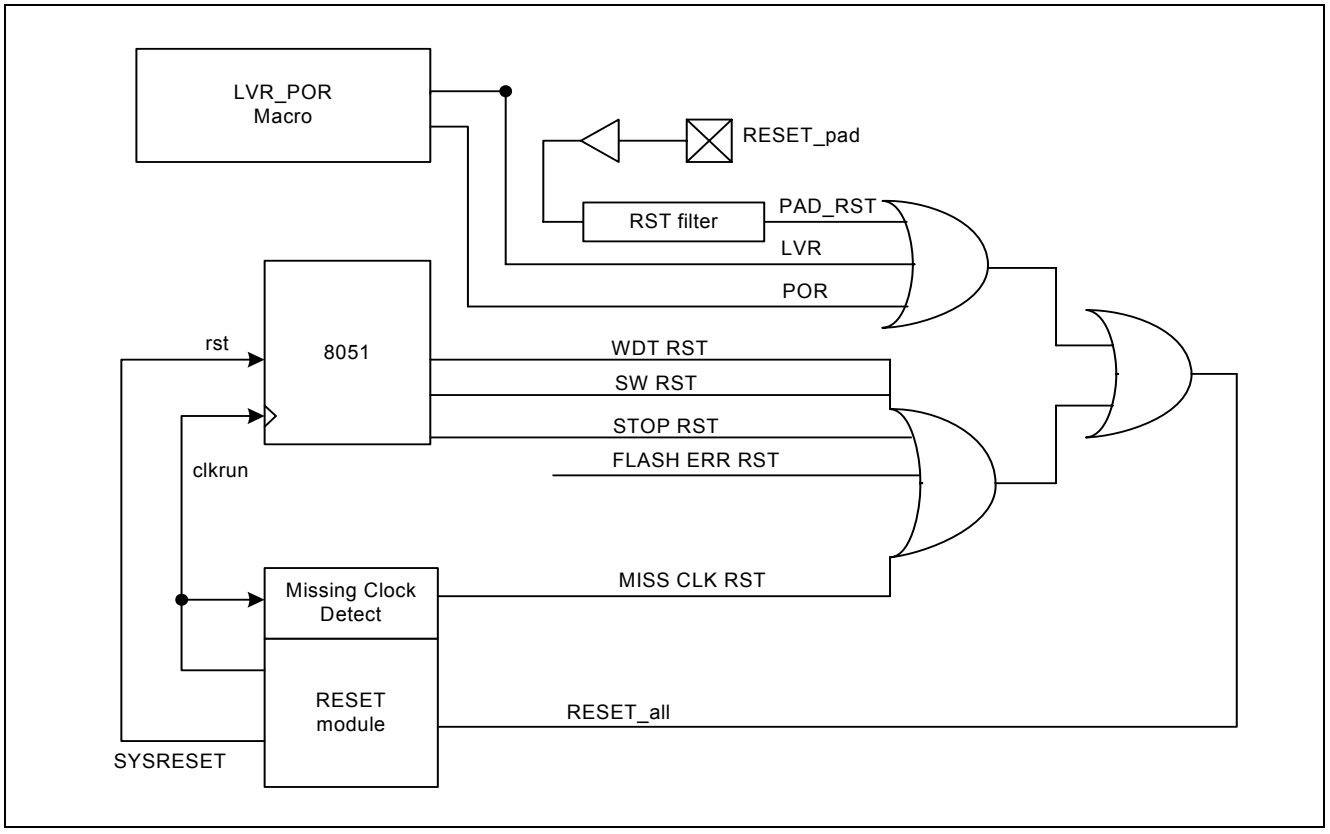


Figure 5-6 Reset sources

5.7.2. Power-On Reset (POR)

A POR is generated when VDD is rising from 0v. When VDD rises to an acceptable level (~1.5V), the power on reset circuit will starts a power-on sequence. After that, the system starts to activate and will operate in target speed. The POR will reset whole chip and registers.

5.7.3. Low Voltage Reset (LVR)

The on-chip Low Voltage Reset (LVR) circuitry forces the system entering reset state when power supplying voltage falls below the specific LVR trigger voltage. This function prevents MCU from working at an invalid operating voltage range.

To enable or disable this function, SYSCON[7] can be set. If this function is enabled, the LVR circuit will monitor power level while chip is operating. If the power is lower than the specific level for a specific period, the system reset will take place and go to initial state. The trigger level of LVR can be selected by SYSCON[1:0]. Table 5-35 shows the three trigger levels in GPM8F2702A.

5.7.4. Pad Reset (PAD_RST)

The GPM8F2702A provides an external pin to force the system returning to its initial status when the RSTPIN_ENB bit of CONFIG_BYTE is set to “0”. If the P32 is set as reset pin, its pull low resistor is forced to enable automatically (the bit2 of P3_PU/P3_PD is forced to 0/1). The RESET pin is high active as shown in Figure 5-7. When the RESET pin equals to VDD, system will be forced to enter reset state, execute instruction from address 0x0000 and all registers go to default state.

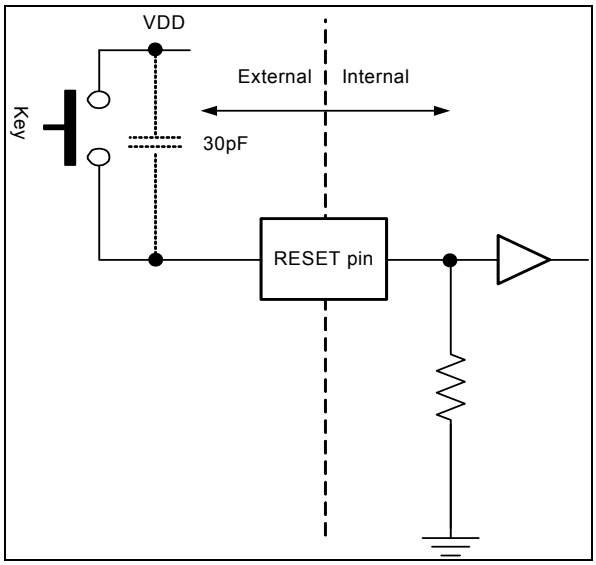


Figure 5-7 Pad reset circuit

CONFIG_BYTE	Address: 0x7FF (Program Memory)			CONFIG_BYTE Register				
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	PUEN	--	RSTPIN_ENB	--	CODE_LOCK
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:5	--	R	Reserved	
4	PUEN	R/W	GPIO IO pull up or low select bit 0: set all GPIO as pull low after reset status 1: set all GPIO as pull high after reset status	
3	--	R	Reserved	
2	RSTPIN_ENB	R/W	External reset pin enable bit 0: set P32 as external reset pin 1: set P32 as GPIO	
1	--	R	Reserved	
0	CODE_LOCK	R/W	Program memory protection enable bit 0: CODE is locked 1: CODE is unlocked	

Table 5-34 The CONFIG_BYTE register

5.7.5. Watchdog Timer Reset (WDT_RST)

On-chip watchdog circuitry makes the device entering reset state when MCU goes into unknown state and has no watchdog cleared information. This function prevents the MCU to be stuck in an abnormal condition. The WDT can be enabled or disabled through WDCON register bit 1. At any time prior to reaching its user selected terminal value, software can set the Reset Watchdog Timer (WDCON[0]) bit. If RWT is set before the timeout is reached, the timer will start over. If timeout is reached without RWT being set, the watchdog will reset the CPU. Hardware will automatically clear RWT after software sets it. When the reset occurs, the Watchdog Timer Reset Flag (RSTSTS[2]) will automatically be set to indicate the cause of the reset, however software must clear this bit manually. WDCON register is a timed access register that prevent it from accidental writes. TA is located at 0xEB. Correct sequence, 0xAA and 0x55, is required before write to WDCON register. Reading from such register is not protected. The Watchdog has four timeout selections based on the system clock frequency. The selections are a pre-selected number of clocks and can be set by CKCON[7:6]. Therefore, the actual timeout interval is dependent on the SYSCLK frequency. Figure 5-8 shows the block diagram of Watchdog timer.

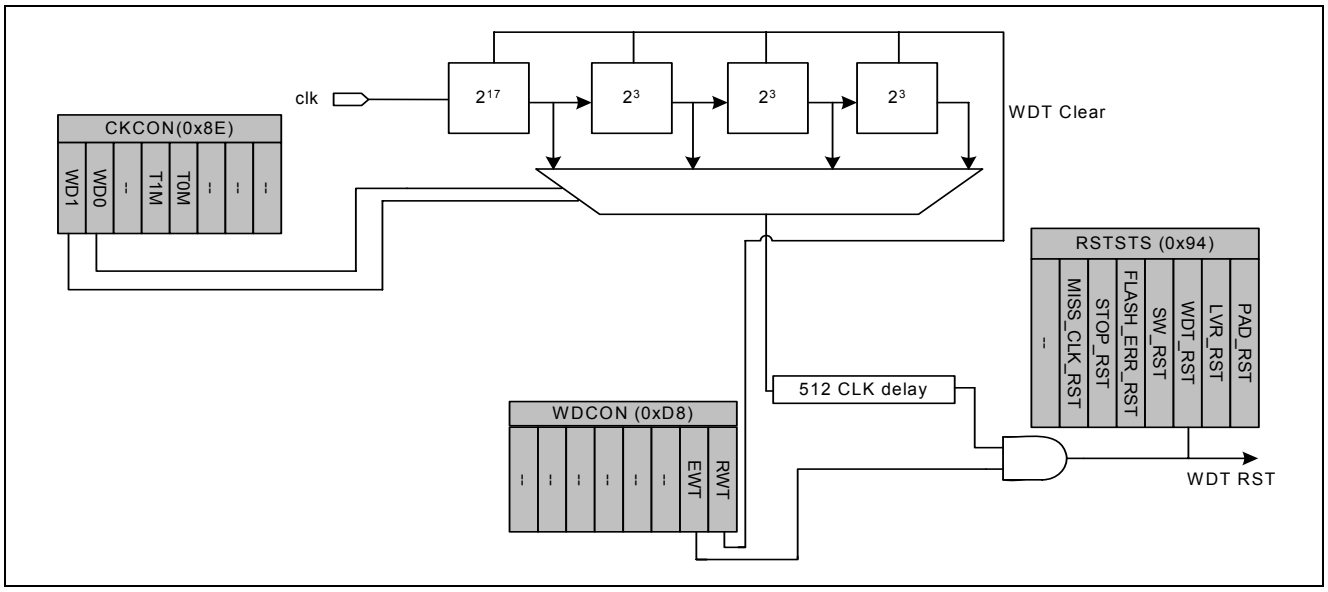


Figure 5-8 The block diagram of Watchdog timer

5.7.6. Other Reset Sources

Other reset sources includes Software Reset (SW_RST), STOP mode Reset (STOP_RST), Flash Error Reset (FLASH_ERR_RST), and missing system clock Reset (MISS_CLK_RST). Software Reset is occurred when writing key codes, 0x3c and 0xc3, to TA register (0xEB). The timing does not matter, but the key codes must be written in order before SW reset take place. STOP mode Reset is enabled by setting PCON[3] bit. This is the reset source when system is reset from STOP mode.

Flash Error Reset is the reset source when three flash related errors are arisen. The first error is to access the exceeding ROM address (>0x7FF). The second error is when flash is programmed in a wrong way or to program READONLY_PAGE. The third error is to program CONFIG_BYTE. Each flash error related reset source can be enabled or disabled by clearing or setting a bit in the RSTCON (0x94) as shown in Table 5-40. The corresponding flag when flash error reset occurs can be observed in FLASHERRF register which is shown in Table 5-41. Missing system clock Reset is the reset when system clock is missed over 4095 IOSC clocks if external crystal is utilized as clock source. There are seven reset status flag can be monitored by RSTSTS register which is shown as Table 5-42.

SYSCON	**Address: 0xAE**				**System Control Register**			
Bit	7	6	5	4	3	2	1	0
Function	LVRENB	--	--	--	--	--	LVRSEL1	LVRSEL0
Default	0	0	0	0	0	0	0	0
Key Code	0xFF, 0x00							

Bit	Function	Type	Description	Condition
7	LVRENB	R/W	LVR enable control 0 : enable LVR function 1 : disable LVR function	
6:0	--	R/W	Reserved	
1:0	LVRSEL[1:0]	R/W	LVR trigger level select bit LVRSEL[1:0] LVR Trigger Level 00 <1.92V 01 <2.61V 10 <4.25V 11 <1.92V	

Table 5-35 SYSCON register

WDCON			Address: 0xD8		Watchdog Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	EWT	RWT
Default	0	0	0	0	0	0	0	0
Key Code	0xAA, 0x55							

Bit	Function	Type	Description	Condition
7:2	--	R/W	Reserved	
1	EWT	R/W	Watchdog timer reset enable bit 0: Disable 1: Enable	
0	RWT	R/W	Reset watchdog timer 0: NA 1: Reset	

Table 5-36 WDCON register

TA			Address: 0xEB		Timed Access Protection Register			
Bit	7	6	5	4	3	2	1	0
Function	Timed Access protection register							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
0	TA[7:0]	R/W	Timed Access protection register	

Note: Some protected registers are needed to write correct key code to TA register before write data to them.

Table 5-37 TA register

CKCON			Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	--	T1M	T0M	--	--	--
Default	0	0	0	0	0	0	0	1

Bit	Function	Type	Description	Condition
7:6	WD[1:0]	R/W	Watchdog timeout selection bits WD[1:0] Watchdog internal Number of clocks 00 2^{17} 131072 01 2^{20} 1048576 10 2^{23} 8388608 11 2^{26} 67108864	
5	--	R/W	Reserved	
4	T1M	R/W	Division selection of the system clock that drives Timer 1 0: Timer 1 uses a divide-by-12 of the system clock frequency 1: Timer 1 uses a divide-by-4 of the system clock frequency	
3	T0M	R/W	Division selection of the system clock that drives Timer 0 0: Timer 0 uses a divide-by-12 of the system clock frequency 1: Timer 0 uses a divide-by-4 of the system clock frequency	
2:0	--	R/W	Reserved	

Table 5-38 CKCON register

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	--	CPU_IDLE	PWE	STOP_RST_EN	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	--	R/W	Reserved	
5	CPU_IDLE	R/W	IDLE mode enable bit 0: IDLE mode disabled ; 1: IDLE mode entered	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3	STOP_RST_EN	R/W	Wakeup state selection bit 0: Next instruction state after wakeup 1: Reset state afer wakeup	
2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-39 PCON register

RSTCON			Address: 0x8F			Flash Error RESET Enable Control Register		
Bit	7	6	5	4	3	2	1	0
Function	CB_P_ENB	--	FLASH_FLOW _ENB	ERR_XROM _ENB	--	--	MISS_CLK _ENB	FLASH_ERR __ENB
Default	0	0	0	0	0	0	0	0
Key Code	0x4F, 0x72, 0x7A							

Bit	Function	Type	Description	Condition
7	CB_P_ENB	R/W	CONFIG_BYTE program reset disable control bit	
6	--	R/W	Reserved	
5	FLASH_FLOW_ ENB	R/W	Error flash flow/ READONLY_PAGE program reset disable control bit	
4	ERR_XROM_ENB	R/W	Error ROM address exceed reset disable control bit	
3	--	R/W	Reserved	
2	--	R/W	Reserved	
1	MISS_CLK _ ENB	R/W	Miss clock reset disable control bit	
0	FLASH_ERR _ ENB	R/W	Global Flash related error reset disable control bit	

Table 5-40 RSTCON register

FLASHERRF			Address: 0xA6		Flash Error RESET Status Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	CB_P_F	--	FLASH_FLOW_F	ERR_XROM_F	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CB_P_F	R/W	Error CONFIG_BYTE program reset flag	
6	--	R/W	Reserved	
5	FLASH_FLOW_F	R/W	Error flash flow/READONLY_PAGE program reset flag	
4	ERR_XROM_F	R/W	Error ROM address exceed reset flag	
3	--	R/W	Reserved	
2	--	R/W	Reserved	
1	--	R/W	Reserved	
0	--	R/W	Reserved	

Table 5-41 FLASHERRF register

RSTSTS			Address: 0x94		RESET Status Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	--	MISS_CLK_RST	STOP_RST	FLASH_ERR_RST	SW_RST	WDT_RST	LVR_RST	RAD_RST
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	MISS_CLK_RST	R/W	RESET from system clock missing clock	
5	STOP_RST	R/W	RESET from STOP mode	
4	FLASH_ERR_RST	R/W	RESET from FLASH error	
3	SW_RST	R/W	RESET from SW RST	
2	WDT_RST	R/W	RESET from WDT	
1	LVR_RST	R/W	RESET from LVR	
0	PAD_RST	R/W	RESET from RESET PAD	

Table 5-42 RSTSTS register

5.8. I/O Ports

5.8.1. Introduction

The GPM8F2702A has two ports, including standard Port 0, Port 3. These port pins may be multiplexed with an alternate function for the peripheral features on the device. In general, when an initial reset state occurs, all ports are used as a general purpose input port with open-drain structure. User can select IO as pull low or pull high after reset status by setting the PUEN bit of CONFIG_BYTE. All the ports can be programmable pull high/low by PU and PD registers. The PU and PD registers of Port 0 are controlled by 0x9A and 0x9B and the PU and PD registers of P3 are controlled by 0xA2 and 0xA3. Read and write accesses to the I/O port are performed via their corresponding SFRs P0(0x80) and P3(0xB0). When PU and PD are enabled at the same time, the port can output high or low depending on the data. Table 5-43 and Table 5-44 show the truth table of analog pad and digital pad respectively. In GPM8F2702A, P0[7:0], P3[2:0] and P3[7:5]can be analog pad for special function. P0[7:0] are used for ADC input. P3[2:0] and P3[7:5] are used for compare input. The detail descriptions of analog function are in corresponding sections. The built-in pull high/low resister is 50KΩ typically. All of port pins in GPM8F2702A are implemented with 30ns slew rate control. Figure 5-9 and Figure 5-10 show the block diagrams of analog pad and digital pad respectively.

PU	PD	DATA	ANAEN	PAD
0	0	0	0	Driving Low
0	0	1	0	Floating
0	1	0	0	Driving Low
0	1	1	0	Pull low
1	0	0	0	Illegal
1	0	1	0	Pull high
1	1	0	0	Driving Low
1	1	1	0	Driving High
x	x	x	1	Floating

Table 5-43 The truth table of analog pad

PU	PD	DATA	PAD
0	0	0	Driving Low
0	0	1	Floating
0	1	0	Driving Low
0	1	1	Pull low
1	0	0	Illegal
1	0	1	Pull high
1	1	0	Driving Low
1	1	1	Driving High

Table 5-44 The truth table of digital pad

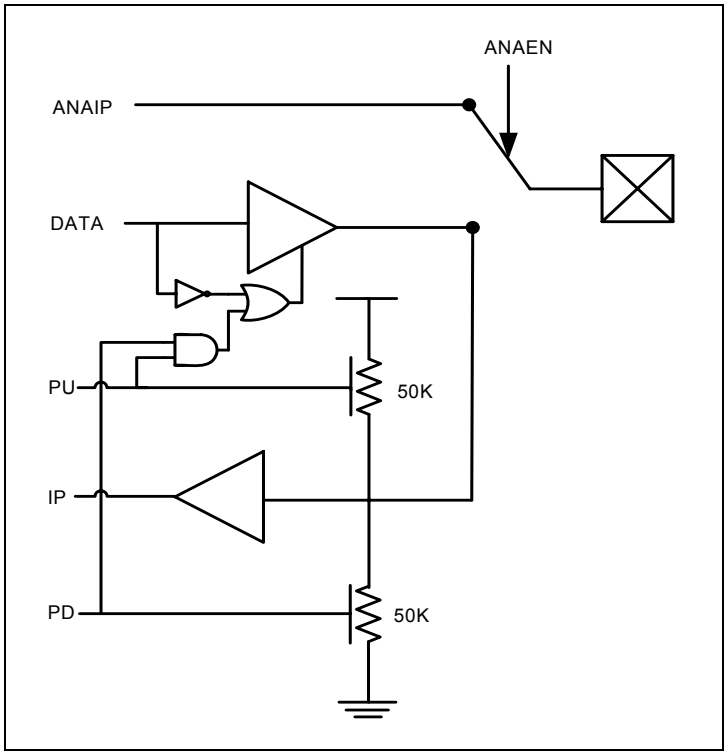


Figure 5-9 The block diagram of analog pad

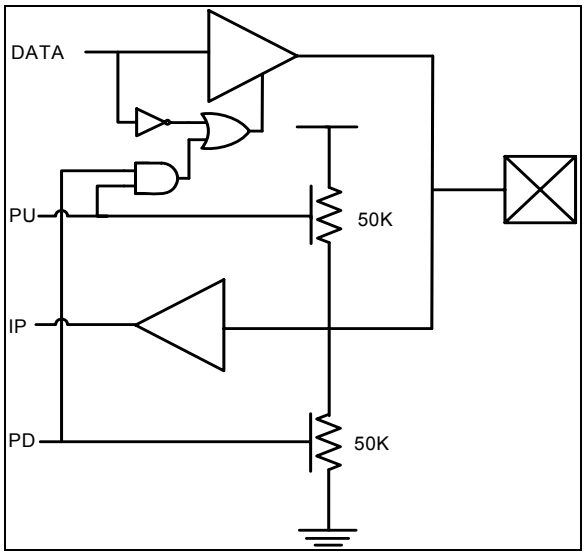


Figure 5-10 The block diagram of digital pad

CONFIG_BYTE	Address: 0x7FF (Program Memory)			CONFIG_BYTE Register				
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	PUEN	--	RSTPIN_ENB	--	CODE_LOCK
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:5	--	R	Reserved	
4	PUEN	R/W	GPIO IO pull up or low select bit 0: set all GPIO as pull low after reset status 1: set all GPIO as pull high after reset status	
3	--	R	Reserved	
2	RSTPIN_ENB	R/W	External reset pin enable bit 0: set P32 as external reset pin 1: set P32 as GPIO	
1	--	R	Reserved	
0	CODE_LOCK	R/W	Program memory protection enable bit 0: CODE is locked 1: CODE is unlocked	

Table 5-45 The CONFIG_BYTE register

P0	Address: 0x80			Port0 Register				
Bit	7	6	5	4	3	2	1	0
Function	--	--	P05	P04	P03	P02	P01	P00
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	P0[5:0]	R/W	Port0	

Table 5-46 P0 register

P3			Address: 0xB0		Port3 Register			
Bit	7	6	5	4	3	2	1	0
Function	P37	P36	P35	P34	P33	P32	P31	P30
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P3[7:0]	R/W	Port3	

Table 5-47 P3 register

P0_PU			Address: 0x9A		Port0 pull up configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	P05_PU	P04_PU	P03_PU	P02_PU	P01_PU	P00_PU
Default	0	0	Note1	Note1	Note1	Note1	Note1	Note1

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	P0_PU[5:0]	R/W	Port0 pull up control bits 0: floating 1: pull up	

Table 5-48 P0_PU register

P0_PD			Address: 0x9B		Port0 pull down configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	P05_PD	P04_PD	P03_PD	P02_PD	P01_PD	P00_PD
Default	0	0	Note1	Note1	Note1	Note1	Note1	Note1

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	P0_PD[5:0]	R/W	Port0 pull down control bits 0: floating 1: pull down	

Note1: If P0_PU and P0_PD are setting to '1' simultaneously, P0 will be output mode

Note2: P00_PU ~ P05_PU/P00_PD~P05_PD are all "0" during reset status, and they can be set or clear by PUEN bit of CONFIG_BYTE after reset status.

Table 5-49 P0_PD register

P3_PU			Address: 0xA2		Port3 pull up configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P37_PU	P36_PU	P35_PU	P34_PU	P33_PU	P32_PU	P31_PU	P30_PU
Default	Note1	Note1	Note1	Note1	Note1	Note1	Note1	Note1

Bit	Function	Type	Description	Condition
7:0	P3_PU[7:0]	R/W	Port3 pull up control bits 0: floating 1: pull up	

Table 5-50 P3_PU register

P3_PD			Address: 0xA3		Port3 pull down configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P37_PD	P36_PD	P35_PD	P34_PD	P33_PD	P32_PD	P31_PD	P30_PD
Default	Note1	Note1	Note1	Note1	Note1	Note2	Note1	Note1

Bit	Function	Type	Description	Condition
7:0	P3_PD[7:0]	R/W	Port3 pull down control bits 0: floating 1: pull down	

Note1: If P3_PU and P3_PD are setting to '1' simultaneously, P3 will be output mode

Note2: P30_PU~P37_PU/ P30_PD~P31_PD and P33_PD~P37_PD are all "0" during reset status, and they can be set or clear by setting the PUEN bit of CONFIG_BYTE after reset status.

Note3: P32_PD is "1" during reset status, and it can be set or clear by setting the PUEN bit of CONFIG_BYTE after reset status. If the P32 is set as external reset pin (RSTPIN_ENB bit of CONFIG_BYTE is set to "0"), P32_PU and P32_PD are force to "0" and "1" respectively.

Table 5-51 P3_PD register

ADAEN			Address: 0xF3		ADC Analog PAD Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	P05_AEN	P04_AEN	P03_AEN	P02_AEN	P01_AEN	P00_AEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	P05_AEN	R/W	P05 analog PAD enable control bit 0: P05 can be I/O PAD 1: P05 can be analog PAD	
4	P04_AEN	R/W	P04 analog PAD enable control bit 0: P04 can be I/O PAD 1: P04 can be analog PAD	
3	P03_AEN	R/W	P03 analog PAD enable control bit 0: P03 can be I/O PAD 1: P03 can be analog PAD	
2	P02_AEN	R/W	P02 analog PAD enable control bit 0: P02 can be I/O PAD 1: P02 can be analog PAD	
1	P01_AEN	R/W	P01 analog PAD enable control bit 0: P01 can be I/O PAD 1: P01 can be analog PAD	
0	P00_AEN	R/W	P00 analog PAD enable control bit 0: P00 can be I/O PAD 1: P00 can be analog PAD	

Table 5-52 ADAEN register

IOSCCON			Address: 0xF9		IOSC Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	XTAL_PAD_EN	XTAL_EN	--	CLKDIV[2:0]		
Default	0	0	0	0	0	0	1	0

Bit	Function	Type	Description
7:6	--	R/W	Reserved
5	XTAL_PAD_EN	R/W	If using XTAL, XTAL_PAD_EN should be set to “1” XTI and XTO can be analog PAD.
4	XTAL_EN	R/W	0: ROSC 1: XTAL
3	--	R/W	Reserved
2:0	CLK_DIV	R/W	System Clock source divider CLK_DIV Clock control 000 SYSCLK_SOURCE 001 SYSCLK_SOURCE/2 010 SYSCLK_SOURCE/4 011 SYSCLK_SOURCE/8 100 SYSCLK_SOURCE/16 101 SYSCLK_SOURCE/32 110 SYSCLK_SOURCE/64 111 SYSCLK_SOURCE/1.5

Table 5-53 The IOSCCON register

CMPAEN			Address: 0xBB		Comparator Analog PAD Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	P37_AEN	P36_AEN	P35_AEN	P32_AEN	P31_AEN	P30_AEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	P37_AEN	R/W	P37 analog PAD enable control bit 0: P37 can be I/O PAD 1: P37 can be analog PAD	
4	P36_AEN	R/W	P36 analog PAD enable control bit 0: P36 can be I/O PAD 1: P36 can be analog PAD	
3	P35_AEN	R/W	P35 analog PAD enable control bit 0: P35 can be I/O PAD 1: P35 can be analog PAD	
2	P32_AEN	R/W	P32 analog PAD enable control bit 0: P32 can be I/O PAD 1: P32 can be analog PAD	
1	P31_AEN	R/W	P31 analog PAD enable control bit 0: P31 can be I/O PAD 1: P31 can be analog PAD	
0	P30_AEN	R/W	P30 analog PAD enable control bit 0: P30 can be I/O PAD 1: P30 can be analog PAD	

Table 5-54 CMPAEN register

5.9. Timer Module

5.9.1. Introduction

GPM8F2702A is equipped with three timers. They are Timer 0, Timer 1 and Timer 2 respectively. In addition, Timer 2 also features Compare/Capture/Reload function. All of these three timers are up-count timers and 16-bit timer/counter. Each timer's function is described in the following sections.

5.9.2. Timer 0/1

Timer 0 and Timer 1 are fully compatible with the standard 8051 timers. Each timer consists of two 8-bit registers TH0(0x8C), TL0(0x8A), TH1(0x8D), TL1(0x8B). Timers 0 and Timer 1 work in the same three modes except for mode 3 and the related control registers are TMOD(0x89), TCON(0x88) and CKCON(0x8E) registers. In the timer mode, timer registers are incremented every 4/12 SYSCLK periods depends on CKCON(0x8E) setting, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on theirs corresponding input pins: T0 or T1. The input pins are sampled every CLK period.

TH0			Address: 0x8C		Timer0 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH0[7:0]	R/W	Timer 0 Load value – high byte	

Table 5-55 TH0 register

TL0			Address: 0x8A		Timer0 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL0[7:0]	R/W	Timer 0 Load value – low byte	

Table 5-56 TL0 register

TH1			Address: 0x8D		Timer1 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH1[7:0]	R/W	Timer 1 Load value – high byte	

Table 5-57 TH1 register

TL1			Address: 0x8B		Timer1 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL1[7:0]	R/W	Timer 1 Load value – low byte	

Table 5-58 TL1 register

TMOD			Address: 0x89		Timer0/1 Control Mode Register			
Bit	7	6	5	4	3	2	1	0
Function	GATE1	CT1	M11	M10	GATE0	CT0	M01	M00
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	GATE1	R/W	Gating control 0: Timer 1 enabled while TR1 control bit is set 1: Timer 1 enabled while GATE1 pin is high and TR1 control bit is set	
6	CT1	R/W	Counter or timer select bit 0: Timer mode, internally clocked 1: Counter mode, Timer 1 clock source is from T1 pin	
5:4	M1[1:0]	R/W	Mode select bits of timer 1, which is tabled as Table 5-60	
3	GATE0	R/W	Gating control 0: Timer 0 enabled while TR0 control bit is set 1: Timer 0 enabled while GATE0 pin is high and TR0 control bit is set	
2	CT0	R/W	Counter or timer select bit 0: Timer mode, internally clocked 1: Counter mode, Timer 0 clock source is from T0 pin	
1:0	M0[1:0]	R/W	Mode select bits of timer 0, which is tabled as Table 5-60	

Table 5-59 TMOD register

M1	M0	Mode	Function description
0	0	0	TH0/1 operates as 8-bit timer/counter with a divide by 32 prescaler served by lower 5-bit of TL0/1.
0	1	1	16-bit timer/counter. TH0/1 and TL0/1 are cascaded
1	0	2	TL0/1 operates as 8-bit timer/counter with 8-bit auto-reload by TH0/1
1	1	3	TL0 is configured as 8-bit timer/counter controlled by the standard Timer 0 bits. TH0 is an 8-bit timer controlled by the Timer 1 controls bits. Timer 1 holds its count.

Table 5-60 Four modes of Timer 0 and Timer 1

TCON			Address: 0x88		Timer0/1 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TF1	R/W	Timer 1 interrupt (overflow) flag	
6	TR1	R/W	Timer 1 run control bit 0: disabled 1: enabled	
5	TF0	R/W	Timer 0 interrupt (overflow) flag	

Bit	Function	Type	Description	Condition
4	TR0	R/W	Timer 0 run control bit 0: disabled 1: enabled	
3	IE1	R/W	INT1 interrupt flag	
2	IT1	R/W	INT1 level (at 0)/ edge (at 1) sensitivity	
1	IE0	R/W	INT0 interrupt flag	
0	IT0	R/W	INT0 level (at 0)/ edge (at 1) sensitivity	

Table 5-61 TCON register

CKCON	Address: 0x8E				Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	--	T1M	T0M	--	--	--
Default	0	0	0	0	0	0	0	1

Bit	Function	Type	Description	Condition
7:6	WD[1:0]	R/W	Watchdog timeout selection bits WD[1:0] Watchdog internal Number of clocks 00 2^{17} 131072 01 2^{20} 1048576 10 2^{23} 8388608 11 2^{26} 67108864	
5	--	R/W	Reserved	
4	T1M	R/W	Division selection of the system clock that drives Timer 1 0: Timer 1 uses a divide-by-12 of the system clock frequency 1: Timer 1 uses a divide-by-4 of the system clock frequency	
3	T0M	R/W	Division selection of the system clock that drives Timer 0 0: Timer 0 uses a divide-by-12 of the system clock frequency 1: Timer 0 uses a divide-by-4 of the system clock frequency	
2:0	--	R/W	Reserved	

Table 5-62 CKCON register

5.9.2.1. Timer 0: Mode 0(13-Bit Timer/Counter)

In this mode, Timer 0 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer 0 interrupt flag TF0 is set. The counted input is enabled to the Timer 0 when TR0(TCON[4]) = 1 and either GATE0(TMOD[3]) = 0 or GATE0 input pin(P36)= 1. (Setting GATE0(TMOD[3]) = 1 allows the Timer 0 to be controlled by external input GATE0(P36), to facilitate pulse width measurements). The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Figure 5-11 shows the block diagram of Timer 0 for Mode 0.

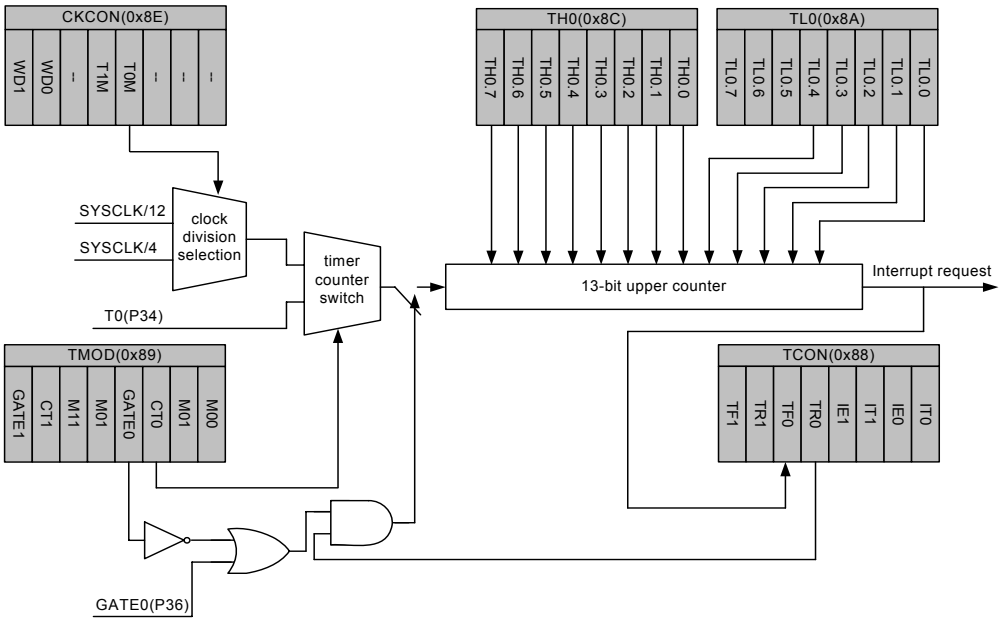


Figure 5-11 The block diagram of Timer 0 for Mode 0

5.9.2.2. Timer 0: Mode 1(16-Bit Timer/Counter)

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. The block diagram of Mode 1 is shown in Figure 5-12.

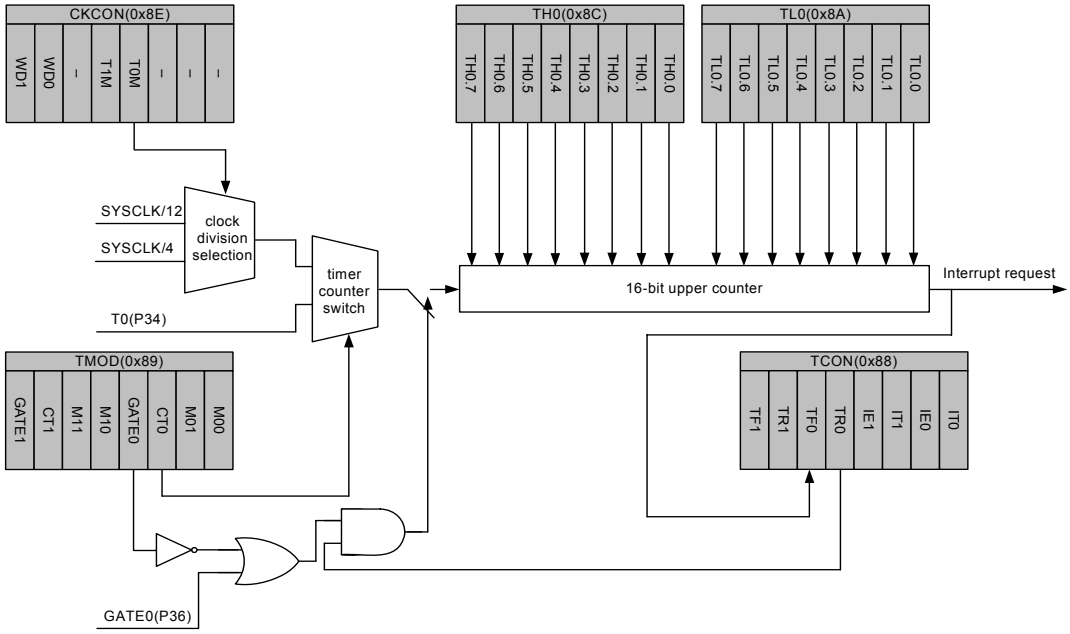


Figure 5-12 The block diagram of Timer 0 for Mode 1

5.9.2.3. Timer 0: Mode 2(8-Bit Timer/Counter with Auto-reload Function)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reloads, as shown in Figure 5-13. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is loaded by software. The reload leaves TH0 unchanged.

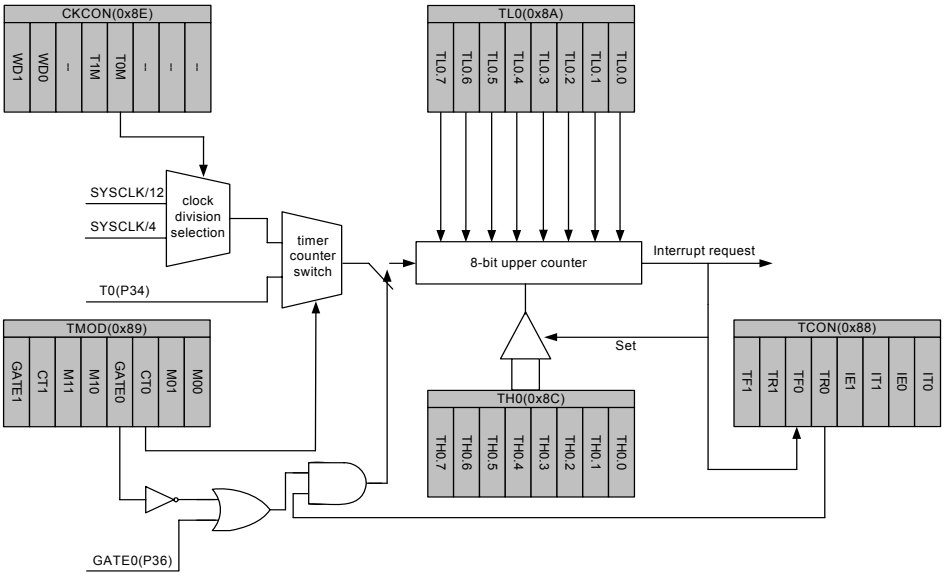


Figure 5-13 The block diagram of Timer 0 for Mode 2

5.9.2.4. Timer 0: Mode 3(Two 8-Bit Timers/Counters)

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The block diagram for Mode 3 on Timer 0 is shown in Figure 5-14. TL0 uses the Timer 0 control bits: CT0, GATE0, TR0, and TF0. TH0 is locked into a timer function and uses the TR1 and TF1 flags from Timer 1 and controls Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer/counter. When Timer 0 is in Mode 3, Timer 1 can be turned off by switching it into its own Mode 3, or can still be used by the serial channel as a baud rate generator, or in any application where interrupt from Timer 1 is not required.

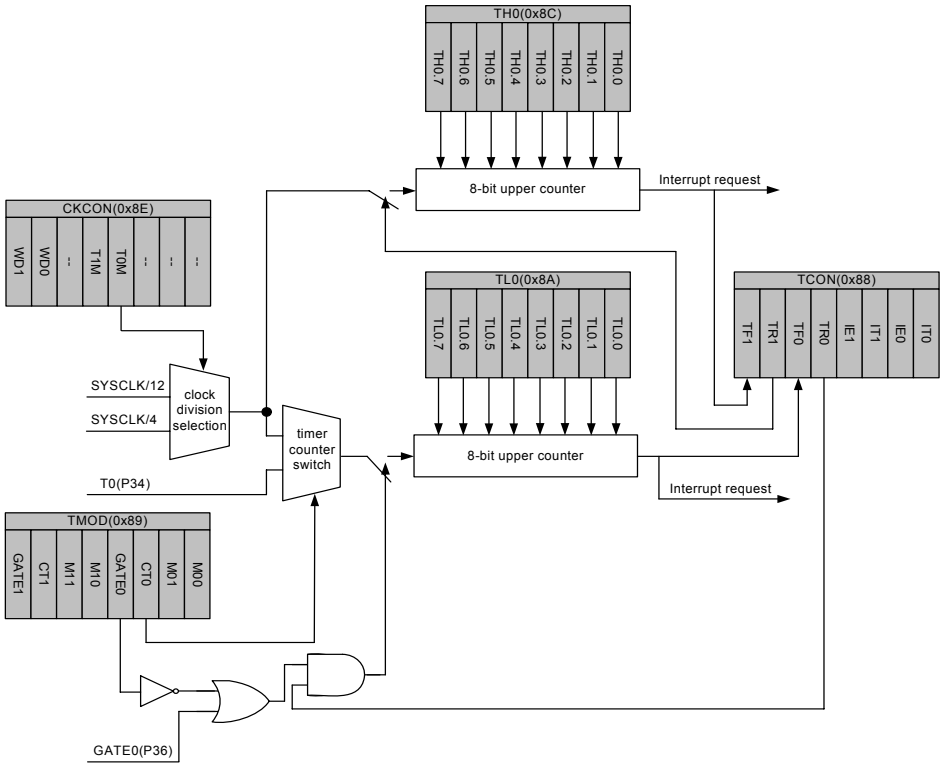


Figure 5-14 The block diagram of Timer 0 for Mode 3

5.9.2.5. Timer 1: Mode 0(13-Bit Timer/Counter)

In this mode, the Timer 1 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer 1 interrupt flag TF1 is set. The counted input is enabled to the Timer1 when TR1(TCON[6]) = 1 and either GATE1(TMOD[7]) = 0 or GATE1 input pin(P37)= 1. (Setting GATE1(TMOD[7]) = 1 allows the Timer1 to be controlled by external input GATE1(P37), to facilitate pulse width measurements). The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Figure 5-15 shows the block diagram of Timer1 for Mode 0.

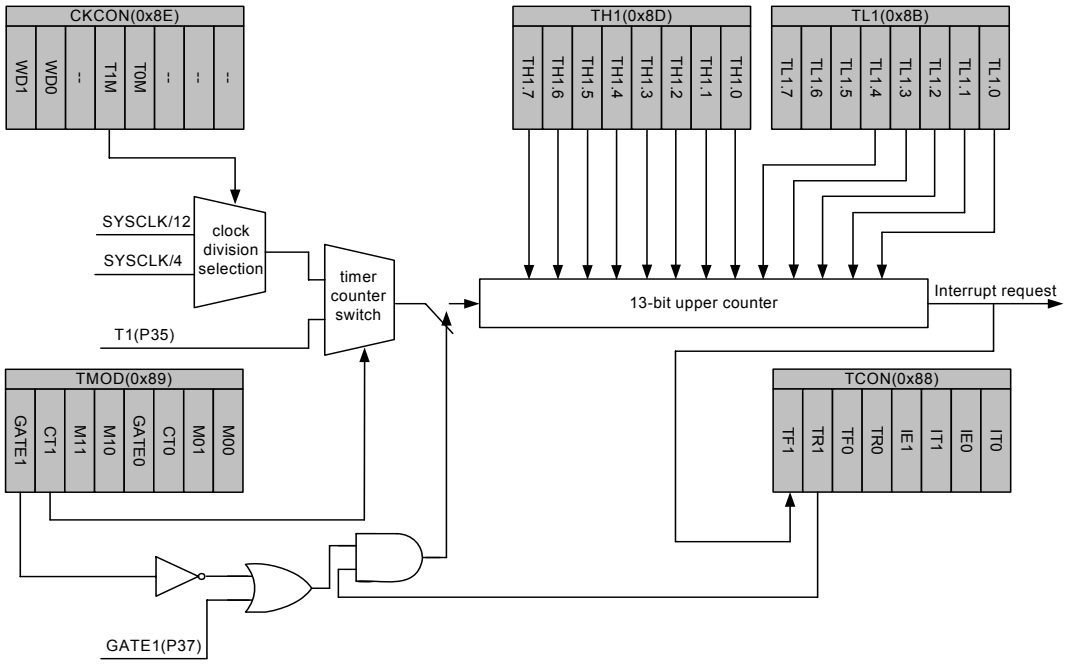


Figure 5-15 The block diagram of Timer 1 for Mode 0

5.9.2.6. Timer 1: Mode 1(16-Bit Timer/Counter)

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. The block diagram of Mode 1 is shown in Figure 5-16.

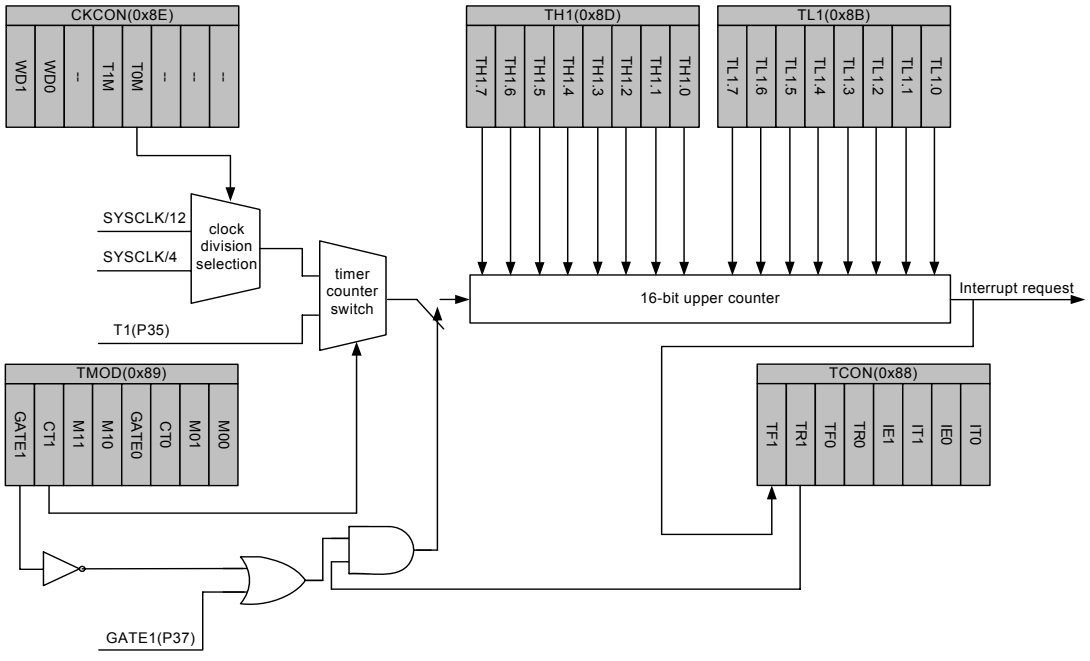


Figure 5-16 The block diagram of Timer 1 for Mode 1

5.9.2.7. Timer 1: Mode 2(8-Bit Timer/Counter with Auto-reload Function)

Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic reloads, as shown in Figure 5-17. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is loaded by software. The reload leaves TH1 unchanged.

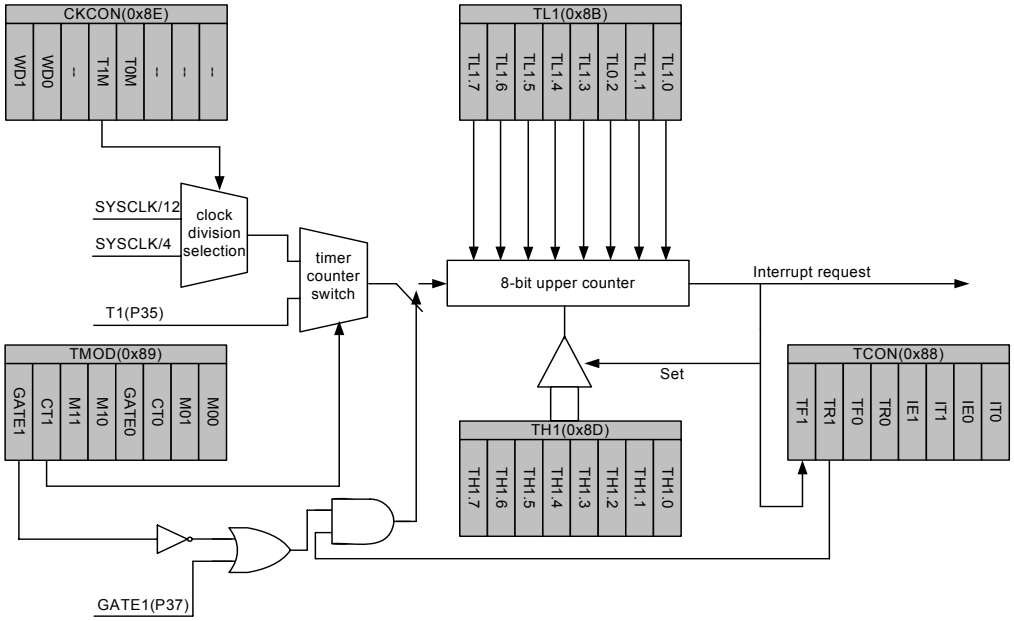


Figure 5-17 The block diagram of Timer 1 for Mode 2

5.9.2.8. Timer 1: Mode 3

Timer 1 in Mode 3 is has no timer function. The effect is the same as setting TR1=0.

5.9.3. Timer 2

The Timer 2, which is a 16-bit-wide register, can operate as timer. The additional Compare/Capture/Reload feature is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generator and event capturing like pulse generator, pulse width modulation, pulse width measuring etc. Figure 5-18 shows the block diagram of compare/capture function for Timer 2.

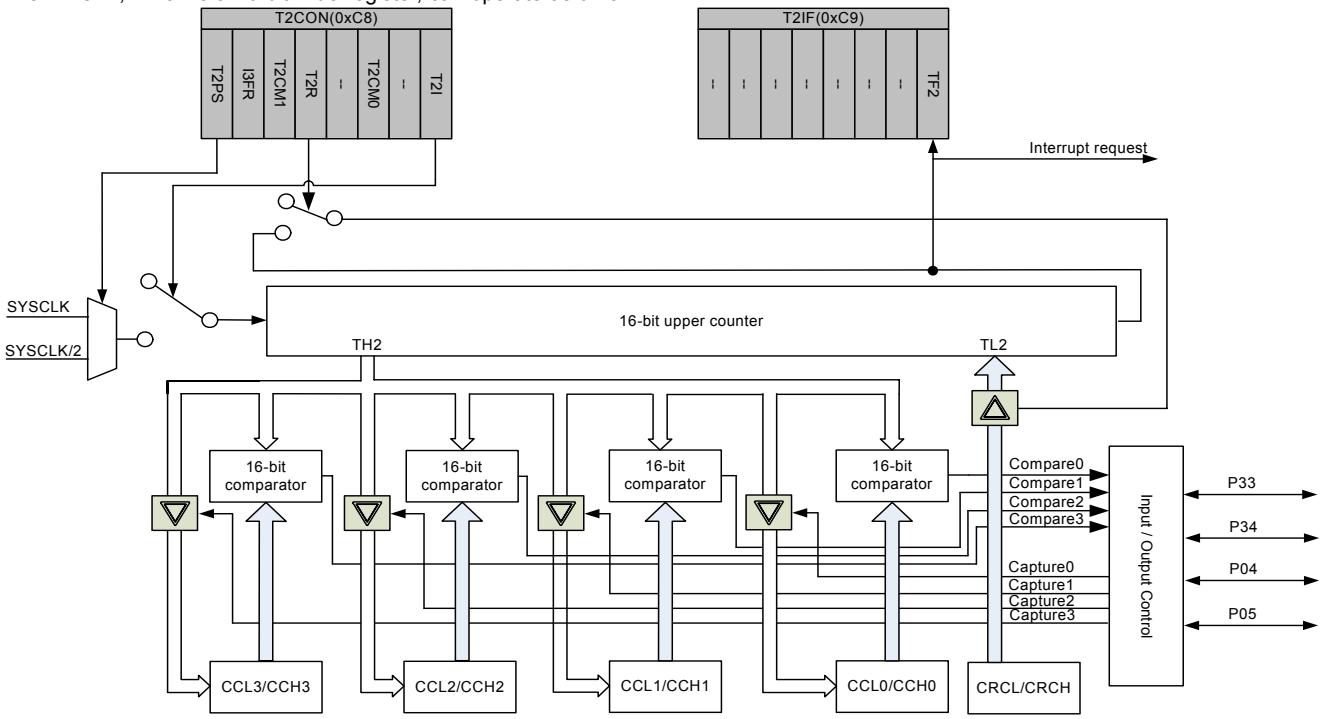


Figure 5-18 The block diagram of compare/capture function for Timer 2

5.9.3.1. Timer Mode

In timer function, the count rate is derived from the oscillator frequency. A prescaler offers the possibility of selecting a count rate of 1 or 1/2 of an oscillator frequency. Thus, the 16-bit timer register (consisted of TH2 and TL2) is either incremented in every 1 clock periods or in every 2 clock periods. The prescaler is selected by bit T2PS of T2CON.

5.9.3.2. Reload of Timer 2

The reload mode for timer 2 is selected by T2R bit of T2CON. When timer 2 rolls over from all 1's to all 0's, not only TF2 is set but also timer 2 registers is loaded with the 16-bit value from CRC register. Required CRC value can be preset by software. The reload occurs in the same clock cycle in which TF2 is set, thus overwriting the count value 0x0000.

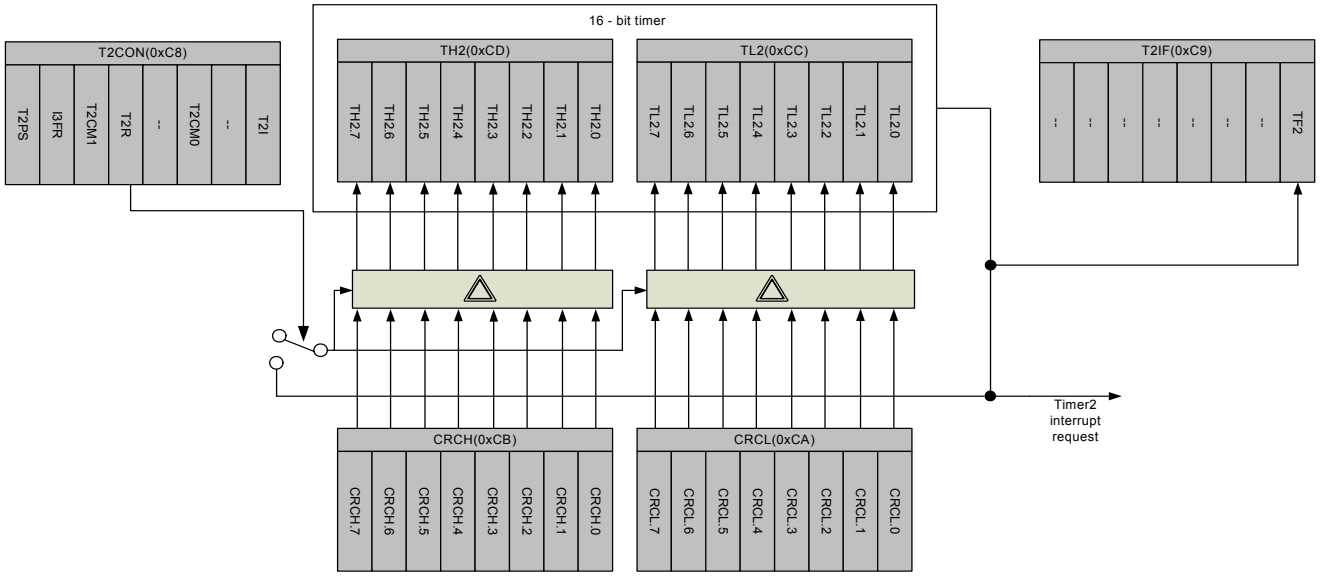


Figure 5-19 The block diagram of reload function for Timer 2

5.9.3.3. Compare Functions

The 16-bit value stored in a compare/capture register is compared with the contents of the timer register. If the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin, and an interrupt is requested. The contents of a compare register can be considered as time stamp at which a dedicated output reacts in a predefined way (either with a positive or negative transition). Variation of this time stamp somehow changes the wave of a rectangular output signal at a port pin. This may - as a variation of the duty cycle of a periodic signal - be used for pulse width modulation as well as for a continually controlled generation of any kind of square waveforms. Two compare modes are implemented to cover a wide range of possible applications. The compare mode 0 and mode 1 are selected by bit T2CM0 and T2CM1 in special function register T2CON. In all compare modes, the new value arrives at certain pin of P3[4:3] and P0[5:4] within the same clock cycle in which the internal compare signal is activated.

❑ Compare Mode 0

In mode 0, upon matching the timer and compare register contents, an output signal changes from low to high. It goes back to a low level on timer overflow. Figure 5-20 shows a functional diagram of a port register in compare mode 0. The port register is directly controlled by the two signals: timer overflow and compare.

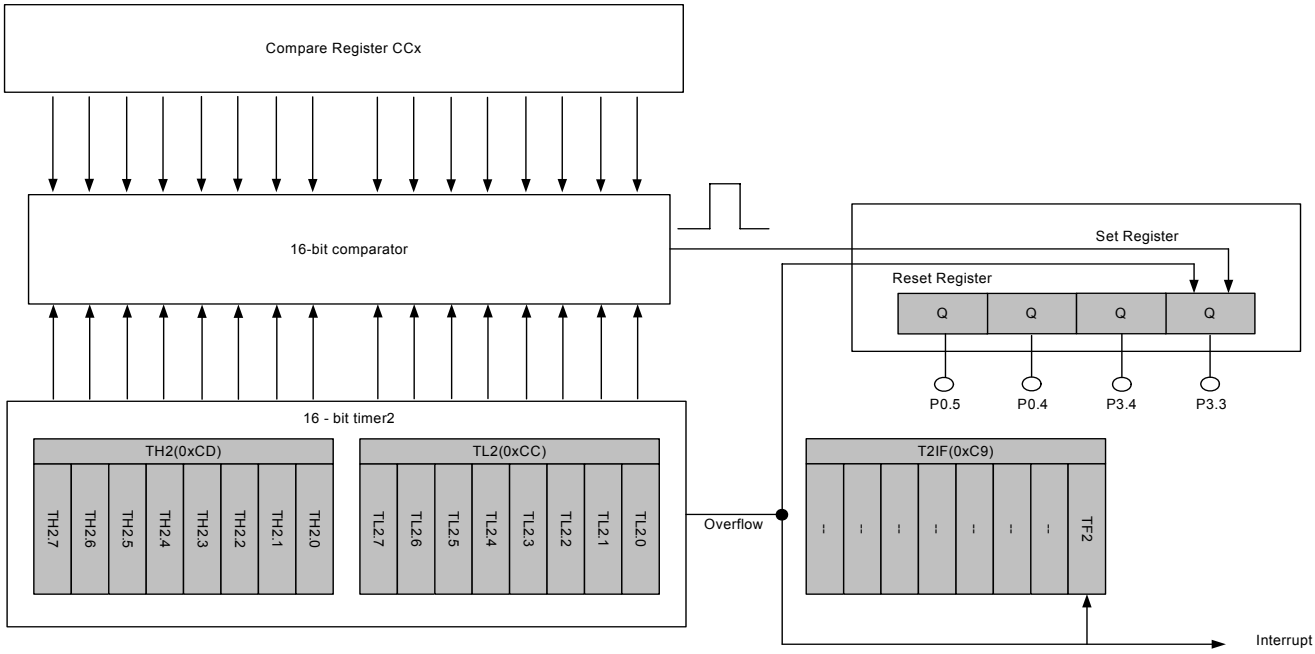


Figure 5-20 The block diagram of compare mode 0 for Timer 2

❑ Compare Mode 1

In compare mode 1, the 8-bit comparator is selected. Upon matching the timer and compare register (CCLx) contents, an output signal changes from low to high. It goes back to a low level on timer overflow. In mode 1, the CCHx is used as reload register of CCLx. It means that the CCLx register is loaded with the 8-bit value from CCHx register. Figure 5-21 shows a functional diagram of Timer 2 in compare mode 1.

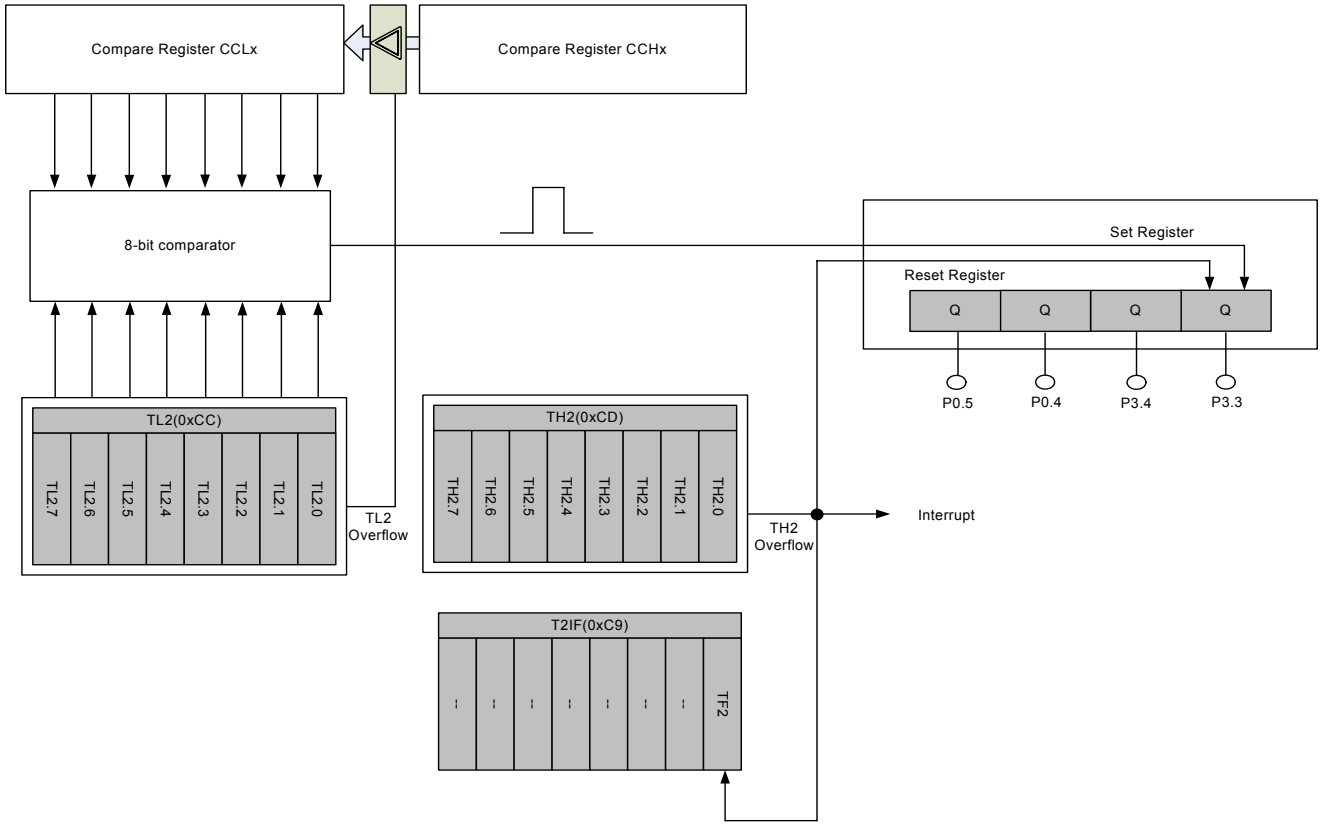


Figure 5-21 The block diagram of compare mode 1 for Timer 2

5.9.3.4. Capture Functions

Each of compare/capture registers include CC0, CC1, CC2 and CC3 register can be used to latch the current 16-bit value of the timer 2 registers TL2 and TH2. Two different modes are provided for this function.

❑ Capture Mode 0

In mode 0, an external event latches timer 2 contents to a dedicated capture register. The external event causing a capture is

- for the CC registers 1 to 3: a positive transition on pins CAPTURE1 to CAPTURE3
- for the CC0 register: a positive or negative transition on the CAPTURE0 pin, depending on the bit I3FR of T2CON. If the I3FR flag is cleared, a capture occurs in response to a negative transition; otherwise, a capture occurs in response to a positive transition on CAPTURE0 pin.

❑ Capture Mode 1

In mode 1, a capture will occur upon writing to the low order byte of the dedicated 16-bit capture register. This mode is provided to allow software reading of timer 2 contents on-the fly. The capture occurs in response to a write instruction to the low order byte of a capture register. The write-to-register signal (e.g. write-to-CCL0) is used to initiate a capture. The value written to the dedicated capture register is irrelevant for this function. The timer 2 contents will be latched into the appropriate capture register in the cycle following the write instruction. In this mode, no interrupt request will be generated.

Figure 5-22 and Figure 5-23 show functional diagrams of the timer 2 capture function.

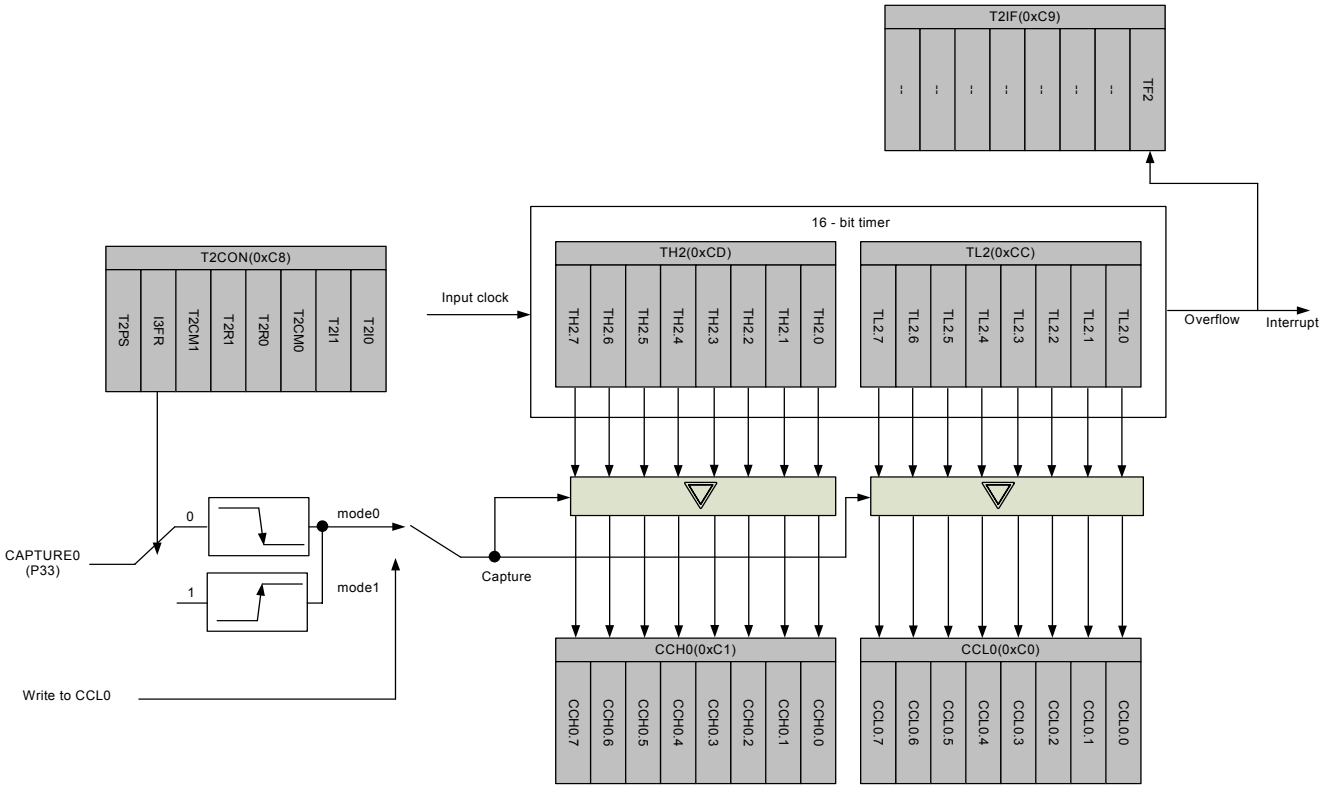


Figure 5-22 The block diagram of Timer 2 capture mode 0 for CCL0 and CCH0

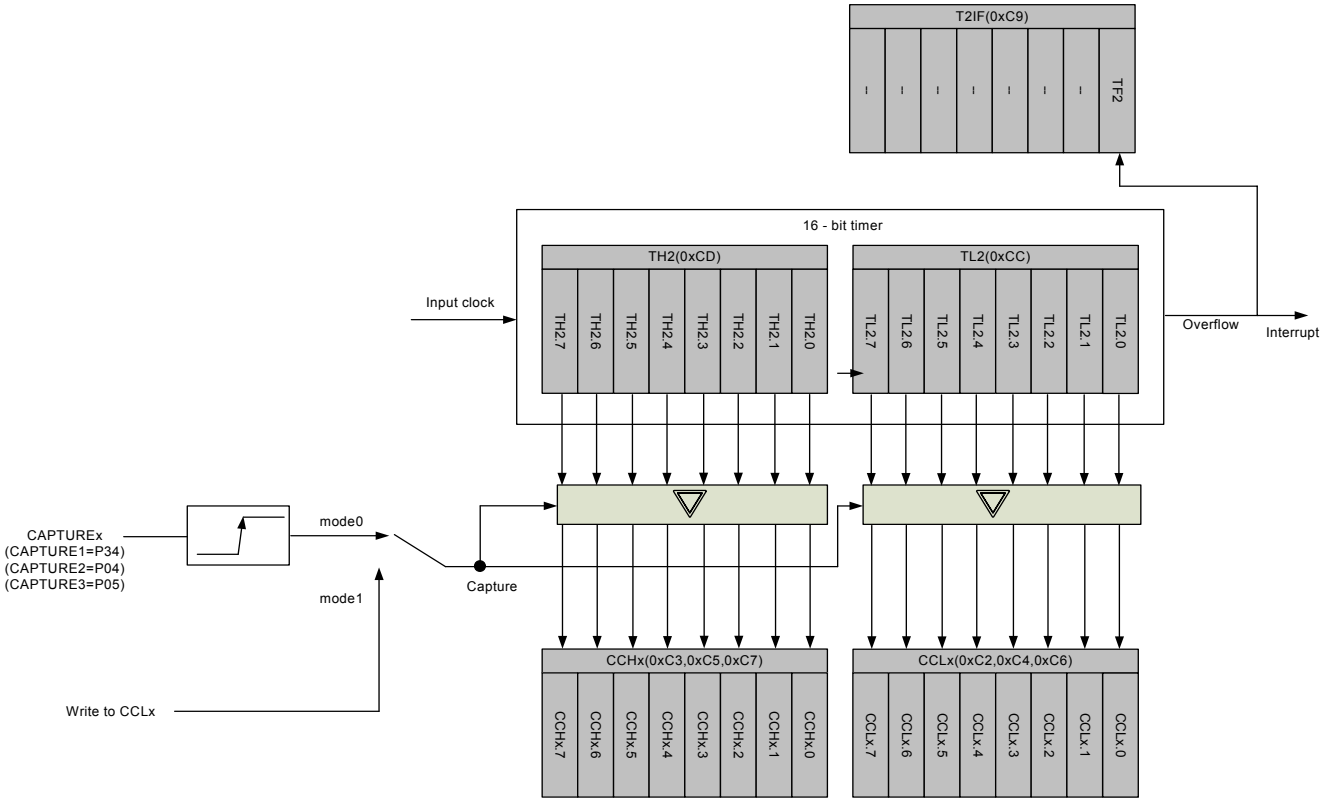


Figure 5-23 The block diagram of Timer 2 capture mode 0 for CCLx and CCHx (x=1, 2, 3)

5.9.3.5. Timer 2 Related Registers

T2CON			Address: 0xC8		Timer2 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	T2PS	I3FR	T2CM1	T2R	--	T2CM0	--	T2I
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	T2PS	R/W	Prescaler select bit 0: SYSCLK 1: SYSCLK/2	
6	I3FR	R/W	Interrupt edge activity selection bit of compare 0 function in combination with capture 0 function and register CRC Capture 0: 0: capture to CRC register occurs on a positive transition of CAPTURE0 pin 1: capture to CRC register occurs on a positive transition of CAPTURE0 pin	
5	T2CM1	R/W	Compare mode select bit for registers CRC, CC1, CC2, and CC3 0: Compare mode 1 is disable 1: Compare mode 1 is enable and compare mode 0 is force to disable	
4:3	T2R	R/W	Timer 2 auto-reload mode enable bit	
3	--	R/W	Reserved	
2	T2CM0	R/W	Compare mode select bit for registers CRC, CC1, CC2, and CC3 0: compare mode 0 is enable 1: compare mode 0 is disable	
1	--	R/W	Reserved	

Bit	Function	Type	Description	Condition
0	T2I	R/W	Timer 2 input selection bit 0: No input selected, timer 2 is stopped 1: Timer function input frequency SYSCLK (T2PS=0) SYSCLK/2 (T2PS=1)	

Table 5-63 T2CON register

CCEN	Address: 0xCE				Compare/Capture Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	CMH3	CML3	CMH2	CML2	CMH1	CML1	CMH0	CML0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	CM3[1:0]	R/W	Compare/capture mode for CC3 register CMH3 CML3 Function 0 0 Compare/capture disabled 0 1 Capture on falling/rising edge of CAPTURE3 pin 1 0 Compare enabled 1 1 Capture on write operation into register CCL3	
5:4	CM2[1:0]	R/W	Compare/capture mode for CC2 register CMH2 CML2 Function 0 0 Compare/capture disabled 0 1 Capture on falling/rising edge of CAPTURE2 pin 1 0 Compare enabled 1 1 Capture on write operation into register CCL2	
3:2	CM1[1:0]	R/W	Compare/capture mode for CC1 register CMH1 CML1 Function 0 0 Compare/capture disabled 0 1 Capture on falling/rising edge of CAPTURE1 pin 1 0 Compare enabled 1 1 Capture on write operation into register CCL1	
1:0	CM0[1:0]	R/W	Compare/capture mode for CC0 register CMH0 CML0 Function 0 0 Compare/capture disabled 0 1 Capture on falling/rising edge of CAPTURE0 pin 1 0 Compare enabled 1 1 Capture on write operation into register CCL0	

Table 5-64 CCEN register

T2IF	Address: 0xC9				Timer 2 Interrupt Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	--	TF2
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	--	R/W	Reserved	

Bit	Function	Type	Description	Condition
0	TF2	R/W	Timer 2 overflow flag Cleared by the software	

Table 5-65 T2IF register

CCH0	Address: 0xC1				Timer 2 CC0 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	CC0[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC0[15:8]	R/W	Timer2 compare/capture 0 - high byte	

Table 5-66 The CCH0 register

CCL0	Address: 0xC0				Timer 2 CC0 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	CC0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC0[7:0]	R/W	Timer2 compare/capture 0 - low byte	

Table 5-67 The CCL0 register

CCH1	Address: 0xC3				Timer 2 CC1 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	CC1[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC1[15:8]	R/W	Timer2 compare/capture 1 - high byte	

Table 5-68 The CCH1 register

CCL1	Address: 0xC2				Timer 2 CC1 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	CC1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC1[7:0]	R/W	Timer2 compare/capture 1 - low byte	

Table 5-69 The CCL1 register

CCH2	Address: 0xC5				Timer 2 CC2 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	CC2[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC2[15:8]	R/W	Timer2 compare/capture 2 - high byte	

Table 5-70 The CCH2 register

CCL2	Address: 0xC4				Timer 2 CC2 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	CC2[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC2[7:0]	R/W	Timer2 compare/capture 2 - low byte	

Table 5-71 The CCL2 register

CCH3	Address: 0xC7				Timer 2 CC3 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	CC3[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC3[15:8]	R/W	Timer2 compare/capture 3 - high byte	

Table 5-72 The CCH3 register

CCL3	Address: 0xC6				Timer 2 CC3 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	CC3[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC3[7:0]	R/W	Timer2 compare/capture 3 - low byte	

Table 5-73 The CCL3 register

CRCH	Address: 0xCB				CRC Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	CRC[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CRC[15:8]	R/W	CRC - high byte	

Table 5-74 The CRCH register

CRCL	Address: 0xCA				CRC Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	CRC[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CRC[7:0]	R/W	CRC - low byte	

Table 5-75 The CRCL register

TH2	Address: 0xCD				Timer 2 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH2[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH2[7:0]	R/W	Timer 2 Load value – high byte	

Table 5-76 TH2 register

TL2	Address: 0xCC				Timer 2 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL2[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL2[7:0]	R/W	Timer 2 Load value – low byte	

Table 5-77 TL2 register

5.10. UART0

UART0 has the same functionality as a standard 8051 UART. The serial port is full duplex, meaning it can transmit and receive concurrently. It is reception with double-buffer, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0 reads a physically separate receive register. The serial port can operate in 4 modes: one synchronous and three asynchronous modes. Mode 2 and 3 has a special feature for multiprocessor communications. This feature is enabled by setting SM02 bit in SCON0 register. The master processor first sends out an address byte, which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM02 = 1, no slave will be interrupted by a data byte. An address byte will interrupt all slaves. The addressed slave will clear its SM02 bit and prepare to receive the data bytes that will be coming. The slaves that were not being addressed leave their SM02 set and ignoring the incoming data.

5.10.1. UART0: Mode 0(Synchronous Shift register)

This mode is used as shift register IO control, and not for real communication application. The baud rate is fixed at 1/12 of the system clock frequency and TXD0(P31) output is a shift clock. Eight bits are transmitted with LSB first. Reception is initialized by setting the flags in SCON0 as follows: RI0 =0 and REN0 =1. Figure 5-24 shows the timing diagram of UART0 transmission mode 0.

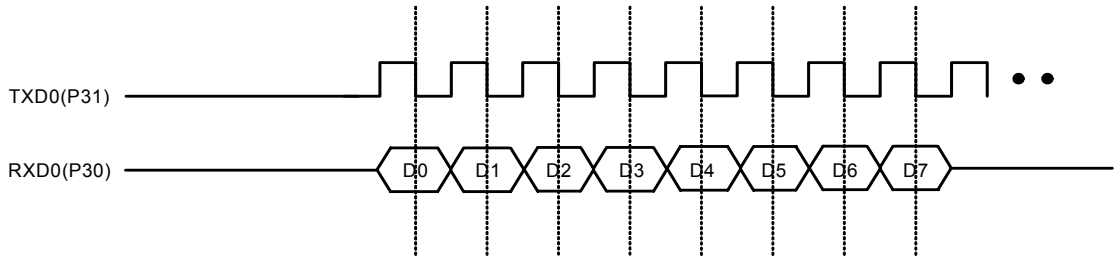


Figure 5-24 The timing diagram of UART0 transmission mode 0

5.10.2. UART0: Mode 1(8-Bit UART, Variable Baud Rate, Timer1 Clock Source)

In mode 1, TXD0 serves as serial output. 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receiving, a start bit synchronizes the reception, 8 data bits are available by reading SBUF0 and stop bit sets the flag RB08 in the SFR SCON0. The baud rate is variable and depends from Timer 1 mode. The SMOD0 bit of PCON (0x87) is used to set the baud rate as $T1_{ov}/32$ or $T1_{ov}/16$. Figure 5-25 shows the format of UART0 transmission mode 1.

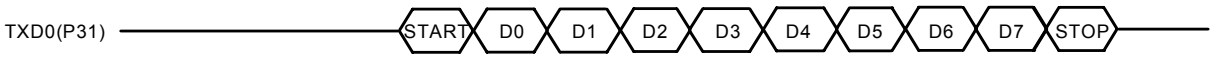


Figure 5-25 The format of UART0 transmission mode 1

5.10.3. UART0: Mode 2(9-Bit UART, Fixed Baud Rate)

This mode is similar to Mode 1 with two differences. The baud rate is fixed at 1/32 or 1/64 of system clock frequency, and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the UART0 interface: at transmission, bit TB08 in SCON0 is output as the 9th bit, and at receive, the 9th bit affects RB08 in SCON0. Figure 5-26 shows the format of UART0 transmission mode 2.

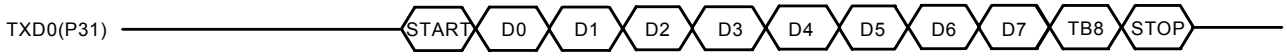


Figure 5-26 The format of UART0 transmission mode 2

5.10.4. UART0: Mode 3(9-Bit UART, Variable Baud Rate, Timer1 Clock Source)

The only difference between Mode 2 and Mode 3 is that the baud rate is a variable in Mode 3. When REN0 =1 data receiving is enabled. The baud rate is variable and depends from Timer 1 mode. The SMOD0 bit of PCON (0x87) is used to set the baud rate as $T1_{ov}/32$ or $T1_{ov}/16$.

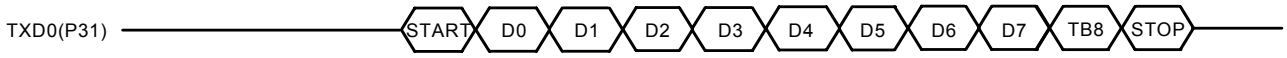


Figure 5-27 The format of UART0 transmission mode 3

5.10.5. UART0 Related Registers

The UART0 related registers are: SBUF0(0x99), SCON0(0x98), PCON(0x87), IE(0xA8) and IP(0xB8). The UART0 data buffer (SBUF0) consists of two separate registers: transmit and receive registers. A data writes into the SBUF0 sets this data in UART0 output register and starts a transmission. A data reads from SBUF0, reads data from the UART0 receive register.

SBUF0			**Address: 0x99**		**UART0 Buffer Register**			
Bit	7	6	5	4	3	2	1	0
Function	SBUF0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	**Function**	**Type**	**Description**	**Condition**
2:0	SBUF0[7:0]	R/W	UART 0 buffer	

Table 5-78 SBUF0 register

SCON0			**Address: 0x98**		**UART0 Configuration Register**			
Bit	7	6	5	4	3	2	1	0
Function	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	SM0[1:0]	R/W	Mode and baud rate setting which described as below table	
5	SM02	R/W	Enables a multiprocessor communication feature	
4	REN0	R/W	Enable serial reception.	
3	TB08	R/W	The 9th transmitted data bit in Modes 2 and Mode 3	
2	RB08	R/W	In Mode 0 this bit is not used In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 2 and Mode 3, it is the 9th data bit received	
1	TI0	R/W	UART0 transmitter interrupt flag	
0	RI0	R/W	UART0 receiver interrupt flag	

Table 5-79 SCON0 register

SM00	SM01	Mode	Function	Baud Rate
0	0	0	Shift register	SYSCLK/12
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	SYSCLK/32(SMOD0=0) SYSCLK/64(SMOD0=1)
1	1	3	9-bit UART	variable

❑ **Variable : in Mode1 and Mode 3**

Timer	Baud Rate
Timer 1 overflow rate	$T1_{ov}$/32 (SMOD0=0)
Timer 1 overflow rate	$T1_{ov}$/16 (SMOD0=1)

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	--	CPU_IDLE	PWE	STOP_RST_EN	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	--	R/W	Reserved	
5	CPU_IDLE	R/W	IDLE mode enable bit 0: IDLE mode disabled ; 1: IDLE mode entered	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3	STOP_RST_EN	R/W	Wakeup state selection bit 0: Next instruction state after wakeup 1: Reset state afer wakeup	
2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	

Bit	Function	Type	Description	Condition
0	--	R/W	Reserved	

Table 5-80 PCON register

IE	Address: 0xA8			Interrupt Enable Register				
Bit	7	6	5	4	3	2	1	0
Function	EA	--	ET2	ES0	ET1	EX1	ET0	EX0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EA	R/W	Enable global interrupts	
6	--	R/W	Reserved	
5	ET2	R/W	Enable Timer 2 interrupt	
4	ES0	R/W	Enable UART0 interrupt	
3	ET1	R/W	Enable Timer 1 interrupt	
2	EX1	R/W	Enable INT1 interrupt	
1	ET0	R/W	Enable Timer 0 interrupt	
0	EX0	R/W	Enable INT0 interrupt	

Table 5-81 IE register

IP	Address: 0xB8			Interrupt Priority Register				
Bit	7	6	5	4	3	2	1	0
Function	-	--	PT2	PS0	PT1	PX1	PT0	PX0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	PT2	R/W	Timer 2 priority level control (1: high level)	
4	PS0	R/W	UART0 priority level control (1: high level)	
3	PT1	R/W	Timer 1 priority level control (1: high level)	
2	PX1	R/W	INT1 priority level control (1: high level)	
1	PT0	R/W	Timer 0 priority level control (1: high level)	
0	PX0	R/W	INT0 priority level control (1: high level)	

Table 5-82 IP register

5.11. ADC

There is one Analog-to-Digital-Converter (ADC) in GPM8F2702A. It provides general purpose usages such as voice record feature and any other analog functions.

- ❑ 6+1 Channels, 12-bit resolution ADC
- ❑ Supports programming sample hold and ADC clock function
- ❑ Supports ADC output window detection

5.11.1. ADC Control

Seven channels of 12-bit SAR ADC are built in GPM8F2702A. They are defined as general-purpose line input P00~P05 and one internal 1.23V. These six channels are very suitable for system voltage detection and other general-purpose usages. Figure 5-28 and Figure 5-29 show the related timing and block diagrams.

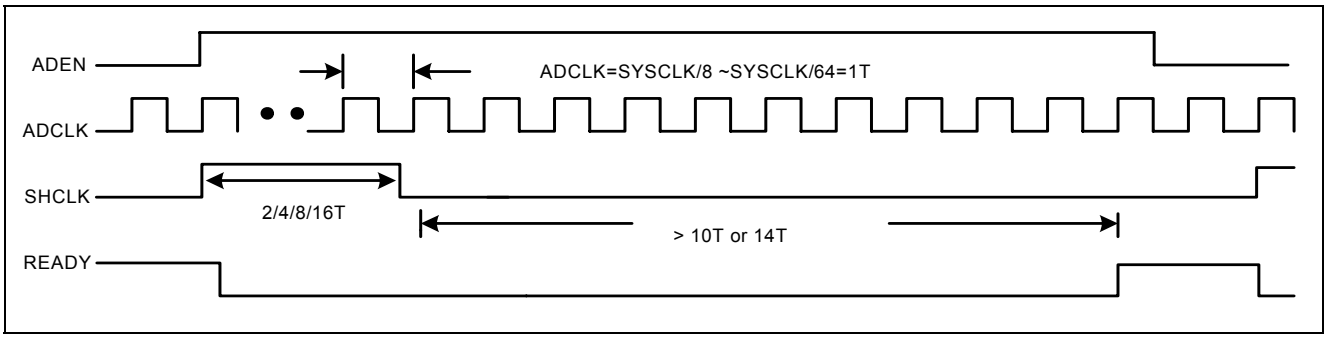


Figure 5-28 The timing diagram of ADC control

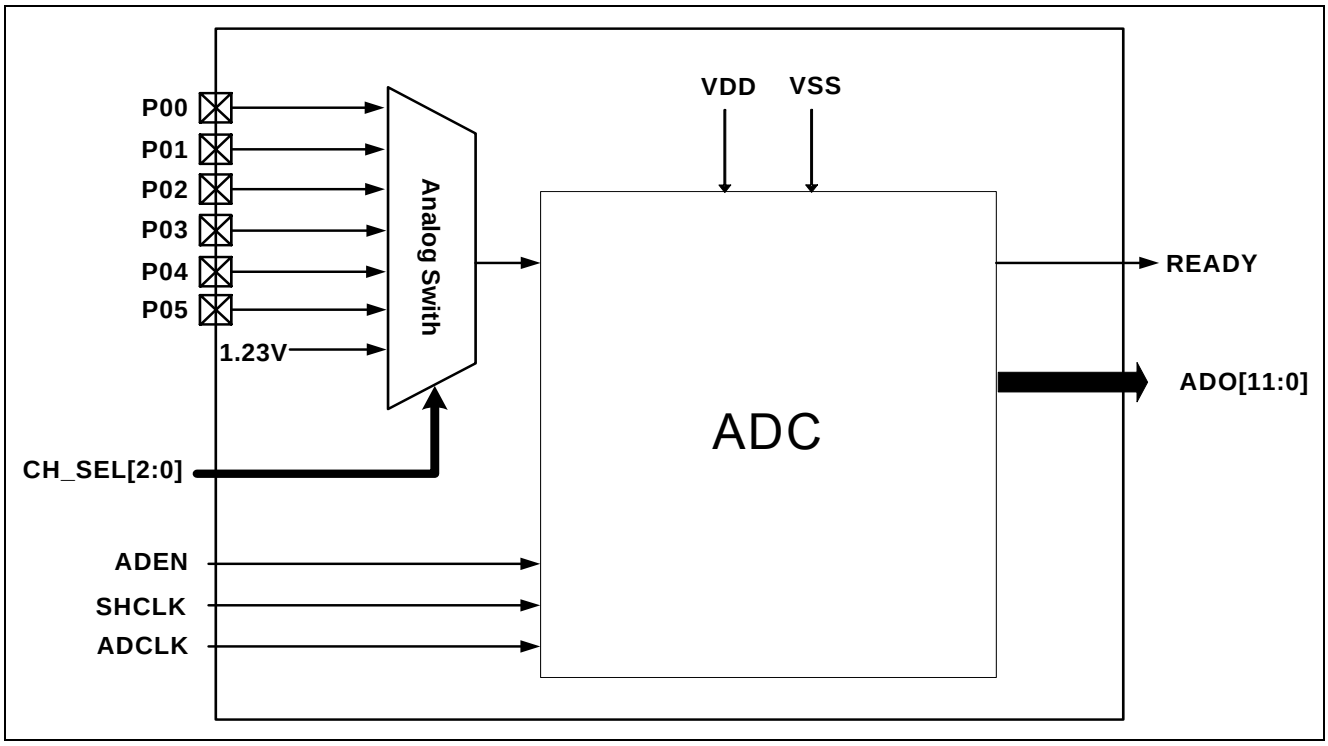


Figure 5-29 The block diagram of ADC

5.11.2. ADC Related Register

ADCON			Address: 0xF1		ADC Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WINF	READYF	WIN_SEL	WINIE	ADIE	--	PSIDLE	START
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	WINF	R/W	Window detect flag	
6	READYF	R/W	ADC transfer ready flag	
5	WIN_SEL	R/W	ADC output window selection 0: ADC output is between ADLB and ADUB 1: ADC output isn't between ADLB and ADUB	
4	WINIE	R/W	ADC window interrupt enable	
3	ADIE	R/W	ADC transfer ready interrupt enable	

Bit	Function	Type	Description	Condition
2	--	R/W	Reserved	
1	PSIDLE	R/W	IDLE mode enable bit (ADC start transfer with suspending CPU clock)	
0	START	R/W	ADC start transfer control	

Table 5-83 ADCON register

ADCFG			Address: 0xF2		ADC Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	--	CH_SEL[2:0]			SHCLK[1:0]		ADCLK[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6:4	CH_SEL[2:0]	R/W	ADC channel selection 0: P00 is selected 1: P01 is selected 2: P02 is selected 3: P03 is selected 4: P04 is selected 5: P05 is selected 6: Internal 1.23V is selected 7: Reserved	
3:2	SHCLK[1:0]	R/W	ADC sample and hold period 0: 2T of ADCLK 1: 4T of ADCLK 2: 8T of ADCLK 3: 16T of ADCLK	
1:0	ADCLK	R/W	ADC clock selection 0: ADC conversion clock = 2MHz (F_{OSC} /8) 1: ADC conversion clock = 1MHz (F_{OSC} /16) 2: ADC conversion clock = 512KHz (F_{OSC} /32) 3: ADC conversion clock = 256KHz (F_{OSC} /64)	

Table 5-84 ADCFG register

ADAEN			Address: 0xF3		ADC Analog PAD Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	P05_AEN	P04_AEN	P03_AEN	P02_AEN	P01_AEN	P00_AEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	P05_AEN	R/W	P05 analog PAD enable control bit 0: P05 can be I/O PAD 1: P05 can be analog PAD	
4	P04_AEN	R/W	P04 analog PAD enable control bit 0: P04 can be I/O PAD	

Bit	Function	Type	Description	Condition
			1: P04 can be analog PAD	
3	P03_AEN	R/W	P03 analog PAD enable control bit 0: P03 can be I/O PAD 1: P03 can be analog PAD	
2	P02_AEN	R/W	P02 analog PAD enable control bit 0: P02 can be I/O PAD 1: P02 can be analog PAD	
1	P01_AEN	R/W	P01 analog PAD enable control bit 0: P01 can be I/O PAD 1: P01 can be analog PAD	
0	P00_AEN	R/W	P00 analog PAD enable control bit 0: P00 can be I/O PAD 1: P00 can be analog PAD	

Table 5-85 ADAEN register

ADOL			Address: 0xF4		ADC Output Low Data Register			
Bit	7	6	5	4	3	2	1	0
Function	ADO[3:0]				--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	ADO[3:0]	R/W	ADC output data[3:0]	

Table 5-86 ADOL register

ADOH			Address: 0xF5		ADC Output High Data Register			
Bit	7	6	5	4	3	2	1	0
Function	ADO[11:4]							
Default	1	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	ADO[11:4]	R/W	ADC output data[11:4]	

Table 5-87 ADOH register

ADLB			Address: 0xF6		ADC Low Boundary register			
Bit	7	6	5	4	3	2	1	0
Function	ADLB[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	ADLB	R/W	ADC low boundary, compare to ADO[11:4]	

Table 5-88 ADLB register

ADUB			Address: 0xF7		ADC UP Boundary register			
Bit	7	6	5	4	3	2	1	0
Function	ADUB[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	ADUB	R/W	ADC up boundary, compare to ADO[11:4]	

Table 5-89 ADUB register

5.12. Built-in Comparators

In GPM8F2702A, built-in two comparators are very suitable for voltage detection and other general-purpose usages and the related control registers are CMPICON, CMPAEN, VCMPCON and CCMPCON. Figure 5-30 shows the diagram of built-in comparators. The VCMPIE and CCMPIE bits are used to enable voltage comparator (VCMP) interrupt and current comparator (CCMP) interrupt respectively. VCMPIF and CCMPIF are their corresponding interrupt flags. Any transition from low to high on output of VCMP/CCMP (VFOUT/CFOUT), the VCMPIF/CCMPIF is set. The input of VCMP and CCMP can be selected by VFSEL[1:0] and CFSEL [1:0] bits respectively. User can select reference voltage of VCMP/CCMP by VCMP_SEL[3:0]/CCMP_SEL[3:0]. The output of VCMP/CCMP is shown in VFOUT/CFOUT bit. The detailed description is shown in Table 5-92 and Table 5-93.

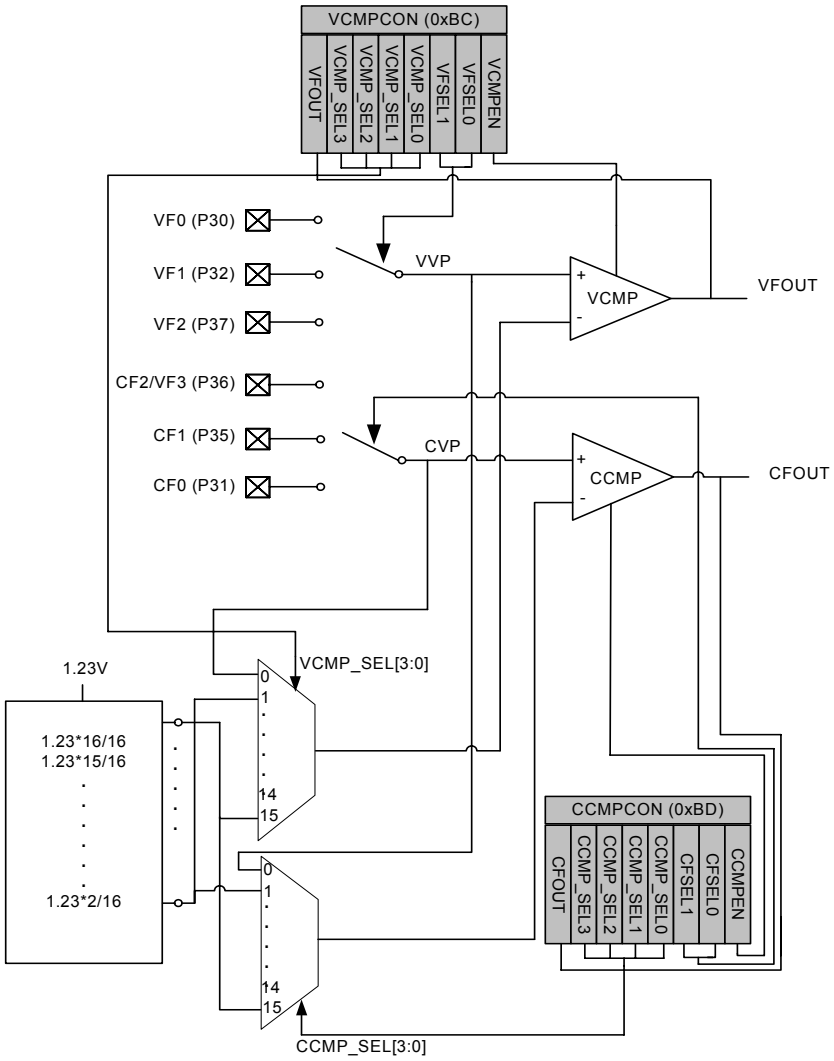


Figure 5-30 Built-in comparator diagram

CMPICON			Address: 0xBA		Comparator Interrupt Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	CCMPIF	VCMPIF	CCMPIE	VCMPIE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3	CCMPIF	R/W	Current comparator (CCMP) interrupt flag Cleared by the software Set as CFOUT form low to high	
2	VCMPIF	R/W	Voltage comparator (VCMP) interrupt flag Cleared by the software Set as VFOUT form low to high	
1	CCMPIE	R/W	Enable Current comparator (CCMP) interrupt 0: CCMP interrupt disable 1: CCMP interrupt enable	
0	VCMPIE	R/W	Enable Voltage comparator (VCMP) interrupt 0: VCMP interrupt disable 1: VCMP interrupt enable	

Table 5-90 CMPICON register

CMPAEN			Address: 0xBB		Comparator Analog PAD Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	P37_AEN	P36_AEN	P35_AEN	P32_AEN	P31_AEN	P30_AEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	P37_AEN	R/W	P35 analog PAD enable control bit 0: P35 can be I/O PAD 1: P35 can be analog PAD	
4	P36_AEN	R/W	P36 analog PAD enable control bit 0: P36 can be I/O PAD 1: P36 can be analog PAD	
3	P35_AEN	R/W	P35 analog PAD enable control bit 0: P35 can be I/O PAD 1: P35 can be analog PAD	
2	P32_AEN	R/W	P32 analog PAD enable control bit 0: P32 can be I/O PAD 1: P32 can be analog PAD	
1	P31_AEN	R/W	P31 analog PAD enable control bit 0: P31 can be I/O PAD 1: P31 can be analog PAD	
0	P30_AEN	R/W	P30 analog PAD enable control bit 0: P30 can be I/O PAD 1: P30 can be analog PAD	

Table 5-91 CMPAEN register

VCMPCON			Address: 0xBC		Voltage Comparator Control Register			
Bit	7	6	5	4	3	2	1	0
Function	VFOUT	VCMP_SEL3	VCMP_SEL2	VCMP_SEL1	VCMP_SEL0	VFSEL1	VFSEL0	VCMPEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	VFOUT	R/W	Voltage comparator output	
6:3	VCMP_SEL[3:0]	R/W	Reference voltage select bit VCMP_SEL — Reference Voltage 0000 — select CVP input 0001 — select 1.23V * 2/16 0010 — select 1.23V * 3/16 0011 — select 1.23V * 4/16 0100 — select 1.23V * 5/16 0101 — select 1.23V * 6/16 0110 — select 1.23V * 7/16 0111 — select 1.23V * 8/16 1000 — select 1.23V * 9/16 1001 — select 1.23V * 10/16 1010 — select 1.23V * 11/16 1011 — select 1.23V * 12/16 1100 — select 1.23V * 13/16 1101 — select 1.23V * 14/16 1110 — select 1.23V * 15/16 1111 — select 1.23V * 16/16	
2:1	VFSEL[1:0]	R/W	Voltage comparator input select bits VFSEL — VCMP input 00 — select VF0 (P30) 01 — select VF1 (P32) 10 — select VF2 (P37) 11 — select VF3 (P36)	
0	VCMPEN	R/W	Voltage comparator enable bit 0: VCMP Disable 1: VCMP Enable	

Table 5-92 VCMPCON register

CCMPCON			Address: 0xBD		Current Comparator Control Register			
Bit	7	6	5	4	3	2	1	0
Function	CFOUT	CCMP_SEL3	CCMP_SEL2	CCMP_SEL1	CCMP_SEL0	CFSEL1	CFSEL0	CCMPEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CFOUT	R/W	Current comparator output	

Bit	Function	Type	Description	Condition
6:3	CCMP_SEL[3:0]	R/W	Reference voltage select bit CCMP_SEL — Reference Voltage 0000 — select VVP input 0001 — select 1.23V * 2/16 0010 — select 1.23V * 3/16 0011 — select 1.23V * 4/16 0100 — select 1.23V * 5/16 0101 — select 1.23V * 6/16 0110 — select 1.23V * 7/16 0111 — select 1.23V * 8/16 1000 — select 1.23V * 9/16 1001 — select 1.23V * 10/16 1010 — select 1.23V * 11/16 1011 — select 1.23V * 12/16 1100 — select 1.23V * 13/16 1101 — select 1.23V * 14/16 1110 — select 1.23V * 15/16 1111 — select 1.23V * 16/16	
2:1	CFSEL[1:0]	R/W	Current comparator input select bits CFSEL — CCMP input 00 — select CF0 (P31) 01 — select CF1 (P35) 10 — select CF2 (P36) 11 — select CF0 (P31)	
0	CCMPEN	R/W	Current comparator enable bit 0: CCMP Disable 1: CCMP Enable	

Table 5-93 CCMPCON register

5.13. Alphabetical List of Instruction Set

5.13.1. Arithmetic Operations

Mnemonic	Description	Code	Bytes	Cycles
ADD A,Rn	Add register to accumulator	0x28-0x2F	1	1
ADD A,direct	Add direct byte to accumulator	0x25	2	2
ADD A,@Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A,#data	Add immediate data to accumulator	0x24	2	2
ADDC A,Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A,direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A,#data	Add immediate data to A with carry flag	0x34	2	2
SUBB A,Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A,direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A,@Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A,#data	Subtract immediate data from A with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	2
INC direct	Increment direct byte	0x05	2	3
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	2
DEC direct	Decrement direct byte	0x15	1	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	2	3
INC DPTR	Increment data pointer	0xA3	1	1
MUL A,B	Multiply A and B	0xA4	1	2
DIV A,B	Divide A by B	0x84	1	6
DA A	Decimal adjust accumulator	0xD4	1	3

5.13.2. Logic Operations

Mnemonic	Description	Code	Bytes	Cycles
ANL A,Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A,direct	AND direct byte to accumulator	0x55	2	2
ANL A,@Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A,#data	AND immediate data to accumulator	0x54	2	2
ANL direct,A	AND accumulator to direct byte	0x52	2	3
ANL direct,#data	AND immediate data to direct byte	0x53	3	3
ORL A,Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A,direct	OR direct byte to accumulator	0x45	2	2
ORL A,@Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A,#data	OR immediate data to accumulator	0x44	2	2
ORL direct,A	OR accumulator to direct byte	0x42	2	3
ORL direct,#data	OR immediate data to direct byte	0x43	3	3
XRL A,Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2

Mnemonic	Description	Code	Bytes	Cycles
XRL A,#data	Exclusive OR immediate data to accumulator	0x64	2	2
XRL direct,A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct,#data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	1

5.13.3. Boolean Operations

Mnemonic	Description	Code	Bytes	Cycles
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C,bit	AND direct bit to carry flag	0x82	2	2
ANL C,/bit	AND complement of direct bit to carry	0xB0	2	2
ORL C,bit	OR direct bit to carry flag	0x72	2	2
ORL C,/bit	OR complement of direct bit to carry	0xA0	2	2
MOV C,bit	Move direct bit to carry flag	0xA2	2	2
MOV bit,C	Move carry flag to direct bit	0x92	2	3

5.13.4. Data Transfers

Mnemonic	Description	Code	Bytes	Cycles
MOV A,Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A,direct	Move direct byte to accumulator	0xE5	2	2
MOV A,@Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV A,#data	Move immediate data to accumulator	0x74	2	2
MOV Rn,A	Move accumulator to register	0xF8-0xFF	1	1
MOV Rn,direct	Move direct byte to register	0xA8-0xAF	2	3
MOV Rn,#data	Move immediate data to register	0x78-0x7F	2	2
MOV direct,A	Move accumulator to direct byte	0xF5	2	2
MOV direct,Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1,direct2	Move direct byte to direct byte	0x85	3	3
MOV direct,@Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct,#data	Move immediate data to direct byte	0x75	3	3
MOV @Ri,A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri,direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV @Ri,#data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV DPTR,#data16	Load 16-bit constant into active DPH and DPL in LARGE mode	0x90	3	3

Mnemonic	Description		Code	Bytes	Cycles
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator		0x93	1	5
MOVC A,@A+PC	Move code byte relative to PC to accumulator		0x83	1	4
MOVX A,@Ri	Move external RAM (8-bit address) to A	XDM	0xE2-0xE3	1	3*
		SXDM			3
MOVX A,@DPTR	Move external RAM (16-bit address) to A	XDM	0xE0	1	2*
		SXDM			2
MOVX @Ri,A	Move A to external XDM (8-bit address)	CODE inside ROM/RAM	0xF2-0xF3	1	4*
		Other cases			5*
	Move A to external SXDM (8-bit address)	All cases			3
MOVX @DPTR,A	Move A to external XDM (16-bit address)	CODE inside ROM/RAM	0xF0	1	3*
		Other cases			4*
	Move A to external SXDM (16-bit address)	All cases			2
PUSH direct	Push direct byte onto IDM stack		0xC0	2	3
POP direct	Pop direct byte from IDM stack		0xD0	2	2
XCH A,Rn	Exchange register with accumulator		0xC8-0xCF	1	2
XCH A,direct	Exchange direct byte with accumulator		0xC5	2	3
XCH A,@Ri	Exchange indirect RAM with accumulator		0xC6-0xC7	1	3
XCHD A,@Ri	Exchange low-order nibble indirect RAM with A		0xD6-0xD7	1	3

5.13.5. Program Branches

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	0x11-0xF1	2	4
LCALL addr16	Long subroutine call	0x12	3	4
RET	Return from subroutine	0x22	1	4
RETI	Return from interrupt	0x32	1	4
AJMP addr11	Absolute jump	0x01-0xE1	2	3
LJMP addr16	Long jump	0x02	3	4
SJMP rel	Short jump (relative address)	0x80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	0x73	1	5
JZ rel	Jump if accumulator is zero	0x60	2	4
JNZ rel	Jump if accumulator is not zero	0x70	2	4
JC rel	Jump if carry flag is set	0x40	2	3
JNC	Jump if carry flag is not set	0x50	2	3
JB bit,rel	Jump if direct bit is set	0x20	3	5
JNB bit,rel	Jump if direct bit is not set	0x30	3	5
JBC bit,direct rel	Jump if direct bit is set and clear bit	0x10	3	5
CJNE A,direct rel	Compare direct byte to A and jump if not equal	0xB5	3	5
CJNE A,#data rel	Compare immediate to A and jump if not equal	0xB4	3	4
CJNE Rn,#data rel	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4
CJNE @Ri,#data rel	Compare immediate to ind. and jump if not equal	0xB6-0xB7	3	5
DJNZ Rn,rel	Decrement register and jump if not zero	0xD8-0xDF	2	4
DJNZ direct,rel	Decrement direct byte and jump if not zero	0xD5	3	5
NOP	No operation	0x00	1	1

6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 6.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	-40℃ to +85℃
VDD Total MAX Current	I_{VDDM}	70mA
VSS Total MAX Current	I_{VSSM}	120mA

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
INOSC Frequency	F_{OSC}	16/8/4×(1-2%)	16/8/4	16/8/4×(1+2%)	MHz	VDD = 2.0~5.5V

6.3. DC Characteristics (VDD = 5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	V_{LVR}	5	5.5	V	
Operating Current	I_{OP}	-	25	-	mA	F_{CPU} = 16MHz @ 5.5V, no load
Standby Current	I_{STBY}	-	2.0	5.0	uA	VDD = 5.5V
Input High Level	V_{IH}	0.7VDD	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.3VDD	V	VDD = 5.0V
Output High Level	V_{OH}	0.8VDD	-	-	V	I_{OH} = -8mA at VDD = 5.0V
Output Low Level	V_{OL}	-	-	0.2VDD	V	I_{OL} = 20mA at VDD = 5.0V
Input Pull High Resistor	R_{PH}	30	50	70	KΩ	VDD = 5.0V
Input Pull High Resistor	R_{PL}	30	50	70	KΩ	VDD = 5.0V
Low Voltage Reset	V_{LVR}	1.92/2.61/4.5 ×(1-5%)	1.92/2.61/4.25	1.92/2.61/4.25 ×(1+5%)	V	

6.4. ADC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Condition
Resolution	-	-	-	12	Bit	
Integral Linearity Error	E_{INL}	-	±2	±3	LSB	VDD =5V
Differential Linearity Error	E_{DNL}	-	±2	±3	LSB	VDD =5V
No Missing Code	-	-	12	-	bits	VDD =2.0~5.5V
ADC input voltage range	V_{ADCIN}	0	-	VDD	V	
ADC Operating current	I_{AD}	-	-	1.5	mA	VDD =5.5V
ADC clock period	T_{AD}	0.5	-	-	us	
ADC Conversion time	T_{CON}	16	-	-	T_{AD}	SHCLK = $2T_{AD}$
Input channel	-	-	-	6+1	channel	
Internal 1.23V	-	1.23×(1-5%)	1.23	1.23×(1+5%)	V	

6.5. Comparator Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Offset	Voff	-	-	10	mV	
Unit Gain Bandwidth	BW	-	1	-	MHz	VDD =5V
Typical Active Current	I_{cmp}	-	-	100	uA	VDD =5.5V
Internal 1.23V	-	1.23×(1-5%)	1.23	1.23×(1+5%)	V	

7. PACKAGE INFORMATION

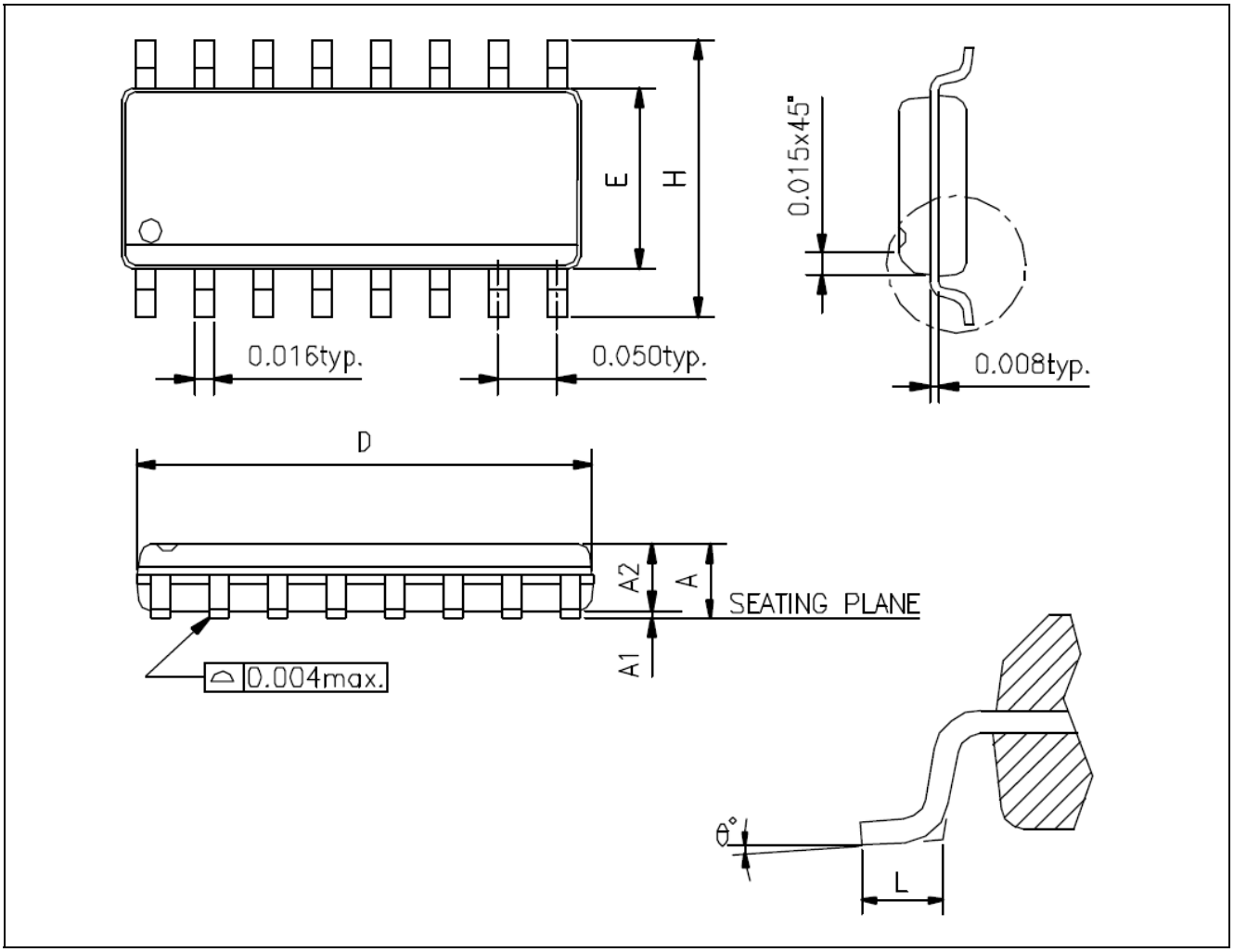
7.1. Ordering Information

Product Number	Package Type
GPM8F2702A- HS03x	Green Package

Note1: Package form number (x = 1 - 9, serial number).

7.2. Package Information

SOP 16



Symbols	Min.	Max.
A	0.053	0.069
A1	0.004	0.010
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

Unit: Inch

8.DISCLAIMER

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9. REVISION HISTORY

Date	Revision #	Description	Page
Dec. 16, 2011	0.2	Add 7.2 Package Information.	65
Dec. 02, 2010	0.1	Original	71