DATA SHEET

GPM8F3132C
GPM8F3132C-QV043

44 /32 Pin 8-bit Microcontroller with 32KB Flash

Preliminary

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Version 0.3

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44/32 PIN 8-BIT MICROCONTROLLER WITH 32KB FLASH

1. GENERAL DESCRIPTION

The GPM8F3132C/ GPM8F3132C-QV043 is a highly integrated microcontroller which integrates a pipelined 1T 8051 CPU, 1K / 8K byte XRAM, 256-byte IDM SRAM and 32K-byte program Flash. It supports up to 35 programmable multi-functional I/Os, Timer0/1/A/B/C, UART0, SPI (master/slaver), I2C (master/slaver), 1 set OP, 2 sets comparator, 64MHz PLL, 16-bit X 16-bit multiplier, 32-bit / 16-bit divider, 16-bit adder, 16-bit subtractor, 32-bit shifter and two sets of 8-channle SAR ADC with 12-bit resolution for general-purpose application. It operates over a wide range of working voltage, from 2.4V through 5.5V, in different clock sources. It has one mode in power management unit. Moreover, there is one on-chip debug circuit with two pins to facilitate full speed in-system debug.

2. FEATURES

- **CPU**
  - High speed, high performance 1T 8051
    - 100% software compatible with industry standard 8051
    - Pipeline RISC architecture enables to execute instructions 10 times faster than standard 8051
    - Up to 64MHz clock operation
- **Memories**
  - GPM8F3132C is 1K bytes XRAM. GPM8F3132C-QV043 is 8K bytes XRAM.
  - 256 bytes internal Data Memory (IDM) SRAM
  - 32K bytes Flash with high endurance
    - Minimum 200,000 program/erase cycles
    - Minimum 20 years data retention
    - 1KB page size
  - Programming read only level for software security
- **Clock Management**
  - Internal oscillator: 8.533MHz±2% @ 2.4V~5.5V
  - Internal oscillator with PLL : 64MHz
- **Power Management**
  - 1 Sleep mode for power saving
- **Interrupt Management**
  - 13 interrupt sources
  - Up to 4 external interrupt sources
- **Reset Management**
  - Power On Reset (POR)
  - Low Voltage Reset (LVR)
  - Pad Reset (PAD_RST)
  - Watchdog Reset (WDT_RST)
  - Software Reset (S/W_RST)
  - Flash Access Error Reset (ADDR_ERR_RST)
- **Programmable Watchdog Timer**
  - A time-base generator
  - An event timer
  - System supervisor
- **One OP**
- **Two Comparator**
- **I/O Ports**
  - Max. 35 multifunction bi-direction I/Os
  - Each incorporate with pull-up resistor, pull-down resistor, output high, output low , output driving capability and floating input which depending on programmer's settings on the corresponding registers
  - I/O ports with 12mA current sink
  - I/O ports with 12mA current drive
- **Two 16-bit Timer/Counter (Timer 0/1)**
  - Timer mode with clock source selectable
  - Auto reload 8-bit timers
  - Externally gated event counters
- **Three Powerful Timer A / B / C with 16-bit Compare / Capture / PWM Unit**
  - Timer mode with clock source selectable
  - Auto-reload 16-bit timers
  - Event capturing
  - Pulse width modulation and measurement
- **UART0**
  - One synchronous mode
  - Three asynchronous modes
- **SPI (master / slaver mode)**
  - Programmable phase and polarity of master clock
  - Programmable master SPI clock frequency
  - Max SPI clock: 24MHz (F_{pll} /2) @64MHz
- **I2C (master / slaver mode)**
  - Programmable master I2C clock frequency
  - Max I2C clock: 375KHz (F_{pll} /128) @64MHz
- **A/D Converter**
  - Two 8-channel 12-bit resolution ADC
  - Control independent per set
- **Built-in Low Voltage Reset**
  - Trigger level: 1.9V, 2.4V, 3.2V, 4.2V
- **Built-in Low Voltage Detect**
  - Programmable level: 2.1V, 2.6V, 3.4V, 4.4V
- **MDU**
  - Built-in 16-bit X 16-bit signed multiplier
  - Built-in 32-bit / 16-bit signed divider
  - Built-in 16-bit + 16-bit signed adder.

– Built-in 16-bit - 16-bit signed subtracter.

– Built-in 32-bit arithmetic shifter.

■ **On-chip Debug Unit**

– C compatible development tools

IC Family	GPM8F3132C	
Product Number	**GPM8F3132C**	**GPM8F3132C-QV043**
System CLK (MHz)	64	64
CPU CLK (MHz)	64	16
Operating Voltage (V)	2.4~5.5	2.4~5.5
Flash (Kbytes)	32	32
XRAM (bytes)	1K	8K
IDM (bytes)	256	256
Timer (sets)	5	5
UART	1	1
SPI (master / slaver)	1	1
I2C (master / slaver)	1	1
Built-in OP (sets)	1	1
Built-in Comparator (sets)	2	2
8-Channel 12-bit ADC (sets)	2	2
Multiplier (signed)	16-bit X 16-bit	16-bit X 16-bit
Divider (signed)	32-bit / 16-bit	32-bit / 16-bit
Adder (signed)	16-bit + 16-bit	16-bit + 16-bit
Subtracter (signed)	16-bit – 16-bit	16-bit – 16-bit
Shifter (signed)	32-bit	32-bit
IO	35	28
Package Type	LQFP44	QFN32

3. BLOCK DIAGRAM

3.1. GPM8F3132C Family

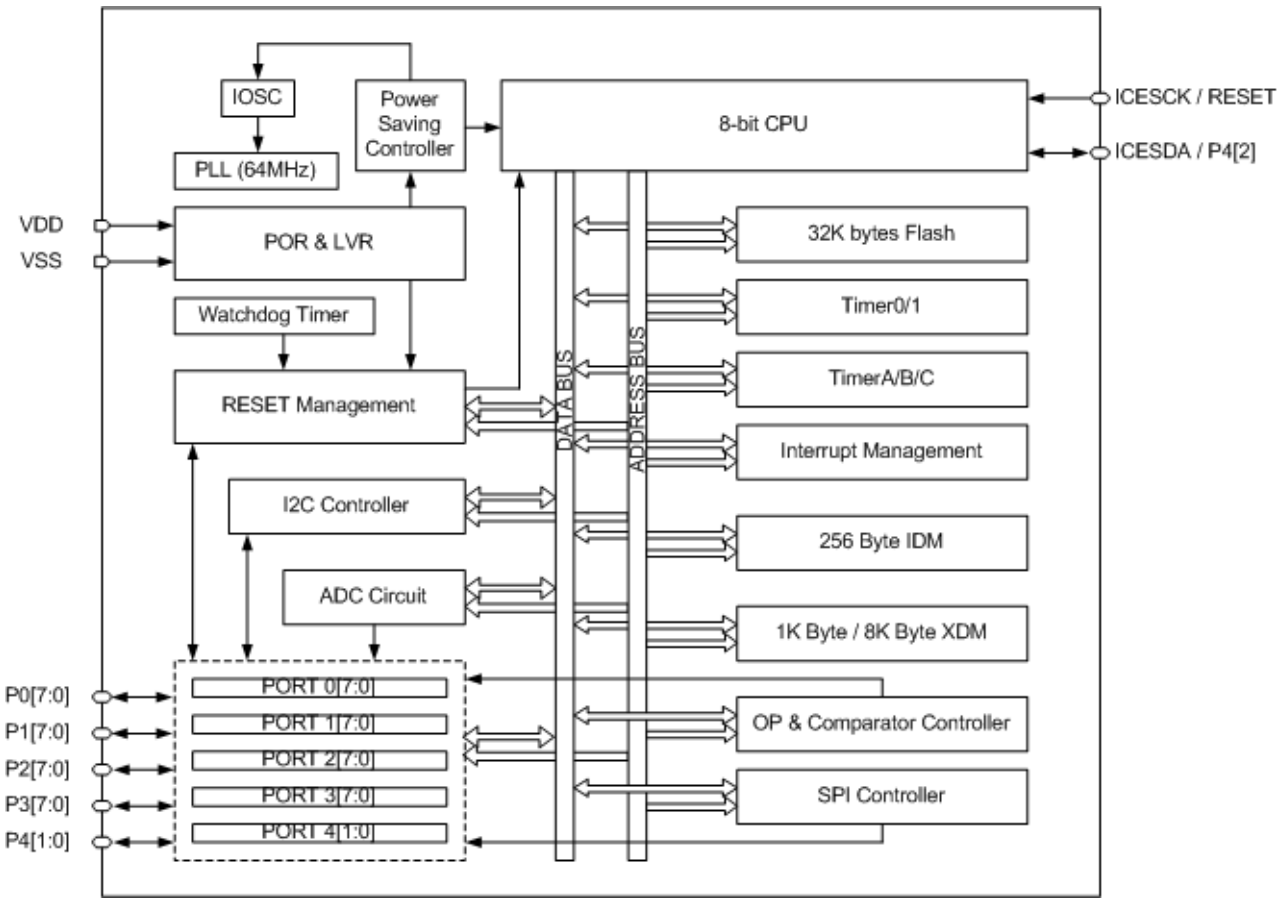


Figure 3.1-1 Block diagram of GPM8F3132C family

4. SIGNAL DESCRIPTIONS

4.1. Pin Descriptions

4.1.1. GPM8F3132C

Type：I = Input, O = Output, S = Supply

Pin Name	LQFP44	Type	Description
P10	1	I/O	Port 1 bit 0 / AN14 (ADC1 channel 4 input)
P11	2	I/O	Port 1 bit 1 / OPP
P12	3	I/O	Port 1 bit 2 / OPN
P13	4	I/O	Port 1 bit 3 / OPO
P14	5	I/O	Port 1 bit 4 / CMP_I
P15	6	I/O	Port 1 bit 5 / EXT_IRQ0
P16	7	I/O	Port 1 bit 6 / EXT_IRQ1
P17	8	I/O	Port 1 bit 7 / EXT_IRQ2
P20	9	I/O	Port 2 bit 0 / I2C_DA
P21	10	I/O	Port 2 bit 1 / I2C_CK
P22	11	I/O	Port 2 bit 2 / UARTRX / EXT_IRQ3
P23	12	I/O	Port 2 bit 3 / UARTTX
P24	13	I/O	Port 2 bit 4 / TCCAP0
P25	14	I/O	Port 2 bit 5 / TCCAP1
P26	15	I/O	Port 2 bit 6 / TCCAP2 / CMPU_O
P27	16	I/O	Port 2 bit 7 / TCCAP3 / CMPD_O
P30	17	I/O	Port 3 bit 0 / TBCAP0 / TBPWM0
P31	18	I/O	Port 3 bit 1 / TBCAP1 / TBPWM1
P32	19	I/O	Port 3 bit 2 / TBCAP2 / TBPWM2
P33	20	I/O	Port 3 bit 3 / TBCAP3 / TBPWM3
P34	21	I/O	Port 3 bit 4 / TACAP0 / TAPWM0 / SPICLK
P35	22	I/O	Port 3 bit 5 / TACAP1 / TAPWM1 / SPICSN
P36	23	I/O	Port 3 bit 6 / TACAP2 / TAPWM2 / SPIRX
NC	24	--	No connect
NC	25	--	No connect
NC	26	--	No connect
P37	27	I/O	Port 3 bit 7 / TACAP3 / TAPWM3 / SPITX
P40	28	I/O	Port 4 bit 0 / TACAP4 / TAPWM4
P41	29	I/O	Port 4 bit 1 / TACAP5 / TAPWM5
P42	30	I/O	Port 4 bit 2 / ICEDA (2 wire serial bus data input/output line) / UARTRX
RESET	31	I	RESET signal, high active/ ICECK (2 wire serial bus clock input line)
NC	32	--	No connect
VDD	33	S	Power 5V input
VSS	34	S	Ground
V18	35	S	Regulator output, needs 2.2uF Cap.
P00	36	I/O	Port 0 bit 0 / AN00 (ADC0 channel 0 input)
P01	37	I/O	Port 0 bit 1 / AN01 (ADC0 channel 1 input)
P02	38	I/O	Port 0 bit 2 / AN02 (ADC0 channel 2 input)
P03	39	I/O	Port 0 bit 3 / AN03 (ADC0 channel 3 input)
P04	40	I/O	Port 0 bit 4 / AN10 (ADC1 channel 0 input)
ADC_VREF	41	S	ADC reference voltage regulator output, needs 2.2uF Cap.

Pin Name	LQFP44	Type	Description
P05	42	I/O	Port 0 bit 5 / AN11 (ADC1 channel 1 input)
P06	43	I/O	Port 0 bit 6 / AN12 (ADC1 channel 2 input)
P07	44	I/O	Port 0 bit 7 / AN13 (ADC1 channel 3 input)

4.1.2. GPM8F3132C-QV043

Pin Name	QFN32	Type	Description
P11	1	I/O	Port 1 bit 1 / OPP
P12	2	I/O	Port 1 bit 2 / OPN
P13	3	I/O	Port 1 bit 3 / OPO
P14	4	I/O	Port 1 bit 4 / CMP_I
P15	5	I/O	Port 1 bit 5 / EXT_IRQ0
P16	6	I/O	Port 1 bit 6 / EXT_IRQ1
P17	7	I/O	Port 1 bit 7 / EXT_IRQ2
P20	8	I/O	Port 2 bit 0 / I2C_DA
P21	9	I/O	Port 2 bit 1 / I2C_CK
P22	10	I/O	Port 2 bit 2 / UARTRX / EXT_IRQ3
P23	11	I/O	Port 2 bit 3 / UARTTX
P26	12	I/O	Port 2 bit 6 / TCCAP2 / CMPU_O
P27	13	I/O	Port 2 bit 7 / TCCAP3 / CMPD_O
P30	14	I/O	Port 3 bit 0 / TBCAP0 / TBPWM0
P31	15	I/O	Port 3 bit 1 / TBCAP1 / TBPWM1
P34	16	I/O	Port 3 bit 4 / TACAP0 / TAPWM0 / SPICLK
P35	17	I/O	Port 3 bit 5 / TACAP1 / TAPWM1 / SPICSN
P36	18	I/O	Port 3 bit 6 / TACAP2 / TAPWM2 / SPIRX
P37	19	I/O	Port 3 bit 7 / TACAP3 / TAPWM3 / SPITX
P42	20	I/O	Port 4 bit 2 / ICEDA (2 wire serial bus data input/output line) / UARTRX
RESET	21	I	RESET signal, high active/ ICECK (2 wire serial bus clock input line)
VDD	22	S	Power 5V input
V18	23	S	Regulator output, needs 2.2uF Cap.
P00	24	I/O	Port 0 bit 0 / AN00 (ADC0 channel 0 input)
P01	25	I/O	Port 0 bit 1 / AN01 (ADC0 channel 1 input)
P02	26	I/O	Port 0 bit 2 / AN02 (ADC0 channel 2 input)
P03	27	I/O	Port 0 bit 3 / AN03 (ADC0 channel 3 input)
P04	28	I/O	Port 0 bit 4 / AN10 (ADC1 channel 0 input)
ADC_VREF	29	S	ADC reference voltage regulator output, needs 2.2uF Cap.
P05	30	I/O	Port 0 bit 5 / AN11 (ADC1 channel 1 input)
P06	31	I/O	Port 0 bit 6 / AN12 (ADC1 channel 2 input)
P07	32	I/O	Port 0 bit 7 / AN13 (ADC1 channel 3 input)
VSS	33	S	Ground

4.2. PIN Map

Package Pin Sequence - LQFP 44 pin map

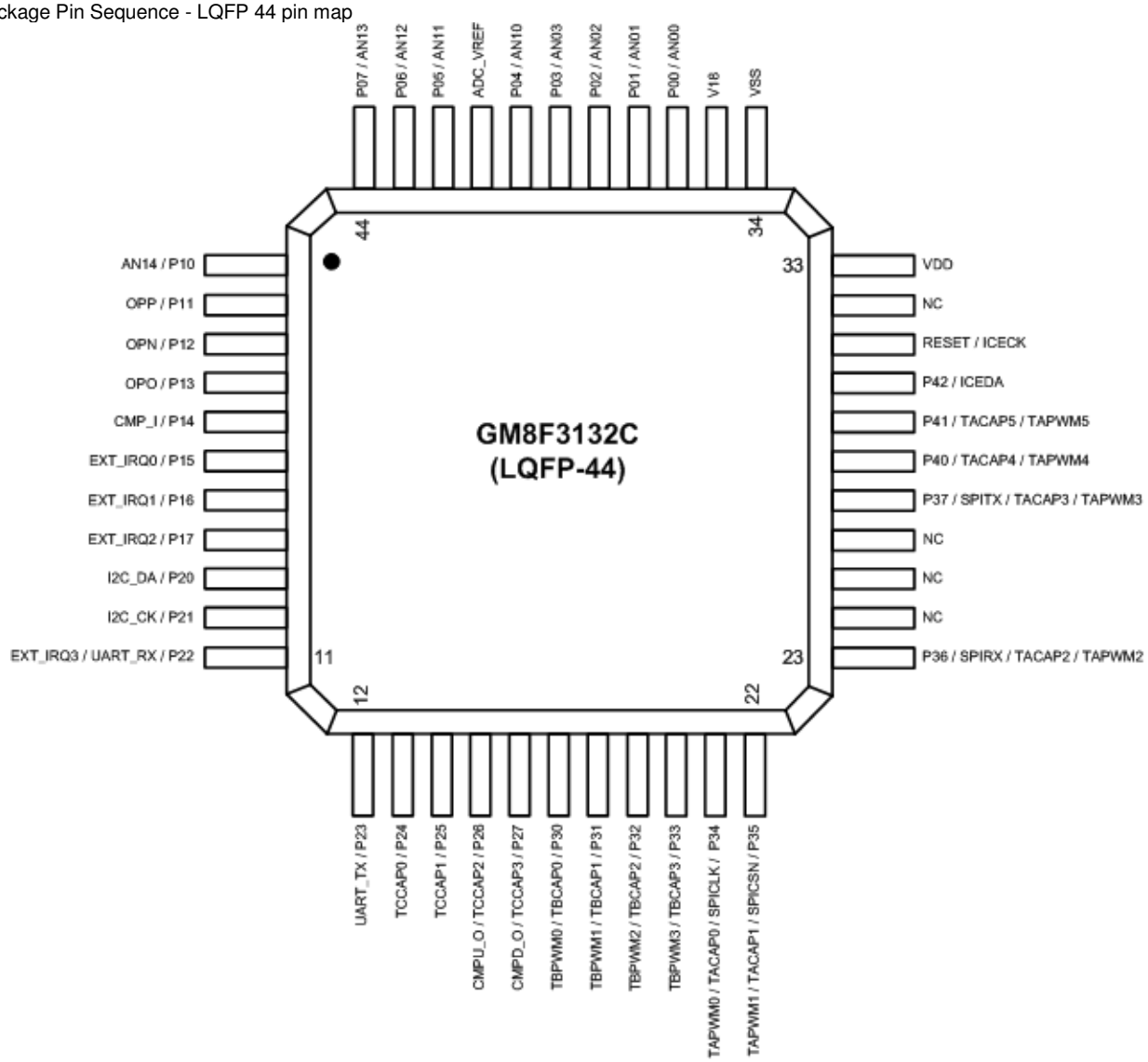


Figure 4.2-1 The pin assignment of GPM8F3132C

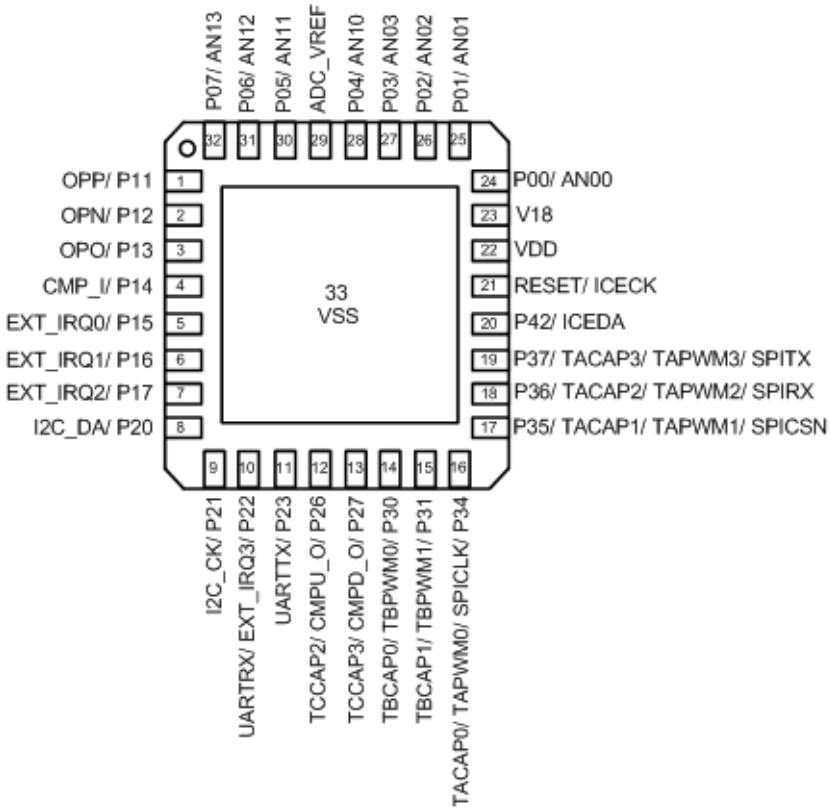


Figure 4.2-2 The pin assignment of GPM8F3132C-QV043

5. FUNCTIONAL DESCRIPTIONS

5.1. Central Processing Unit

5.1.1. CPU Introduction

The CPU is an ultra high performance, high speed embedded microcontroller. Pipelined architecture enables the CPU 10 times faster than standard architecture. This performance can also be exploited to great advantage in low power application where the core can be clocked over ten times slower than original implementation for no performance penalty.

5.1.2. CPU Features

- ❑ 100 % software compatible with industry 8051
- ❑ 24 times faster multiplication
- ❑ 12 times faster addition

The CPU is fully compatible with industry standard 8051 microcontroller, maintaining all instruction mnemonics and binary compatibility. It incorporates some great architectural enhancements, allowing the CPU instructions execution with high performance and high speed.

The arithmetic section of the processor performs extensive data manipulation and is comprised of an 8-bit arithmetic logic unit (ALU), an ACC(0xE0) register, B(0xF0) register and PSW(0xD0) register.

5.1.3. Arithmetic Logic Unit (ALU)

The ALU performs the arithmetic and logic operations during one instruction execution. Typical arithmetic operations are addition, subtraction, multiplication and division. Additional operations are such as increment, decrement, BCD-decimal-add-adjust and compare. Within logic unit, operation such as AND, OR, Exclusive OR, complement and rotation are performed. The Boolean processor performs the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry.

5.1.4. Accumulator A register

The accumulation is the 8-bit general-purpose register, which can be operated with data transfer, temporary saving, condition judgment, etc.

5.1.5. B register

The B register is used during multiply and divide operations. In other cases, it may be used as normal SFR.

5.1.6. Program Status Word (PSW)

The PSW contains several bits that reflect the current state of the CPU which is similar to the flag-register of general CPU.

5.1.7. Program Counter (PC)

The program counter is a 16-bit wide register. It consists of two 8-bit registers which are PCH and PCL. This register indicates the address of next instruction to be executed. In Reset state, the content of 0x0000 is stored into program counter.

ACC			**Address: 0xE0**		**Accumulator A Register**			
Bit	7	6	5	4	3	2	1	0
Function	ACC[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	**Function**	**Type**	**Description**	**Condition**
7:0	ACC[7:0]	R/W	Accumulator A	

Table 5-1 The ACC register

B			**Address: 0xF0**		**B Register**			
Bit	7	6	5	4	3	2	1	0
Function	B[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	**Function**	**Type**	**Description**	**Condition**
7:0	B[7:0]	R/W	B	

Table 5-2 The B register

PSW			Address: 0xD0		Program Status Word Register			
Bit	7	6	5	4	3	2	1	0
Function	CY	AC	F0	RS1	RS0	OV	F1	P
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CY	R/W	Carry flag	
6	AC	R/W	Auxiliary carry flag	
5	F0	R/W	General purpose flag 0	
4:3	RS[1:0]	R/W	Register bank select bits RS[1:0] / Function description 00 / Bank 0, data address 0x00-0x07 01 / Bank 1, data address 0x08-0x0F 10 / Bank 2, data address 0x10-0x17 11 / Bank 3, data address 0x18-0x1F	
2	OV	R/W	Overflow flag	
1	F1	R/W	General purpose flag 1	
0	P	R/W	Parity flag	

Table 5-3 The PSW register

5.2. Memory Organization

5.2.1. Introduction

The GPM8F3132C/ GPM8F3132C-QV043 has three separated address spaces for program memory and data memory. The program memory is on-chip, re-programmable Flash memory and contains up to 32K bytes spaces. The data memory is 1K/8K bytes of external RAM, 256 bytes IDM with 128 bytes x 4 pages of SFR which can be read and written. The upper IDM and SFR use the same access address in different access ways which are described in Figure 5.2-2

5.2.2. Program Memory Allocation

The GPM8F3132C program memory allocation is divided into two parts, including code area and high speed code area with 32KB memory size. If system clock is set to PLL output with 64MHz PLL output frequency. CPU operating in 16MHz frequency when program is stored in code area(0x2000 ~ 0x7FFF). In high speed code area, CPU is operating in 64MHz frequency. The high speed code area is located during address 0x0000 to 0x1FFF.

The GPM8F3132C-QV043 program memory is code area with 32KB memory size. If system clock is set to PLL output with 64MHz PLL output frequency. CPU operating in 16MHz frequency.

The address 0x008F is used for CONFIG_BYTE whose definition of each bit is described inTable 5-4. User can lock the program or content by setting CONFIG_BYTE [0]. If CONFIG_BYTE[0] is programmed to be '0', the whole chip memory is protected and any page erase or program by two wire serial interface is not allowed. The only thing user can do is to erase whole chip. Figure 5.2-1 shows the program memory map of 32KB Flash.

After each reset, CPU starts execution in the program memory at location 0x0000. Each interrupt has its own start address for service routine. The Flash memory can be programmed in-system, through the ICESCK/ICESDA interface or by software using the MOVX instruction when PWE= 1. User can refer to the example code in the programming guide for the procedure of write and erase operations. Flash data can not be programmed from a '0' to a '1', and only erase operation can realize it. Therefore, flash data would typically be erased (set to 0xFF) before being programmed. The write and erase operations are executed by using Pseudo-idle mode to be automatically timed by hardware without data polling to determine the end of the write and erase operation.

For software security consideration, user can set the programmable Flash level by FLH_CTRL1 register to limit the code area that avoids inadvertently erased or written by software; the protected region is called READONLY_PAGE.

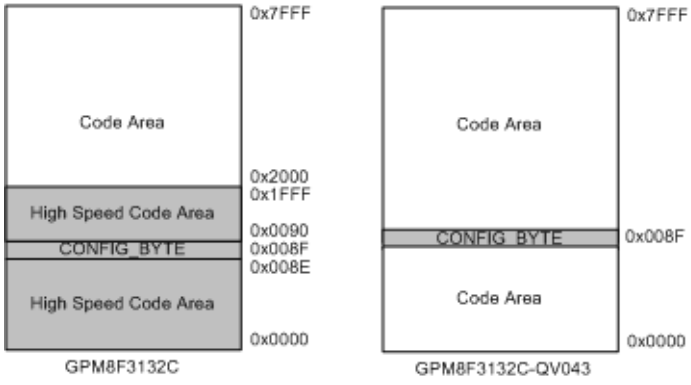


Figure 5.2-1 Program memory organization

CONFIG_BYTE			Address: 0x8F (Code Area)		CONFIG_BYTE Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	--	CODE Lock
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:1	--	R	Reserved	

Bit	Function	Type	Description	Condition
0	CODE Lock	R	0 : CODE is locked; 1 : CODE is unlocked	

Table 5-4 The CONFIG_BYTE register

FLH_CTRL0			Address: 0xEC		Flash Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	FLH_PERASE	FLH_PROG
Default	0	0	0	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x51							

Bit	Function	Type	Description	Condition
7:2	--	R/W	Reserved	
1	FLH_PERASE	R/W	Flash page erase enable bit. ***The page erase is prohibited if address is range over 0x0000 to 0x1FFF.*** 0: Flash page erase is disabled 1: Flash page erase is enabled	
0	FLH_PROG		Flash program enable bit. ***The program is prohibited if address is range over 0x0000 to 0x1FFF.*** 0: Flash program is disabled 1: Flash program is enabled	

Table 5-5 The FL_LEVELLASH_CTRL0 register

FLH_CTRL1			Address: 0xED		Flash Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	FLASH_LEVEL[4:0]				
Default	0	0	0	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x51							

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	FLASH_LEVEL[4:0]	R/W	FLASH_LEVEL, it determines how many 1K pages are read only	

FLASH_LEVEL	Note
0	no page is read only
1	Prohibit
2	Prohibit
3	Prohibit
4	Prohibit
5	Prohibit
6	Prohibit
7	address < 0x2000 is read only
8	address < 0x2400 is read only
9	address < 0x2800 is read only
10	address < 0x2C00 is read only
11	address < 0x3000 is read only
12	address < 0x3400 is read only
13	address < 0x3800 is read only

Bit	Function	Type	Description		Condition
			14	address < 0x3C00 is read only	
			15	address < 0x4000 is read only	
			16	address < 0x4400 is read only	
			17	address < 0x4800 is read only	
			18	address < 0x4C00 is read only	
			19	address < 0x5000 is read only	
			20	address < 0x5400 is read only	
			21	address < 0x5800 is read only	
			22	address < 0x5C00 is read only	
			23	address < 0x6000 is read only	
			24	address < 0x6400 is read only	
			25	address < 0x6800 is read only	
			26	address < 0x6C00 is read only	
			27	address < 0x7000 is read only	
			28	address < 0x7400 is read only	
			29	address < 0x7800 is read only	
			30	address < 0x7C00 is read only	
			31	address < 0x8000 is read only	
			Note 1. Only FLASH_LEVEL[4:0] is useful in GPM8F3132C		

Table 5-6 The FLH_CTRL1 register

5.2.3. Data Memory Allocation

Data memory addresses allocates on the GPM8F3132C/ GPM8F3132C-QV043 are divided into two parts. The first part is 1K/ 8K bytes of external RAM and the second one is 256 byte IDM shown in Figure 5.2-2 . The lowest internal data memory (IDM) consists of four register banks with eight registers each. A bit addressable segment with 128 bits (16 bytes) begins at 0x20. The address from 0x30 to 0x7F is not defined and can be utilized freely by user. The last 128 bytes of data memory can be used by different addressing modes. With the indirect addressing mode, address from 0x80 to 0xFF shared with stack space is addressed. With the direct addressing mode, the SFR addressing from 0x80 to 0xFF is accessed. The SFR memory map is shown in Table 5-7

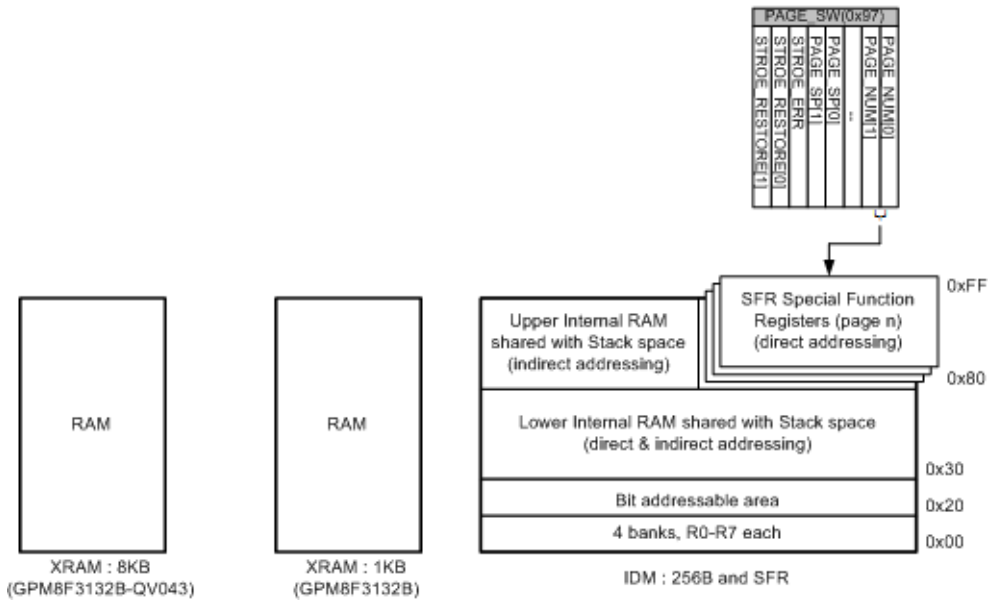


Figure 5.2-2 Data memory organization

Note1: Gray Area : common SFR register ; White area : additional SFR register;
Note2: Switch page is unnecessary when user gray area is written.

Page0	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	EIP	SYS_CTRL0	SYS_CTRL1	SYS_CTRL2	SYS_CTRL3	SYS_CTRL4	SYS_CTRL5	SYS_CTRL6
0xF0	B	OP_CTRL0	OP_CTRL1	OP_CTRL2				
0xE8	EIE	Reserved	Reserved	KEYCODE	FLH_CTRL0	FLH_CTRL1	Reserved	Reserved
0xE0	ACC	ADC1_CTRL0	ADC1_CTRL1	ADC1_DATA_L	ADC1_DATA_H	EXT_INT_EN	EXT_INT_EDGE	EXT_INT_STS
0xD8	WDCON	ADC0_CTRL0	ADC0_CTRL1	ADC0_DATA_L	ADC0_DATA_H	ADC_VREF_CTRL		
0xD0	PSW	I2C_CTRL	I2C_STS	I2C_DID	I2C_DATA	Reserved	Reserved	Reserved
0xC8	Reserved	Reserved						I2C_DEBOUNCE
0xC0	P4	P4_ID						
0xB8	IP	P1_ID	P1_DIR	P1_ATT		P1_SR		
0xB0	P3	P3_ID	P3_DIR	P3_ATT		P3_SR		
0xA8	IE	P0_ID	P0_DIR	P0_ATT		P0_SR		
0xA0	P2	P2_ID	P2_DIR	P2_ATT		P2_SR		
0x98	SCON0	SBUF0	SPI_CTRL	SPI_STS	SPI_TXD	SPI_RXD	BODY_ID0	BODY_ID1
0x90	P1	EIF	Reserved	Reserved	Reserved	Reserved		PAGE_SW
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	Reserved
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

Page1	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	EIP						SYS_CTRL5	SYS_CTRL6
0xF0	B							
0xE8	EIE	Reserved	Reserved	KEYCODE	FLH_CTRL0	FLH_CTRL1	Reserved	Reserved
0xE0	ACC							EXT_INT_STS
0xD8	WDCON							
0xD0	PSW					Reserved	Reserved	Reserved
0xC8	Reserved	Reserved						
0xC0	P4	P4_ID	P4_DIR	P4_ATT		P4_SR		
0xB8	IP	P1_ID						
0xB0	P3	P3_ID						
0xA8	IE	P0_ID						
0xA0	P2	P2_ID						
0x98	SCON0	SBUF0						
0x90	P1	EIF	Reserved	Reserved	Reserved	Reserved		PAGE_SW
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	Reserved
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F

Page2	*0/8*	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*
0xF8	EIP						SYS_CTRL5	SYS_CTRL6
0xF0	B							
0xE8	EIE	Reserved	Reserved	KEYCODE	FLH_CTRL0	FLH_CTRL1	Reserved	Reserved
0xE0	ACC							EXT_INT_STS
0xD8	WDCON							
0xD0	PSW	TMC_CAP4_L	TMC_CAP4_H	TMC_CAP5_L	TMC_CAP5_H	Reserved	Reserved	Reserved
0xC8	Reserved	Reserved	TMC_CAP1_L	TMC_CAP1_H	TMC_CAP2_L	TMC_CAP2_H	TMC_CAP3_L	TMC_CAP3_H
0xC0	P4	P4_ID	TMC_CAP_CTRL1		TMC_CAP_INTEN	TMC_CAP_INTSTS	TMC_CAP0_L	TMC_CAP0_H
0xB8	IP	P1_ID	TMC_CTRL	TMC_PLOAD_L	TMC_PLOAD_H	TMC_L	TMC_H	TMC_CAP_CTRL0
0xB0	P3	P3_ID	TMB_CCP3_L	TMB_CCP3_H				
0xA8	IE	P0_ID	TMB_CCP0_L	TMB_CCP0_H	TMB_CCP1_L	TMB_CCP1_H	TMB_CCP2_L	TMB_CCP2_H
0xA0	P2	P2_ID	TMB_CAP_CTRL1	TMB_CAP_INTCTR	TMB_PWM_CTRL0	TMB_PWM_CTRL1	TMB_PWM_DTIME	
0x98	SCON0	SBUF0	TMB_CTRL	TMB_PLOAD_L	TMB_PLOAD_H	TMB_L	TMB_H	TMB_CAP_CTRL0
0x90	P1	EIF	Reserved	Reserved	Reserved	Reserved		PAGE_SW
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	Reserved
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

Page3	*0/8*	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*
0xF8	EIP						SYS_CTRL5	SYS_CTRL6
0xF0	B							
0xE8	EIE	Reserved	Reserved	KEYCODE	FLH_CTRL0	FLH_CTRL1	Reserved	Reserved
0xE0	ACC							EXT_INT_STS
0xD8	WDCON	MDU_CTRL0	MDU_DSRC_ADR0	MDU_DSRC_ADR1	MDU_DTAR_ADDR	MDU_CTRL1		
0xD0	PSW	TMA_PWM5_END_L	TMA_PWM5_END_H		TMA_PWM_DTSEL	Reserved	Reserved	Reserved
0xC8	Reserved	Reserved	TMA_PWM2_END_L	TMA_PWM2_END_H	TMA_PWM3_END_L	TMA_PWM3_END_H	TMA_PWM4_END_L	TMA_PWM4_END_H
0xC0	P4	P4_ID	TMA_ADC_TRG1_L	TMA_ADC_TRG1_H	TMA_PWM0_END_L	TMA_PWM0_END_H	TMA_PWM1_END_L	TMA_PWM1_END_H
0xB8	IP	P1_ID	TMA_CCP4_L	TMA_CCP4_H	TMA_CCP5_L	TMA_CCP5_H	TMA_ADC_TRG0_L	TMA_ADC_TRG0_H
0xB0	P3	P3_ID	TMA_CCP1_L	TMA_CCP1_H	TMA_CCP2_L	TMA_CCP2_H	TMA_CCP3_L	TMA_CCP3_H
0xA8	IE	P0_ID	TMA_PWM_CTRL2	TMA_PWM_CTRL3	TMA_PWM_OVRD	TMA_PWM_DTIME	TMA_CCP0_L	TMA_CCP0_H
0xA0	P2	P2_ID	TMA_CAP_CTRL1	TMA_CAP_CTRL2	TMA_CAP_INTEN	TMA_CAP_INTSTS	TMA_PWM_CTRL0	TMA_PWM_CTRL1
0x98	SCON0	SBUF0	TMA_CTRL	TMA_PLOAD_L	TMA_PLOAD_H	TMA_L	TMA_H	TMA_CAP_CTRL0
0x90	P1	EIF	Reserved	Reserved	Reserved	Reserved		PAGE_SW
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	Reserved
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*

Table 5-7 SFR memory map

PAGE_SW			Address: 0x97		Page Switch Register			
Bit	7	6	5	4	3	2	1	0
Function	STORE_RESTORE		STORE_ERR	PAGE_SP		--	PAGE_NUM	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	STORE_RESTORE	W	PAGE_NUM load or restore contorl bit. STORE_RESTORE: Description 0X: The PAGE_NUM is directly updated by CPU write and PAGE_SP is inactive. 10: The latest page number is written to the PAGE_NUM. In the same time, the previous contents of PAGE_NUM are saved in the storage register which is indicated by PAGE_SP. 11: The PAGE_NUM is overwritten by the contents of the storage register which indicated by PAGE_SP and the CPU write will be ignored.	
5	STORE_ERR	R/W	This bit is used to indicate the status of PAGE_NUM store / restore function. read: 0 : page number store / restore function is normally operating. 1 : page number store / restore function is abnormally. Because successive store or restore is over 2 times. write: 0 : clear this bit 1 : no effect	
4:3	PAGE_SP	R	Page number storage pointer	
2	--	R/W	Reserved	
1:0	PAGE_NUM	R/W	These bits are used to indicate which SFR page is active now. 00 : page 0 01 : page 1 10 : page 2 11 : page 3	

Table 5-8 The PAGE_SW register

5.2.4. Memory Related SFR

The following sub-sections describe program, external and internal memories related SFRs of 8051 core and their functionality. For other information about standard SFRs, please refer to appropriate peripheral section.

5.2.4.1. Program write enable bit

The Program Write Enable (PWE) bit, located in PCON register bit 4, is used during MOVX instructions. When PWE bit is set to logic 1, the MOVX @DPTR, An instruction writes data located in accumulator register into program memory addressed by DPTR register. Program memory can be read by MOVC only regardless of PWE bit.

5.2.4.2. Data pointer registers

Dual data pointer registers are implemented to speed up data block copying. DPTR0 and DPTR1 are located in four SFR addresses. Active DPTR register is selected by SEL bit (DPS[0]). If SEL=0 then DPTR0 is selected otherwise DPTR1.

5.2.4.3. Stack pointer

The 8051 has 8-bit stack pointer called SP (0x81) located in the internal RAM space. It is incremented before data is stored during PUSH and CALL execution and decremented after data is popped during POP, RET and RETI execution. In the other words, it always points to the last valid stack byte. The SP is accessed as any other SFRs. Figure 5.2-3 shows an example when PUSH A is executed and Figure 5.2-4 shows an example when POP PSW is executed.

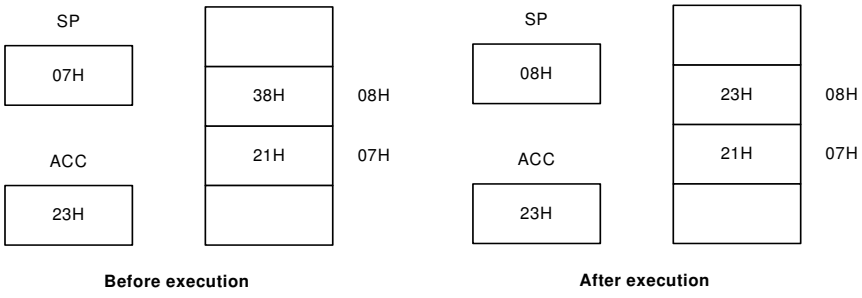


Figure 5.2-3 Stack byte order for PUSH A instruction

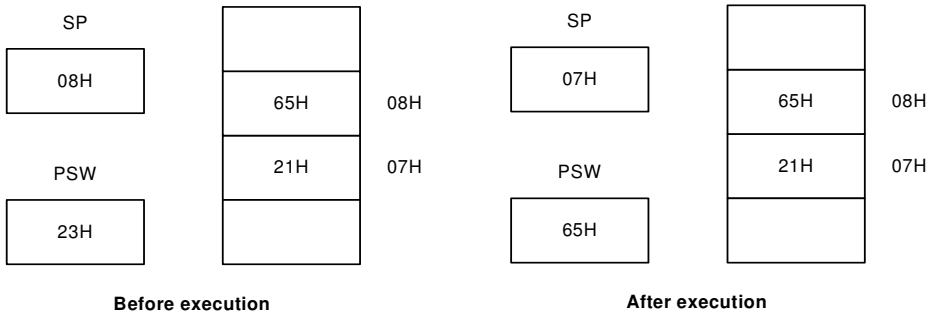


Figure 5.2-4 Stack byte order for POP PSW instruction

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	--	PWE	--	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 double baud rate bit when clocked by Timer1	

Bit	Function	Type	Description	Condition
5	--	R/W	Reserved	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3:2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-9 The PCON register

DPH0			Address: 0x83		Data Pointer Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[15:8]	R/W	Data pointer register DPTR0 - high byte	

Table 5-10 The DPH0 register

DPL0			Address: 0x82		Data Pointer Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[7:0]	R/W	Data pointer register DPTR0 - low byte	

Table 5-11 The DPL0 register

DPH1			Address: 0x85		Data Pointer 1 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR1[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[15:8]	R/W	Data pointer 1 register DPTR1 - high byte	

Table 5-12 The DPH1 register

DPL1			Address: 0x84		Data Pointer 1 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[7:0]	R/W	Data pointer 1 register DPTR1 - low byte	

Table 5-13 The DPL1 register

DPS			Address: 0x86		Data Pointer Select Register			
Bit	7	6	5	4	3	2	1	0
Function	ID1	ID0	TSL	-	-	-	-	SEL
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	ID[1:0]	R/W	Increment/decrement function select. See Table **5-15**	
5	TSL	R/W	Toggle select enable bit 0: DPTR related instructions do not affect state of SEL bit 1: DPTR related instructions to toggle the SEL bit p.s. The DPTR related instructions are as below a.MOVX A,@DPTR b.MOVX @DPTR,A c.INC DPTR d.MOV DPTR,#data16 e.MOVC A,@A+DPTR	
4:1	--	R/W	Reserved	
0	SEL	R/W	Active data pointer select bit See Table **5-15**	

Table 5-14 The DPS register

ID1	ID0	SEL=0	SEL=1
0	0	INC DPTR0	INC DPTR1
0	1	DEC DPTR0	INC DPTR1
1	0	INC DPTR0	DEC DPTR1
1	1	DEC DPTR0	DEC DPTR1

Table 5-15 DPTR0/DPTR1 operations

SP			Address: 0x81		Stack Pointer Register			
Bit	7	6	5	4	3	2	1	0
Function	SP[7:0]							
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:0	SP[7:0]	R/W	Stack pointer	

Table 5-16 The SP register

5.3. Special Function Registers(SFR)

GPM8F3132C family has up to 178 control registers for special function registers. All of the SFRs are used by MCU and peripheral function block for controlling the desired operation. Some of the SFRs contain control and status bits for peripheral module such as Timer unit, Interrupt control unit, etc. Some of bits in SFRs are read only, so write to those bits don't have any effect on corresponding bits. Some SFRs have key code design that KEYCODE register must be written with correct key codes, in sequence, before writing a value to it for software security. The following table shows the summary of the SFRs. The detailed information of each SFRs are explained in each peripheral section.

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
Any	0x80	P0		0xFF	Port 0							
Any	0x81	SP		0x07	Stack Pointer							
Any	0x82	DPL0		0x00	Data pointer register DPTR0 - low byte							
Any	0x83	DPH0		0x00	Data pointer register DPTR0 - high byte							
Any	0x84	DPL1		0x00	Data pointer register DPTR1 - low byte							
Any	0x85	DPH1		0x00	Data pointer register DPTR1 - high byte							
Any	0x86	DPS		0x00	ID1	ID0	TSL	--	--	--	--	SEL
Any	0x87	PCON		0x00	SMOD0	SMOD1	--	PWE	--	--	STOP	--
Any	0x88	TCON		0x00	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Any	0x89	TMOD		0x00	--	CT1	M11	M10	--	CT0	M01	M00
Any	0x8A	TL0		0x00	Timer 0 Load value – low byte							
Any	0x8B	TL1		0x00	Timer 1 Load value – low byte							
Any	0x8C	TH0		0x00	Timer 0 Load value – high byte							
Any	0x8D	TH1		0x00	Timer 1 Load value – high byte							
Any	0x8E	CKCON		0x07	WD1	WD0	WDFM	T1M	T0M	--	--	--
Any	0x8F	--		--	Reserved							
Any	0x90	P1		0xFF	Port 1							
Any	0x91	EIF		0x00	--	--	--	EXTF	LVDF	SPIF	I2CF	MDUF
Any	0x92	--		--	Reserved							
Any	0x93	--		--	Reserved							
Any	0x94	--		--	Reserved							
Any	0x95	--		--	Reserved							
Any	0x97	PAGE_SW		0x00	STORE_RESTORE[1:0]		STORE_ERR	PAGE_SP[1:0]		--	PAGE_NUM[1:0]	
Any	0x98	SCON0		N/A	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Any	0x99	SBUF0		N/A	UART 0 buffer							
Any	0xA0	P2		0xFF	Port 2							
Any	0xA1	P2_ID		0x00	Port 2 input data							
Any	0xA8	IE		0x00	EA	ETC	ETB	ES0	ET1	EX1	ET0	ETA
Any	0xA9	P0_ID		0x00	Port 0 input data							
Any	0xB0	P3		0xFF	--	--	--	--	Port 3[3:0]			
Any	0xB1	P3_ID		0x00	--	--	--	--	Port 3 input data[3:0]			
Any	0xB8	IP		0x00	--	PTC	PTB	PS0	PT1	PX1	PT0	PTA
Any	0xB9	P1_ID		0x00	Port 1 input data							
Any	0xC0	P4		N/A	MDU_INTF	--	--	--	--	Port 4[2:0]		
Any	0xC1	P4_ID		0x00	--	--	--	--	--	Port 4 input data[2:0]		
Any	0xC8	--		--	Reserved							
Any	0xC9	--		--	Reserved							

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
Any	0xD0	PSW		0x00	CY	AC	F0	RS1	RS0	OV	F1	P
Any	0xD5	--		--	Reserved							
Any	0xD6	--		--	Reserved							
Any	0xD7	--		--	Reserved							
Any	0xD8	WDCON		0x00	--	--	--	--	WDIF	--	EWT	RWT
Any	0xE0	ACC		0x00	ACC register							
Any	0xE7	EXT_INT_STS		0x00	--	--	EXT_INT_STS[5:0]					
Any	0xE8	EIE		0x00	--	--	EWDI	EEXT	ELVD	ESPI	EI2C	EMDU
Any	0xE9	--		--	Reserved							
Any	0xEA	--		--	Reserved							
Any	0xEB	KEYCODE		0x00	Key Code							
Any	0xEC	FLH_CTRL0	8F/32/51	0x00	--	--	--	--	--	--	FLH_PERASE	FLH_PROG
Any	0xED	FLH_CTRL1	8F/32/51	0x00	--	--	--	FLASH_LEVEL[4:0]				
Any	0xEE	--		--	Reserved							
Any	0xEF	--		--	Reserved							
Any	0xF0	B		0x00	B register							
Any	0xF8	EIP		0x00	--	--	PWDI	PEXT	PLVD	PSPI	PI2C	PMDU
Any	0xFE	SYS_CTRL5	8F/32/50	0xC4	TMR_CKEN	--	MDU_CKEN	--	SPI_CKEN	UART_CKEN	I2C_CKEN	ADC_CKEN
Any	0xFF	SYS_CTRL6	8F/32/50	0x02	--	--	UART_IF_EN	T01_CK_SEL	--	AERR_RSTEN	WDOG_CKEN	--

Table 5-17 The common SFR register

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0	0x9A	SPI_CTRL		0x00	POLARITY	PHASE	CSB_KEEP	SPI_CLK_SEL[1:0]		SPI_EN	SPI_MODE	SPI_START
0	0x9B	SPI_STS		0x00	SPI_INTEN	--	--	--	--	--	RX_DONE	TX_DONE
0	0x9C	SPI_TXD		0x00	SPI transmission data							
0	0x9D	SPI_RXD		0x00	SPI receive data							
0	0x9E	BODY_ID0		0x00	BODY ID0							
0	0x9F	BODY_ID1		0x00	BODY ID1							
0	0xA2	P2_DIR		0x00	Port 2 direction control bit							
0	0xA3	P2_ATT		0x00	Port 2 attribute control bit							
0	0xA	P2_SR		0x00	Port 2 slew rate control bit							
0	0xAA	P0_DIR		0x00	Port 0 direction control bit							
0	0xAB	P0_ATT		0x00	Port 0 attribute control bit							
0	0xAD	P0_SR		0x00	Port 0 slew rate control bit							
0	0xB2	P3_DIR		0x00	Port 3 direction control bit							
0	0xB3	P3_ATT		0x00	Port 3 attribute control bit							
0	0xB5	P3_SR		0x00	Port 3 slew rate control bit							
0	0xBA	P1_DIR		0x00	Port 1 direction control bit							
0	0xBB	P1_ATT		0x00	Port 1 attribute control bit							
0	0xBD	P1_SR		0x00	Port 1 slew rate control bit							
0	0xCF	I2C_DEBOUNCE		0x00	--	--	I2C de-bounce count[5:0]					
0	0xD1	I2C_CTRL		0x20	MST_STR	MST_STP	MST_NACK	MODE	I2C_CLK_SEL[1:0]		I2C_TRIG	I2C_EN
0	0xD2	I2C_STS		0x00	SLV_DID_OK	SLV_DAT_OK	SLV_STP_OK	ERR_SDID_IE	--	I2C_INT_EN	NO_ACK	TS_DONE

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0	0xD3	I2C_DID		0x01	I2C device ID							
0	0xD4	I2C_DATA		0x00	I2C Tx / Rx data							
0	0xD9	ADC0_CTRL0		0x00	ADC0_INTEN	ADC0_SH_CYCLE[1:0]		ADC0_CLK_SEL[1:0]			--	--
0	0xDA	ADC0_CTRL1		0x00	ADC0_START	--	--	ADC0_INTF	--	ADC0_CH_SEL[2:0]		
0	0xDB	ADC0_DATA_L		0x00	ADC0 output data – low nibble byte				--	--	--	--
0	0xDC	ADC0_DATA_H		0x00	ADC0 output data – high byte							
0	0xDD	ADC_VREF_CTRL		0x00	--	--	--	--	ADCVREF_SEL[2:0]			ADVREF_EN
0	0xE1	ADC1_CTRL0		0x00	ADC1_INTEN	ADC1_SH_CYCLE[1:0]		ADC1_CLK_SEL[1:0]			--	--
0	0xE2	ADC1_CTRL1		0x00	ADC1_START	--	--	ADC1_INTF	--	ADC1_CH_SEL[2:0]		
0	0xE3	ADC1_DATA_L		0x00	ADC1 output data – low nibble byte				--	--	--	--
0	0xE4	ADC1_DATA_H		0x00	ADC1 output data – high byte							
0	0xE5	EXT_INT_EN		0x00	DEBOUNCE_TIME[1:0]		EXT_INT_EN[5:0]					
0	0xE6	EXT_INT_EDGE		0x00	--	--	EXT_INT_EDGE[5:0]					
0	0xF1	OP_CTRL0		0x00	--	--	--	--	--	OP_BIAS_ADJ[1:0]		OP_EN
0	0xF2	OP_CTRL1		0x00	CMPU_O	CU_IO_OEN	CMPU_VREF_SEL[4:0]					CMPU_EN
0	0xF3	OP_CTRL2		0x00	CMPD_O	CD_IO_OEN	CMPD_VREF_SEL [4:0]					CMPD_EN
0	0xF9	SYS_CTRL0	8F/32/50	0x01	--	CLK_DIV[1:0]		--	--	--	--	--
0	0xFA	SYS_CTRL1	8F/32/50	0x00	PLL_LOCKIN	PLL_N		CLK_DIV_SEL	--	CLK_SRC_SEL	PLL_CHG_EN	PLL_EN
0	0xFB	SYS_CTRL2	8F/32/50	0x03	--	--	--	--	V18_SEL[1:0]		IOSC32K_EN	--
0	0xFC	SYS_CTRL3	8F/32/50	0x25	--	LVD_INT_EN	LVD_SEL[1:0]		LVD_EN	LVR_SEL[1:0]		LVR_EN
0	0xFD	SYS_CTRL4	8F/32/50	0x00	--	WDOG_RST	SW_RST_EN	LVR_RST	LVD_INTF	LVD_STS	ADDR_ERR	ERR_WR

Table 5-18 The additional SFR register (page0)

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
1	0xC2	P4_DIR		0x00	--	--	--	--	--	Port 4 direction control bit[2:0]		
1	0xC3	P4_ATT		0x00	--	--	--	--	--	Port 4 attribute control bit[2:0]		
1	0xC5	P4_SR		0x00	--	--	--	--	--	Port 4 slew rate control bit[2:0]		

Table 5-19 The additional SFR register (page1)

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
2	0x9A	TMB_CTRL		0x00	TMB_EDGE	ALIGN_TYPE	TMB_INTF	TMB_INTEN	CLK_SRC_SEL[2:0]			TMB_EN
2	0x9B	TMB_PLOAD_L		0x00	Timer B pre-load data– low byte							
2	0x9C	TMB_PLOAD_H		0x00	Timer B pre-load data – high byte							
2	0x9D	TMB_L		0x00	Timer B – low byte							
2	0x9E	TMB_H		0x00	Timer B – high byte							
2	0x9F	TMB_CAP_CTRL0		0x00	--	--	--	--	Timer B capture enable			
2	0xA2	TMB_CAP_CTRL1		0x00	TMB_CAP3_EDGE[1:0]		TMB_CAP2_EDGE[1:0]		TMB_CAP1_EDGE[1:0]		TMB_CAP0_EDGE[1:0]	
2	0xA3	TMB_CAP_INTCR		0x00	TMB_CAP_STS[3:0]				TMB_CAP_INTEN[3:0]			
2	0xA4	TMB_PWM_CTRL0		0x00	--	TMB_PWM 23_MODE	--	TMB_PWM 01_MODE	TMB_PWMx_EN[3:0]			
2	0xA5	TMB_PWM_CTRL1		0x00	--	PWM_INT_POINT[1:0]		DUTY_DIR_ WR_EN	TMB_PWMx_POL[3:0]			

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
2	0xA6	TMB_PWM_DTIME		0x00	Timer B PWM dead time							
2	0xAA	TMB_CCP0_L		0x00	Timer B CCP0 – low byte							
2	0xAB	TMB_CCP0_H		0x00	Timer B CCP0 – high byte							
2	0xAC	TMB_CCP1_L		0x00	Timer B CCP1 – low byte							
2	0xAD	TMB_CCP1_H		0x00	Timer B CCP1 – high byte							
2	0xAE	TMB_CCP2_L		0x00	Timer B CCP2 – low byte							
2	0xAF	TMB_CCP2_H		0x00	Timer B CCP2 – high byte							
2	0xB2	TMB_CCP3_L		0x00	Timer B CCP3 – low byte							
2	0xB3	TMB_CCP3_H		0x00	Timer B CCP3 – high byte							
2	0xBA	TMC_CTRL		0x00	--	--	TMC_INTF	TMC_INTEN	CLK_SRC_SEL[2:0]			TMC_EN
2	0xBB	TMC_PLOAD_L		0x00	Timer C pre-load data – low byte							
2	0xBC	TMC_PLOAD_H		0x00	Timer C pre-load data – high byte							
2	0xBD	TMC_L		0x00	Timer C – low byte							
2	0xBE	TMC_H		0x00	Timer C – high byte							
2	0xBF	TMC_CAP_CTRL0		0x00	--	--	Timer C capture enable[5:0]					
2	0xC2	TMC_CAP_CTRL1		0x00	TMC_CAP3_EDGE[1:0]		TMC_CAP2_EDGE[1:0]		TMC_CAP1_EDGE[1:0]		TMC_CAP0_EDGE[1:0]	
2	0xC3	TMC_CAP_CTRL2		0x00	--	--	--	--	TMC_CAP5_EDGE[1:0]		TMC_CAP4_EDGE[1:0]	
2	0xC4	TMC_CAP_INTEN		0x00	--	--	Timer C capture interrupt enable[5:0]					
2	0xC5	TMC_CAP_INTSTS		0x00	--	--	Timer C capture interrupt status flag[5:0]					
2	0xC6	TMC_CAP0_L		0x00	TMC_CAP0 – low byte							
2	0xC7	TMC_CAP0_H		0x00	TMC_CAP0 – high byte							
2	0xCA	TMC_CAP1_L		0x00	TMC_CAP1 – low byte							
2	0xCB	TMC_CAP1_H		0x00	TMC_CAP1 – high byte							
2	0xCC	TMC_CAP2_L		0x00	TMC_CAP2 – low byte							
2	0xCD	TMC_CAP2_H		0x00	TMC_CAP2 – high byte							
2	0xCE	TMC_CAP3_L		0x00	TMC_CAP3 – low byte							
2	0xCF	TMC_CAP3_H		0x00	TMC_CAP3 – high byte							
2	0xD1	TMC_CAP4_L		0x00	TMC_CAP4 – low byte							
2	0xD2	TMC_CAP4_H		0x00	TMC_CAP4 – high byte							
2	0xD3	TMC_CAP5_L		0x00	TMC_CAP5 – low byte							
2	0xD4	TMC_CAP5_H		0x00	TMC_CAP5 – high byte							

Table 5-20 The additional SFR register (page2)

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
3	0x9A	TMA_CTRL		0x00	TMA_EDGE	ALIGN_TYPE	TMA_INTF	TMA_INTEN	CLK_SRC_SEL[2:0]			TMA_EN
3	0x9B	TMA_PLOAD_L		0x00	Timer A pre-load data– low byte							
3	0x9C	TMA_PLOAD_H		0x00	Timer A pre-load data – high byte							
3	0x9D	TMA_L		0x00	Timer A – low byte							
3	0x9E	TMA_H		0x00	Timer A – high byte							
3	0x9F	TMA_CAP_CTRL0		0x00	--	--	Timer A capture enable					
3	0xA2	TMA_CAP_CTRL1		0x00	TMA_CAP3_EDGE[1:0]		TMA_CAP2_EDGE[1:0]		TMA_CAP1_EDGE[1:0]		TMA_CAP0_EDGE[1:0]	
3	0xA 3	TMA_CAP_CTRL2		0x00	--	--	--	--	TMA_CAP5_EDGE[1:0]		TMA_CAP4_EDGE[1:0]	
3	0xA4	TMA_CAP_INTEN		0x00	--	--	Timer A capture interrupt enable					

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
3	0xA5	TMA_CAP_INTSTS		0x00	---	--	Timer A capture interrupt status flag					
3	0xA6	TMA_PWM_CTRL0		0x00	DUTY_MODE	ADC_TRG_EN	TMA_PWMx_EN[5:0]					
3	0xA7	TMA_PWM_CTRL1		0x00	OVC_EN	DUTY_DIR _WR_EN	--	TMA_PWM 45_MODE	--	TMA_PWM 23_MODE	--	TMA_PWM0 1_MODE
3	0xAA	TMA_PWM_CTRL2		0x00	ADC_TRG_EDGE[1:0]		TMA_PWMx_POL[5:0]					
3	0xAB	TMA_PWM_CTRL3		0x3F	PWM_INT_POINT[1:0]		TMA_PWMx_CTR_SRC[5:0]					
3	0xAC	TMA_PWM_OVRD		0x00	EINT_SEL[1:0]		TMA_PWMx_OVRD[5:0]					
3	0xAD	TMA_PWM_DTIME		0x00	Timer A PWM dead time							
3	0xAE	TMA_CCP0_L		0x00	Timer A CCP0 – low byte							
3	0xAF	TMA_CCP0_H		0x00	Timer A CCP0 – high byte							
3	0xB2	TMA_CCP1_L		0x00	Timer A CCP1 – low byte							
3	0xB3	TMA_CCP1_H		0x00	Timer A CCP1 – high byte							
3	0xB4	TMA_CCP2_L		0x00	Timer A CCP2 – low byte							
3	0xB5	TMA_CCP2_H		0x00	Timer A CCP2 – high byte							
3	0xB6	TMA_CCP3_L		0x00	Timer A CCP3 – low byte							
3	0xB7	TMA_CCP3_H		0x00	Timer A CCP3 – high byte							
3	0xBA	TMA_CCP4_L		0x00	Timer A CCP4 – low byte							
3	0xBB	TMA_CCP4_H		0x00	Timer A CCP4 – high byte							
3	0xBC	TMA_CCP5_L		0x00	Timer A CCP5 – low byte							
3	0xBD	TMA_CCP5_H		0x00	Timer A CCP5 – high byte							
3	0xBE	TMA_ADC_TRG0_L		0x00	Timer A ADC trigger data-0 – low byte							
3	0xBF	TMA_ADC_TRG0_H		0x00	Timer A ADC trigger data-0 – high byte							
3	0xC2	TMA_ADC_TRG1_L		0x00	Timer A ADC trigger data-1 – low byte							
3	0xC3	TMA_ADC_TRG1_H		0x00	Timer A ADC trigger data-1 – high byte							
3	0xC4	TMA_PWM0_END_L		0x00	Timer A PWM0 end edge – low byte							
3	0xC5	TMA_PWM0_END_H		0x00	Timer A PWM0 end edge – high byte							
3	0xC6	TMA_PWM1_END_L		0x00	Timer A PWM1 end edge – low byte							
3	0xC7	TMA_PWM1_END_H		0x00	Timer A PWM1 end edge – high byte							
3	0xCA	TMA_PWM2_END_L		0x00	Timer A PWM2 end edge – low byte							
3	0xCB	TMA_PWM2_END_H		0x00	Timer A PWM2 end edge – high byte							
3	xCC	TMA_PWM3_END_L		0x00	Timer A PWM3 end edge – low byte							
3	0xCD	TMA_PWM3_END_H		0x00	Timer A PWM3 end edge – high byte							
3	0xCE	TMA_PWM4_END_L		0x00	Timer A PWM4 end edge – low byte							
3	0xCF	TMA_PWM4_END_H		0x00	Timer A PWM4 end edge – high byte							
3	0xD1	TMA_PWM5_END_L		0x00	Timer A PWM5 end edge – low byte							
3	0xD2	TMA_PWM5_END_H		0x00	Timer A PWM5 end edge – high byte							
3	0xD4	TMA_PWM_REV		0x00	--	--	--	--	--	TMA_PWM_REV[2:0]		
3	0xD9	MDU_CTRL0		0x00	--	DIV_ERR	MDU_INTF	MDU_MODE[2:0]			MDU_INTEN	MDU_EN
3	0xDA	MDU_DSRC_ADR0		0x00	MDU DMA source address 0							
3	0xDB	MDU_DSRC_ADR1		0x00	MDU DMA source address 1							
3	0xDC	MDU_DTAR_ADDR		0x00	MDU DMA target address							
3	0xDD	MDU_CTRL1		0x00	--	--	SFT_R_L	A_SHIFT_BIT[4:0]				

Table 5-21 The additional SFR register (page3)

5.4. Clock Source

GPM8F3132C family has two clock sources including internal oscillator (8.533MHz) and internal PLL clock source. These two clocks are chosen to be system clock source by controlling CLK_DIV_SEL and CLK_SRC_SEL bits of SYS_CTRL1 register. In addition, a clock divisor for the system clock source is contained to obtain different frequencies. There are four selection totally and can be controlled by CLK_DIV[1:0] bits of SYS_CTRL0 register. The block diagram of clock source and detailed description of SYS_CTRL0 and SYS_CTRL1 register are shown in Figure 5.4-1 , Table 5-22 and Table 5-23, respectively.

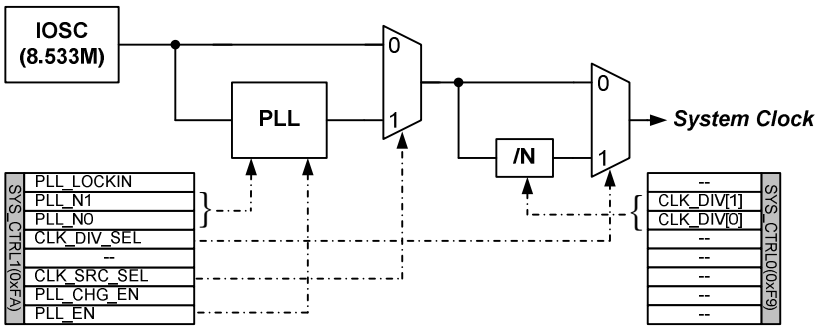


Figure 5.4-1 The block diagram of clock sources

SYS_CTRL0			Page : 0 / Address: 0xF9		System Control-0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	CLK_DIV[1 :0]		--	--	--	--	--
Default	0	0	0	0	0	0	0	1
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description
7	--	R/W	Reserved
6:5	CLK_DIV[1 :0]	R/W	System Clock divider. This function will disable automatic if CLK_SRC_SEL[1] of SYS_CTRL1 register is set to 1. CLK_DIV: System Divider 00: Clock Source / 2 01: Clock Source / 4 10: Clock Source / 8 11: Clock Source / 16
4:0	--	R/W	Reserved

Table 5-22 The SYS_CTRL0 register

SYS_CTRL1			Page : 0 / Address: 0xFA		System Control-1 Register			
Bit	7	6	5	4	3	2	1	0
Function	PLL_LOCKIN	PLL_N		CLK_DIV_SEL	--	CLK_SRC_SEL	PLL_CHG_EN	PLL_EN
Default	0	0	0	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description	Condition
7	PLL_LOCKIN	R	PLL lock-in flag. 0 : PLL is tracking or PLL is disable	

Bit	Function	Type	Description	Condition
			1 : PLL is locked-in	
6:5	PLL_N	R/W	PLL frequency select signals. ***User must to set CLK_DIV_SEL of SYS_CTRL1 register to 1 before set PLL_N to 11. After this setting, system clock is active in 38.403MHz / N , where N is depended on the setting value of CLK_DIV of SYS_CTRL0 register.*** PLL_N: 00 → PLL Output Frequency: 51.204MHz 01 → Prohibit 10 → 64MHz 11 → 38.403MHz	
4	CLK_DIV_SEL	R/W	System clock select signal. 0 : system clock = input clock source 1 : system clock = input clock source / N	
3	--	R/W	Reserved	
2	CLK_SRC_SEL	R/W	Clock input source select signals. CLK_SRC_SEL: 0 → Clock Source: 8.533M IOSC clock 1 → 38.403 / 51.204 / 64M PLL clock	
1	PLL_CHG_EN	R/W	PLL_N change enable signal. This bit must be set when users want to update PLL_N or 1st PLL enable. That will be cleared by H/W automatic. 0 : disable 1 : enable	
0	PLL_EN	R/W	Embedded PLL enable signal. 0 : disable 1 : enable	

Table 5-23 SYS_CTRL1 register

5.5. Power Saving Mode

5.5.1. Introduction

Although GPM8F3132C family is a high-speed microcontrollers designed for maximum performance, it also provide Power Management Unit (PMU) with an advanced power conservation modes. This mode is SLEEP mode. In order to reduce the current consumption when system does not need to be active, SLEEP mode can be utilized. For more information about this modes, please see the following section. Table 5-24 shows the two operating modes in GPM8F3132C family. In addition, user can save power consumption by reduce core power voltage by setting SYS_CTRL2.

5.5.2. SLEEP mode

SLEEP mode is the lowest power consumption state that the microcontroller can enter. It is achieved by cutting-off frequency provided to system clock, resulting in a fully static condition. Processor operation will be postponed on the instruction that sets the STOP bit. SLEEP mode can be exited by a Non-clocked interrupt such as the external interrupts EXT_IRQ0 to EXT_IRQ3. Clocked interrupts such as the watchdog timer and serial ports do not operate in SLEEP mode. After wakeup source trigger, processor operation will resume with the fetching of the interrupt vector associated with the interrupt that caused the exit from SLEEP mode. When the interrupt service routine is completed, RETI returns the program to the instruction immediately following the one that invoked the SLEEP mode. When EXT_IRQ0 to EXT_IRQ3 are used for wakeup source, EXT_INT_EN and EXT_INT_EDGE register must be set as shown in Table 5-26 , Table 5-27 and Table 5-28. The SLEEP mode operation flowed is showmen as Figure 5.5-1

In order to reduce power consumption when system operating in normal mode. User can switch-off clock of unused block by register setting independent. These register description are shown as Table 5-29 and Table 5-30.

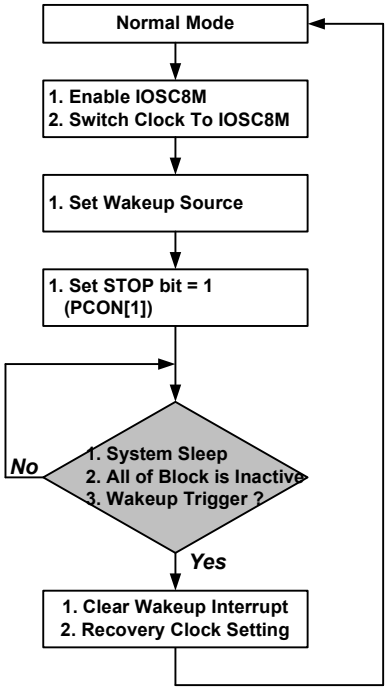


Figure 5.5-1 The SLEEP mode operating flow

	CPU clock	Peripheral clock	Wakeup source	After wakeup
Normal Mode	ON	Register setting	--	--
SLEEP Mode	OFF	OFF	1. External Interrupt	Next instruction state

Table 5-24 The two operation modes for GPM8F3132C family

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	--	PWE	--	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 double baud rate bit when clocked by Timer1	
5	--	R/W	Reserved	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3:2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-25 The PCON register

EXT_INT_EN			Page : 0 / Address : 0xE5		External Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0

Function	DEBOUNCE_TIME[1 :0]		EXT_INT5_EN	EXT_INT4_EN	EXT_INT3_EN	EXT_INT2_EN	EXT_INT1_EN	EXT_INT0_EN
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:6	DEBOUNCE_TIME	R/W	External interrupt de-bounce time select signal DEBOUNCE_TIME[1 :0] / Clock Cycle 00 / 4 01 / 37 10 / 72 11 / 142	
5	EXT_INT5_EN	R/W	Comparator down side interrupt enable signal. That is triggered by comparator down side output. 0 : disable 1 : enable	
4	EXT_INT4_EN	R/W	Comparator up side interrupt enable signal. That is triggered by comparator up side output. 0 : disable 1 : enable	
3	EXT_INT3_EN	R/W	External interrupt 3 enable signal that is mapped to P2_2. 0 : disable 1 : enable	
2	EXT_INT2_EN	R/W	External interrupt 2 enable signal that is mapped to P1_7. 0 : disable 1 : enable	
1	EXT_INT1_EN	R/W	External interrupt 1 enable signal that is mapped to P1_6. 0 : disable 1 : enable	
0	EXT_INT0_EN	R/W	External interrupt 0 enable signal that is mapped to P1_5. 0 : disable 1 : enable	

Table 5-26 The EXT_INT_EN register

EXT_INT_EDGE			**Page : 0 / Address : 0xE6**		**External Interrupt Edge Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	EXT_INT5_EDGE	EXT_INT4_EDGE	EXT_INT3_EDGE	EXT_INT2_EXGE	EXT_INT1_EDGE	EXT_INT0_EDGE
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	EXT_INT5_EDGE	R/W	Comparator down side interrupt trigger edge control signal 0 : falling edge 1 : rising edge	
4	EXT_INT4_EDGE	R/W	Comparator up side interrupt trigger edge control signal	

Bit	Function	Type	Description	Condition
			0 : falling edge 1 : rising edge	
3	EXT_INT3_EDGE	R/W	External interrupt 3 trigger edge control signal 0 : falling edge 1 : rising edge	
2	EXT_INT2_EDGE	R/W	External interrupt 2 trigger edge control signal 0 : falling edge 1 : rising edge	
1	EXT_INT1_EDGE	R/W	External interrupt 1 trigger edge control signal 0 : falling edge 1 : rising edge	
0	EXT_INT0_EDGE	R/W	External interrupt 0 trigger edge control signal 0 : falling edge 1 : rising edge	

Table 5-27 The EXT_INT_EDGE register

EXT_INT_STS			Address : 0xE7		External Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	EXT_INT5_STS	EXT_INT4_STS	EXT_INT3_STS	EXT_INT2_STS	EXT_INT1_STS	EXT_INT0_STS
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	EXT_INT5_STS	R/W	Comparator down side interrupt status flag. read: 0 : comparator down side interrupt is not occurred 1 : comparator down side interrupt is occurred write: 0 : clear this bit 1 : on effect	
4	EXT_INT4_STS	R/W	Comparator up side interrupt status flag. read: 0 : comparator up side interrupt is not occurred 1 : comparator up side interrupt is occurred write: 0 : clear this bit 1 : on effect	
3	EXT_INT3_STS	R/W	External interrupt 3 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clear this bit 1 : on effect	
2	EXT_INT2_STS	R/W	External interrupt 2 status flag.	

Bit	Function	Type	Description	Condition
			read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clear this bit 1 : on effect	
1	EXT_INT1_STS	R/W	External interrupt 1 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clear this bit 1 : on effect	
0	EXT_INT0_STS	R/W	External interrupt 0 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clear this bit 1 : on effect	

Table 5-28 The EXT_INT_STS register

SYS_CTRL5			Address : 0xFE		System Control-5 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMR_CKEN	--	MDU_CKEN	--	SPI_CKEN	UART_CKEN	I2C_CKEN	ADC_CKEN
Default	1	1	0	0	0	1	0	0
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description	Condition
7	TMR _CKEN	R/W	Timer controller clock enable signal. 0 : disable 1 : enable	
6	--	R/W	Reserved	
5	MDU_CKEN	R/W	MDU controller clock enable signal. 0 : disable 1 : enable	
4	--	R/W	Reserved	
3	SPI_CKEN	R/W	SPI controller clock enable signal. 0 : disable 1 : enable	
2	UART_CKEN	R/W	USRT controller clock enable signal. 0 : disable 1 : enable	
1	I2C_CKEN	R/W	I2C controller clock enable signal. 0 : disable 1 : enable	

Bit	Function	Type	Description	Condition
0	ADC_CKEN	R/W	ADC controller clock enable signal. 0 : disable 1 : enable	

Table 5-29 The SYS_CTRL5 register

SYS_CTRL6			Address : 0xFF		System Control-6 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	UART_IF_EN	T01_CK_SEL	--	AERR_RSTEN	WDOG_CKEN	--
Default	1	1	0	0	0	0	1	0
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	UART_IF_EN	R/W	UART interface enable signal. 0 : disable 1 : enable	
4	T01_CK_SEL	R/W	Timer0/1 clock source select signal.This bit is used combining with T0M/T1M of CKCON(0x8E). T0M /T1M | T01_CK_SEL | Timer0/1 Clock 0 | 0 | System Clock / 8 0 | 1 | System Clock / 2 1 | 0 | System Clock / 4 1 | 1 | System Clock / 1	
3	--	R/W	Reserved	
2	AERR_RSTEN	R/W	Flash address over range reset enable 0 : disable 1 : enable	
1	WDOG_CKEN	R/W	Watch dog controller clock enable control bit 0 : disable 1 : enable	
0	--	R/W	Reserved	

Table 5-30 The SYS_CTRL6 register

SYS_CTRL2			Page : 0 / Address: 0xFB		System Control 2 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	V18_SEL[1:0]		IOSC32K_EN	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R	Reserved	
3:2	V18_SEL	R/W	1.8V power domain select bit. V18_SEL[1:0] | Voltage of V18 00 | 2.1V	

Bit	Function	Type	Description	Condition
			01 prohibit 10 2.2V 11 2.3V	
1	IOSC32K_EN	R/W	Internal 32K oscillator enable bir 0 : disable 1 : enable	
0	--	R/W	Reserved	

Table 5-31 SYS_CTRL2 register

5.6. Interrupt System

5.6.1. Introduction

The GPM8F3132C family provides 13 types of interrupt sources with two levels interrupt priority control which tabled in Table 5-32 **錯誤! 找不到參照來源。**. For standard 8051 interrupt sources, each interrupt can be in high or low level priority group by setting or clearing a bit in the IP(0xB8) and EIP(0xF8) registers. INT0 has the top priority in default state and user can choose the related interrupt source to be the top priority by IP register. Interrupt requests are sampled each system clock at the rising edge of clock control. Each interrupt vector can be individually enabled or disabled by setting or clearing a corresponding bit in the IE(0xA8), EIE(0xE8). The IE contains global interrupt system disable(0) / enable(1) bit called EA.

In general, once an interrupt event occurs, the corresponding flag bit will be set. The related registers of interrupt flag are described as below.

If the related interrupt control bit is set to enable interrupt, an interrupt request signal will be generated and then CPU executes service routine. If the related interrupt control bit is disabled, programmer still can observe the corresponding flag bit, but no interrupt request signal will be generated. The interrupt flag bits must be cleared in the interrupt service routine to prevent program from deadlock in interrupt service routine. With any instruction, interrupts pending during the previous instruction is served. Before entering interrupt service routine, the system saves the current PC address into top of stack pointer and jumps to corresponding vector to execute the interrupt service. After finishing the interrupt service, the system abstract the return PC address from the top of the stack to execute the following instruction.

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Vector number	Priority
IE0	Timer A Interrupt	Low/Falling	Software(cleared by 0)	0x03	0	1
TF0	Timer 0 Interrupt	--	Hardware	0x0B	1	2
IE1	ADC0/1 Interrupt	Low/Falling	Software(cleared by 0)	0x13	2	3
TF1	Timer 1 Interrupt	--	Hardware	0x1B	3	4
TI0 & RI0	UART0 Interrupt	--	Software(cleared by 0)	0x23	4	5
TF2	Timer B Interrupt	--	Software(cleared by 0)	0x2B	5	6
TI1 & RI1	Timer C Interrupt	--	Software(cleared by 0)	0x33	6	7
INT2F	MDU	Low	Software(cleared by 0)	0x3B	7	8
INT3F	I2C	Low	Software(cleared by 0)	0x43	8	9
INT4F	SPI	Low	Software(cleared by 0)	0x4B	9	10
INT5F	LVD	Falling	Software(cleared by 0)	0x53	10	11
INT6F	External Interrupt	Falling	Software(cleared by 0)	0x5B	11	12
WDIF	Watchdog Interrupt	-	Software(cleared by 0)	0x63	12	13

Table 5-32 Summaries of all interrupt sources

IP			Address: 0xB8		Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	-	PTC	PTB	PS0	PT1	PX1	PT0	PTA
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	PTC	R/W	Timer C interrupt priority level control (1: high level)	
5	PTB	R/W	Timer B interrupt priority level control (1: high level)	
4	PS0	R/W	UART0 interrupt priority level control (1: high level)	
3	PT1	R/W	Timer 1 interrupt priority level control (1: high level)	
2	PX1	R/W	ADC0/1 interrupt priority level control (1: high level)	
1	PT0	R/W	Timer 0 interrupt priority level control (1: high level)	
0	PTA	R/W	Timer A interrupt priority level control (1: high level)	

Table 5-33 IP register

EIP			Address: 0xF8		Extended Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	PWDI	PEXT	PLVD	PSPI	PI2C	PMDU
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	--	R/W	Reserved	
5	PWDI	R/W	Watchdog interrupt priority level control (1: high level)	
4	PEXT	R/W	External interrupt priority level control (1: high level)	
3	PLVD	R/W	LVD interrupt priority level control (1: high level)	
2	PSPI	R/W	SPI interrupt priority level control (1: high level)	
1	PI2C	R/W	I2C interrupt priority level control (1: high level)	
0	PMDU	R/W	MDU interrupt priority level control (1: high level)	

Table 5-34 EIP register

IE			Address: 0xA8		Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	EA	ETC	ETB	ES0	ET1	EX1	ET0	ETA
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EA	R/W	Enable global interrupts	
6	ETC	R/W	Enable Timer C interrupt	
5	ETB	R/W	Enable Timer B interrupt	
4	ES0	R/W	Enable UART0 interrupt	
3	ET1	R/W	Enable Timer 1 interrupt	
2	EX1	R/W	Enable ADC0/1 interrupt	
1	ET0	R/W	Enable Timer 0 interrupt	

Bit	Function	Type	Description	Condition
0	ETA	R/W	Enable Timer A interrupt	

Table 5-35 IE register

EIE			Address: 0xE8		Extended Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	-	-	EWDI	EEXT	ELVD	ESPI	EI2C	EMDU
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	--	R/W	Reserved	
5	EWDI	R/W	Enable watchdog interrupt	
4	EEXT	R/W	Enable External interrupts	
3	ELVD	R/W	Enable LVD interrupts	
2	ESPI	R/W	Enable SPI interrupts	
1	EI2C	R/W	Enable I2C interrupts	
0	EMDU	R/W	Enable MDU interrupts	

Table 5-36 EIE register

TCON			Address: 0x88		Timer0/1 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TF1	R/W	Timer 1 interrupt (overflow) flag	
6	TR1	R/W	Timer 1 run control bit 0: disabled ; 1: enabled	
5	TF0	R/W	Timer 0 interrupt (overflow) flag	
4	TR0	R/W	Timer 0 run control bit 0: disabled ; 1: enabled	
3	IE1	R/W	ADC0/1 interrupt flag	
2	IT1	R/W	ADC0/1 level (at 0) / edge (at 1) sensitivity	
1	IE0	R/W	Timer A interrupt flag	
0	IT0	R/W	Timer A level (at 0) / edge (at 1) sensitivity	

Table 5-37 TCON register

WDCON			Address: 0xD8		Watchdog Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	WDIF	--	EWT	RWT
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	

Bit	Function	Type	Description	Condition
3	WDIF	R/W	Watchdog interrupt flag	
2	--	R/W	Reserved	
1	EWT	R/W	Watchdog timer reset enable bit 0: Disable; 1: Enable	
0	RWT	R/W	Reset watchdog timer 0: NA; 1: Reset	

Table 5-38 WDCON register

SCON0			Address: 0x98		UART0 configuration register			
Bit	7	6	5	4	3	2	1	0
Function	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Function	Type	Description	Condition
7:6	SM0[1:0]	R/W	Mode and baud rate setting	
5	SM02	R/W	Enables a multiprocessor communication feature	
4	REN0	R/W	Enable serial reception.	
3	TB08	R/W	The 9th transmitted data bit in Modes 2 and Mode 3	
2	RB08	R/W	In Mode 0, this bit is not used In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 2 and Mode 3, it is the 9th data bit received.	
1	TI0	R/W	UART0 transmitter interrupt flag	
0	RI0	R/W	UART0 receiver interrupt flag	

Table 5-39 SCON0 register

EIF			Address: 0x91		Extended interrupt flag			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	EXTF	LVDF	SPIF	I2CF	MDUF
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	EXTF	R/W	External interrupt flag	
3	LVDF	R/W	LVD interrupt flag	
2	SPIF	R/W	SPI interrupt flag	
1	I2CF	R/W	I2C interrupt flag	
0	MDUF	R/W	MDU interrupt flga	

Table 5-40 EIF register

TMA_CTRL			Page : 3 / Address: 0x9A		Timer A Control Register			
Bit	7	6	5	4	3	2	1	0
Function	TMA_EDGE	ALIGN_TYPE	TMA_INTF	TMA_INTEN	CLK_SRC_SEL			TMA_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TMA_EDGE	R	Timer A up/down count edge indication flag. 0 : falling edge 1 : rising edge	
6	ALIGN_TYPE	R/W	0 : edge align 1 : center align	
5	TMA_INTF	R/W	Timer A interrupt flag. read : 0 : idle / busy 1 : timer A interrupt trigger write : 0 : clear this bit 1 : no effect	
4	TMA_INTEN	R/W	Timer A interrupt enable signal 0 : disable 1 : enable	
3:1	CLK_SRC_SEL[2:0]	R/W	Timer A input clock source select signal. CLK_SRC_SEL[2:0] / Clock Source 000 / System clock 001 / System clock / 2 010 / System clock / 4 011 / System clock / 8 100 / System clock / 16 101 / System clock / 32 110 / IOSC_17.0667M 111 / ~32K (IOSC_32K)	
0	TMA_EN	R/W	Timer A enable signal. 0 : disable 1 : enable	

Table 5-41 TMA_CTRL register

TMA_CAP_INTEN			Page : 3 / Address: 0xA4		Timer A Capture Mode Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMA_CAP_INTEN[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	TMA_CAP_INTEN[5:0]	R/W	Timer A capture mode interrupt enable signals. These are map to CAP0 ~ CAP5 respectively. 0 : disable 1 : enable	

Table 5-42 TMA_CAP_INTEN register

TMA_CAP_INTSTS			Page : 3 / Address: 0xA5		Timer A Capture Mode Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMA_CAP_INTSTS[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	TMA_CAP_INTSTS[5:0]	R/W	Timer A capture mode interrupt flag. These are map to CAP0 ~ CAP5 respectively. read : 0 : no capture signal triggered 1 : capture signal triggered write : 0 : clear this bit 1 : no effect	

Table 5-43 TMA_CAP_INTSTS register

TMB_CTRL			Page : 2 / Address: 0x9A		Timer B Control Register			
Bit	7	6	5	4	3	2	1	0
Function	TMB_EDGE	ALIGN_TYPE	TMB_INTF	TMB_INTEN	CLK_SRC_SEL[2:0]			TMB_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TMB_EDGE	R	Timer B up/down count edge indication flag. 0 : falling edge 1 : rising edge	
6	ALIGN_TYPE	R/W	0 : edge align 1 : center align	
5	TMB_INTF	R/W	Timer B interrupt flag. read : 0 : idle / busy 1 : timer B interrupt trigger write : 0 : clear this bit 1 : no effect	
4	TMB_INTEN	R/W	Timer B interrupt enable signal 0 : disable 1 : enable	
3:1	CLK_SRC_SEL[2:0]	R/W	Timer B input clock source select signal. CLK_SRC_SEL[2:0] / Clock Source 000 / System clock 001 / System clock / 2 010 / System clock / 4 011 / System clock / 8 100 / System clock / 16 101 / System clock / 32	

Bit	Function	Type	Description	Condition
			110 IOSC_17.0667M 111 ~32K (IOSC_32KI)	
0	TMB_EN	R/W	Timer B enable signal. 0 : disable 1 : enable	

Table 5-44 TMB_CTRL register

TMB_CAP_INTCTR			Page : 2 / Address: 0xA3		Timer B Capture Mode Interrupt Control Register			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CAP_INTSTS[3:0]				TMB_CAP_INTEN[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	TMB_CAP_INTSTS[3:0]	R/W	Timer B capture mode interrupt flag. These are map to CAP0 ~ CAP3 respectively. read : 0 : no capture signal triggered 1 : capture signal triggered write : 0 : clear this bit 1 : no effect	
3:0	TMB_CAP_INTEN[5:0]	R/W	Timer B capture mode interrupt enable signals. These are map to CAP0 ~ CAP3 respectively. 0 : disable 1 : enable	

Table 5-45 TMB_CAP_INTEN register

TMC_CTRL			Page : 2 / Address: 0xBA		Timer C Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_INTF	TMC_INTEN	CLK_SRC_SEL[2:0]			TMC_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R	Reserved	
5	TMC_INTF	R/W	Timer C interrupt flag. read : 0 : idle / busy 1 : timer C interrupt trigger write : 0 : clear this bit 1 : no effect	
4	TMC_INTEN	R/W	Timer C interrupt enable signal 0 : disable 1 : enable	
3:1	CLK_SRC_SEL[2:0]	R/W	Timer C input clock source select signal.	

Bit	Function	Type	Description	Condition
			CLK_SRC_SEL[2:0] Clock Source 000 System clock 001 System clock / 2 010 System clock / 4 011 System clock / 128 100 System clock / 256 101 System clock / 512 110 System clock / 1024 111 Prohibit	
0	TMC_EN	R/W	Timer C enable signal. 0 : disable 1 : enable	

Table 5-46 TMC_CTRL register

TMC_CAP_INTEN			Page : 2 / Address: 0xC4		Timer C Capture Mode Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_CAP_INTEN[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:4	TMC_CAP_INTEN[5:4]	R/W	Timer C capture mode interrupt enable signals. These are map to comparator up/down side output respectively. 0 : disable 1 : enable	
3:0	TMC_CAP_INTEN[3:0]	R/W	Timer C capture mode interrupt enable signals. These are map to CAP0 ~ CAP3 respectively. 0 : disable 1 : enable	

Table 5-47 TMC_CAP_INTEN register

TMC_CAP_INTSTS			Page : 2 / Address: 0xC5		Timer C Capture Mode Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_CAP_INTSTS[3:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	TMC_CAP_INTSTS[5]	R/W	Timer C capture mode interrupt flag. This is map to comparator down side output respectively. read : 0 : no capture signal triggered 1 : capture signal triggered write : 0 : clear this bit	

Bit	Function	Type	Description	Condition
			1 : no effect	
4	TMC_CAP_INTSTS[4]	R/W	Timer C capture mode interrupt flag. This is map to comparator up side output respectively. read : 0 : no capture signal triggered 1 : capture signal triggered write : 0 : clear this bit 1 : no effect	
3:0	TMC_CAP_INTSTS[3:0]	R/W	Timer C capture mode interrupt flag. These are map to CAP0 ~ CAP3 respectively. read : 0 : no capture signal triggered 1 : capture signal triggered write : 0 : clear this bit 1 : no effect	

Table 5-48 TMC_CAP_INTSTS register

ADC0_CTRL0			Page : 0 / Address: 0xD9		ADC0 Control 0 register			
Bit	7	6	5	4	3	2	1	0
Function	ADC0_INTEN	ADC0_SH_CYCLE		ADC0_CLK_SEL			--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ADC0_INTEN	R/W	ADC0 interrupt enable control bit. 0 : disable 1 : enable	
6:5	ADC0_SH_CYCLE	R/W	ADC0 sample and hold cycle selection control bit. ADC0_SH_CYCLE / Cycle (ADC0_CLK) 00 / 2 01 / 4 10 / 8 11 / 16	
4:2	ADC0_CLK_SEL	R/W	ADC0 clock selection control bit ADC0_CLK_SEL / ADC0_CLK 000 / System clock / 2 001 / System clock / 4 010 / System clock / 8 011 / System clock / 12 100 / System clock / 16 101 / System clock / 20 110 / System clock / 24 111 / System clock / 28	
1:0	-	R/W	Reserved	

Table 5-49 ADC0_CTRL0 register

ADC0_CTRL1			Page : 0 / Address: 0xDA		ADC0 Control 1 register			
Bit	7	6	5	4	3	2	1	0
Function	ADC0_START	--	--	ADC0_INTF	--	ADC0_CH_SEL[2:0]		
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ADC0_START	R/W	ADC0 start transfer control bit 0: idle 1: start transfer	
6:5	-	R/W	Reserved	
4	ADC0_INTF	R/W	ADC0 interrupt flag. read : 0 : idle / converting 1 : conversion ready write : 0 : clear this bit 1 : no effect	
3	-	R/W	Reserved	
2:0	ADC0_CH_SEL	R/W	ADC0 channel selection control bit ADC0_CH_SEL / ADC0_CLK 000 / ADC0_CH0 (P0[0]) 001 / ADC0_CH1 (P0[1]) 010 / ADC0_CH2 (P0[2]) 011 / ADC0_CH3 (P0[3]) 100 / ADC0_CH4 (P0[4]) 101 / ADC0_CH5 (P0[5]) 110 / ADC0_CH6 (P0[6]) 111 / ADC0_CH7 (P0[7])	

Table 5-50 ADC0_CTRL1 register

ADC1_CTRL0			Page : 0 / Address: 0xE1		ADC1 Control 0 register			
Bit	7	6	5	4	3	2	1	0
Function	ADC1_INTEN	ADC1_SH_CYCLE		ADC1_CLK_SEL			--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ADC1_INTEN	R/W	ADC1 interrupt enable control bit. 0 : disable 1 : enable	
6:5	ADC1_SH_CYCLE	R/W	ADC1 sample and hold cycle selection control bit. ADC1_SH_CYCLE / Cycle (ADC1_CLK) 00 / 2 01 / 4 10 / 8	

Bit	Function	Type	Description	Condition
			11 16	
4:2	ADC1_CLK_SEL	R/W	ADC1 clock selection control bit ADC1_CLK_SEL: ADC1_CLK 000: System clock / 2 001: System clock / 4 010: System clock / 8 011: System clock / 12 100: System clock / 16 101: System clock / 20 110: System clock / 24 111: System clock / 28	
1:0	-	R/W	Reserved	

Table 5-51 ADC1_CTRL0 register

ADC1_CTRL1	Page : 0 / Address: 0xE2			ADC1 Control 1 register				
Bit	7	6	5	4	3	2	1	0
Function	ADC1_START	--	--	ADC1_INTF	--	ADC1_CH_SEL[2:0]		
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ADC1_START	R/W	ADC1 start transfer control bit 0: idle 1: start transfer	
6:5	-	R/W	Reserved	
4	ADC1_INTF	R/W	ADC1 interrupt flag. read : 0 : idle / converting 1 : conversion ready write : 0 : clear this bit 1 : no effect	
3	-	R/W	Reserved	
2:0	ADC1_CH_SEL	R/W	ADC1 channel selection control bit ADC1_CH_SEL: ADC1_CLK 000: ADC1_CH0 (P0[0]) 001: ADC1_CH1 (P0[1]) 010: ADC1_CH2 (P0[2]) 011: ADC1_CH3 (P0[3]) 100: ADC1_CH4 (P0[4]) 101: ADC1_CH5 (P0[5]) 110: ADC1_CH6 (P0[6]) 111: ADC1_CH7 (P0[7])	

Table 5-52 ADC1_CTRL1 register

MDU_CTRL0	Page : 3 / Address: 0xD9	Multiplier / Divider Control 0 Register

Bit	7	6	5	4	3	2	1	0
Function	--	DIV_ERR	MDU_INTF	MDU_MODE[2:0]			MDU_INTEN	MDU_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	DIV_ERR	R	Divisor error flag. read : 0 : divisor is a nonzero value. 1 : divisor is zero. This flag will be cleared automatic when divisor is updated to nonzero value.	
5	MDU_INTF	R/W	MDU interrupts flag. read : 0 : idle / busy 1 : MDU interrupt trigger write : 0 : clear this bit 1 : no effect	
4:2	MDU_MODE[2:0]	R/W	MDU operating mode MDU_MODE[2:0] / Mode 000 / Multiplier 001 / Divider with remainder 010 / Divider without remainder 011 / Adder 100 / Subtractor 101 / Arithmetic shift 110 / Prohibit 111 / Prohibit	
1	MDU_INTEN	R/W	MDU interrupt enable control bit. 0 : disable 1 : enable	
0	MDU_EN	R/W	MDU enable control bit. 0 : disable 1 : enable	

Table 5-53 MDU_CTRL register

P4			Address: 0xC0		Port4 Register			
Bit	7	6	5	4	3	2	1	0
Function	MDU_INTF	--	--	--	--	P42	P41	P40
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Function	Type	Description	Condition
7	MDU_INTF	R	MDU interrupt flag. 0 : idle / busy 1 : MDU interrupt trigger	
6:3	--	R/W	Reserved	

Bit	Function	Type	Description	Condition
2:0	P4[2:0]	R/W	P4 is used to set IO output data only. Otherwise, that also can be used to configure the Port4 function.	

Table 5-54 P5 register

I2C_STS			Page : 0 / Address: 0xD2		I2C Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	SLV_DID_OK	SLV_DAT_OK	SLV_STP_OK	ERR_SDID_IE	--	I2C_INT_EN	NO_ACK	TS_DONE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SLV_DID_OK	R/W	This bit indicates device ID was received by i2c controller. This is for slaver mode only. read: 0 : device ID is not asserted 1 : device ID is asserted write: 0 : clear this bit 1 : on effect	
6	SLV_DAT_OK	R/W	This bit indicates data was received or transmitted by i2c controller. This is for slaver mode only. read: 0 : data is transmitting or idle now 1 : data is transmission complete write: 0 : clear this bit 1 : on effect	
5	SLV_STP_OK	R/W	This bit indicates stop command was received by i2c controller. This is for slaver mode only. read: 0 : stop command is not assert 1 : stop command is asserted write: 0 : clear this bit 1 : on effect	
4	ERR_SDID_IE	R/W	Device ID error interrupt enable of slaver mode. 0 : disable 1 : enable	
3	--	R/W	Reserved	
2	I2C_INT_EN	R/W	I2C interrupt enable control bit. 0 : disable 1 : enable	
1	NO_ACK	R/W	I2C not have received acknowledging signal. read : 0 : acknowledge 1 : no acknowledge write :	

Bit	Function	Type	Description	Condition
			0 : clear this bit 1 : on effect	
0	TS_DONE	R	I2C transmission complete flag. read: 0 : i2c is idle or on going 1 : i2c is finished data transmission write: 0 : clear this bit 1 : on effect	

Table 5-55 I2C_STS register

SPI_STS			Page : 0 / Address: 0x9B		SPI Status Register			
Bit	7	6	5	4	3	2	1	0
Function	SPI_INTEN	--	--	--	--	--	RX_DONE	TX_DONE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SPI_INTEN	R/W	SPI interrupt enable 0 : disable 1 : enable	
6:2	--	R/W	Reserved	
1	RX_DONE	R	SPI finished data receiving with slaver mode. 0: Idle / Busy 1:Done	
0	TX_DONE	R	SPI finished data transmission with master mode. 0: Idle / Busy 1:Done	

Table 5-56 SPI_STS register

SYS_CTRL3			Page : 0 / Address: 0xFC		System Control 3 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	LVD_INT_EN	LVD_SEL[1:0]		LVD_EN	LVR_SEL[1:0]		LVR_EN
Default	0	0	1	0	0	1	0	1
Key Code	0x8F, 0x32, 0x50							

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	LVD_INT_EN	R/W	LVD interrupt enable 0 : disable 1 : enable	
5:4	LVD_SEL[1:0]	R/W	LVD voltage selection bits LVD_SEL[1:0] / Voltage 00 / 3.4V 01 / 4.4V 10 / 2.1V 11 / 2.6V	

Bit	Function	Type	Description	Condition
3	LVD_EN	R/W	LVD enable control 0: disable LVD function 1: enable LVD function	
2:1	LVR_SEL[1:0]	R/W	LVR voltage selection bits LVR_SEL[1:0] / Voltage 00 / 3.2V 01 / 4.2V 10 / 1.9V 11 / 2.4V	
0	LVR_EN	R/W	LVR enable control 0: disable LVD function 1: enable LVD function	

Table 5-57 SYS_CTRL3 register

SYS_CTRL4			Page : 0 / Address: 0xFD		System Control 4 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	WDOG_RST	SW_RST_EN	LVR_RST	LVD_INTF	LVD_STS	ADDR_ERR	ERR_WR
Default	0	0	0	0	0	0	0	0
Key Code	0x8F, 0x32, 0x50							

Bit	Function	Type	Description	Condition
7	--	R	Reserved	
6	WDOG_RST	R/W	Watch dog reset indicated flag read: 0 : Watch dog reset is inactive 1 : Watch dog reset is active Write: 0 : clear this bit 1 : no effect	
5	SW_RST_EN	R/W	Software reset enable signal 0 : disable software reset 1 : enable software reset	
4	LVR_RST	R/W	LVR indicated flag read: 0 : LVR is inactive 1 : LVR is active Write: 0 : clear this bit 1 : no effect	
3	LVD_INTF	R/W	LVD interrupt flag read: 0 : LVD is inactive 1 : LVD is active Write: 0 : clear this bit 1 : no effect	

Bit	Function	Type	Description	Condition
2	LVD_STS	R	LVD status flag. 0 : LVD is inactive 1 : LVD is active	
1	ADDR_ERR	R/W	Flash access address over range flag. read: 0 : flash access address is not over range 1 : flash access address is over range Write: 0 : clear this bit 1 : no effect	
1	ERR_WR	R/W	Flash is illegal programming or erasing flag. This flag will be set to high when a programming or erasing is out-of space or among lock_level range. read: 0 : legal programming or erasing 1 : illegal programming or erasing Write: 0 : clear this bit 1 : no effect	

Table 5-58 SYS_CTRL4 register

EXT_INT_EN			Page : 0 / Address : 0xE5		External Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	DEBOUNCE_TIME[1 :0]		EXT_INT5_EN	EXT_INT4_EN	EXT_INT3_EN	EXT_INT2_EN	EXT_INT1_EN	EXT_INT0_EN
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:6	DEBOUNCE_TIME	R/W	External interrupt de-bounce time select signal DEBOUNCE_TIME[1 :0] / Clock Cycle 00 / 4 01 / 37 10 / 72 11 / 142	
5	EXT_INT5_EN	R/W	Comparator down side interrupt enable signal. That is triggered by comparator down side output. 0 : disable 1 : enable	
4	EXT_INT4_EN	R/W	Comparator up side interrupt enable signal. That is triggered by comparator up side output. 0 : disable 1 : enable	
3	EXT_INT3_EN	R/W	External interrupt 3 enable signal that is mapped to P2_2. 0 : disable 1 : enable	

Bit	Function	Type	Description	Condition
2	EXT_INT2_EN	R/W	External interrupt 2 enable signal that is mapped to P1_7. 0 : disable 1 : enable	
1	EXT_INT1_EN	R/W	External interrupt 1 enable signal that is mapped to P1_6. 0 : disable 1 : enable	
0	EXT_INT0_EN	R/W	External interrupt 0 enable signal that is mapped to P1_5. 0 : disable 1 : enable	

Table 5-59 The EXT_INT_EN register

EXT_INT_EDGE			Page : 0 / Address : 0xE6		External Interrupt Edge Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	EXT_INT5_EDGE	EXT_INT4_EDGE	EXT_INT3_EDGE	EXT_INT2_EDGE	EXT_INT1_EDGE	EXT_INT0_EDGE
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	EXT_INT5_EDGE	R/W	External interrupt 5 trigger edge control signal 0 : falling edge 1 : rising edge	
4	EXT_INT4_EDGE	R/W	External interrupt 4 trigger edge control signal 0 : falling edge 1 : rising edge	
3	EXT_INT3_EDGE	R/W	External interrupt 3 trigger edge control signal 0 : falling edge 1 : rising edge	
2	EXT_INT2_EDGE	R/W	External interrupt 2 trigger edge control signal 0 : falling edge 1 : rising edge	
1	EXT_INT1_EDGE	R/W	External interrupt 1 trigger edge control signal 0 : falling edge 1 : rising edge	
0	EXT_INT0_EDGE	R/W	External interrupt 0 trigger edge control signal 0 : falling edge 1 : rising edge	

Table 5-60 The EXT_INT_EDGE register

EXT_INT_STS			Address : 0xE7		External Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	EXT_INT5_STS	EXT_INT4_STS	EXT_INT3_STS	EXT_INT2_STS	EXT_INT1_STS	EXT_INT0_STS
Default	0	0	0	0	0	0	0	0
Key Code								

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	EXT_INT5_STS	R/W	Comparator down side interrupt status flag. read: 0 : comparator down side interrupt is not occurred 1 : comparator down side interrupt is occurred write: 0 : clear this bit 1 : on effect	
4	EXT_INT4_STS	R/W	Comparator up side interrupt status flag. read: 0 : comparator up side interrupt is not occurred 1 : comparator up side interrupt is occurred write: 0 : clear this bit 1 : on effect	
3	EXT_INT3_STS	R/W	External interrupt 3 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clear this bit 1 : on effect	
2	EXT_INT2_STS	R/W	External interrupt 2 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clear this bit 1 : on effect	
1	EXT_INT1_STS	R/W	External interrupt 1 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clear this bit 1 : on effect	
0	EXT_INT0_STS	R/W	External interrupt 0 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clear this bit 1 : on effect	

Table 5-61 The EXT_INT_STS register

5.7. Reset Sources

5.7.1. Introduction

There are six types of reset sources for the GPM8F3132C family including Power-On Reset (POR), Low Voltage Reset (LVR), Pad Reset (RAD_RST), Watchdog Timer Reset (WDT_RST), Software Reset (S/W_RST) and Flash Error Reset (ADDR_ERR_RST). Figure 5.7-1 shows the block diagram of each reset source.

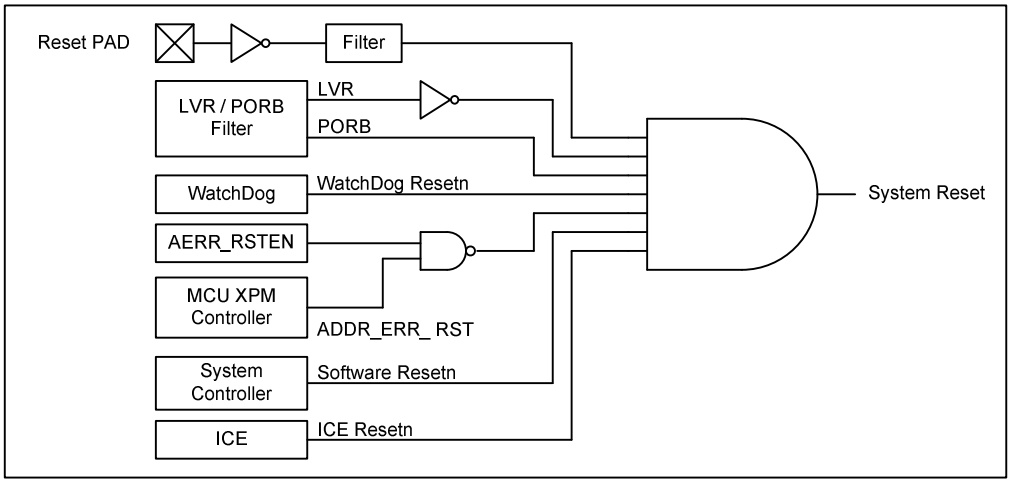


Figure 5.7-1 Reset sources

5.7.2. Power-On Reset (POR)

A POR is generated when VDD is rising from 0v. When VDD rises to an acceptable level (~1.5V), the power on reset circuit will starts a power-on sequence. After that, the system starts to activate and will operate in target speed. The POR will reset whole chip and registers.

5.7.3. Low Voltage Reset / Low Voltage Detect (LVR/LVD)

The on-chip Low Voltage Reset (LVR) circuitry forces the system entering reset state when power supplying voltage falls below the specific LVR trigger voltage. This function prevents MCU from working at an invalid operating voltage range.

To enable or disable this function, SYS_CTRL3[0] can be set. If this function is enabled, the LVR circuit will monitor power level while chip is operating. And the LVR voltage level can be 1.9V, 2.4V, 3.2V or 4.2V by setting SYS_CTRL3[2:1]. If the power is lower than the specific level for a specific period, the system reset will take place and go to initial state.

In order to allow software to early notify that a power failure is about to occur, the LVD flag bit can be monitored. Built-in voltage detection circuit controls the LVD flag. The LVD flag is set while VDD supply is below LVD voltage and is cleared when the VDD supply is over LVD voltage. The LVD voltage can be 2.1V, 2.6V, 3.4V or 4.4V by setting SYS_CTRL3[5:4] bits.

5.7.4. Pad Reset (PAD_RST)

The GPM8F3132C provides an external pin to force the system returning to its initial status. The RESET pin is high active as shown in Figure 5.7-2 When the RESET pin equals to VDD over 120us, system will be forced to enter reset state, execute instruction from address 0x0000 and all registers go to default state.

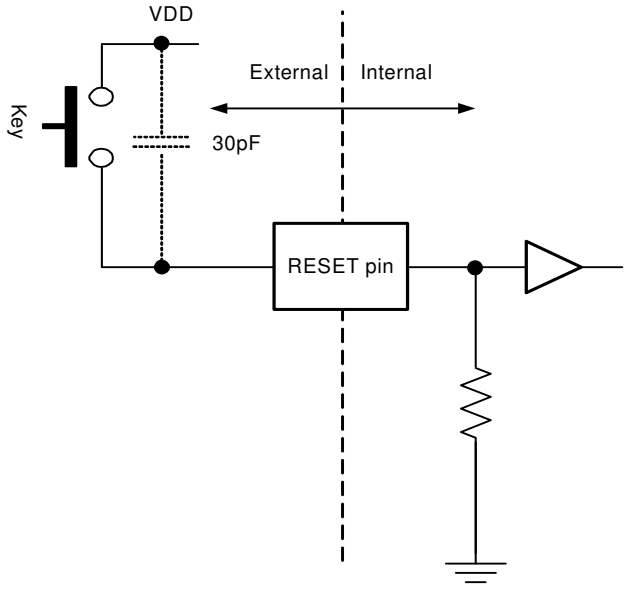


Figure 5.7-2 Pad reset circuit

5.7.5. Watchdog Timer Reset (WDT_RST)

On-chip watchdog circuitry makes the device entering reset state

when MCU goes into unknown state and has no watchdog cleared information. This function prevents the MCU to be stuck in an abnormal condition. The WDT can be enabled or disabled through WDCON register bit 1. At any time prior to reaching its user selected terminal value, software can set the Reset Watchdog Timer (WDCON[0]) bit. If RWT is set before the timeout is reached, the timer will start over. If timeout is reached without RWT being set, the watchdog will reset the CPU. Hardware will automatically clear RWT after software sets it. When the reset occurs, the Watchdog Timer Reset Flag (SYSCON_CTRL4[6]) will automatically be set to indicate the cause of the reset, however software must clear this bit manually.

WDCON register is a timed access register that prevent it from accidental writes. KEYCODE is located at 0xEB. Correct sequence, 0xAA and 0x55, is required before write to WDCON register. Reading from such register is not protected.

The Watchdog has four timeout selections based on the internal 32K clock frequency. The selections are a pre-selected number of clocks and can be set by CKCON[7:6]. In addition, CKCON[5] can be used to set these four timeout selections in fast mode or not. Figure 5.7-3 shows the block diagram of Watchdog timer.

5.7.6. Other Reset Sources

Other reset sources includes Software Reset and Flash Address Error Reset. Software Reset is occurred when writing KEY code to KEYCODE register(0xEB). The key codes are 0x8F, 0x32 and 0x50. The timing does not matter, but the key codes must be written in order before SW reset is take place. Flash Address Error Reset is the reset when flash access addresses is out of flash space and AERR_RSTEN(SYS_CTRL6[2]) is set to 1.

In GPM8F3132C, system supports four reset status flag can be monitored by SYS_CTRL4 register which is shown as Table **5-67**

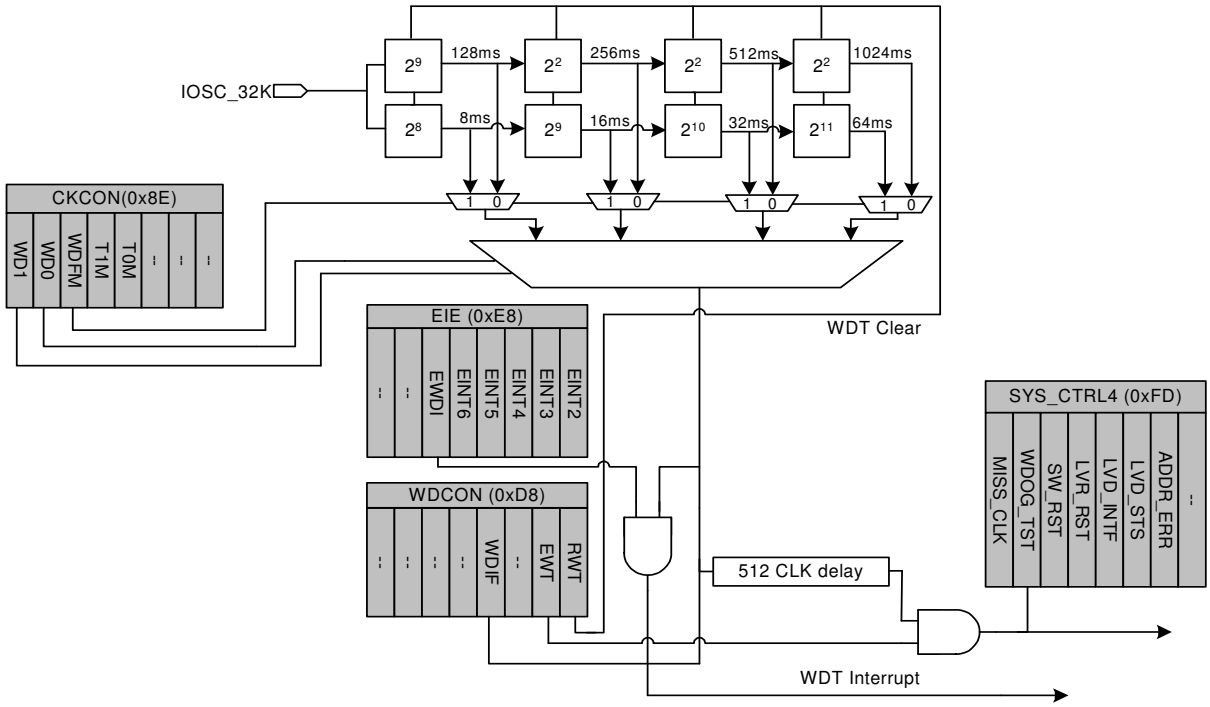


Figure 5.7-3 The block diagram of Watchdog timer

SYS_CTRL3			Page : 0 / Address: 0xFC		System Control 3 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	LVD_INT_EN	LVD_SEL[1:0]		LVD_EN	LVR_SEL[1:0]		LVR_EN
Default	0	0	1	0	0	1	0	1
Key Code	0x8F, 0x32, 0x50							

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	LVD_INT_EN	R/W	LVD interrupt enable	

Bit	Function	Type	Description	Condition
			0 : disable 1 : enable	
5:4	LVD_SEL[1:0]	R/W	LVD voltage selection bits LVD_SEL[1:0] / Voltage 00 / 3.4V 01 / 4.4V 10 / 2.1V 11 / 2.6V	
3	LVD_EN	R/W	LVD enable control 0: disable LVD function 1: enable LVD function	
2:1	LVR_SEL[1:0]	R/W	LVR voltage selection bits LVR_SEL[1:0] / Voltage 00 / 3.2V 01 / 4.2V 10 / 1.9V 11 / 2.4V	
0	LVR_EN	R/W	LVR enable control 0: disable LVD function 1: enable LVD function	

Table 5-62 SYS_CTRL3 register

WDCON			Address: 0xD8		Watchdog Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	WDIF	--	EWT	RWT
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3	WDIF	R/W	Watchdog interrupt flag	
2	--	R/W	Reserved	
1	EWT	R/W	Watchdog timer reset enable bit 0: Disable 1: Enable	
0	RWT	R/W	Reset watchdog timer 0: NA 1: Reset	

Table 5-63 WDCON register

KEYCODE			Address: 0xEB		KEYCODE Register			
Bit	7	6	5	4	3	2	1	0
Function	KC7	KC6	KC5	KC4	KC3	KC2	KC1	KC0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	KEYCODE[7:0]	R/W	KEYCODE register	

Note 1: Some protected registers are needed to write correct key code to KEYCODE register before write data to them.

Note 2: User must turn-off global interrupt enable before using KEYCODE function.

Table 5-64 KEYCODE register

CKCON			Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	WDFM	T1M	T0M	--	--	--
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:6	WD[1:0]	R/W	Watchdog timeout selection bits If WDFM=0: WD[1:0] / Timeout 00 / 128ms 01 / 256ms 10 / 512ms 11 / 1024ms If WDFM=1: WD[1:0] / Timeout 00 / 8ms 01 / 16ms 10 / 32ms 11 / 64ms	
5	WDFM	R/W	Watchdog fast mode selection bit 0: watchdog fast mode is disabled 1: watchdog fast mode is enabled	
4	T1M	R/W	Timer 1 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF). T1M / T01_CK_SEL / Timer1 Clock 0 / 0 / System Clock / 8 0 / 1 / System Clock / 2 1 / 0 / System Clock / 4 1 / 1 / System Clock / 1	
3	T0M	R/W	Timer 0 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF). T0M / T01_CK_SEL / Timer0 Clock 0 / 0 / System Clock / 8 0 / 1 / System Clock / 2 1 / 0 / System Clock / 4 1 / 1 / System Clock / 1	
2:0	--	R/W	Reserved	

Table 5-65 CKCON register

SYS_CTRL6	Address : 0xFF	System Control-6 Register

Bit	7	6	5	4	3	2	1	0
Function	--	--	UART_IF_EN	T01_CK_SEL	--	AERR_RSTEN	WDOG_CKEN	--
Default	1	1	0	0	0	0	1	0
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	UART_IF_EN	R/W	UART interface enable signal. 0 : disable 1 : enable	
4	T01_CK_SEL	R/W	Timer0/1 clock source select signal.This bit is used combining with T0M/T1M of CKCON(0x8E). T0M /T1M | T01_CK_SEL | Timer0/1 Clock 0 | 0 | System Clock / 8 0 | 1 | System Clock / 2 1 | 0 | System Clock / 4 1 | 1 | System Clock / 1	
3	--	R/W	Reserved	
2	AERR_RSTEN	R/W	Flash address over range reset enable 0 : disable 1 : enable	
1	WDOG_CKEN	R/W	Watch dog controller clock enable control bit 0 : disable 1 : enable	
0	--	R/W	Reserved	

Table 5-66 The SYS_CTRL6 register

SYS_CTRL4			**Page : 0 / Address: 0xFD**		**System Control 4 Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	WDOG_RST	SW_RST_EN	LVR_RST	LVD_INTF	LVD_STS	ADDR_ERR	ERR_WR
Default	0	0	0	0	0	0	0	0
Key Code	0x8F, 0x32, 0x50							

Bit	Function	Type	Description	Condition
7	--	R	Reserved	
6	WDOG_RST	R/W	Watch dog reset indicated flag read: 0 : Watch dog reset is inactive 1 : Watch dog reset is active Write: 0 : clear this bit 1 : no effect	
5	SW_RST_EN	R/W	Software reset enable signal 0 : disable software reset 1 : enable software reset	
4	LVR_RST	R/W	LVR indicated flag	

Bit	Function	Type	Description	Condition
			read: 0 : LVR is inactive 1 : LVR is active Write: 0 : clear this bit 1 : no effect	
3	LVD_INTF	R/W	LVD interrupt flag read: 0 : LVD is inactive 1 : LVD is active Write: 0 : clear this bit 1 : no effect	
2	LVD_STS	R	LVD status flag. 0 : LVD is inactive 1 : LVD is active	
1	ADDR_ERR	R/W	Flash access address over range flag. read: 0 : flash access address is not over range 1 : flash access address is over range Write: 0 : clear this bit 1 : no effect	
1	ERR_WR	R/W	Flash is illegal programming or erasing flag. This flag will be set to high when a programming or erasing is out-of space or among lock_level range. read: 0 : legal programming or erasing 1 : illegal programming or erasing Write: 0 : clear this bit 1 : no effect	

Table 5-67 SYS_CTRL4 register

5.8. I/O Ports

5.8.1. Introduction

The GPM8F3132C family has five I/O ports, including standard Port 0, Port 1, Port 2, Port 3 and additional Port 4. These port pins may be multiplexed with an alternate function for the peripheral features on the device. In general, when an initial reset state occurs, all ports are used as a general purpose input floating port with Schmitt trigger function. All the input ports can be programmable pull high/low by DIR, ATT and Px registers. The P0, P0_ID, P0_DIR nd P0_ATT registers of Port 0 are controlled by 0x80, 0xA9 and SFRs 0xAA, 0xAB registers of page-0. The P1, P1_ID, P1_DIR and P1_ATT registers of Port 1 are controlled by 0x90, 0xB9 and SFRs 0xBA, 0xBB registers of page-0. The P2, P2_ID, P2_DIR and P2_ATT registers of Port 2 are controlled by 0xA0, 0xA1 and SFRs 0xA2, 0xA3 registers of page-0. The P3, P3_ID, P3_DIR and P3_ATT registers of Port 3 are controlled by 0xB0, 0xB1 and SFRs 0xB2, 0xB3 registers of page-0. The P4, P4_ID, P4_DIR and P4_ATT registers of Port 4 are controlled by 0xC0, 0xC1 and SFRs 0xC2, 0xC3 registers of page-1. The writing output data to the I/O port are performed via their corresponding SFRs P0(0x80), P1(0x90), P2(0xA0), P3(0xB0) and P4(0xC0). The reading data from the I/O port are performed via their corresponding SFRs P0_ID(0xA9), P1(0xB9), P2(0xA1), P3(0xB1) and P4(0xC1). Table 5-68 shows the truth table of analog pad and digital pad respectively. In GPM8F3132C, all of the GPIO port can be program to analog pad for special function. The detail descriptions of analog function are in corresponding sections. The built-in pull high/low resister is 50KΩ. In addition to, there is a register for slew rate control (Px_SR) of each port. The default state of Px_SR register is '0x00' without slew rate control function. **錯誤! 找不到參照來源。**Figure 5.8-1 show the block diagrams of the general purpose I/O.

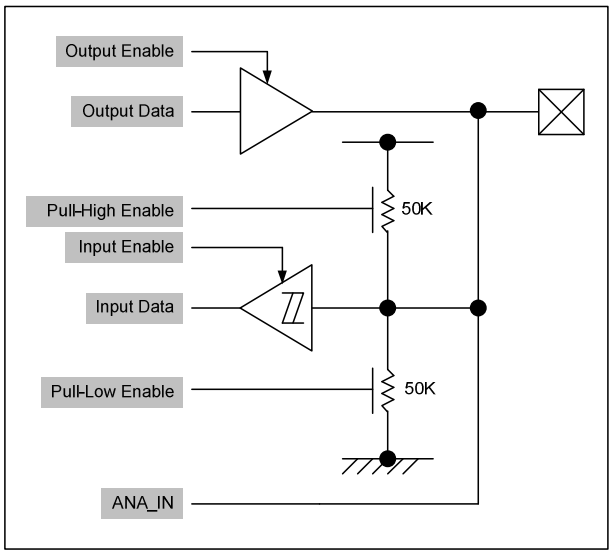


Figure 5.8-1 The block diagram of GPIO

DIR	ATT	Px	Function	Description
0	0	0	Floating	Float (High Impendence)
0	0	1	Floating	Float (High Impendence)
0	1	0	Pull Low*	Input with pull low
0	1	1	Pull High	Input with pull high
1	0	0	Output High	Output with buffer (inverted -content of buffer register)
1	0	1	Output Low	Output with buffer (inverted -content of buffer register)
1	1	0	Output Low	Output with buffer
1	1	1	Output High	Output with buffer

Table 5-68 The truth table of GPIO

P0			Address: 0x80		Port0 Register			
Bit	7	6	5	4	3	2	1	0
Function	P07	P06	P05	P04	P03	P02	P01	P00
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P0[7:0]	R/W	P0 is used to set IO output data only. Otherwise, that also can be used to configure the Port0 function.	

Table 5-69 P0 register

P1			Address: 0x90		Port1 Register			
Bit	7	6	5	4	3	2	1	0
Function	P17	P16	P15	P14	P13	P12	P11	P10
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P1[7:0]	R/W	P1 is used to set IO output data only. Otherwise, that also can be used to configure the Port1 function.	

Table 5-70 P1 register

P2			Address: 0xA0		Port2 Register			
Bit	7	6	5	4	3	2	1	0
Function	P27	P26	P25	P24	P23	P22	P21	P20
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P2[7:0]	R/W	P2 is used to set IO output data only. Otherwise, that also can be used to configure the Port2 function.	

Table 5-71 P2 register

P3			Address: 0xB0		Port3 Register			
Bit	7	6	5	4	3	2	1	0
Function	P37	P36	P35	P34	P33	P32	P31	P30
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P3[7:0]	R/W	P3 is used to set IO output data only. Otherwise, that also can be used to configure the Port3 function.	

Table 5-72 P3 register

P4			Address: 0xC0		Port4 Register			
Bit	7	6	5	4	3	2	1	0
Function	MDU_INTF	--	--	--	--	P42	P41	P40
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Function	Type	Description	Condition
7	MDU_INTF	R	MDU interrupts flag. 0 : idle / busy 1 : MDU interrupt trigger	

Bit	Function	Type	Description	Condition
6:3	--	R/W	Reserved	
2:0	P4[2:0]	R/W	P4 is used to set IO output data only. Otherwise, that also can be used to configure the Port4 function.	

Table 5-73 P4 register

P0_ID			Address: 0xA9		Port0 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_ID[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_ID[7:0]	R/W	P0_ID is used to read-back I/O input state only.	

Table 5-74 P0_ID register

P1_ID			Address: 0xB9		Port1 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_ID[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P1_ID[7:0]	R/W	P1_ID is used to read-back I/O input state only.	

Table 5-75 P1_ID register

P2_ID			Address: 0xA1		Port2 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_ID[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_ID[7:0]	R/W	P2_ID is used to read-back I/O input state only.	

Table 5-76 P2_ID register

P3_ID			Address: 0xB1		Port3 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	P3_ID[3:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P3_ID[7:0]	R/W	P3_ID is used to read-back I/O input state only.	

Table 5-77 P3_ID register

P4_ID			Address: 0xC1		Port4 Input Data Register			
Bit	7	6	5	4	3	2	1	0

Function	--	--	--	--	--	P4_ID[2]	P4_ID[1]	P4_ID[0]
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2:0	P4_ID[2:0]	R/W	P4_ID is used to read-back I/O input state only.	

Table 5-78 P4_ID register

P0_DIR			Page : 0 / Address: 0xAA		Port0 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_DIR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_DIR[7:0]	R/W	P0_DIR is use to configure the Port0 function. That indicates direction of corresponding I/O.	

Table 5-79 P0_DIR register

P1_DIR			Page : 0 / Address: 0xBA		Port1 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_DIR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P1_DIR[7:0]	R/W	P1_DIR is use to configure the Port1 function. That indicates direction of corresponding I/O.	

Table 5-80 P1_DIR register

P2_DIR			Page : 0 / Address: 0xA2		Port2 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_DIR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_DIR[7:0]	R/W	P2_DIR is use to configure the Port2 function. That indicates direction of corresponding I/O.	

Table 5-81 P2_DIR register

P3_DIR			Page : 0 / Address: 0xB2		Port3 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P3_DIR[3:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition

Bit	Function	Type	Description	Condition
7:0	P3_DIR[7:0]	R/W	P3_DIR is use to configure the Port3 function. That indicates direction of corresponding I/O.	

Table 5-82 P3_DIR register

P4_DIR			Page : 1 / Address: 0xC2		Port4 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	P4_DIR[2:0]		
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2:0	P4_DIR[2:0]	R/W	P4_DIR is use to configure the Port4 function. That indicates direction of corresponding I/O.	

Table 5-83 P4_DIR register

P0_ATT			Page : 0 / Address: 0xAB		Port0 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_ATT[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_ATT[7:0]	R/W	P0_ATT can use to configure the Port0 function.	

Table 5-84 P0_ATT register

P1_ATT			Page : 0 / Address: 0xBB		Port1 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_DIR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P1_ATT[7:0]	R/W	P1_ATT can use to configure the Port1 function.	

Table 5-85 P1_ATT register

P2_ATT			Page : 0 / Address: 0xA3		Port2 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_ATT[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_ATT[7:0]	R/W	P2_ATT can use to configure the Port2 function.	

Table 5-86 P2_ATT register

P3_ATT	Page : 0 / Address: 0xB3	Port3 Attribute Register

Bit	7	6	5	4	3	2	1	0
Function	P3_ATT[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P3_ATT[7:0]	R/W	P3_ATT can use to configure the Port3 function.	

Table 5-87 P3_ATT register

P4_ATT			Page : 1 / Address: 0xC3		Port4 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	P4_ATT[2:0]		
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2:0	P4_ATT[2:0]	R/W	P4_ATT can use to configure the Port4 function.	

Table 5-88 P4_ATT register

P0_SR			Page : 0 / Address: 0xAD		Port0 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_SR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_SR[7:0]	R/W	P0_SR can use to configure the Port0 output slew rate,	

Table 5-89 P0_SR register

P1_SR			Page : 0 / Address: 0xBD		Port1 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_SR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P1_SR[7:0]	R/W	P1_SR can use to configure the Port1 output slew rate,	

Table 5-90 P1_SR register

P2_SR			Page : 0 / Address: 0xA5		Port2 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_SR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_SR[7:0]	R/W	P2_SR can use to configure the Port2 output slew rate,	

Table 5-91 P2_SR register

P3_SR			Page : 0 / Address: 0xB5		Port3 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P3_SR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P3_SR[7:0]	R/W	P3_SR can use to configure the Port3 output slew rate,	

Table 5-92 P3_SR register

P4_SR			Page : 1 / Address: 0xC5		Port4 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	P4_SR [2:0]		
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2:0	P4_SR [2:0]	R/W	P4_SR can use to configure the Port4 output slew rate,	

Table 5-93 P4_SR register

5.9. Timer Module

5.9.1. Introduction

GPM8F3132C family is equipped with five timers. They are Timer 0, Timer 1, Timer A, Timer B and Timer C respectively. In addition, Timer A, Timer B also features Compare/Capture/PWM function.

Timer C features Capture function. The Timer 0 and Timer 1 are up-count timers with 16-bit resolution. The Timer A, Timer B, Timer C are down-count timers and with 16-bit resolution. Each timer's function is described in the following sections.

5.9.2. Timer 0/1

Timer 0 and Timer 1 are fully compatible with the standard 8051 timers. Each timer consists of two 8-bit registers TH0(0x8C), TL0(0x8A), TH1(0x8D), TL1(0x8B). Timer 0 and Timer 1 work in the same three modes except for mode 3 and the related control registers are TMOD(0x89), TCON(0x88) and CKCON(0x8E) registers. In the timer mode, timer registers are incremented every 1/2/4/8 SYSCLK periods depends on CKCON(0x8E) and SYS_CTRL6(0xFF) setting, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on theirs corresponding input pins: T0 or T1. The input pins are sampled every CLK period.

TH0			Address: 0x8C		Timer0 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH0[7:0]	R/W	Timer 0 Load value – high byte	

Table 5-94 TH0 register

TL0			Address: 0x8A		Timer0 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL0[7:0]	R/W	Timer 0 Load value – low byte	

Table 5-95 TL0 register

TH1			Address: 0x8D		Timer1 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH1[7:0]	R/W	Timer 1 Load value – high byte	

Table 5-96 TH1 register

TL1			Address: 0x8B		Timer1 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL1[7:0]	R/W	Timer 1 Load value – low byte	

Table 5-97 TL1 register

TMOD			Address: 0x89		Timer0/1 Control Mode Register			
Bit	7	6	5	4	3	2	1	0
Function	--	CT1	M11	M10	--	CT0	M01	M00
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	CT1	R/W	Counter or timer select bit 0: Timer mode, internally clocked 1: Counter mode, Timer 1 clock source is from T1 pin	
5:4	M1[1:0]	R/W	Mode select bits of timer 1, which is tabled as **錯誤! 找不到參照來源。**99.	
3	--	R/W	Reserved	
2	CT0	R/W	Counter or timer select bit 0: Timer mode, internally clocked 1: Counter mode, Timer 0 clock source is from IOSC 32K	
1:0	M0[1:0]	R/W	Mode select bits of timer 0, which is tabled as **錯誤! 找不到參照來源。**99.	

Table 5-98 TMOD register

M1	M0	Mode	Function description
0	0	0	TH0/1 operates as 8-bit timer/counter with a divide by 32 pre-scaler served by lower 5-bit of TL0/1.
0	1	1	16-bit timer/counter. TH0/1 and TL0/1 are cascaded
1	0	2	TL0/1 operates as 8-bit timer/counter with 8-bit auto-reload by TH0/1
1	1	3	TL0 is configured as 8-bit timer/counter controlled by the standard Timer 0 bits. TH0 is an 8-bit timer controlled by the Timer 1 controls bits. Timer 1 holds its count.

Table 5-99 Four modes of Timer 0 and Timer 1

TCON			Address: 0x88		Timer0/1 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TF1	R/W	Timer 1 interrupt (overflow) flag	
6	TR1	R/W	Timer 1 run control bit 0: disabled ; 1: enabled	
5	TF0	R/W	Timer 0 interrupt (overflow) flag	
4	TR0	R/W	Timer 0 run control bit 0: disabled ; 1: enabled	
3	IE1	R/W	ADC0/1 interrupt flag	
2	IT1	R/W	ADC0/1 level (at 0) / edge (at 1) sensitivity	
1	IE0	R/W	Timer A interrupt flag	
0	IT0	R/W	Timer A level (at 0) / edge (at 1) sensitivity	

Table 5-100 TCON register

CKCON			Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	WDFM	T1M	T0M	--	--	--
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:6	WD[1:0]	R/W	Watchdog timeout selection bits If WDFM=0: WD[1:0] / Timeout 00 / 128ms 01 / 256ms 10 / 512ms 11 / 1024ms If WDFM=1: WD[1:0] / Timeout 00 / 8ms 01 / 16ms	

Bit	Function	Type	Description	Condition
			10 32ms 11 64ms	
5	WDFM	R/W	Watchdog fast mode selection bit 0: watchdog fast mode is disabled 1: watchdog fast mode is enabled	
4	T1M	R/W	Timer 1 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF). T1M / T01_CK_SEL / Timer1 Clock 0 / 0 / System Clock / 8 0 / 1 / System Clock / 2 1 / 0 / System Clock / 4 1 / 1 / System Clock / 1	
3	T0M	R/W	Timer 0 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF). T0M / T01_CK_SEL / Timer0 Clock 0 / 0 / System Clock / 8 0 / 1 / System Clock / 2 1 / 0 / System Clock / 4 1 / 1 / System Clock / 1	
2:0	--	R/W	Reserved	

Table 5-101 CKCON register

SYS_CTRL6	Address : 0xFF				System Control-6 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	UART_IF_EN	T01_CK_SEL	--	AERR_RSTEN	WDOG_CKEN	--
Default	1	1	0	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	UART_IF_EN	R/W	UART interface enable signal. 0 : disable 1 : enable	
4	T01_CK_SEL	R/W	Timer0/1 clock source select signal.This bit is used combining with T0M/T1M of CKCON(0x8E). T0M /T1M / T01_CK_SEL / Timer0/1 Clock 0 / 0 / System Clock / 8 0 / 1 / System Clock / 2 1 / 0 / System Clock / 4 1 / 1 / System Clock / 1	
3	--	R/W	Reserved	
2	AERR_RSTEN	R/W	Flash address over range reset enable 0 : disable 1 : enable	

Bit	Function	Type	Description	Condition
1	WDOG_CKEN	R/W	Watch dog controller clock enable control bit 0 : disable 1 : enable	
0	--	R/W	Reserved	

Table 5-102 The SYS_CTRL6 register

5.9.2.1. Timer 0: Mode 0 (13-Bit Timer/Counter)

In this mode, Timer 0 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer 0 interrupt flag TF0 is set. The counted input is enabled to the Timer 0 when TR0(TCON[4]) = 1 and the input source is 32KHz clock. The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Figure 5.9-1 shows the block diagram of Timer 0 for Mode 0. In addition, before assign the timer clock as system clock / 256. User must open one of these functions first, they contain TimerA enable / TimeA PWM enable / TimerB enable / TimerB PWM enable / TimerC enable

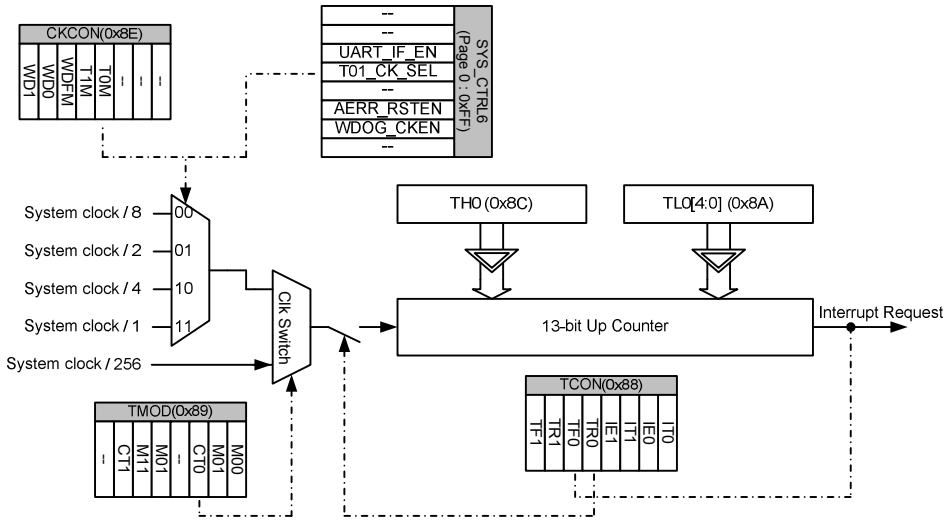


Figure 5.9-1The block diagram of Timer 0 for Mode 0

5.9.2.2. Timer 0: Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. The block diagram of Mode 1 is shown in Figure 5.9-2

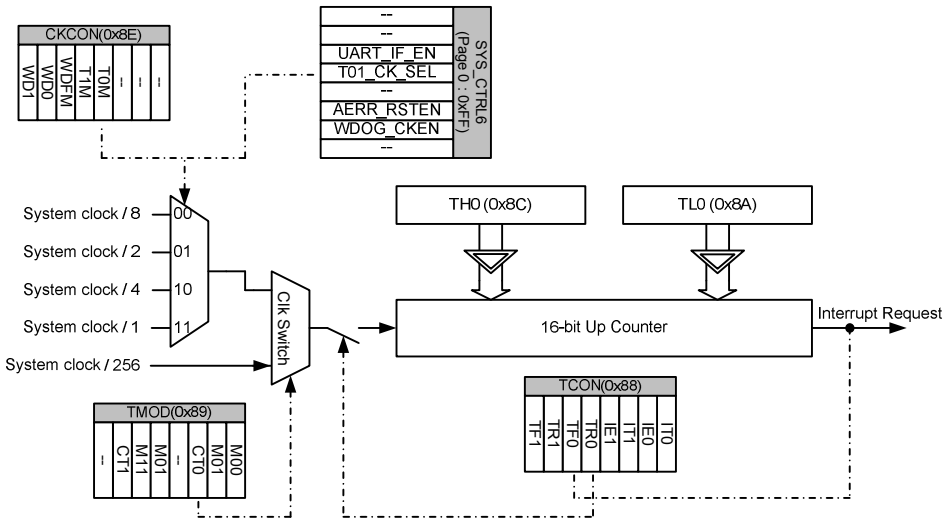


Figure 5.9-2 The block diagram of Timer 0 for Mode 1

5.9.2.3. Timer 0: Mode 2 (8-bit Timer/Counter with Auto-reload Function)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reloads, as shown in Figure 5.9-3 . Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is loaded by software. The reload leaves TH0 unchanged.

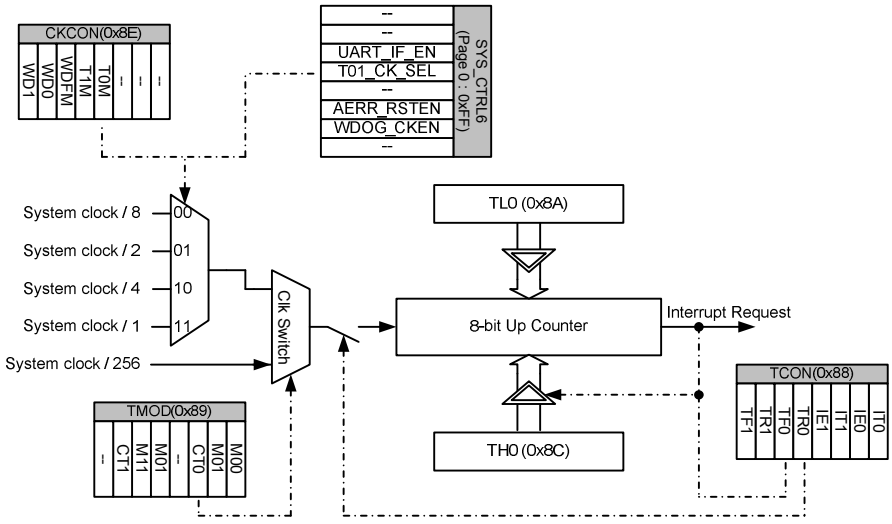


Figure 5.9-3 The block diagram of Timer 0 for Mode 2

5.9.2.4. Timer 0: Mode 3 (Two 8-Bit Timers/Counters)

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The block diagram for Mode 3 on Timer 0 is shown in Figure 5.9-4. TL0 uses the Timer 0 control bits: CT0, GATE0, TR0, and TF0. TH0 is locked into a timer function and uses the TR1 and TF1 flags from Timer 1 and controls Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer/counter. When Timer 0 is in Mode 3, Timer 1 can be turned off by switching it into its own Mode 3, or can still be used by the serial channel as a baud rate generator, or in any application where interrupt from Timer 1 is not required.

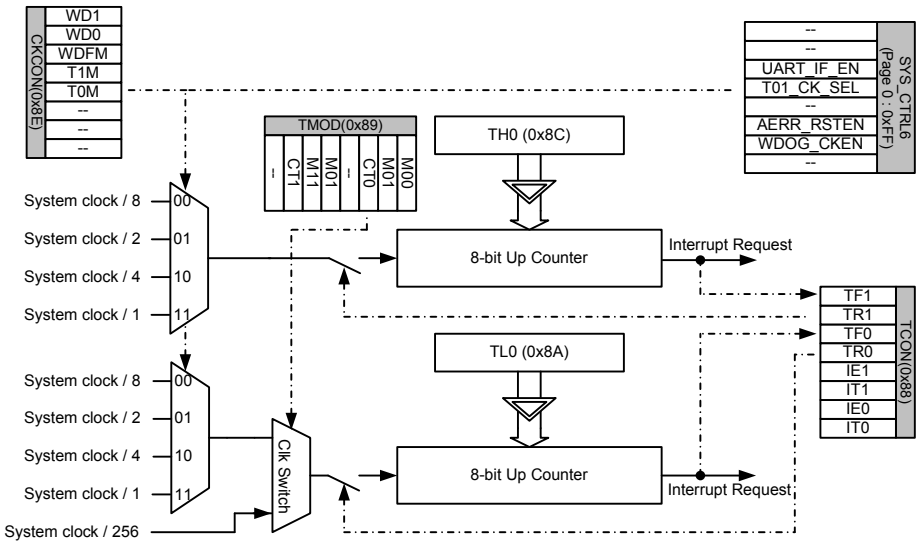


Figure 5.9-4 The block diagram of Timer 0 for Mode 3

5.9.2.5. Timer 1: Mode 0 (13-Bit Timer/Counter)

In this mode, the Timer 1 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer 1 interrupt flag TF1 is set. The counted input is enabled to the Timer1 when TR1(TCON[6]) = 1 and the input source is 32KHz clock. The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Figure 5.9-5 shows the block diagram of Timer1 for Mode 0.

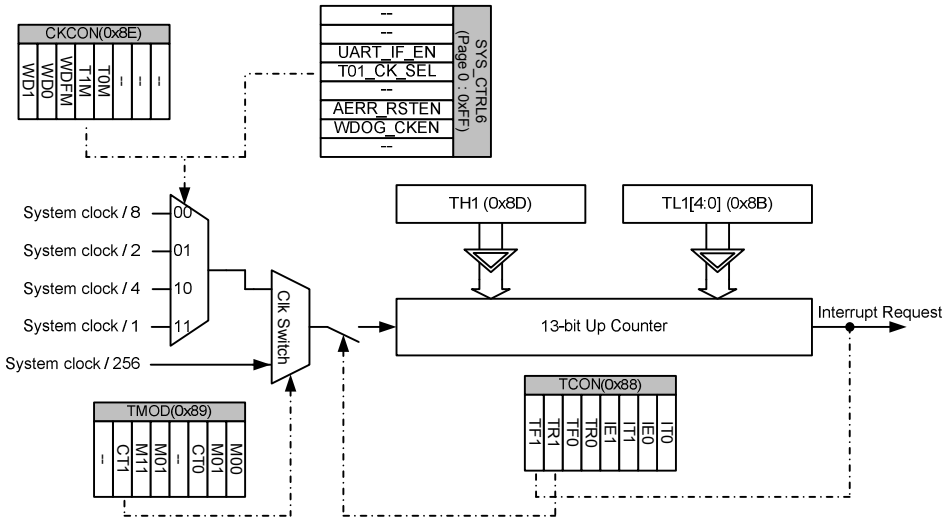


Figure 5.9-5 The block diagram of Timer 1 for Mode 0

5.9.2.6. Timer 1: Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. The block diagram of Mode 1 is shown in Figure 5.9-6.

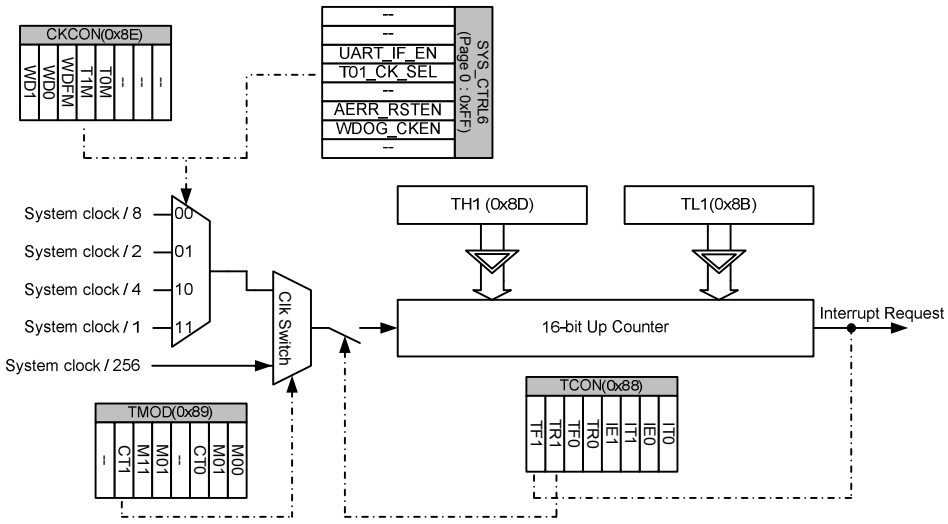


Figure 5.9-6 The block diagram of Timer 1 for Mode 1

5.9.2.7. Timer 1: Mode 2 (8-Bit Timer/Counter with Auto-reload Function)

Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic reloads, as shown in Figure 5.9-7. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is loaded by software. The reload leaves TH1 unchanged.

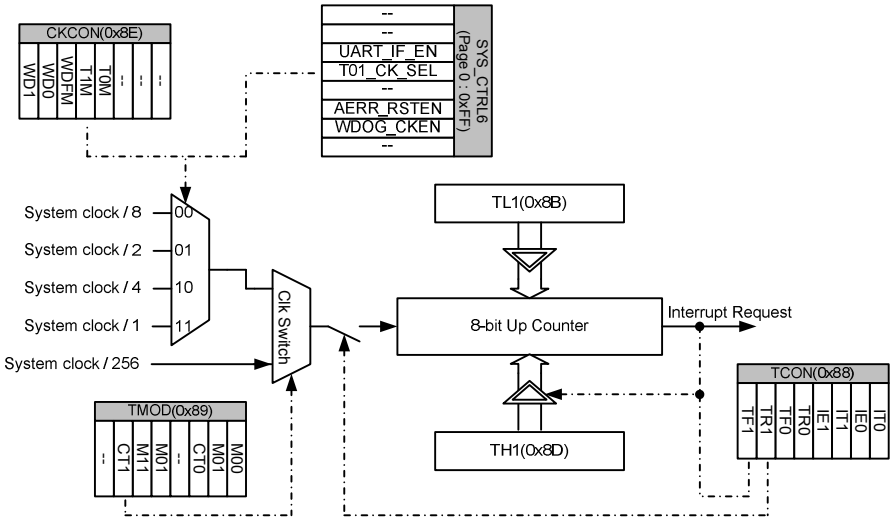


Figure 5.9-7 The block diagram of Timer 1 for Mode 2

5.9.2.8. Timer 1: Mode 3

Timer 1 in Mode 3 is has no timer function. The effect is the same as setting TR1=0.

5.9.3. Timer A

The Timer A, which is a 16-bit-wide register, can operate as timer. The additional Counter/Capture/PWM feature is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc.

5.9.3.1. Timer / Counter mode

In timer / counter function, that have up to 8 clock source can be selected. Thus, the 16-bit timer register is decremented in every clock periods. The Figure 5.9-8 shows the block diagram of counter / timer function for Timer A. When Timer A rolls over from pre-load data (TMA_PLOAD_H/L) to 0, not only TMA_INTF is set but also Timer A registers is loaded with the 16-bit value from TMA_PLOAD_H/L register. Required TMA_PLOAD_H/L value can be preset by software.

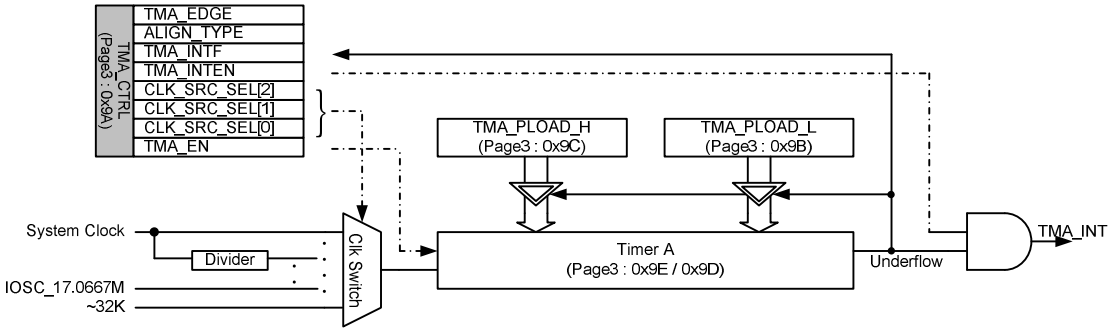


Figure 5.9-8 The block diagram of counter / timer function for Timer A

5.9.3.2. Capture functions

Each of capture registers can be used to latch the current 16-bit value of the Timer A registers (TMA_H and TMA_L) when an external event is triggered.

Figure 5.9-9 shows functional diagrams of the Timer A capture function.

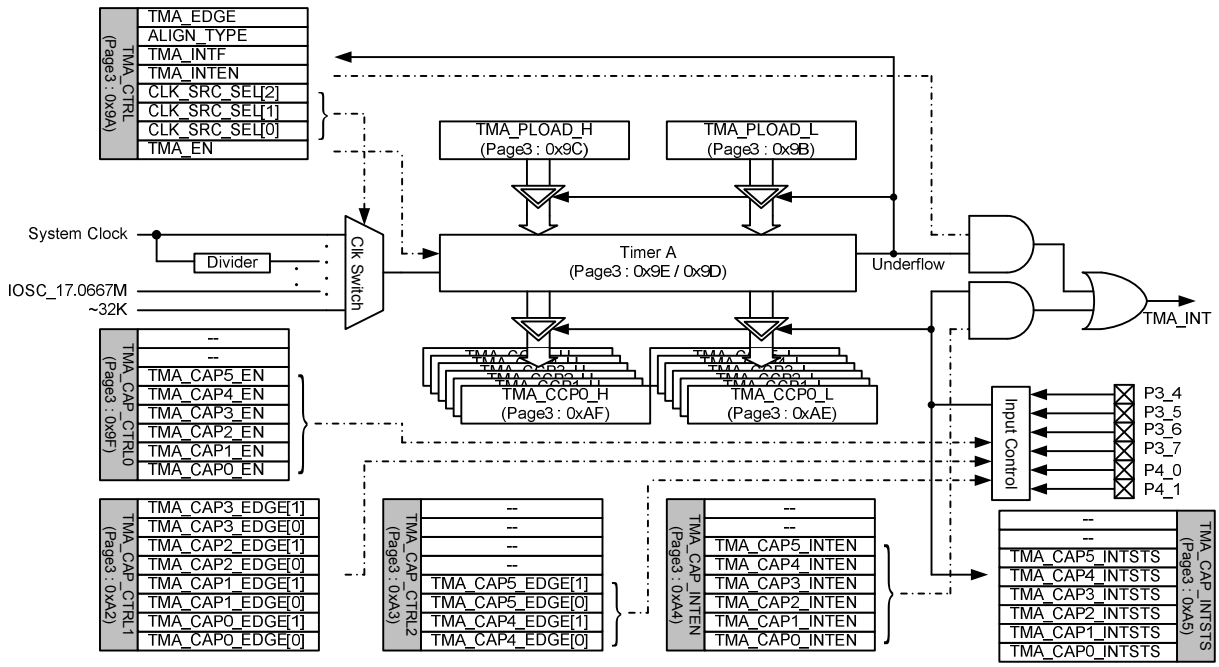


Figure 5.9-9 The block diagram of Timer A capture mode

5.9.3.3. PWM functions

The Timer A consists of 6 sets PWM function. When the TMA_PWMx_EN is enabled, the PWM output will toggle at the TMA_H/L are lesser or greater than TMA_CCPx_H/L (TMA_END_HL) value. About Timer count policy, there are two options can be choice between edge and center alignment. In edge alignment, the counter decrease counter value per clock cycle. Hardware will auto re-load TMA_PLOAD_H/L value to counter when counter is underflow. In center alignment, the counter is executing down count first and executing up-count next.

There are two output mode of PWM output pin: independent and complement mode. In each mode, user can change output polarity with TMA_PWM_CTRL2 randomly. **錯誤! 找不到參照來源。**Figure 5.9-10 shows functional diagrams of the Timer A PWM function, Figure 5.9-11 to Figure 5.9-17 are shows PWM operating waveform.

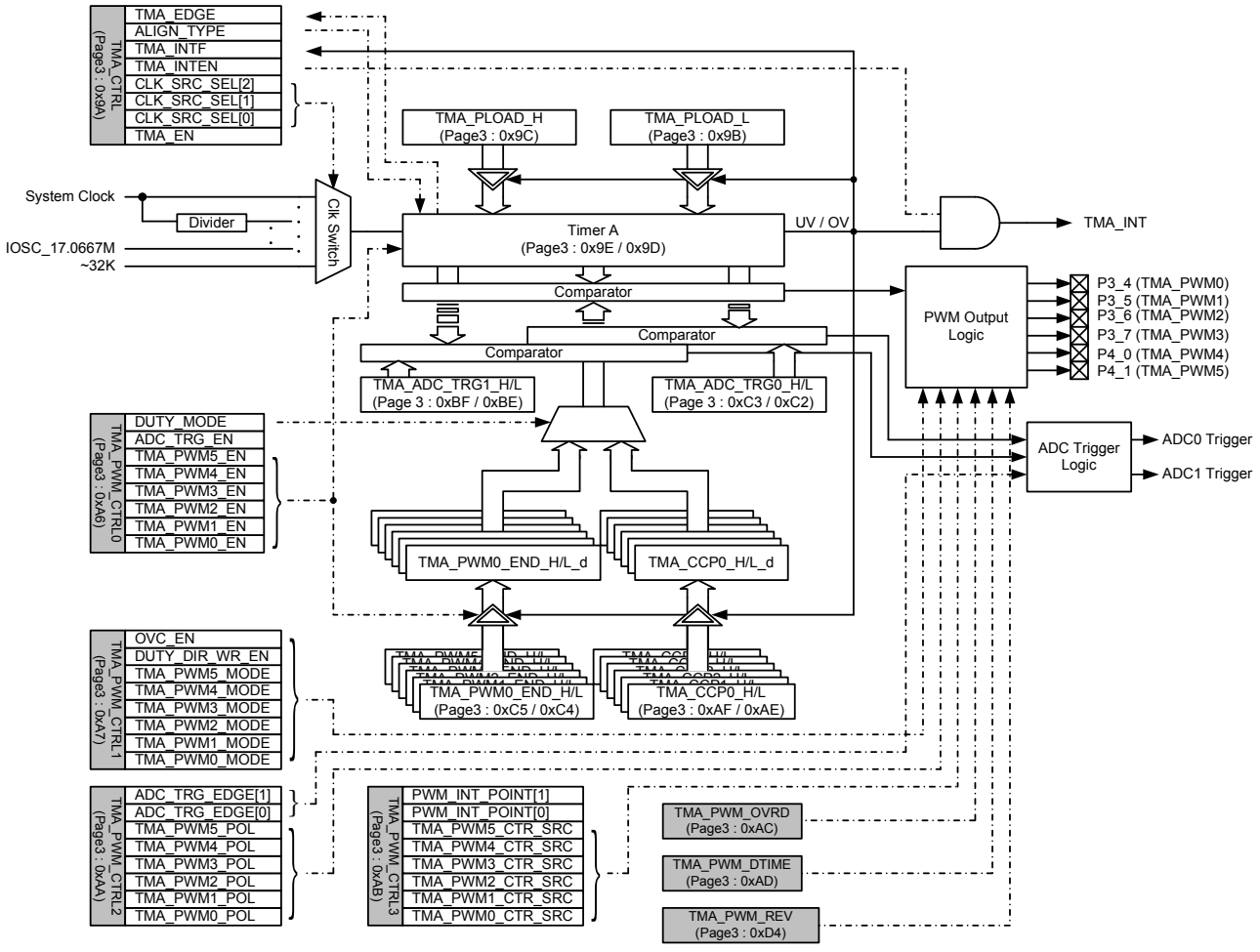


Figure 5.9-10 The block diagram of Timer A PWM mode

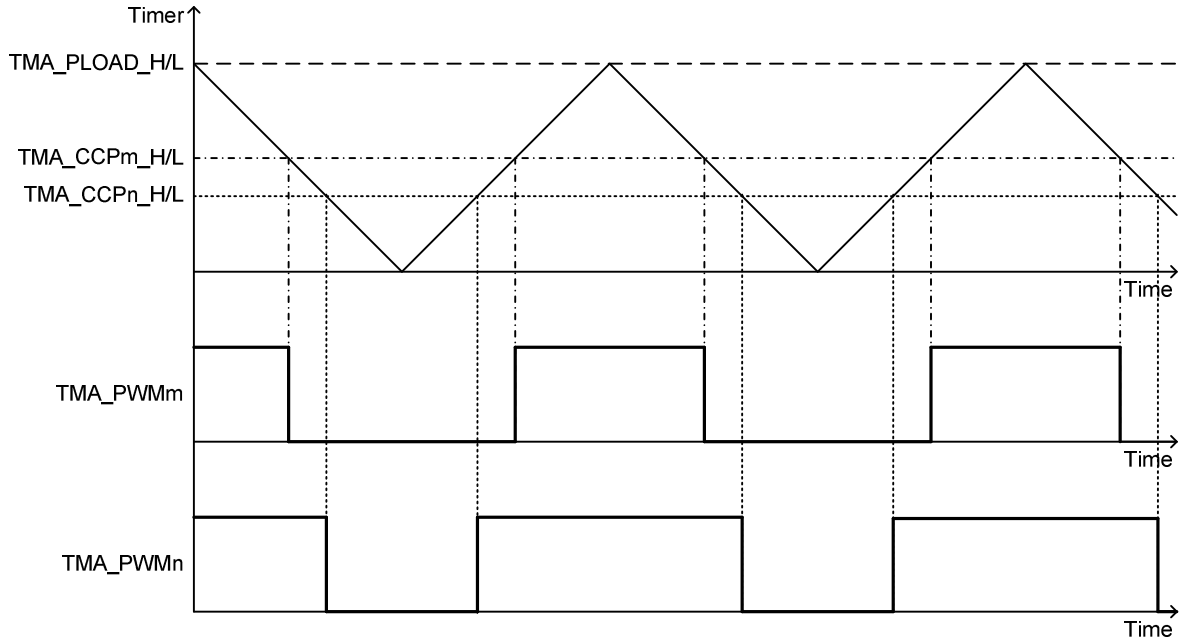


Figure 5.9-11The waveform of Timer A PWM w/o dead time (ALIGN_TYPE : 1 / DUTY_MODE : 0 / TMA_PWMx_MODE : 0)

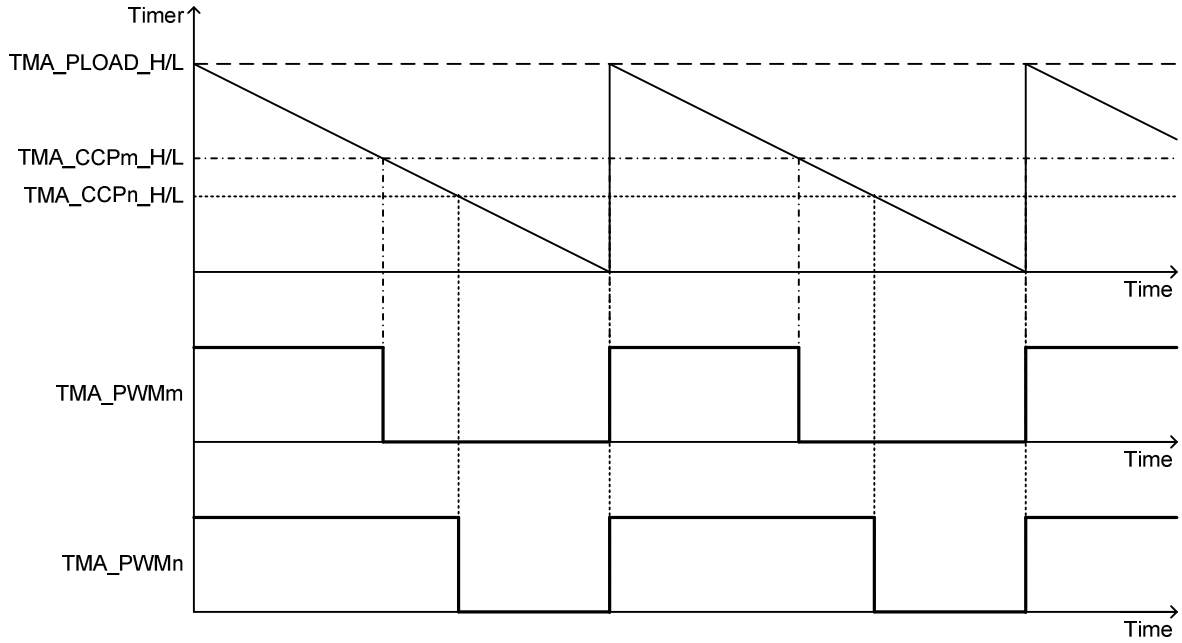


Figure 5.9-12 The waveform of Timer A PWM w/o dead time (ALIGN_TYPE : 0 / DUTY_MODE : 0 / TMA_PWMx_MODE : 0)

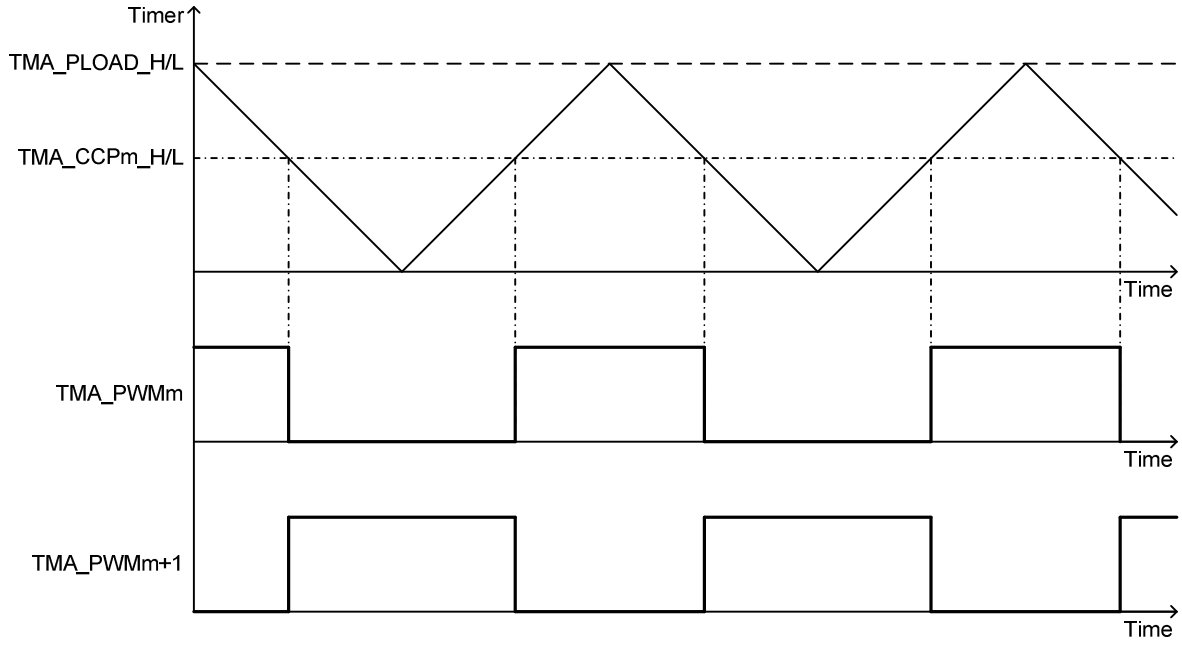


Figure 5.9-13The waveform of Timer A PWM w/o dead time (ALIGN_TYPE : 1 / DUTY_MODE : 0 / TMA_PWMx_MODE : 1)

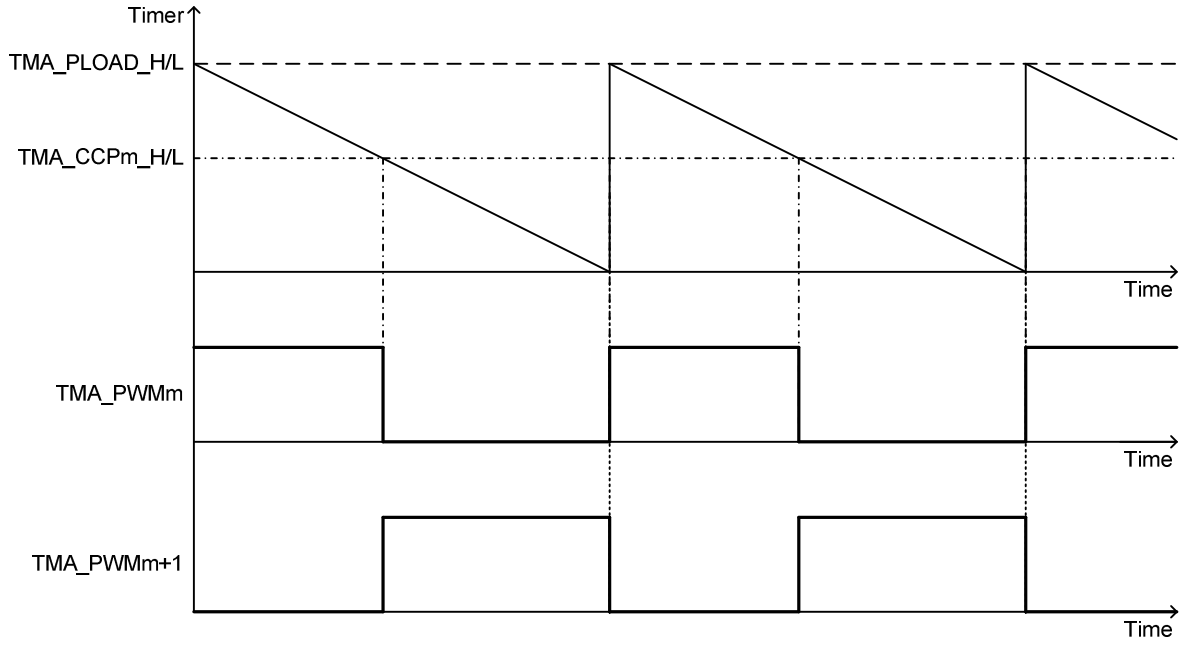


Figure 5.9-14 The waveform of Timer A PWM w/o dead time(ALIGN_TYPE : 0 / DUTY_MODE : 0 / TMA_PWMx_MODE : 1)

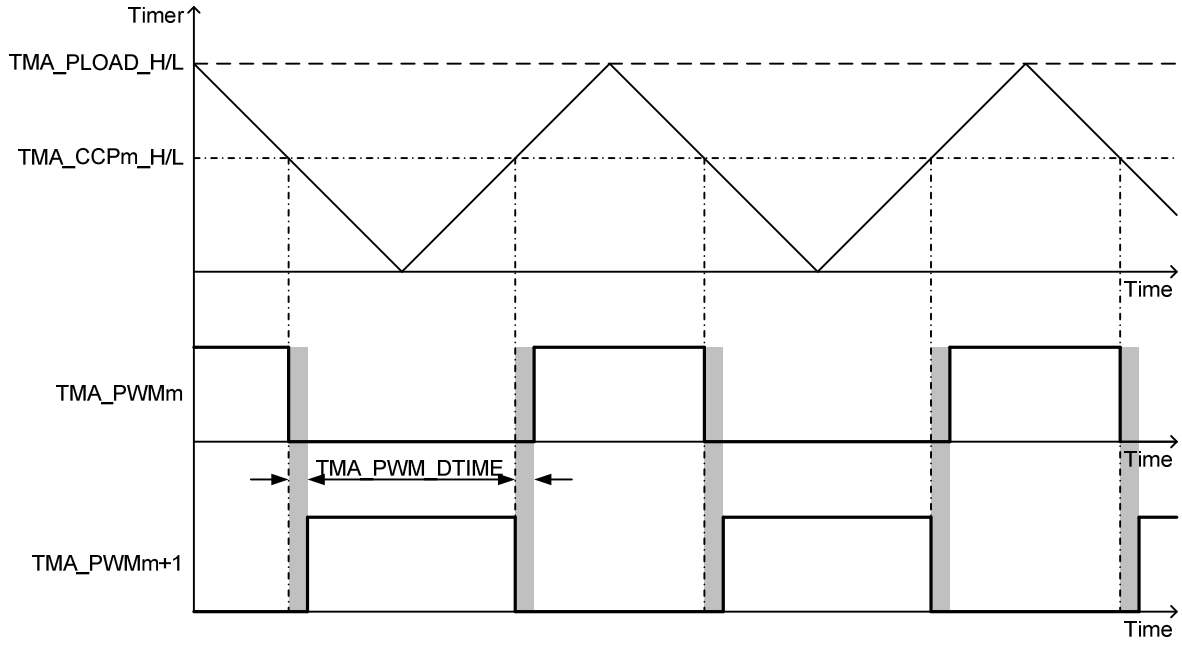


Figure 5.9-15 The waveform of Timer A PWM w/i dead time (ALIGN_TYPE : 1 / DUTY_MODE : 0 / TMA_PWMx_MODE : 1)

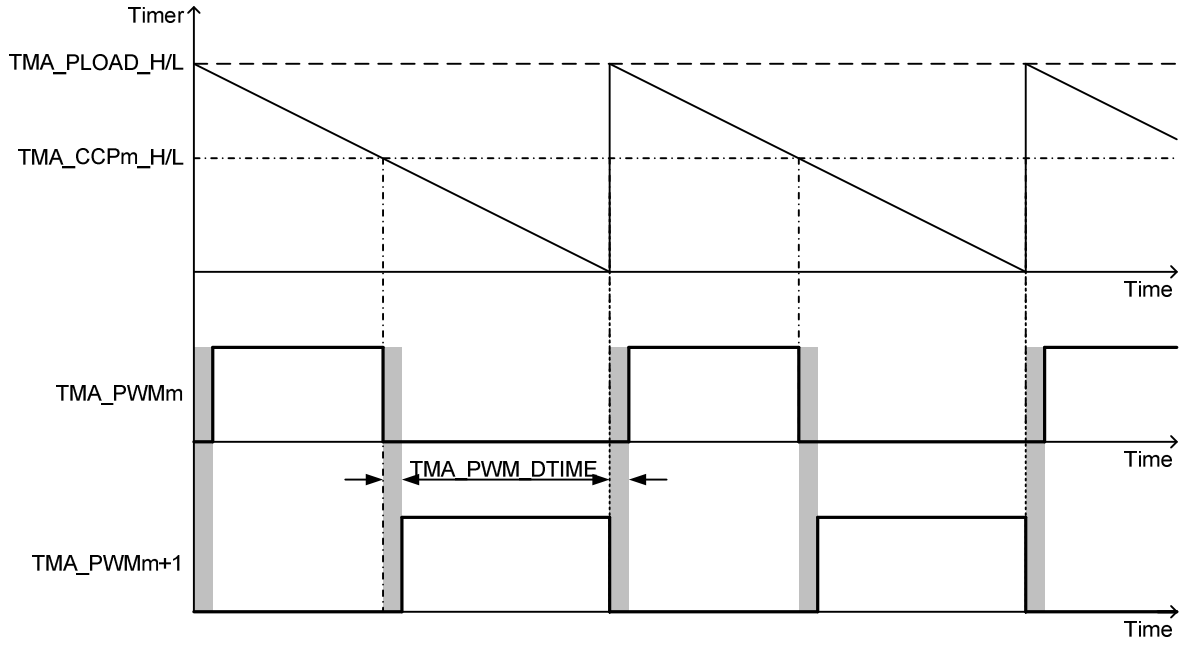


Figure 5.9-16 The waveform of Timer A PWM w/i dead time (ALIGN_TYPE : 0 / DUTY_MODE : 0 / TMA_PWMx_MODE : 1)

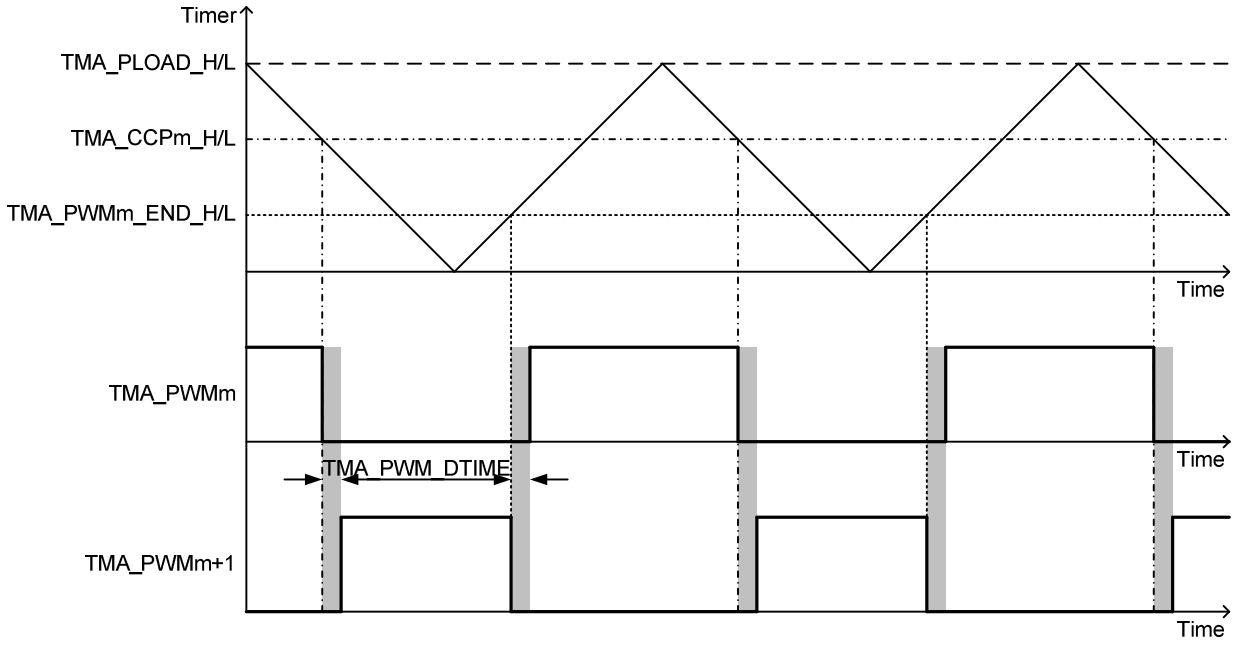


Figure 5.9-17 The waveform of Timer A PWM w/i dead time (ALIGN_TYPE : 1 / DUTY_MODE : 1 / TMA_PWMx_MODE : 1)

GPM8F3132C / GPM8F3132C-QV043 supports a function that provides user to change PWM polarity without turn-off PWM. User can realize this function by setting TMA_PWM_REV register to 1. And return to the original function by setting this bit to 0. A rule must be followed that is don't set TMA_PWM_REV to 1 before PWM enable. Figure 5.9-18 to Figure 5.9-21 is shows the operating waveform.

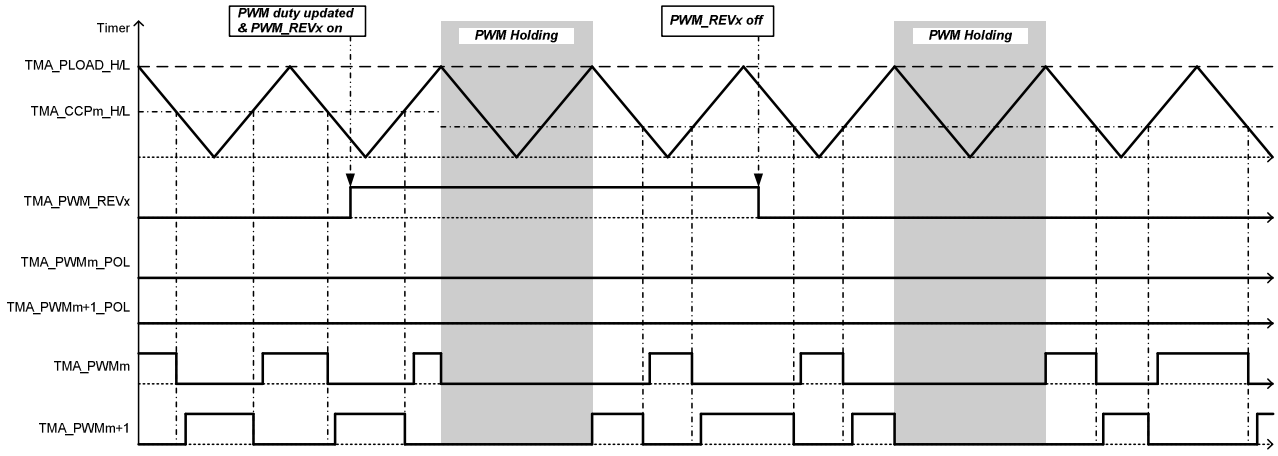


Figure 5.9-18 PWM change polarity with original polarity of PWMm / PWMm+1 is 0/0

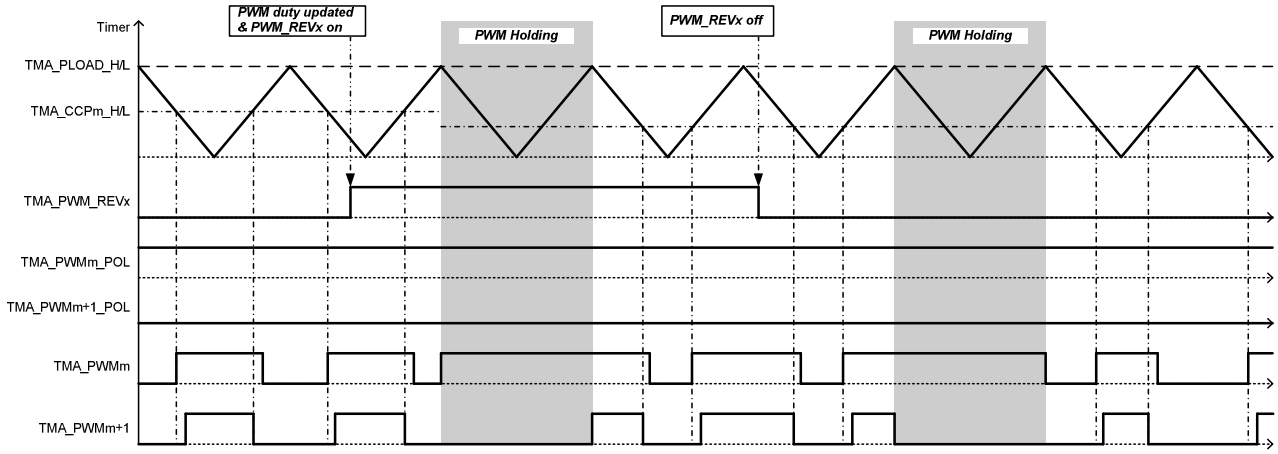


Figure 5.9-19 PWM change polarity with original polarity of PWMm / PWMm+1 is 0/1

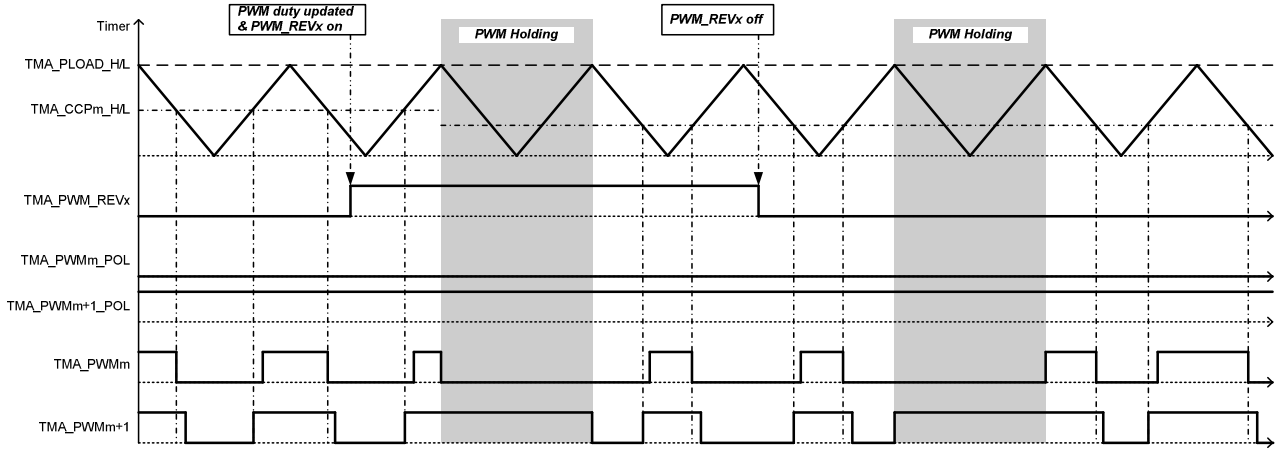


Figure 5.9-20 PWM change polarity with original polarity of PWMm / PWMm+1 is 1/0

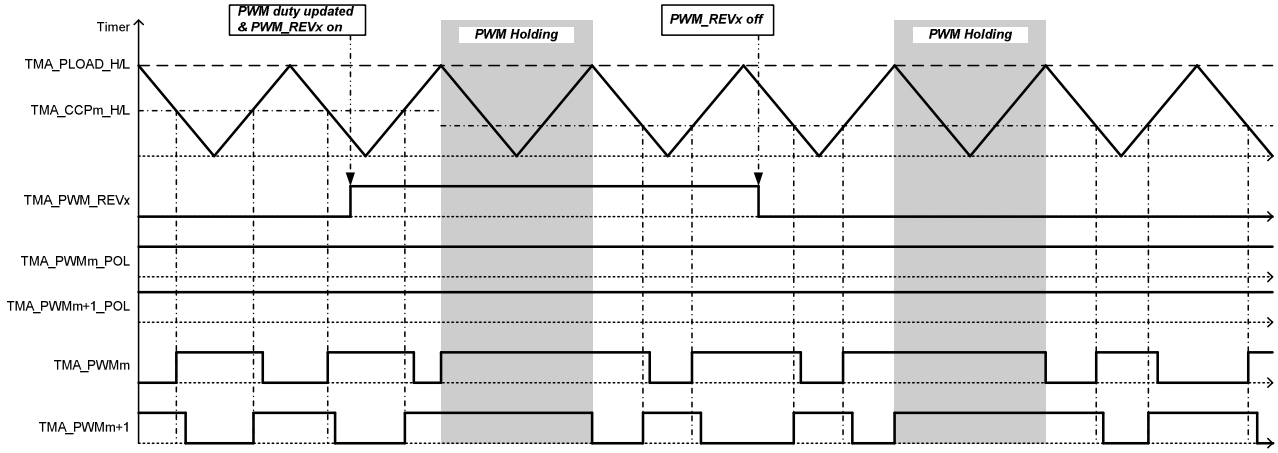


Figure 5.9-21 PWM change polarity with original polarity of PWMm / PWMm+1 is 1/1

5.9.3.4. Timer A Related Registers

TMA_CTRL			Page : 3 / Address: 0x9A		Timer A Control1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMA_EDGE	ALIGN_TYPE	TMA_INTF	TMA_INTEN	CLK_SRC_SEL[2:0]			TMA_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TMA_EDGE	R	Timer A up/down count edge indication. 0 : falling edge 1 : rising edge	
6	ALIGN_TYPE	R/W	0 : edge align 1 : center align	
5	TMA_INTF	R/W	Timer A interrupt flag. read : 0 : idle / busy 1 : timer A interrupt trigger write : 0 : clear this bit 1 : no effect	
4	TMA_INTEN	R/W	Timer A interrupt enable control bit 0 : disable 1 : enable	
3:1	CLK_SRC_SEL	R/W	Timer A input clock source selection control bit	
0	TMA_EN	R/W	Timer A enable control bit. 0 : disable 1 : enable	

CLK_SRC_SEL[2:0]	Clock Source
000	System clock
001	System clock / 2
010	System clock / 4
011	System clock / 8
100	System clock / 16
101	System clock / 32
110	IOSC_17.0667M
111	~32K (IOSC_32K)

Table 5-103 TMA_CTRL register

TMA_PLOAD_L			Page : 3 / Address: 0x9B		Timer A Pre-Load Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PLOAD_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PLOAD_L[7:0]	R/W	Timer A pre-load data or PWM period data register – low byte	

Table 5-104 TMA_PLOAD_L register

TMA_PLOAD_H			Page : 3 / Address: 0x9C		Timer A Pre-Load Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PLOAD_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PLOAD_H[7:0]	R/W	Timer A pre-load data or PWM period data register – high byte	

Table 5-105 TMA_PLOAD_H register

TMA_L			Page : 3 / Address: 0x9D		Timer A Counter Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_L[7:0]	R/W	Timer A counter register – low byte	

Table 5-106 TMA_L register

TMA_H			Page : 3 / Address: 0x9E		Timer A Counter Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_H[7:0]	R/W	Timer A counter register – high byte	

Table 5-107 TMA_H register

TMA_CAP_CTRL0			Page : 3 / Address: 0x9F		Timer A Capture Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMA_CAPx_EN[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
1:0	TMA_CAPx_EN[5:0]	R/W	Timer A capture mode enable control bit. All of the trigger source are from external I/O. Following table is the trigger source mapping table. TMA_CAPx_EN / Mapping I/O TMA_CAP0_EN / P3[4] TMA_CAP1_EN / P3[5] TMA_CAP2_EN / P3[6] TMA_CAP3_EN / P3[7] TMA_CAP4_EN / P4[0] TMA_CAP5_EN / P4[1] 0 : disable 1 : enable	

Table 5-108 TMA_CAP_CTRL0 register

TMA_CAP_CTRL1			Page : 3 / Address: 0xA2		Timer A Capture Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CAP3_EDGE[1:0]		TMA_CAP2_EDGE[1:0]		TMA_CAP1_EDGE[1:0]		TMA_CAP0_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	TMA_CAP3_EDGE[7:6]	R/W	Timer A capture 3 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	
5:4	TMA_CAP2_EDGE[5:4]	R/W	Timer A capture 2 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	
3:2	TMA_CAP1_EDGE[3:2]	R/W	Timer A capture 1 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	
1:0	TMA_CAP0_EDGE[1:0]	R/W	Timer A capture 0 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	

Table 5-109 TMA_CAP_CTRL1 register

TMA_CAP_CTRL2			Page : 3 / Address: 0xA2		Timer A Capture Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMA_CAP5_EDGE[1:0]		TMA_CAP4_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:2	TMA_CAP5_EDGE[3:2]	R/W	Timer A capture 5 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	
1:0	TMA_CAP4_EDGE[1:0]	R/W	Timer A capture 4 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	

Table 5-110 TMA_CAP_CTRL2 register

TMA_CAP_INTEN			Page : 3 / Address: 0xA4		Timer A Capture Mode Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMA_CAPx_INTEN[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
1:0	TMA_CAPx_INTEN[5:0]	R/W	Timer A capture mode interrupt enable control bits. These are map to CAP0 ~ CAP5 respectively. 0 : disable 1 : enable	

Table 5-111 TMA_CAP_INTEN register

TMA_CAP_INTSTS			Page : 3 / Address: 0xA5		Timer A Capture Mode Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMA_CAPx_INTSTS[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
1:0	TMA_CAPx_INTSTS[5:0]	R/W	Timer A capture mode interrupt status register. These are map to CAP0 ~ CAP5 respectively. read : 0 : no capture triggered 1 : capture triggered write : 0 : clear this bit 1 : no effect	

Table 5-112 TMA_CAP_INTSTS register

TMA_PWM_CTRL0			Page : 3 / Address: 0xA6		Timer A PWM Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	DUTY_MODE	ADC_TRG_EN	TMA_PWMx_EN					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	DUTY_MODE	R/W	Timer A PWM duty control selection bit. ***This bit is available when PWM operating in center align mode.*** 0 : PWM duty is controlled by TMA_CCPx_L / TMA_CCPx_H 1 : PWM duty is controlled by TMA_CCPx_L / TMA_CCPx_H / TMA_PWMx_L / TMA_PWMx_END_L / TMA_PWMx_END_H. In PWM rising edge , transition point is depended on TMA_CCPx_L / TMA_CCPx_H. Opposite, transition point is depended on TMA_PWMx_END_L / TMA_PWMx_END_H.	
6	ADC_TRG_EN	R/W	ADC trigger capture function enable control bit. 0 : disable 1 : enable	
[5:0]	TMA_PWMx_EN	R/W	Timer A PWM mode enable bits 0 : disable 1 : enable	

Table 5-113 TMA_PWM_CTRL0 register

TMA_PWM_CTRL1			Page : 3 / Address: 0xA7		Timer A PWM Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	OVC_EN	DUTY_DIR_WR_EN	--	TMA_PWM45_MODE	--	TMA_PWM23_MODE	--	TMA_PWM01_MODE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	OVC_EN	R/W	Over current break enable 0 : disable 1 : enable	
6	DUTY_DIR_WR_EN	R/W	PWM duty is updated immediately when CPU write data into PWM duty registers 0 : disable 1 : enable	
5	--	R/W	Reserved	
4	TMA_PWM45_MODE	R/W	Timer A PWM 4/5 operationg mode selection bit 0 : independent mode 1 : complementary mode	
3	--	R/W	Reserved	
2	TMA_PWM23_MODE	R/W	Timer A PWM 2/3 operationg mode selection bit 0 : independent mode 1 : complementary mode	
1	--	R/W	Reserved	
0	TMA_PWM01_MODE	R/W	Timer A PWM 0/1 operationg mode selection bit 0 : independent mode 1 : complementary mode	

Table 5-114 TMA_PWM_CTRL1 register

TMA_PWM_CTRL2			Page : 3 / Address: 0xAA		Timer A PWM Control 2 Register			
Bit	7	6	5	4	3	2	1	0
Function	ADC_TRG_EDGE[1:0]		TMA_PWMx_POL					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	ADC_TRG_EDGE	R/W	ADC trigger edge control bit. 00 : ADC is triggered at timer's falling edge 01 : ADC is triggered at timer's rising edge 1X : ADC is triggered at timer's both edge	
5	TMA_PWM5_POL	R/W	Timer A PWM5 polarity setting Independent mode: 0: PWM5 output low when PWM_cnt = TMA_CCP5 1: PWM5 output high when PWM_cnt = TMA_CCP5 Complementary mode: 0: PWM5 output high when PWM_cnt = TMA_CCP4 1: PWM5 output low when PWM_cnt = TMA_CCP4	
4	TMA_PWM4_POL	R/W	Timer A PWM4 polarity setting Independent mode:	

Bit	Function	Type	Description	Condition
			0: PWM4 output low when PWM_cnt = TMA_CCP4 1: PWM4 output high when PWM_cnt = TMA_CCP4 Complementary mode: 0: PWM4 output low when PWM_cnt = TMA_CCP4 1: PWM4 output high when PWM_cnt = TMA_CCP4	
3	TMA_PWM3_POL	R/W	Timer A PWM3 polarity setting Independent mode: 0: PWM3 output low when PWM_cnt = TMA_CCP3 1: PWM3 output high when PWM_cnt = TMA_CCP3 Complementary mode: 0: PWM3 output high when PWM_cnt = TMA_CCP2 1: PWM3 output low when PWM_cnt = TMA_CCP2	
2	TMA_PWM2_POL	R/W	Timer A PWM2 polarity setting Independent mode: 0: PWM2 output low when PWM_cnt = TMA_CCP2 1: PWM2 output high when PWM_cnt = TMA_CCP2 Complementary mode: 0: PWM2 output low when PWM_cnt = TMA_CCP2 1: PWM2 output high when PWM_cnt = TMA_CCP2	
1	TMA_PWM1_POL	R/W	Timer A PWM1 polarity setting Independent mode: 0: PWM1 output low when PWM_cnt = TMA_CCP1 1: PWM1 output high when PWM_cnt = TMA_CCP1 Complementary mode: 0: PWM1 output high when PWM_cnt = TMA_CCP0 1: PWM1 output low when PWM_cnt = TMA_CCP0	
0	TMA_PWM0_POL	R/W	Timer A PWM0 polarity setting Independent mode: 0: PWM0 output low when PWM_cnt = TMA_CCP0 1: PWM0 output high when PWM_cnt = TMA_CCP0 Complementary mode: 0: PWM0 output low when PWM_cnt = TMA_CCP0 1: PWM0 output high when PWM_cnt = TMA_CCP0	

Table 5-115 TMA_PWM_CTRL2 register

TMA_PWM_CTRL3			Page : 3 / Address: 0xAB		Timer A PWM Control 3 Register			
Bit	7	6	5	4	3	2	1	0
Function	PWM_INT_POINT		TMA_PWMx_SRC_CTR					
Default	0	0	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:6	PWM_INT_POINT	R/W	These bits are used to set PWM interrupt	

PWM_INT_POINT	Trigger Point (with center mode and PWM is enableed)
00	Interrupt is triggered when counter is under flow
01	Interrupt is triggered when counter is over flow
10	Interrupt is triggered when counter is under and over flow

Bit	Function	Type	Description	Condition
			11 No effect	
5:0	TMA_PWMx_CTR_SRC	R/W	PWM output source control bit 0: PWM output is depended on PWMOVRD register 1: PWM output is depended on PWM time base	

Table 5-116 TMA_PWM_CTRL3 register

TMA_PWM_OVRD			Page : 3 / Address: 0xAC		Timer A PWM Override Register			
Bit	7	6	5	4	3	2	1	0
Function	EINT_SEL		TMA_PWMx_OVRD[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	EINT_SEL	R/W	External interrupt select signal EINT_SEL[1 :0] / External Source / I/O Port 00 / Ext_IRQ0 / P15 01 / Ext_IRQ1 / P16 10 / Ext_IRQ2 / P17 11 / Ext_IRQ3 / P22	
5:0	TMA_PWMx_OVRD[5:0]	R/W	PWM override control data 0: PWM output is 0 1: PWM output is 1	

Table 5-117 TMA_PWM_OVRD register

TMA_PWM_DTIME			Page : 3 / Address: 0xAD		Timer A PWM Override Register			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM_DTIME[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM_DTIME[7:0]	R/W	Timer A PWM dead time register	

Table 5-118 TMA_PWM_DTIME register

TMA_CCP0_L			Page : 3 / Address: 0xAE		Timer A Counter / Capture / PWM 0 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP0_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP0_L[7:0]	R/W	Timer A Counter / Capture / PWM 0 register – low byte	

Table 5-119 TMA_CCP0_L register

TMA_CCP0_H			Page : 3 / Address: 0xAF		Timer A Counter / Capture / PWM 0 Register – high byte			
Bit	7	6	5	4	3	2	1	0

Function	TMA_CCP0_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP0_H[7:0]	R/W	Timer A Counter / Capture / PWM 0 register – high byte	

Table 5-120 TMA_CCP0_H register

TMA_CCP1_L			Page : 3 / Address: 0xB2		Timer A Counter / Capture / PWM 1 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP1_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP1_L[7:0]	R/W	Timer A Counter / Capture / PWM 1 register – low byte	

Table 5-121 TMA_CCP1_L register

TMA_CCP1_H			Page : 3 / Address: 0xB3		Timer A Counter / Capture / PWM 1 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP1_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP1_H[7:0]	R/W	Timer A Counter / Capture / PWM 1 register – high byte	

Table 5-122 TMA_CCP1_H register

TMA_CCP2_L			Page : 3 / Address: 0xB4		Timer A Counter / Capture / PWM 2 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP2_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP2_L[7:0]	R/W	Timer A Counter / Capture / PWM 2 register – low byte	

Table 5-123 TMA_CCP2_L register

TMA_CCP2_H			Page : 3 / Address: 0xB5		Timer A Counter / Capture / PWM 2 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP2_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP2_H[7:0]	R/W	Timer A Counter / Capture / PWM 2 register – high byte	

Table 5-124 TMA_CCP2_H register

TMA_CCP3_L			Page : 3 / Address: 0xB6		Timer A Counter / Capture / PWM 3 Register – low byte			
Bit	7	6	5	4	3	2	1	0

Function	TMA_CCP3_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP3_L[7:0]	R/W	Timer A Counter / Capture / PWM 3 register – low byte	

Table 5-125 TMA_CCP3_L register

TMA_CCP3_H			Page : 3 / Address: 0xB7		Timer A Counter / Capture / PWM 3 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP3_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP3_H[7:0]	R/W	Timer A Counter / Capture / PWM 3 register – high byte	

Table 5-126 TMA_CCP3_H register

TMA_CCP4_L			Page : 3 / Address: 0xBA		Timer A Counter / Capture / PWM 4 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP4_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP4_L[7:0]	R/W	Timer A Counter / Capture / PWM 4 register – low byte	

Table 5-127 TMA_CCP4_L register

TMA_CCP4_H			Page : 3 / Address: 0xBB		Timer A Counter / Capture / PWM 4 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP4_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP4_H[7:0]	R/W	Timer A Counter / Capture / PWM 4 register – high byte	

Table 5-128 TMA_CCP4_H register

TMA_CCP5_L			Page : 3 / Address: 0xBC		Timer A Counter / Capture / PWM 5 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP5_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP5_L[7:0]	R/W	Timer A Counter / Capture / PWM 5 register – low byte	

Table 5-129 TMA_CCP5_L register

TMA_CCP5_H			Page : 3 / Address: 0xBD		Timer A Counter / Capture / PWM 5 Register – high byte			
Bit	7	6	5	4	3	2	1	0

Function	TMA_CCP5_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP5_H[7:0]	R/W	Timer A Counter / Capture / PWM 5 register – high byte	

Table 5-130 TMA_CCP5_H register

TMA_ADC_TRG0_L			Page : 3 / Address: 0xBE		Timer A ADC Trigger Level 0 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_ADC_TRG0_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_ADC_TRG0_L[7:0]	R/W	Timer A ADC trigger level 0 register – low byte	

Table 5-131 TMA_ADC_TRG0_L register

TMA_ADC_TRG0_H			Page : 3 / Address: 0xBF		Timer A ADC Trigger Level 0 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_ADC_TRG0_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_ADC_TRG0_H[7:0]	R/W	Timer A ADC trigger level 0 register – high byte	

Table 5-132 TMA_ADC_TRG0_H register

TMA_ADC_TRG1_L			Page : 3 / Address: 0xC2		Timer A ADC Trigger Level 1 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_ADC_TRG1_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_ADC_TRG1_L[7:0]	R/W	Timer A ADC trigger level 1 register – low byte	

Table 5-133 TMA_ADC_TRG1_L register

TMA_ADC_TRG1_H			Page : 3 / Address: 0xC3		Timer A ADC Trigger Level 1 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_ADC_TRG1_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_ADC_TRG1_H[7:0]	R/W	Timer A ADC trigger level 1 register – high byte	

Table 5-134 TMA_ADC_TRG1_H register

TMA_PWM0_END_L			Page : 3 / Address: 0xC4		Timer A PWM0 End Duty Register – low byte			
Bit	7	6	5	4	3	2	1	0

Function	TMA_PWM0_END_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM0_END_L[7:0]	R/W	Timer A PWM0 end duty register – low byte	

Table 5-135 TMA_PWM0_END_L register

TMA_ PWM0_END_H			Page : 3 / Address: 0xC5		Timer A PWM0 End Duty Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM0_END_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM0_END_H[7:0]	R/W	Timer A PWM0 end duty register – high byte	

Table 5-136 TMA_PWM0_END_H register

TMA_PWM1_END_L			Page : 3 / Address: 0xC6		Timer A PWM1 End Duty Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM1_END_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM1_END_L[7:0]	R/W	Timer A PWM1 end duty register – low byte	

Table 5-137 TMA_PWM1_END_L register

TMA_ PWM1_END_H			Page : 3 / Address: 0xC7		Timer A PWM1 End Duty Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM1_END_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM1_END_H[7:0]	R/W	Timer A PWM1 end duty register – high byte	

Table 5-138 TMA_PWM1_END_H register

TMA_PWM2_END_L			Page : 3 / Address: 0xCA		Timer A PWM2 End Duty Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM2_END_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM2_END_L[7:0]	R/W	Timer A PWM2 end duty register – low byte	

Table 5-139 TMA_PWM2_END_L register

TMA_ PWM2_END_H			Page : 3 / Address: 0xCB		Timer A PWM2 End Duty Register – high byte			
Bit	7	6	5	4	3	2	1	0

Function	TMA_PWM2_END_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM2_END_H[7:0]	R/W	Timer A PWM2 end duty register – high byte	

Table 5-140 TMA_PWM2_END_H register

TMA_PWM3_END_L			Page : 3 / Address: 0xCC		Timer A PWM3 End Duty Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM3_END_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM3_END_L[7:0]	R/W	Timer A PWM3 end duty register – low byte	

Table 5-141 TMA_PWM3_END_L register

TMA_ PWM3_END_H			Page : 3 / Address: 0xCD		Timer A PWM3 End Duty Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM3_END_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM3_END_H[7:0]	R/W	Timer A PWM3 end duty register – high byte	

Table 5-142 TMA_PWM3_END_H register

TMA_PWM4_END_L			Page : 3 / Address: 0xCE		Timer A PWM4 End Duty Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM4_END_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM4_END_L[7:0]	R/W	Timer A PWM4 end duty register – low byte	

Table 5-143 TMA_PWM4_END_L register

TMA_ PWM4_END_H			Page : 3 / Address: 0xCF		Timer A PWM4 End Duty Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM4_END_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM4_END_H[7:0]	R/W	Timer A PWM4 end duty register – high byte	

Table 5-144 TMA_PWM4_END_H register

TMA_PWM5_END_L			Page : 3 / Address: 0xD1		Timer A PWM5 End Duty Register – low byte			
Bit	7	6	5	4	3	2	1	0

Function	TMA_PWM5_END_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM5_END_L[7:0]	R/W	Timer A PWM5 end duty register – low byte	

Table 5-145 TMA_PWM5_END_L register

TMA_ PWM5_END_H			Page : 3 / Address: 0xD2		Timer A PWM5 End Duty Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PWM5_END_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PWM5_END_H[7:0]	R/W	Timer A PWM5 end duty register – high byte	

Table 5-146 TMA_PWM5_END_H register

TMA_PWM_REV	Page: 3		Address: 0xD4		Timer A PWM Reverse Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	TMA_PWM_REV		
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description
[7:3]	-	R/W	Reserved
[2:0]	TMA_PWM_REV	R/W	Timer A PWM reverse enable signal. These bits are used in complementary and center alignment only. TMA_PWM_REV[0] : PWM0/1 TMA_PWM_REV[1] : PWM2/3 TMA_PWM_REV[2] : PWM4/5

Table 5-147 TMA_PWM_REV register

5.9.4. Timer B

The Timer B, which is a 16-bit-wide register, can operate as timer. The additional Counter/Capture/PWM feature is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc.

5.9.4.1. Timer / Counter mode

In timer / counter function, that have up to 8 clock source can be selected. Thus, the 16-bit timer register is decremented in every clock periods. The Figure 5.9-22 shows the block diagram of counter / timer function for Timer B. When Timer B rolls over from pre-load data (TMB_PLOAD_H/L) to 0, not only TMB_INTF is set but also Timer B registers is loaded with the 16-bit value from TMB_PLOAD_H/L register. Required TMB_PLOAD_H/L value can be preset by software.

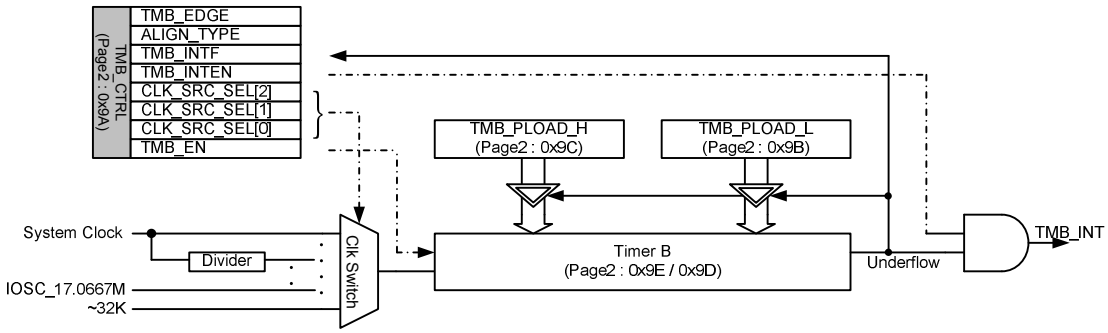


Figure 5.9-22 The block diagram of counter / timer function for Timer B

5.9.4.2. Capture functions

Each of capture registers can be used to latch the current 16-bit value of the Timer B registers (TMB_H and TMB_L) when an external event is triggered.

錯誤! 找不到參照來源。 Figure 5.9-23 shows functional diagrams of the Timer B capture function.

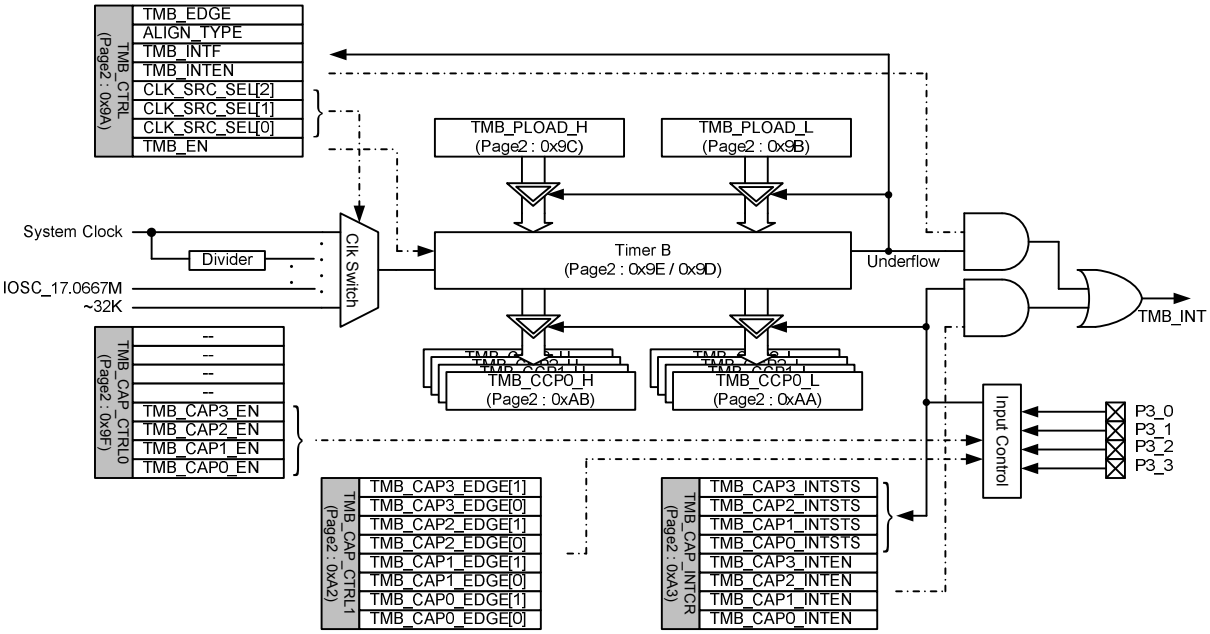


Figure 5.9-23 The block diagram of Timer B capture mode

5.9.4.3. PWM functions

The Timer B consists of 4 sets PWM function. When the TMB_PWMx_EN is enabled, the PWM output will toggle at the TMB_H/L are lesser or greater than TMB_CCPx_H/L value. About Timer count policy, there are two options can be choice between edge and center alignment. In edge alignment, the counter decrease counter value per clock cycle. Hardware will auto re-load TMB_PLOAD_H/L value to counter when counter is underflow. In center alignment, the counter is executing down count first and executing up-count next. There are two output mode of PWM output pin: independent and complement mode. In each mode, user can change output polarity with TMB_PWM_CTRL1 randomly. Figure 5.9-24**錯誤! 找不到參照來源。** shows functional diagrams of the Timer B PWM function, Figure 5.9-25 to Figure 5.9-30 are shows PWM operating waveform.

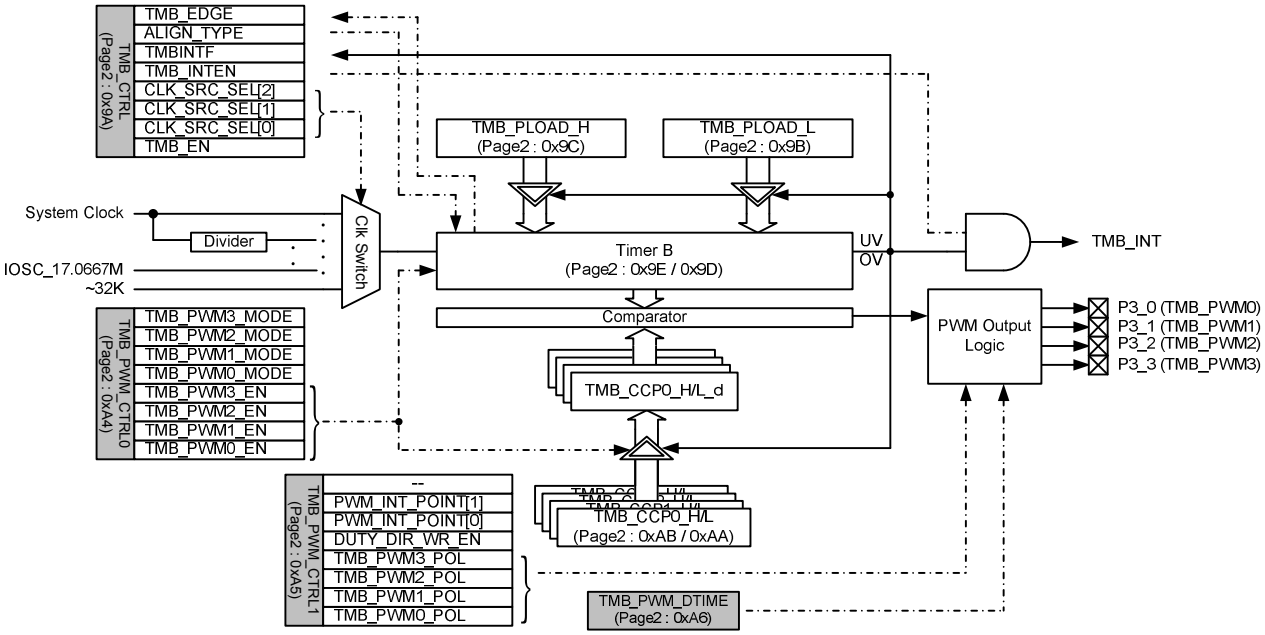


Figure 5.9-24 The block diagram of Timer B PWM mode

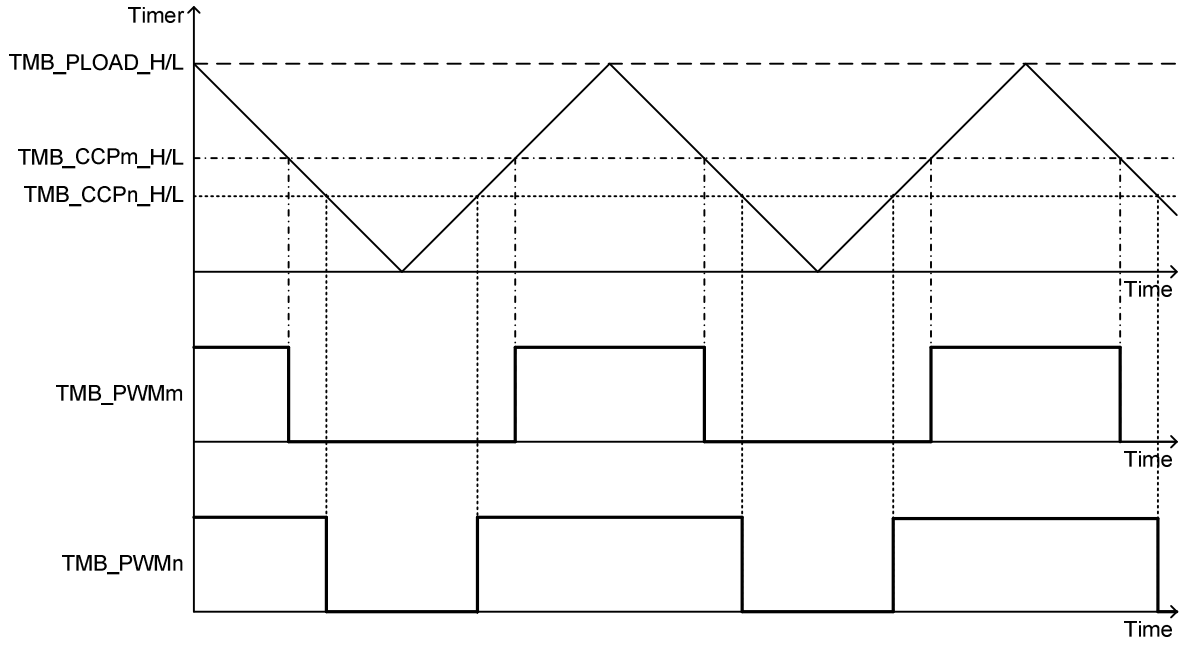


Figure 5.9-25 The waveform of Timer B PWM w/o dead time (ALIGN_TYPE : 1 / DUTY_MODE : 0 / TMB_PWMx_MODE : 0)

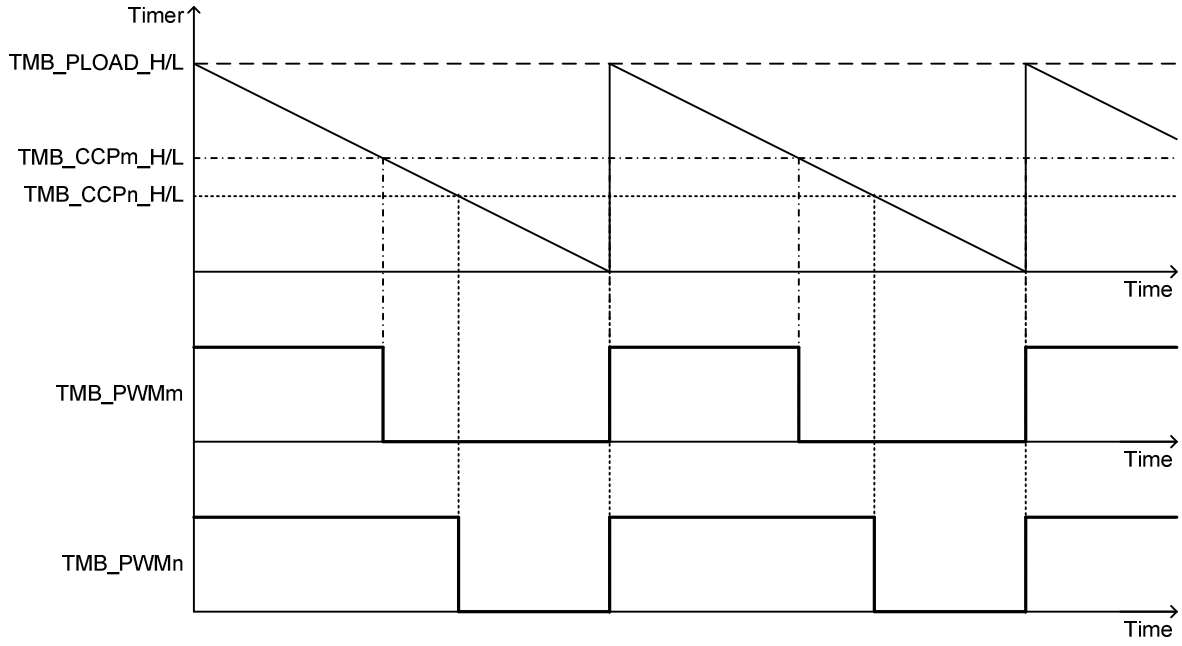


Figure 5.9-26 The waveform of Timer B PWM w/o dead time (ALIGN_TYPE : 0 / DUTY_MODE : 0 / TMB_PWMx_MODE : 0)

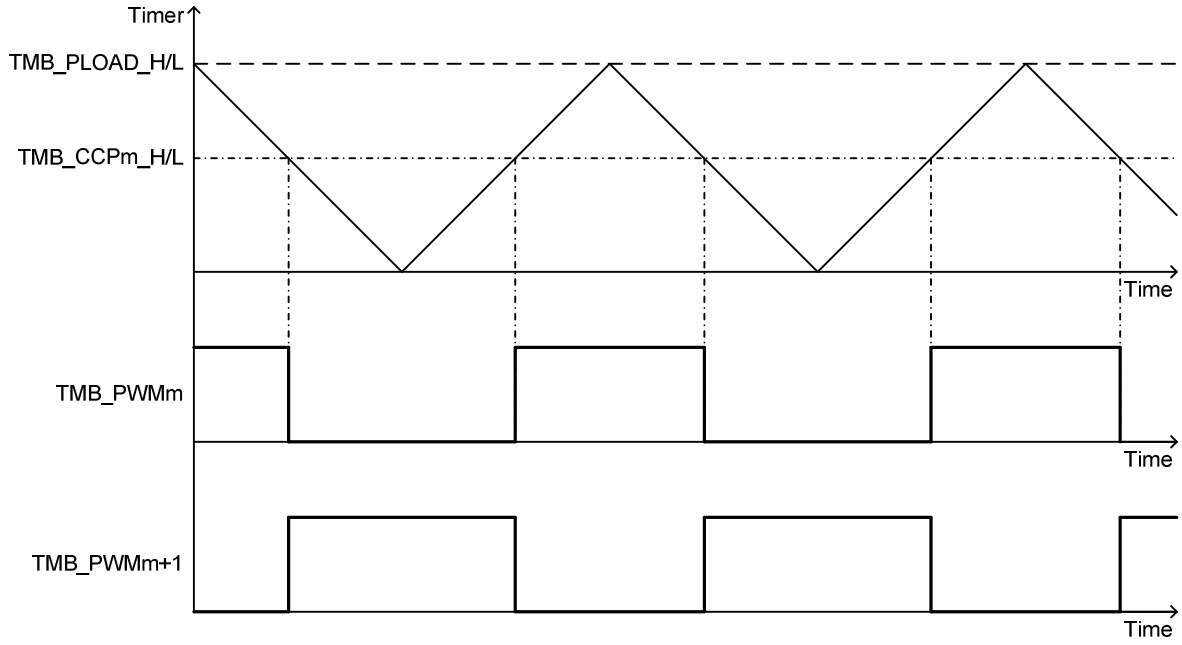


Figure 5.9-27 The waveform of Timer B PWM w/o dead time (ALIGN_TYPE : 1 / DUTY_MODE : 0 / TMB_PWMx_MODE : 1)

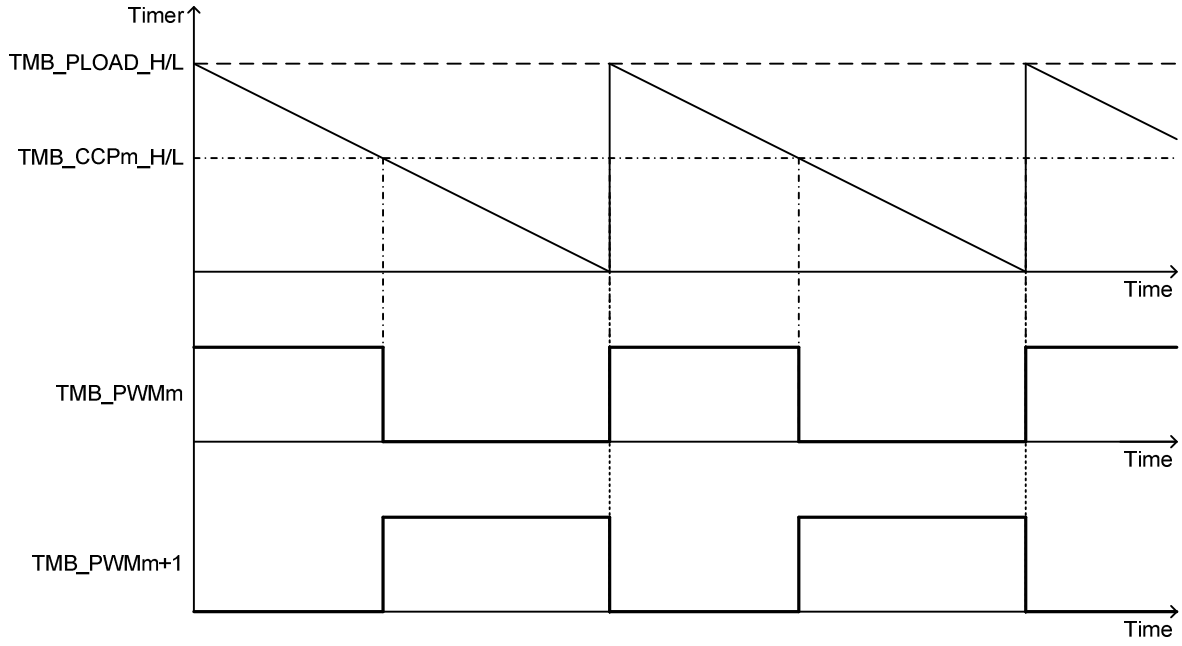


Figure 5.9-28 The waveform of Timer B PWM w/o dead time (ALIGN_TYPE : 0 / DUTY_MODE : 0 / TMB_PWMx_MODE : 1)

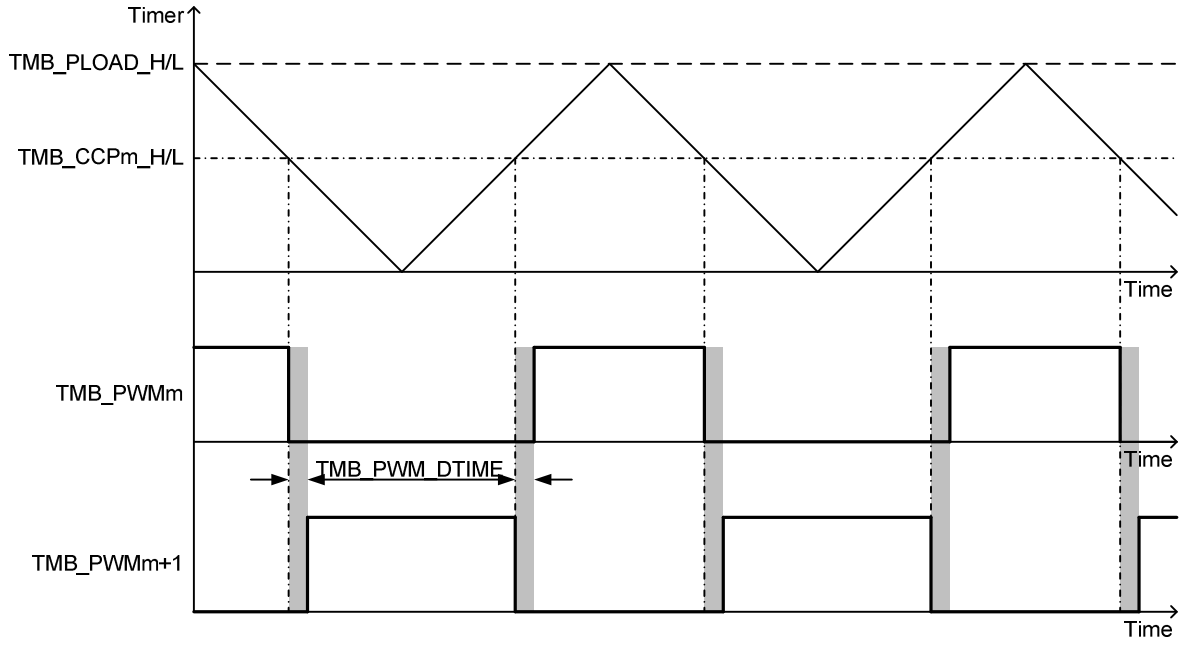


Figure 5.9-29 The waveform of Timer B PWM w/i dead time (ALIGN_TYPE : 1 / DUTY_MODE : 0 / TMB_PWMx_MODE : 1)

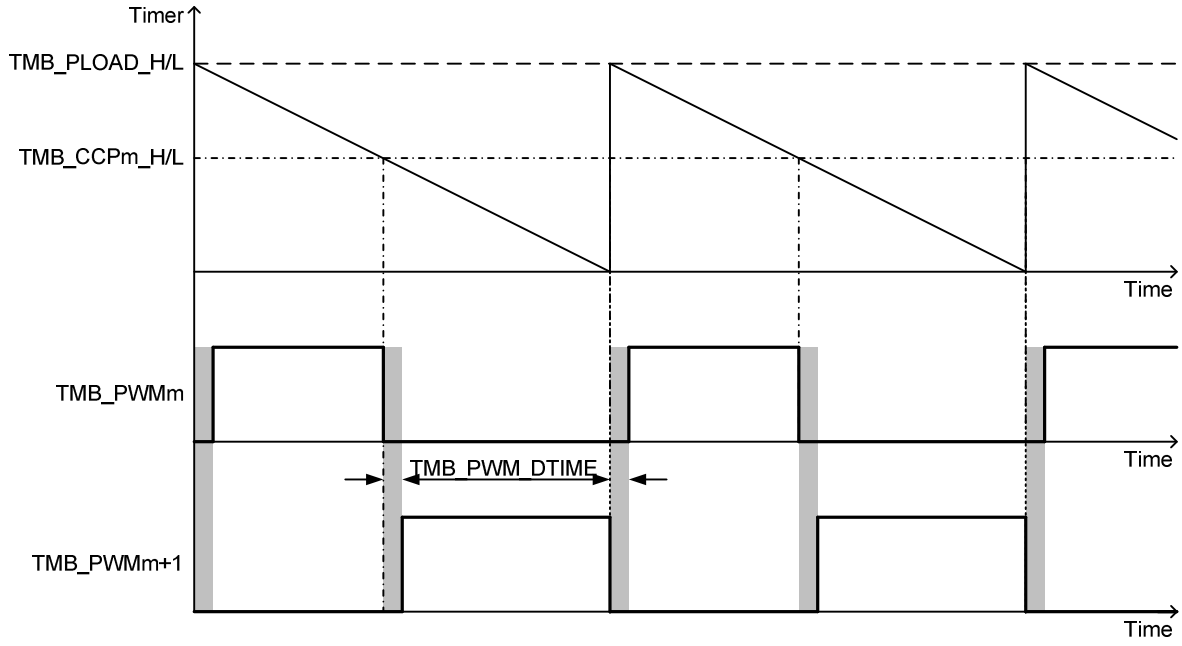


Figure 5.9-30 The waveform of Timer B PWM w/i dead time (ALIGN_TYPE : 0 / DUTY_MODE : 0 / TMB_PWMx_MODE : 1)

5.9.4.4. Timer B Related Registers

TMB_CTRL			Page : 2 / Address: 0x9A		Timer B Control1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMB_EDGE	ALIGN_TYPE	TMB_INTF	TMB_INTEN	CLK_SRC_SEL[2:0]			TMB_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TMB_EDGE	R	Timer B up/down count edge indication. 0 : falling edge 1 : rising edge	
6	ALIGN_TYPE	R/W	0 : edge align 1 : center align	
5	TMB_INTF	R/W	Timer B interrupt flag. read : 0 : idle / busy 1 : timer B interrupt trigger write : 0 : clear this bit 1 : no effect	
4	TMB_INTEN	R/W	Timer B interrupt enable control bit 0 : disable 1 : enable	
3:1	CLK_SRC_SEL	R/W	Timer B input clock source selection control bit CLK_SRC_SEL[2:0] / Clock Source 000 / System clock 001 / System clock / 2 010 / System clock / 4 011 / System clock / 8	

Bit	Function	Type	Description	Condition
			100 System clock / 16 101 System clock / 32 110 IOSC_17.0667M 111 ~32K (IOSC_32KI)	
0	TMB_EN	R/W	Timer B enable control bit. 0 : disable 1 : enable	

Table 5-148 TMB_CTRL register

TMB_PLOAD_L			Page : 2 / Address: 0x9B		Timer B Pre-Load Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_PLOAD_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_PLOAD_L[7:0]	R/W	Timer B pre-load data or PWM period data register – low byte	

Table 5-149 TMB_PLOAD_L register

TMB_PLOAD_H			Page : 2 / Address: 0x9C		Timer B Pre-Load Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_PLOAD_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_PLOAD_H[7:0]	R/W	Timer B pre-load data or PWM period data register – high byte	

Table 5-150 TMB_PLOAD_H register

TMB_L			Page : 2 / Address: 0x9D		Timer B Counter Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_L[7:0]	R/W	Timer B counter register – low byte	

Table 5-151 TMB_L register

TMB_H			Page : 2 / Address: 0x9E		Timer B Counter Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_H[7:0]	R/W	Timer B counter register – high byte	

Table 5-152 TMB_H register

TMB_CAP_CTRL0			Page : 2 / Address: 0x9F		Timer B Capture Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMB_CAPx_EN[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	TMB_CAPx_EN[3:0]	R/W	Timer B capture mode enable control bit. All of the trigger source are from external I/O. Following table is the trigger source mapping table. TMB_CAPx_EN / Mapping I/O TMB_CAP0_EN / P3[0] TMB_CAP1_EN / P3[1] TMB_CAP2_EN / P3[2] TMB_CAP3_EN / P3[3] 0 : disable 1 : enable	

Table 5-153 TMB_CAP_CTRL0 register

TMB_CAP_CTRL1			Page : 2 / Address: 0xA2		Timer B Capture Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CAP3_EDGE[1:0]		TMB_CAP2_EDGE[1:0]		TMB_CAP1_EDGE[1:0]		TMB_CAP0_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	TMB_CAP3_EDGE[7:6]	R/W	Timer B capture 3 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	
5:4	TMB_CAP2_EDGE[5:4]	R/W	Timer B capture 2 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	
3:2	TMB_CAP1_EDGE[3:2]	R/W	Timer B capture 1 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	
1:0	TMB_CAP0_EDGE[1:0]	R/W	Timer B capture 0 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	

Table 5-154 TMB_CAP_CTRL1 register

TMB_CAP_INTCTRL			Page : 2 / Address: 0xA3		Timer B Capture Mode Interrupt Control Register			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CAP_INTSTS[3:0]				TMB_CAP_INTEN[3:0]			

Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	TMB_CAP_INTSTS[3:0]	R/W	Timer B capture mode trigger flag. These are map to CAP0 ~ CAP3 respectively. read : 0 : no capture signal triggered 1 : capture signal triggered write : 0 : clear this bit 1 : no effect	
3:0	TMB_CAP_INTEN	R/W	Timer B capture mode interrupt enable control bits. These are map to CAP0 ~ CAP3 respectively. 0 : disable 1 : enable	

Table 5-155 TMB_CAP_INTCTRL registers

TMB_PWM_CTRL0			Page : 2 / Address: 0xA4		Timer B PWM Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	TMB_PWM23_MODE	--	TMB_PWM01_MODE	TMB_PWMx_EN[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	TMB_PWM23_MODE	R/W	Timer B PWM 2/3 operationg mode selection bit 0 : independent mode 1 : complementary mode	
5	--	R/W	Reserved	
4	TMB_PWM01_MODE	R/W	Timer B PWM 0/1 operationg mode selection bit 0 : independent mode 1 : complementary mode	
3:0	TMB_PWMx_EN[3:0]	R/W	Timer B PWM mode enable bits 0 : disable 1 : enable	

Table 5-156 TMB_PWM_CTRL0 register

TMB_PWM_CTRL1			Page : 2 / Address: 0xA5		Timer B PWM Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	PWM_INT_POINT[1:0]		DUTY_DIR_WR_EN	TMB_PWMx_POL[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6:5	PWM_INT_POONT	R/W	These bits are used to set PWM interrupt when ALIGN_TYPE is set to	

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td></td><td></td><td></td><td>center alignment.<table><tr><td>PWM_INT_POINT[1 :0]</td><td>Trigger Point (with center mode and PWM is enableed)</td></tr><tr><td>00</td><td>Interrupt is triggered when counter is under flow</td></tr><tr><td>01</td><td>Interrupt is triggered when counter is over flow</td></tr><tr><td>10</td><td>Interrupt is triggered when counter is under and over flow</td></tr><tr><td>11</td><td>No effect</td></tr></table></td><td></td></tr>
<tr><td>4</td><td>DUTY_DIR_WR_EN</td><td>R/W</td><td>PWM duty is updated immediately when CPU write data into PWM duty registers
0 : disable
1 : enable</td><td></td></tr>
<tr><td>3</td><td>TMB_PWM3_POL</td><td>R/W</td><td>Timer B PWM3 polarity setting
Independent mode:
0: PWM3 output low when PWM_cnt = TMB_CCP3
1: PWM3 output high when PWM_cnt = TMB_CCP3
Complementary mode:
0: PWM3 output high when PWM_cnt = TMB_CCP2
1: PWM3 output low when PWM_cnt = TMB_CCP2</td><td></td></tr>
<tr><td>2</td><td>TMB_PWM2_POL</td><td>R/W</td><td>Timer B PWM2 polarity setting
Independent mode:
0: PWM2 output low when PWM_cnt = TMB_CCP2
1: PWM2 output high when PWM_cnt = TMB_CCP2
Complementary mode:
0: PWM2 output low when PWM_cnt = TMB_CCP2
1: PWM2 output high when PWM_cnt = TMB_CCP2</td><td></td></tr>
<tr><td>1</td><td>TMB_PWM1_POL</td><td>R/W</td><td>Timer B PWM1 polarity setting
Independent mode:
0: PWM1 output low when PWM_cnt = TMB_CCP1
1: PWM1 output high when PWM_cnt = TMB_CCP1
Complementary mode:
0: PWM1 output high when PWM_cnt = TMB_CCP0
1: PWM1 output low when PWM_cnt = TMB_CCP0</td><td></td></tr>
<tr><td>0</td><td>TMB_PWM0_POL</td><td>R/W</td><td>Timer B PWM0 polarity setting
Independent mode:
0: PWM0 output low when PWM_cnt = TMB_CCP0
1: PWM0 output high when PWM_cnt = TMB_CCP0
Complementary mode:
0: PWM0 output low when PWM_cnt = TMB_CCP0
1: PWM0 output high when PWM_cnt = TMB_CCP0</td><td></td></tr>
</table>

Table 5-157 TMB_PWM_CTRL1 register

TMB_PWM_DTIME	Page : 2 / Address: 0xA6	Timer B PWM Dead Time Register

Bit	7	6	5	4	3	2	1	0
Function	TMB_PWM_DTIME[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_PWM_DTIME[7:0]	R/W	Timer B PWM dead time register	

Table 5-158 TMB_PWM_DTIME register

TMB_CCP0_L			Page : 2 / Address: 0xAA		Timer B Coutner / Capture / PWM 0 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP0_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP0_L[7:0]	R/W	Timer B Counter / Capture / PWM 0 register – low byte	

Table 5-159 TMB_CCP0_L register

TMB_CCP0_H			Page : 2 / Address: 0xAB		Timer B Counter / Capture / PWM 0 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP0_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP0_H[7:0]	R/W	Timer B Counter / Capture / PWM 0 register – high byte	

Table 5-160 TMB_CCP0_H register

TMB_CCP1_L			Page : 2 / Address: 0xAC		Timer B Counter / Capture / PWM 1 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP1_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP1_L[7:0]	R/W	Timer B Counter / Capture / PWM 1 register – low byte	

Table 5-161 TMB_CCP1_L register

TMB_CCP1_H			Page : 2 / Address: 0xAD		Timer B Counter / Capture / PWM 1 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP1_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP1_H[7:0]	R/W	Timer B Counter / Capture / PWM 1 register – high byte	

Table 5-162 TMA_CCP1_H register

TMB_CCP2_L			Page : 2 / Address: 0xAE		Timer B Counter / Capture / PWM 2 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP2_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP2_L[7:0]	R/W	Timer B Counter / Capture / PWM 2 register – low byte	

Table 5-163 TMB_CCP2_L register

TMB_CCP2_H			Page : 2 / Address: 0xAF		Timer B Counter / Capture / PWM 2 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP2_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP2_H[7:0]	R/W	Timer B Counter / Capture / PWM 2 register – high byte	

Table 5-164 TMB_CCP2_H register

TMB_CCP3_L			Page : 2 / Address: 0xB2		Timer B Counter / Capture / PWM 3 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP3_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP3_L[7:0]	R/W	Timer B Counter / Capture / PWM 3 register – low byte	

Table 5-165 TMB_CCP3_L register

TMB_CCP3_H			Page : 2 / Address: 0xB3		Timer B Counter / Capture / PWM 3 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP3_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP3_H[7:0]	R/W	Timer B Counter / Capture / PWM 3 register – high byte	

Table 5-166 TMB_CCP3_H register

5.9.5. Timer C

The Timer C, which is a 16-bit-wide register, can operate as timer. The additional Counter/Capture feature is one of the most powerful peripheral units of the core. It can be used for all kinds of event capturing.

5.9.5.1. Timer / Counter mode

In timer / counter function, that have up to 7 clock source can be selected. Thus, the 16-bit timer register is decremented in every clock periods. The Figure 5.9-31 shows the block diagram of counter / timer function for Timer C. When Timer C rolls over from pre-load data (TMC_PLOAD_H/L) to 0, not only TMC_INTF is set but also Timer C registers is loaded with the 16-bit value from TMC_PLOAD_H/L register. Required TMC_PLOAD_H/L value can be preset by software.

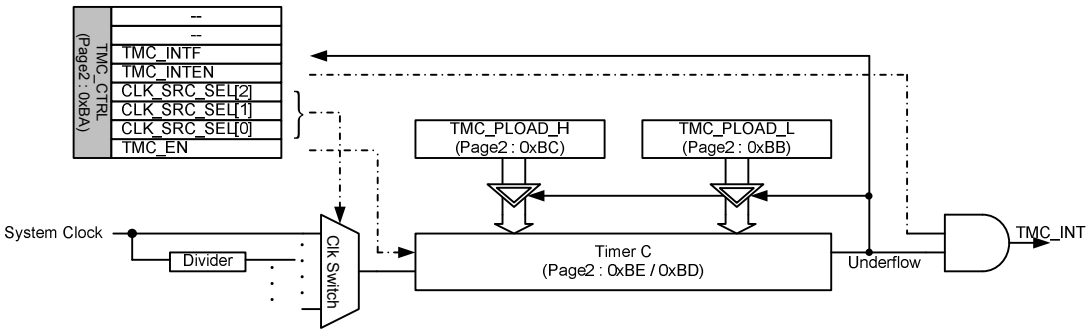


Figure 5.9-31 The block diagram of counter / timer function for Timer C

5.9.5.2. Capture functions

Each of capture registers can be used to latch the current 16-bit value of the Timer C registers (TMC_H and TMC_L) when an external event is triggered.

錯誤! 找不到參照來源。Figure 5.9-32 shows functional diagrams of the Timer C capture function.

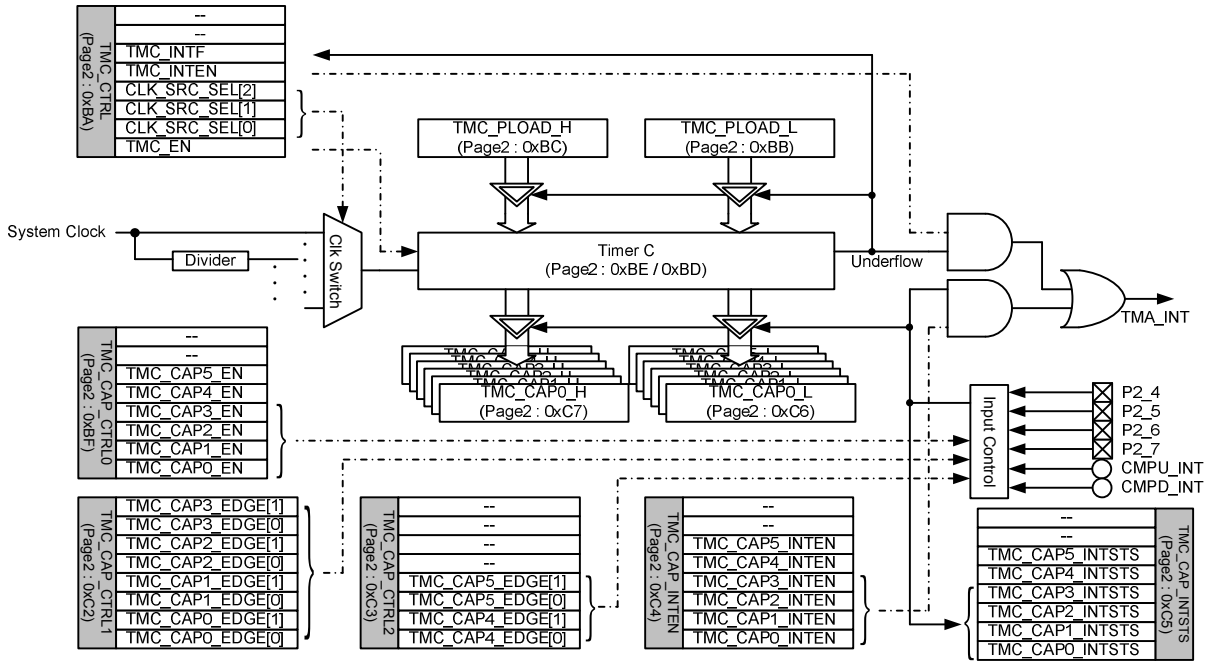


Figure 5.9-32 The block diagram of Timer C capture mode

5.9.5.3. Timer C Related Registers

TMC_CTRL			Page : 2 / Address: 0xBA		Timer C Control1 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_INTF	TMC_INTEN	CLK_SRC_SEL[2:0]			TMC_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R	Reserved	
5	TMC_INTF	R/W	Timer C interrupt flag. read :	

Bit	Function	Type	Description	Condition
			0 : idle / busy 1 : timer C interrupt trigger write : 0 : clear this bit 1 : no effect	
4	TMC_INTEN	R/W	Timer C interrupt enable control bit 0 : disable 1 : enable	
3:1	CLK_SRC_SEL	R/W	Timer C input clock source selection control bit CLK_SRC_SEL[2:0] / Clock Source 000 System clock 001 System clock / 2 010 System clock / 4 011 System clock / 128 100 System clock / 256 101 System clock / 512 110 System clock / 1024 111 Prohibit	
0	TMC_EN	R/W	Timer C enable control bit. 0 : disable 1 : enable	

Table 5-167 TMC_CTRL register

TMC_PLOAD_L			Page : 2 / Address: 0xBB		Timer C Pre-Load Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_PLOAD_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_PLOAD_L[7:0]	R/W	Timer C pre-load data or PWM period data register – low byte	

Table 5-168 TMC_PLOAD_L register

TMC_PLOAD_H			Page : 2 / Address: 0xBC		Timer C Pre-Load Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_PLOAD_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_PLOAD_H[7:0]	R/W	Timer C pre-load data or PWM period data register – high byte	

Table 5-169 TMC_PLOAD_H register

TMC_L			Page : 2 / Address: 0xBD		Timer C Counter Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_L[7:0]							

Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_L[7:0]	R/W	Timer C counter register – low byte	

Table 5-170 TMC_L register

TMC_H			Page : 2 / Address: 0xBE		Timer B Counter Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_H[7:0]	R/W	Timer B counter register – high byte	

Table 5-171 TMB_H register

TMC_CAP_CTRL0			Page : 2 / Address: 0xBF		Timer C Capture Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_CAPx_EN[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	TMC_CAPx_EN[5:0]	R/W	Timer C capture mode enable control bit. All of the trigger source are from external I/O and comparator interrupt. Following table is the trigger source mapping table. TMC_CAPx_EN / Mapping I/O TMC_CAP0_EN / P2[4] TMC_CAP1_EN / P2[5] TMC_CAP2_EN / P2[6] TMC_CAP3_EN / P2[7] TMC_CAP4_EN / CMPU_INT TMC_CAP5_EN / CMPD_INT 0 : disable 1 : enable	

Table 5-172 TMC_CAP_CTRL0 register

TMC_CAP_CTRL1			Page : 2 / Address: 0xC2		Timer C Capture Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP3_EDGE[1:0]		TMC_CAP2_EDGE[1:0]		TMC_CAP1_EDGE[1:0]		TMC_CAP0_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	TMC_CAP3_EDGE[7:6]	R/W	Timer C capture 3 sample edge selection bit 00 : falling edge 01 : rising edge	

Bit	Function	Type	Description	Condition
			1x : both edge	
5:4	TMC_CAP2_EDGE[5:4]	R/W	Timer C capture 2 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	
3:2	TMC_CAP1_EDGE[3:2]	R/W	Timer C capture 1 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	
1:0	TMC_CAP0_EDGE[1:0]	R/W	Timer C capture 0 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edge	

Table 5-173 TMC_CAP_CTRL1 register

TMC_CAP_CTRL2			Page : 2 / Address: 0xC3		Timer C Capture Control 2 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMC_CAP5_EDGE[1:0]		TMC_CAP4_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:2	TMC_CAP5_EDGE[3:2]	R/W	Timer C capture 5 sample edge selection bit (for comparator down side) 00 : falling edge 01 : rising edge 1x : both edge	
1:0	TMC_CAP4_EDGE[1:0]	R/W	Timer C capture 4 sample edge selection bit (for comparator up side) 00 : falling edge 01 : rising edge 1x : both edge	

Table 5-174 TMC_CAP_CTRL1 register

TMC_CAP_INTEN			Page : 2 / Address: 0xC4		Timer C Capture Mode Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_CAPx_INTEN[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	TMC_CAPx_INTEN[5:0]	R/W	Timer C capture mode interrupt enable control bits. These are map to CAP0 ~ CAP3, CMPU_INT and CMPD_INT respectively. 0 : disable 1 : enable	

Table 5-175 TMC_CAP_INTEN register

TMC_CAP_INTSTS			Page : 2 / Address: 0xC5		Timer C Capture Mode Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_CAPx_INTSTS[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	TMC_CAPx_INTSTS[5:0]	R/W	Timer C capture mode interrupt status register. These are map to CAP0 ~ CAP3, CMPU_INT and CMPD_INT respectively. read : 0 : no capture triggered 1 : capture triggered write : 0 : clear this bit 1 : no effect	

Table 5-176 TMC_CAP_INTSTS register

TMC_CAP0_L			Page : 2 / Address: 0xC6		Timer C Capture 0 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP0_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP0_L[7:0]	R/W	Timer C Capture 0 register – low byte	

Table 5-177 TMC_CAP0_L register

TMC_CAP0_H			Page : 2 / Address: 0xC7		Timer C Capture 0 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP0_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP0_H[7:0]	R/W	Timer C Capture 0 register – high byte	

Table 5-178 TMC_CAP0_H register

TMC_CAP1_L			Page : 2 / Address: 0xCA		Timer C Capture 1 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP1_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP1_L[7:0]	R/W	Timer C Capture 1 register – low byte	

Table 5-179 TMC_CAP1_L register

TMC_CAP1_H			Page : 2 / Address: 0xCB		Timer C Capture 1 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP1_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP1_H[7:0]	R/W	Timer C Capture 1 register – high byte	

Table 5-180 TMC_CAP1_H register

TMC_CAP2_L			Page : 2 / Address: 0xCC		Timer C Capture 2 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP2_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP2_L[7:0]	R/W	Timer C Capture 2 register – low byte	

Table 5-181 TMC_CAP2_L register

TMC_CAP2_H			Page : 2 / Address: 0xCD		Timer C Capture 2 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP2_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP2_H[7:0]	R/W	Timer C Capture 2 register – high byte	

Table 5-182 TMC_CAP2_H register

TMC_CAP3_L			Page : 2 / Address: 0xCE		Timer C Capture 3 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP3_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP3_L[7:0]	R/W	Timer C Capture 3 register – low byte	

Table 5-183 TMC_CAP3_L register

TMC_CAP3_H			Page : 2 / Address: 0xCF		Timer C Capture 3 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP3_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition

Bit	Function	Type	Description	Condition
7:0	TMC_CAP3_H[7:0]	R/W	Timer C Capture 3 register – high byte	

Table 5-184 TMC_CAP3_H register

TMC_CAP4_L			Page : 2 / Address: 0xD1		Timer C Capture 4 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP4_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP4_L[7:0]	R/W	Timer C Capture 4 register – low byte	

Table 5-185 TMC_CAP4_L register

TMC_CAP4_H			Page : 2 / Address: 0xD2		Timer C Capture 4 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP4_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP4_H[7:0]	R/W	Timer C Capture 4 register – high byte	

Table 5-186 TMC_CAP4_H register

TMC_CAP5_L			Page : 2 / Address: 0xD3		Timer C Capture 5 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP5_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP5_L[7:0]	R/W	Timer C Capture 5 register – low byte	

Table 5-187 TMC_CAP5_L register

TMC_CAP5_H			Page : 2 / Address: 0xD4		Timer C Capture 5 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP5_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP5_H[7:0]	R/W	Timer C Capture 5 register – high byte	

Table 5-188 TMC_CAP5_H register

5.10. UART0

UART0 has the same functionality as a standard 8051 UART. The serial port is full duplex, meaning it can transmit and receive concurrently. It is reception with double-buffer, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0 reads a

physically separate receive register. The Figure 5.10-1 shows the block diagram of UART module. The serial port can operate in 4 modes: one synchronous and three asynchronous modes. Mode 2 and 3 has a special feature for multiprocessor communications. This feature is enabled by setting SM02 bit in SCON0 register. The master processor first sends out an address byte, which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM02 = 1, no slave will be interrupted by a data byte. An address byte will interrupt all slaves. The addressed slave will clear its SM02 bit and prepare to receive the data bytes that will be coming. The slaves that were not being addressed leave their SM02 set and ignoring the incoming data.

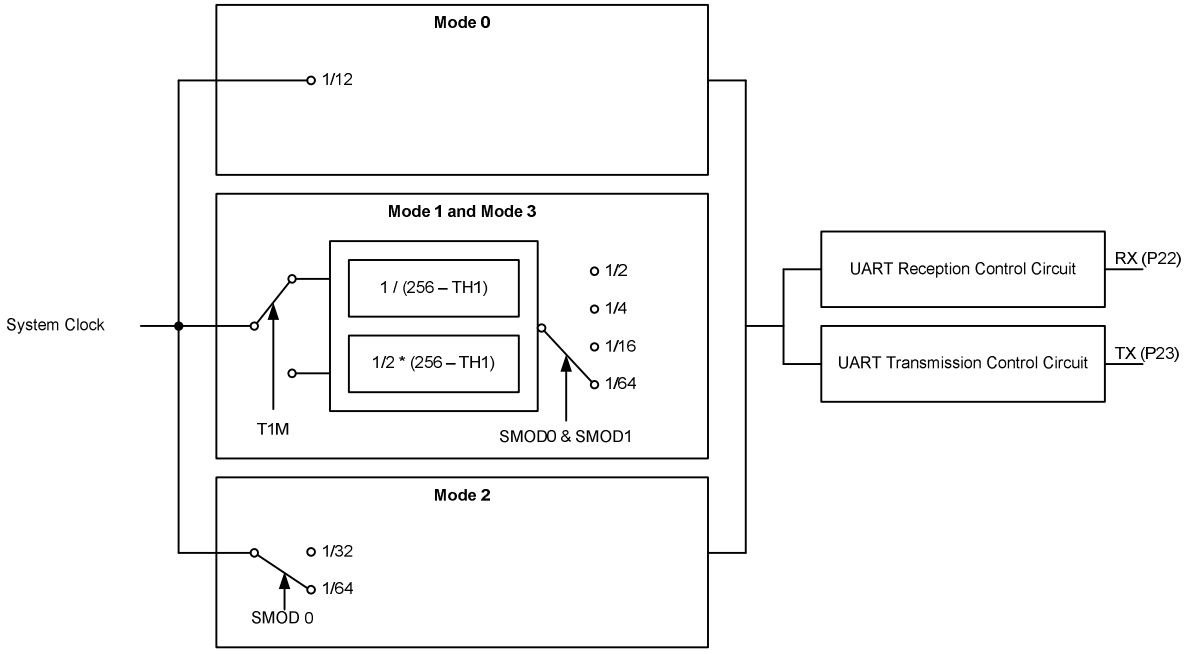


Figure 5.10-1 The block diagram of UART module

5.10.1. UART0: Mode 0(Synchronous Shift register)

This mode is used as shift register IO control, and not for real communication application. The baud rate is fixed at 1/12 of the system clock frequency and TX output is a shift clock. Eight bits are transmitted with LSB first. Reception is initialized by setting the flags in SCON0 as follows: RI0 =0 and REN0 =1. Figure 5.10-2 shows the timing diagram of UART0 transmission mode 0.

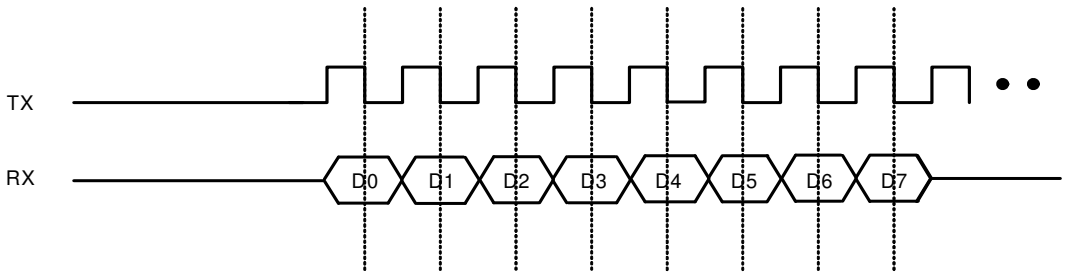


Figure 5.10-2 The timing diagram of UART0 transmission mode 0

5.10.2. UART0: Mode 1(8-Bit UART, Variable Baud Rate, Timer1 Clock Source)

In mode 1, TX serves as serial output. 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receiving, a start bit synchronizes the reception, 8 data bits are available by reading SBUF0 and stop bit sets the flag RB08 in the SFR SCON0. The baud rate is variable and depends from Timer 1 mode. The SMOD0 and SMOD1 bits of PCON (0x87) are used to set the baud rate as $T1_{ov}/2$ or $T1_{ov}/4$ or $T1_{ov}/16$ or $T1_{ov}/64$. Figure 5.10-3 shows the format of UART0 transmission mode 1.

Figure 5.10-3 The format of UART0 transmission mode 1

5.10.3. UART0: Mode 2(9-Bit UART, Fixed Baud Rate)

This mode is similar to Mode 1 with two differences. The baud rate is fixed at 1/32 or 1/64 of system clock frequency, and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the UART0 interface: at transmission, bit TB08 in SCON0 is output as the 9th bit, and at receive, the 9th bit affects RB08 in SCON0. Figure 5.10-4 shows the format of UART0 transmission mode 2.

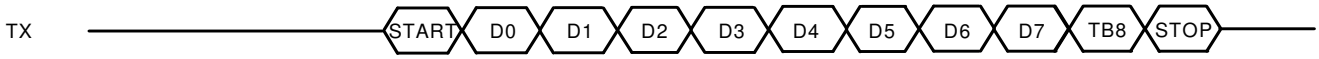


Figure 5.10-4 The format of UART0 transmission mode 2

5.10.4. UART0: Mode 3(9-Bit UART, Variable Baud Rate, Timer1 Clock Source)

The only difference between Mode 2 and Mode 3 is that the baud rate is a variable in Mode 3. When REN0 =1 data receiving is enabled. The baud rate is variable and depends from Timer 1 mode. The SMOD0 and SMOD1 bits of PCON (0x87) are used to set the baud rate as $T1_{ov}/2$ or $T1_{ov}/4$ or $T1_{ov}/16$ or $T1_{ov}/64$. Figure 5.10-5 shows the format of UART0 transmission mode 1.

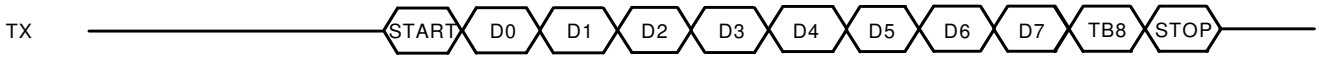


Figure 5.10-5 The format of UART0 transmission mode 3

5.10.5. UART0 Related Registers

The UART0 related registers are: SBUF0(0x99), SCON0(0x98), PCON(0x87), IE(0xA8) and IP(0xB8). The UART0 data buffer (SBUF0) consists of two separate registers: transmit and receive registers. A data written into SBUF0 sets this data in UART0 output register and starts a transmission. A data read from SBUF0, reads data from the UART0 receive register.

SBUF0			**Address: 0x99**		**UART0 Buffer Register**			
Bit	7	6	5	4	3	2	1	0
Function	SBUF0[7:0]							
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Function	Type	Description	Condition
2:0	SBUF0[7:0]	R/W	UART 0 buffer	

Table 5-189 SBUF0 register

SCON0			**Address: 0x98**		**UART0 Configuration Register**			
Bit	7	6	5	4	3	2	1	0
Function	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Function	Type	Description	Condition
7:6	SM0[1:0]	R/W	Mode and baud rate setting which described as below table	
5	SM02	R/W	Enables a multiprocessor communication feature	

Bit	Function	Type	Description	Condition
4	REN0	R/W	Enable serial reception.	
3	TB08	R/W	The 9th transmitted data bit in Modes 2 and Mode 3	
2	RB08	R/W	In Mode 0 this bit is not used In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 2 and Mode 3, it is the 9th data bit received	
1	TI0	R/W	UART0 transmitter interrupt flag	
0	RI0	R/W	UART0 receiver interrupt flag	

Table 5-190 SCON0 register

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	--	PWE	--	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 baud rate bit when clocked by Timer1	
5	--	R/W	Reserved	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3:2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-191 PCON register

SYS_CTRL6			Address : 0xFF		System Control-6 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	UART_IF_EN	T01_CK_SEL	--	AERR_RSTEN	WDOG_CKEN	--
Default	1	1	0	0	0	0	1	0
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	UART_IF_EN	R/W	UART interface enable signal. 0 : disable 1 : enable	
4	T01_CK_SEL	R/W	Timer0/1 clock source select signal.This bit is used combining with T0M/T1M of CKCON(0x8E).	

T0M /T1M	T01_CK_SEL	Timer0/1 Clock
0	0	System Clock / 8
0	1	System Clock / 2

Bit	Function	Type	Description	Condition
			1 0 System Clock / 4 1 1 System Clock / 1	
3	--	R/W	Reserved	
2	AERR_RSTEN	R/W	Flash address over range reset enable 0 : disable 1 : enable	
1	WDOG_CKEN	R/W	Watch dog controller clock enable control bit 0 : disable 1 : enable	
0	--	R/W	Reserved	

Table 5-192 The SYS_CTRL6 register

CKCON			Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	WDFM	T1M	T0M	--	--	--
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:6	WD[1:0]	R/W	Watchdog timeout selection bits If WDFM=0: WD[1:0] Timeout 00 128ms 01 256ms 10 512ms 11 1024ms If WDFM=1: WD[1:0] Timeout 00 8ms 01 16ms 10 32ms 11 64ms	
5	WDFM	R/W	Watchdog fast mode selection bit 0: watchdog fast mode is disabled 1: watchdog fast mode is enabled	
4	T1M	R/W	Timer 1 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF). T1M T01_CK_SEL Timer1 Clock 0 0 System Clock / 8 0 1 System Clock / 2 1 0 System Clock / 4 1 1 System Clock / 1	
3	T0M	R/W	Timer 0 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF). T0M T01_CK_SEL Timer0 Clock 0 0 System Clock / 8	

Bit	Function	Type	Description			Condition
			0	1	System Clock / 2	
			1	0	System Clock / 4	
			1	1	System Clock / 1	
2:0	--	R/W	Reserved			

Table 5-193 CKCON register

SM00	SM01	Mode	Function	Baud rate
0	0	0	Shift register	SYSCLK/12
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	SYSCLK/64(SMOD0=0) SYSCLK/32(SMOD0=1)
1	1	3	9-bit UART	variable

❑ variable: in Mode1 and Mode 3(T1M=0)

SMOD1	SMOD0	Baud rate
0	0	T1ov/64(T1ov=SYSCLK/(256-TH1))
0	1	T1ov/16(T1ov=SYSCLK/(256-TH1))
1	0	T1ov/4(T1ov=SYSCLK/(256-TH1))
1	1	T1ov/2(T1ov=SYSCLK/(256-TH1))

❑ Baud rate setting example (SYSCLK = 64MHz, T1M =1, T01_CK_SEL=1)

Bit rate	Baud rate	Timer reload setting (TH1)	Actual rate	Error deviation (%)
4800	T1ov/64	0x30(48)	4807.69	0.16%
9600	T1ov/64	0x98(152)	9615.38	0.16%
19200	T1ov/16	0x30(48)	19230.77	0.16%
38400	T1ov/16	0x98(152)	38461.54	0.16%
57600	T1ov/16	0xBB(187)	57971.01	0.64%
115200	T1ov/4	0x75(117)	115107.91	-0.079%

❑ Baud rate setting example (SYSCLK = 8.533MHz, T1M=1, T01_CK_SEL=1)

Bit rate	Baud rate	Timer reload setting (TH1)	Actual rate	Error deviation (%)
4800	T1ov/16	0x91(145)	4804.62	0.09%
9600	T1ov/4	0x22(34)	9609.23	0.09%
19200	T1ov/2	0x22(34)	19218.47	0.09%
38400	T1ov/2	0x91(145)	38436.94	0.09%
57600	T1ov/2	0xB6(182)	57655.41	0.09%
115200	T1ov/2	0xDB(219)	115310.81	0.09%

IE			Address: 0xA8		Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	EA	ETC	ETB	ES0	ET1	EX1	ET0	ETA
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EA	R/W	Enable global interrupts	
6	ETC	R/W	Enable Timer C interrupt	
5	ETB	R/W	Enable Timer B interrupt	
4	ES0	R/W	Enable UART0 interrupt	
3	ET1	R/W	Enable Timer 1 interrupt	
2	EX1	R/W	Enable ADC0/1 interrupt	
1	ET0	R/W	Enable Timer 0 interrupt	
0	ETA	R/W	Enable Timer A interrupt	

Table 5-194 IE register

IP			Address: 0xB8		Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	-	PTC	PTB	PS0	PT1	PX1	PT0	PTA
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	PTC	R/W	Timer C interrupt priority level control (1: high level)	
5	PTB	R/W	Timer B interrupt priority level control (1: high level)	
4	PS0	R/W	UART0 interrupt priority level control (1: high level)	
3	PT1	R/W	Timer 1 interrupt priority level control (1: high level)	
2	PX1	R/W	ADC0/1 interrupt priority level control (1: high level)	
1	PT0	R/W	Timer 0 interrupt priority level control (1: high level)	
0	PTA	R/W	Timer A interrupt priority level control (1: high level)	

Table 5-195 IP register

5.11. SPI

A Serial Peripheral Interface (SPI) controller is built in GPM8F3132C family to facilitate communicating with other devices and components. The SPI controller includes four master modes and one slaver mode. There are four control signals on SPI including SPI_CSB, SPI_CLK, SPI_TX, and SPI_RX, these four signals are shared with P3[7:4]. While SPI module is enabled by corresponding control bit, these four pins cannot be GPIOs. In other words, any setting on corresponding GPIO control register will have no effect. The SPI provides following features.

- ❑ Programmable phase and polarity of master clock
- ❑ Programmable master SPI_CLK clock frequency

In master mode, the shifting clock (SPI_CLK) is generated by SPI block. There are two control bits to control the clock phase and polarity. The transmission starts immediately after SPI_START is set(SPI_CTRL[0]=1, Page0 / 0x9A). The SPI shifts the 8-bit data from MSB to LSB through the SPI_TX pin during 8 SPI_CLK cycles. Programmer can read SPI data from SPI_RXD control register. The following four diagrams depict the timing scheme on SPI master mode for different operation types (polarity control bit equals “1” or “0”, phase control bit equals “1” or “0”). The related registers are SPI_CTRL register, SPI_STS register, SPI_TXD register and SPI_RXD registers which are tabled as Table 5-196 to Table 5-199 . Figure 5.11-1 is the block diagram of SPI controller.

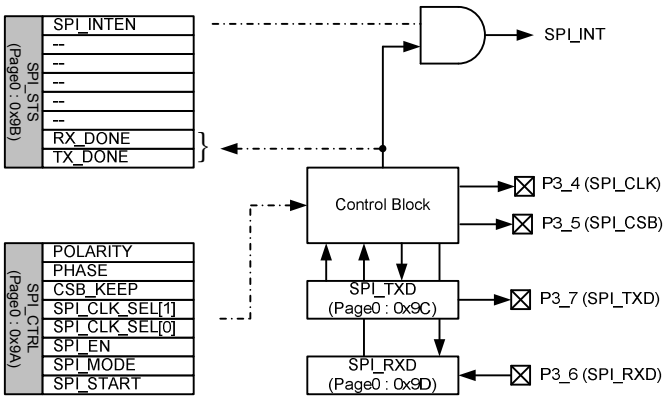


Figure 5.11-1 The block diagram of SPI controller

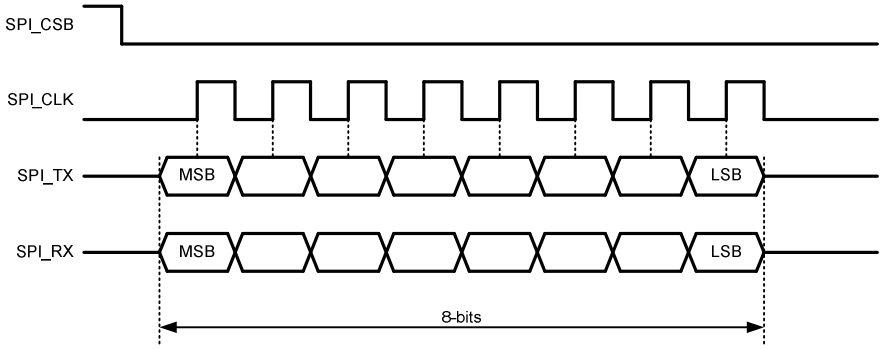


Figure 5.11-2 Master / Slaver Mode, POLARITY=0, PHASE=0

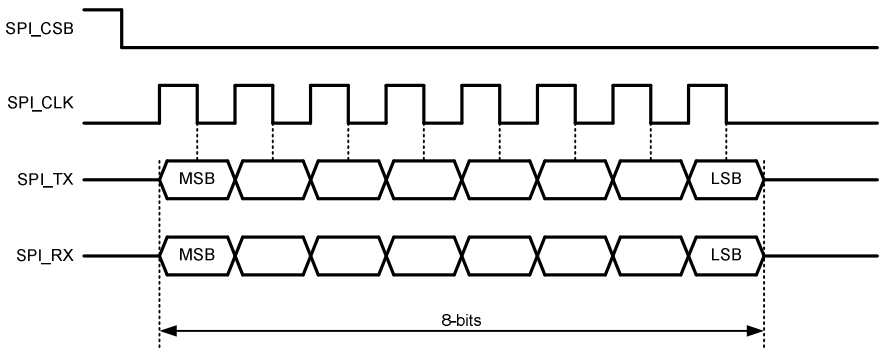


Figure 5.11-3 Master Mode, POLARITY=0, PHASE=1

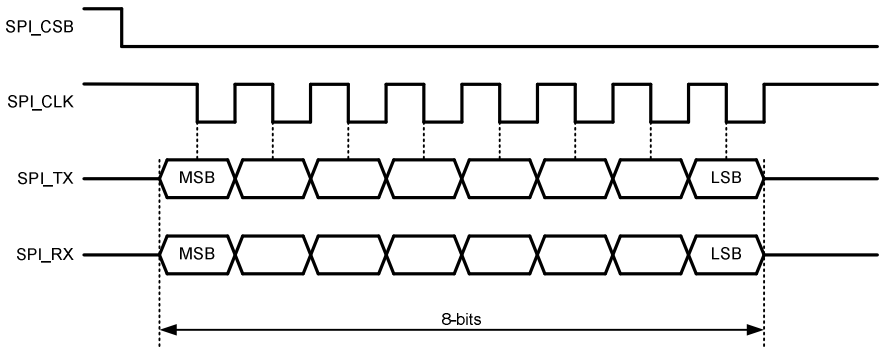


Figure 5.11-4 Master Mode, POLARITY=1, PHASE=0

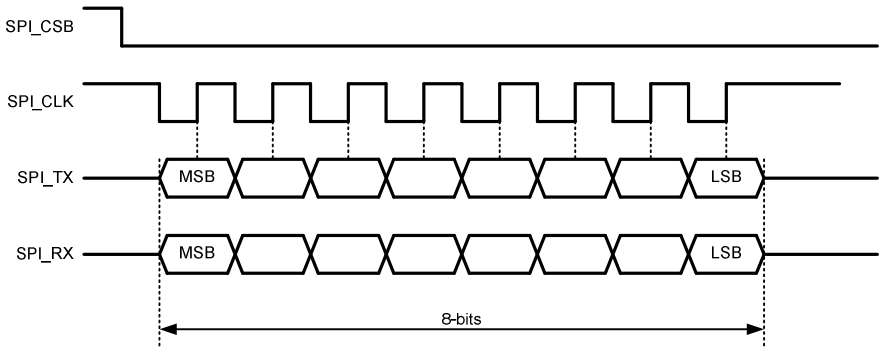


Figure 5.11-5 Master Mode, POLARITY=1, PHASE=1

SPI_CTRL			Page : 0 / Address: 0x9A		SPI Control Register			
Bit	7	6	5	4	3	2	1	0
Function	POLARITY	PHASE	CSB_KEEP	SPI_CLK_SEL[1:0]		SPI_EN	SPI_MODE	SPI_START
Default	0	0	0	0	0	0	0	0
Key Code	FF,00							

Bit	Function	Type	Description	Condition
7	POLARITY	R/W	SPI CLK initial state 0: low state 1: high state	
6	PHASE	R/W	SPI CLK type control 0: 1st edge sample 1: 2nd edge sample	
5	CSB_KEEP	R/W	SPI CSB keep low control	
4:3	SPI_CLK_SEL[1:0]	R/W	SPI Clock output selection: 00: system clock / 2 01: system clock / 4 10: system clock / 8 11: system clock / 16	
2	SPI_EN	R/W	SPI signals forward to P3[7:4] enable P3[4] : SPI_CLK P3[5] : SPI_CSB P3[6] : SPI_RX P3[7] : SPI_TX	
1	SPI_MODE	R/W	SPI operation mode. 0: Master 1:Slaver	
0	SPI_START	R/W	SPI enable(W)/SPI busy flag(R)	

Table 5-196 SYSCON1 register

SPI_STS			Page : 0 / Address: 0x9B		SPI Status Register			
Bit	7	6	5	4	3	2	1	0

Function	SPI_INTEN	--	--	--	--	--	RX_DONE	TX_DONE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SPI_INTEN	R/W	SPI interrupt enable 0 : disable 1 : enable	
6:2	-	R/W	Reserved	
1	RX_DONE	R/W	SPI finished data receiving with slaver mode. read: 0 : Idle / Busy 1 :Done write: 0 : clear this bit 1 : no effect	
0	TX_DONE	R/W	SPI finished data transmission with master mode. 0 : Idle / Busy 1 :Done write: 0 : clear this bit 1 : no effect	

Table 5-197 SPI_STS register

SPI_TXD			Page : 0 / Address: 0x9C		SPI Transmission Data Register			
Bit	7	6	5	4	3	2	1	0
Function	SPI_TXD[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	SPI_TXD[7:0]	R/W	SPI transmission data	

Table 5-198 SPI_TXD register

SPI_RXD			Page : 0 / Address: 0x9D		SPI Receive Data Register			
Bit	7	6	5	4	3	2	1	0
Function	SPI_RXD[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	SPI_RXD	R/W	SPI receive data	

Table 5-199 SPI_RXD register

5.12. ADC

There are two Analog-to-Digital-Converter (ADC) embedded in GPM8F3132C family. It provides general purpose usages such as any other analog functions.

- 8 Channels, 12-bit resolution (11-bit no-missing code) ADC per set
- Supports programming sample hold and ADC clock function

5.12.1. ADC Control

four added five channels of 12-bit SAR ADC per set are built in GPM8F3132C family. They are defined as general-purpose line input P00, P01 … P10. These nine channels are very suitable for system voltage detection and other general-purpose usages. Figure 5.12-1 and Figure 5.12-2 shows the related timing and block diagrams.

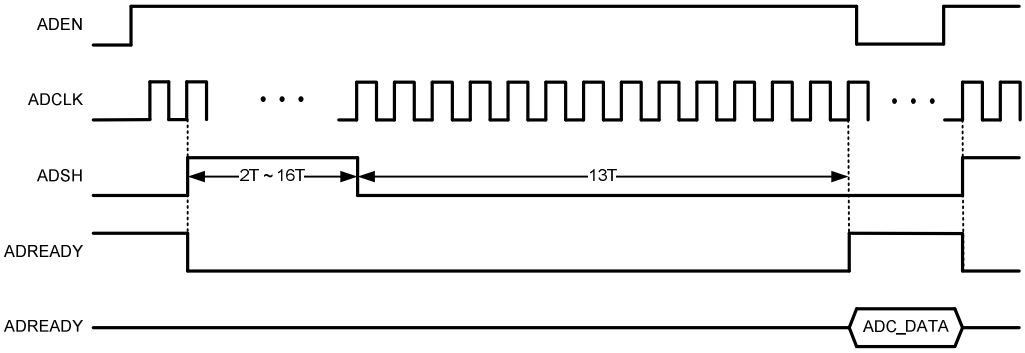


Figure 5.12-1 The timing diagram of ADC control

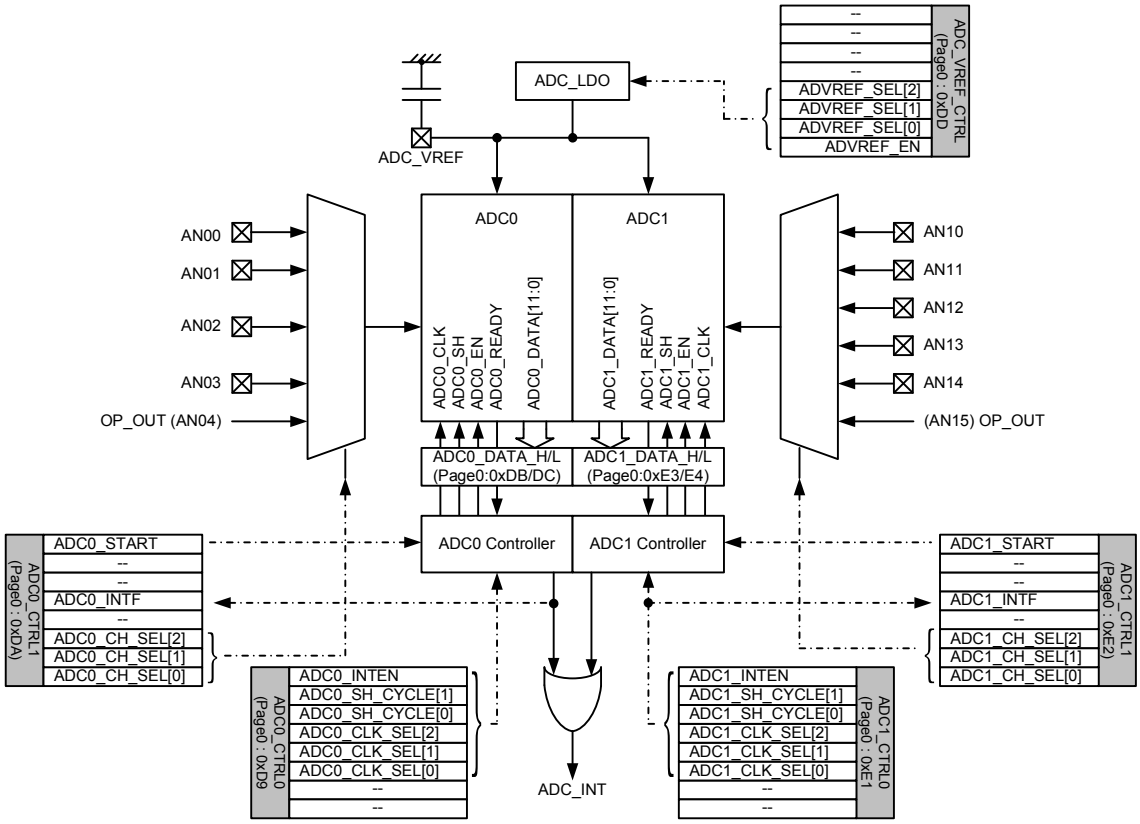


Figure 5.12-2 The block diagram of ADC

ADC Related Register

ADC0_CTRL0			**Page : 0 / Address: 0xD9**		**ADC0 Control 0 Register**			
Bit	7	6	5	4	3	2	1	0
Function	ADC0_INTEN	ADC0_SH_CYCLE[1:0]		ADC0_CLK_SEL[2:0]			--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ADC0_INT_EN	R/W	ADC0 interrupt enable control bit. 0 : disable 1 : enable	
6:5	ADC0_SH_CYCLE	R/W	ADC0 sample and hold cycle selection control bit. ADC0_SH_CYCLE: Cycle (ADC0_CLK) 00: 2 01: 4 10: 8 11: 16	
4:2	ADC0_CLK_SEL	R/W	ADC0 clock selection control bit ADC0_CLK_SEL: ADC0_CLK 000: System clock / 2 001: System clock / 4 010: System clock / 8 011: System clock / 12 100: System clock / 16 101: System clock / 20 110: System clock / 24 111: System clock / 28	
1:0	--	R/W	Reserved	

Table 5-200 ADC0_CTRL0 register

ADC0_CTRL1			**Page : 0 / Address: 0xDA**		**ADC0 Control 1 Register**			
Bit	7	6	5	4	3	2	1	0
Function	ADC0_START	--	--	ADC0_INTF	--	ADC0_CH_SEL[2:0]		
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ADC0_START	R/W	ADC0 start transfer control bit 0: idle 1: start transfer	
6:5	-	R/W	Reserved	
4	ADC0_INTF	R/W	ADC0 interrupt flag. read : 0 : idle / converting 1 : conversion ready write : 0 : clear this bit 1 : no effect	

Bit	Function	Type	Description	Condition
3	--	R/W	Reserved	
2:0	ADC0_CH_SEL	R/W	ADC0 channel selection control bit	

ADC0_CH_SEL	ADC0_Channel
000	ADC0_CH0 (P0[0])
001	ADC0_CH1 (P0[1])
010	ADC0_CH2 (P0[2])
011	ADC0_CH3 (P0[3])
100	OP output (internal pin)
101 ~ 111	Prohibit

Table 5-201 ADC0_CTRL1 register

ADC0_DATA_L			Page : 0 / Address: 0xDB		ADC0 Data Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	ADC0_DATA[3:0]				--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	ADC0_DATA[3:0]	R	ADC0 output data[3:0]	
3:0	-	R/W	Reserved	

Table 5-202 ADC0_DATA_L register

ADC0_DATA_H			Page : 0 / Address: 0xDC		ADC0 Data Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	ADC0_DATA[11:4]							
Default	0	0	0	0				

Bit	Function	Type	Description	Condition
7:0	ADC0_DATA[11:4]	R	ADC0 output data[11:4]	

Table 5-203 ADC0_DATA_H register

ADC_VREF_CTRL			Page : 0 / Address: 0xDD		ADC Reference Voltage Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	ADCVREF_SEL[2:0]			ADC_VREF_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	-	R/W	Reserved	
3:1	ADCVREF_SEL[2:0]	R/W	ADC reference voltage selection control bit	

ADC_VREF_SEL	Voltage
000	1.8V
001	2.0V
010	2.4V
011	2.6V
100	3.0V

Bit	Function	Type	Description	Condition
			101 3.2V 110 3.4V 111 VDD	
0	ADC_VREF_EN	R/W	ADC reference voltage regulator enable 0 : disable 1 : enable	

Table 5-204 ADC_VREF_CTRL register

ADC1_CTRL0			Page : 0 / Address: 0xE1		ADC1 Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	ADC1_INTEN	ADC1_SH_CYCLE[1:0]		ADC1_CLK_SEL[2:0]			--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ADC1_INT_EN	R/W	ADC1 interrupt enable control bit. 0 : disable 1 : enable	
6:5	ADC1_SH_CYCLE	R/W	ADC1 sample and hold cycle selection control bit. ADC1_SH_CYCLE / Cycle (ADC1_CLK) 00 2 01 4 10 8 11 16	
4:2	ADC1_CLK_SEL	R/W	ADC1 clock selection control bit ADC1_CLK_SEL / ADC1_CLK 000 System clock / 2 001 System clock / 4 010 System clock / 8 011 System clock / 12 100 System clock / 16 101 System clock / 20 110 System clock / 24 111 System clock / 28	
1:0	--	R/W	Reserved	

Table 5-205 ADC1_CTRL0 register

ADC1_CTRL1			Page : 0 / Address: 0xE2		ADC1 Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	ADC1_START	--	--	ADC1_INTF	--	ADC1_CH_SEL[2:0]		
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ADC1_START	R/W	ADC1 start transfer control bit 0: idle 1: start transfer	

Bit	Function	Type	Description	Condition
6:5	-	R/W	Reserved	
4	ADC1_INTF	R/W	ADC1 interrupt flag. read : 0 : idle / converting 1 : conversion ready write : 0 : clear this bit 1 : no effect	
3	-	R/W	Reserved	
2:0	ADC1_CH_SEL	R/W	ADC1 channel selection control bit ADC1_CH_SEL | ADC1_Channel 000 | ADC1_CH0 (P0[4]) 001 | ADC1_CH1 (P0[5]) 010 | ADC1_CH2 (P0[6]) 011 | ADC1_CH3 (P0[7]) 100 | ADC1_CH4 (P1[0]) 101 | OP output (internal pin) 110 ~ 111 | Prohibit	

Table 5-206 ADC1_CTRL1 register

ADC1_DATA_L			Page : 0 / Address: 0xE3		ADC1 Data Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	ADC1_DATA[3:0]				--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	ADC1_DATA[3:0]	R	ADC1 output data[3:0]	
3:0	-	R/W	Reserved	

Table 5-207 ADC1_DATA_L register

ADC1_DATA_H			Page : 0 / Address: 0xE4		ADC1 Data Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	ADC1_DATA[11:4]							
Default	0	0	0	0				

Bit	Function	Type	Description	Condition
7:0	ADC1_DATA[11:4]	R	ADC1 output data[11:4]	

Table 5-208 ADC1_DATA_H register

5.13. I2C Unit

An I2C Interface (I2C) is equipped in GPM8F3132C family. Only two wires (SCK and SDA) are needed to implement the protocol. The multi-master I2C-bus controller provides a mechanism to communicate between bus masters and peripheral devices by using two signals, a serial data line (SDA) and a serial clock line (SCK). To avoid all possibilities of confusion, data loss and blockage of information, the master and slave devices must have a defined protocol. In multi-master I2C-bus mode, multiple microprocessors can receive or transmit serial data to or from slave devices. The master that initiates a data transfer over the I2C-bus is responsible for terminating the transfer. It is possible to combine several masters, in addition to several slaves onto an I2C-bus to form a multi-master system. If more than one master simultaneously tries to control the line, an arbitration procedure decides which master gets priority. The maximum number of devices connected to the bus is dictated by the maximum allowable capacitance on the lines, 400 pF, and the protocol's addressing limit of 16K.

5.13.1. I2C Bus Protocol

A Start condition can transfer a one-byte serial data over the SDA line, and a stop condition can terminate the data transfer. A “Start” condition is a high-to-low transition of SDA line while SCK is high. A “Stop” condition is a Low-to-High transition of the SDA line while SCK is high. Start and Stop conditions are always generated by the master. The I2C-bus is busy when a Start condition is generated. A few clocks after a Stop condition, the I2C-bus will be free, again. Figure 5.13-1 shows Start and Stop conditions.

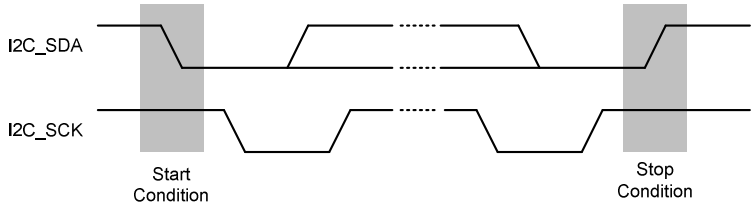


Figure 5.13-1 Start and Stop conditions

When a master initiates a Start condition, it should send a slave address to notify the slave device. The one byte of address field consists of a 7-bit address and a 1-bit transfer direction indicator (that is, writes or read). If bit 8 is 0, it indicates a write operation (transmit operation); if bit 8 is 1, it indicates a request for data read (receive operation). Every byte placed on the SDA line should be eight bits in length. The number of bytes which can be transmitted per transfer is unlimited. The first byte following a Start condition should have the address field. The address field can be transmitted by the master when the I2C-bus is operating in master mode. Each byte should be followed by an acknowledgement (ACK) bit. The MSB bit of the serial data and addresses are always sent first. To finish a one-byte transfer operation completely, the receiver should send an ACK bit to the transmitter. The ACK pulse should occur at the ninth clock of the SCL line. Eight clocks are required for the one-byte data transfer. The master should generate the clock pulse required to transmit the ACK bit. Figure 5.13-2 and Figure 5.13-3 shows the format of I2C master mode with data transmission.

In the master mode, after the data is transferred, the I2C-bus interface will issue an interrupt if interrupt is enabled. After the CPU receives the interrupt request, it should write a new data into I2C_DATA register before clear the interrupt. In the receive mode, after a data is received, the I2C controller will issue an interrupt if interrupt is enabled. After the CPU receives the interrupt request, it should read the data from I2C_DATA before clear the interrupt.

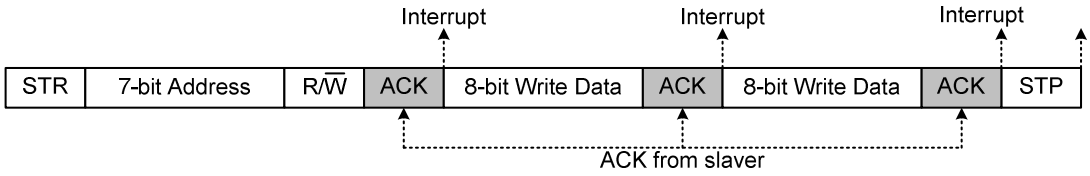


Figure 5.13-2 I2C master mode with data write

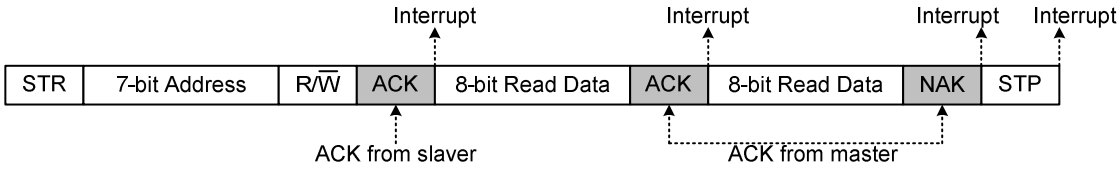


Figure 5.13-3 I2C master mode with data read

Figure 5.13-4 and Figure 5.13-5 shows the format of I2C slaver mode with data transmission.

In the slaver mode, after the data is recovered (which consist of address transfer), the I2C-bus interface will issue an interrupt if interrupt is enabled. After the CPU receives the interrupt request, it should read the data from I2C_DATA before clear the interrupt. During slaver mode data reading, after the CPU receives the interrupt request, I2C controller should write a new data into I2C_DATA register before clear the interrupt.

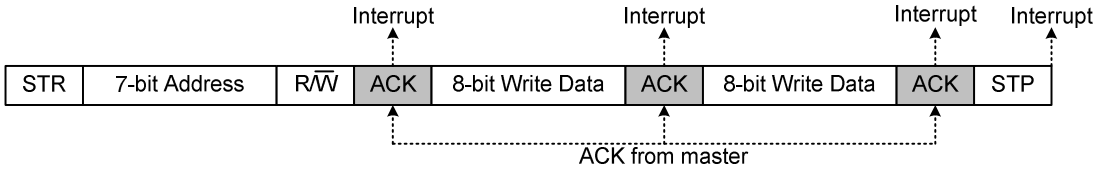


Figure 5.13-4 I2C slaver mode with data write

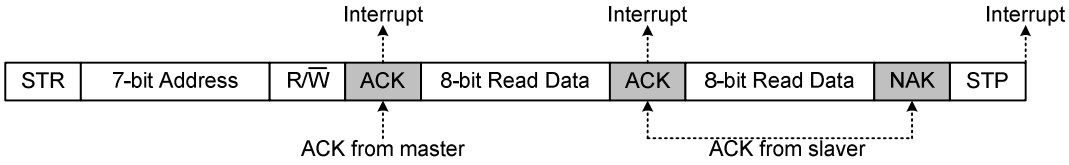


Figure 5.13-5 I2C slaver mode with data read

I2C Related Register

I2C_DEBOUNCE			Page : 0 / Address: 0xCF		I2C De-bounce Count Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	I2C_DB_CNT[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	I2C_DEBOUNCE	R/W	I2C input SCL and SDA de-bounce count.	

Table 5-209 I2C_DEBOUNCE register

I2C_CTRL			Page : 0 / Address: 0xD1		I2C Control Register			
Bit	7	6	5	4	3	2	1	0
Function	MST_STR	MST_STP	MST_NACK	MODE	I2C_CLK_SEL[1:0]		I2C_TRIGGER	I2C_EN
Default	0	0	1	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	MST_STR	R/W	I2C issue start command with divice address enable bit.	

Bit	Function	Type	Description	Condition
			This bit will be auto cleared by hardware when this transfer is finished. 0 : disable 1 : enable	
6	MST_STP	R/W	I2C issue stop command enable bit. This bit will be auto cleared by hardware when this transfer is finished. 0 : disable 1 : enable	
5	MST_NACK	R/W	I2C issue non-acknowledge enable bit. This bit will be auto cleared by hardware when this transfer is finished. 0 : master respond acknowledge 1 : master respond non-acknowledge	
4	MODE	R/W	I2C operating mode selection control bit. 0: master 1: slaver	
3:2	I2C_CLK_SEL[1:0]	R/W	I2C clock selection control bit 00 : I2C clock is system clock / 128 01 : I2C clock is system clock / 256 10 : I2C clock is system clock / 768 11 : I2C clock is system clock / 1024	
1	I2C_TRIGGER	R/W	I2C start transmission trigger bit. This bit is for master mode only. The I2C master will begin to transmit or receive data when I2C_EN is set to 1. After data transmitted this bit will be cleared by H/W automatically. 0 : disable 1 : enable	
0	I2C_EN	R/W	I2C enable control bit. 0 : disable 1 : enable	

Table 5-210 I2C_CTRL register

I2C_STS			Page : 0 / Address: 0xD2		I2C Status Register			
Bit	7	6	5	4	3	2	1	0
Function	SLV_DID_OK	SLV_DAT_OK	SLV_STP_OK	ERR_SDID_IE	--	I2C_INT_EN	NO_ACK	TRS _DONE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SLV_DID_OK	R/W	This bit indicates device ID was received by i2c controller. This is for slaver mode only. read: 0 : device ID is not asserted 1 : device ID is asserted write: 0 : clear this bit 1 : on effect	
6	SLV_DAT_OK	R/W	This bit indicates data was received or transmitted by i2c controller. This is for slaver mode only.	

Bit	Function	Type	Description	Condition
			read: 0 : data is transmitting or idle now 1 : data is transmission complete write: 0 : clear this bit 1 : on effect	
5	SLV_STP_OK	R/W	This bit indicates stop command was received by i2c controller. This is for slaver mode only. read: 0 : stop command is not assert 1 : stop command is asserted write: 0 : clear this bit 1 : on effect	
4	ERR_SDID_IE	R/W	Device ID error interrupt enable of slaver mode. 0 : disable 1 : enable	
3	--	R/W	Reserved	
2	I2C_INT_EN	R/W	I2C interrupt enable control bit. 0 : disable 1 : enable	
1	NO_ACK	R/W	I2C not have received acknowledging signal. read : 0 : acknowledge 1 : no acknowledge write : 0 : clear this bit 1 : on effect	
0	TRS_DONE	R	I2C transmission complete flag. read: 0 : i2c is idle or on going 1 : i2c is finished data transmission write: 0 : clear this bit 1 : on effect	

Table 5-211 I2C_STS register

I2C_DID			Page : 0 / Address: 0xD3		I2C Device ID Register			
Bit	7	6	5	4	3	2	1	0
Function	DEV_ID							R_W
Default	0	0	0	0	0	0	0	1

Bit	Function	Type	Description	Condition
7:1	DEV_ID[6:0]	R/W	I2C device ID register. In master mode, device ID is used to inform which slaver will be connected. In slaver mode, this is used to identify the received ID which is sanded from	

Bit	Function	Type	Description	Condition
			external maser controller.	
0	R_W	R/W	I2C read / write control signal, this register is shared between master and slaver mode.	

Table 5-212 I2C_DID register

I2C_DATA			Page : 0 / Address: 0xD4		I2C Data Register			
Bit	7	6	5	4	3	2	1	0
Function	I2C_DATA[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	I2C_DATA	R/W	I2C read / write Data Register. This register is shared between master and slaver mode.	

Table 5-213 I2C_DATA register

5.14. MDU Unit

The GPM8F3132C family has embedded a MDU controller. That supports sign operation with 16X16 multiplier, 32/16 divider, 16+16 adder, 16-16 subtractor and 32-bit shift. Before operating, user store variables into internal data memory and write related address in MDU_DSRC_ADDR0 / MDU_DSRC_ADDR1 register. Next, user must write the target address in MDU_DTAR_ADDR in order to index the storage address for saving calculation result. Then, set MDU mode and enable MDU. Hardware need some time to finish the calculating (MUL=17T / DIV=33T / ADD=2T / SUB=2T / SFT=2T ; they are not involve DMA transmission time). A special case is shifter mode. User just needs to set a DMA address (MDU_DSRC_ADDR0) only. Others setting are same as aforementioned. In addition, user can mix shift function during multiplier, divider, adder and sutractor mode. The calculating result will be shift n-bit if A_SHIFT_BIT is not equal to zero. Figure 5-60 is the block diagram of MDU controller.

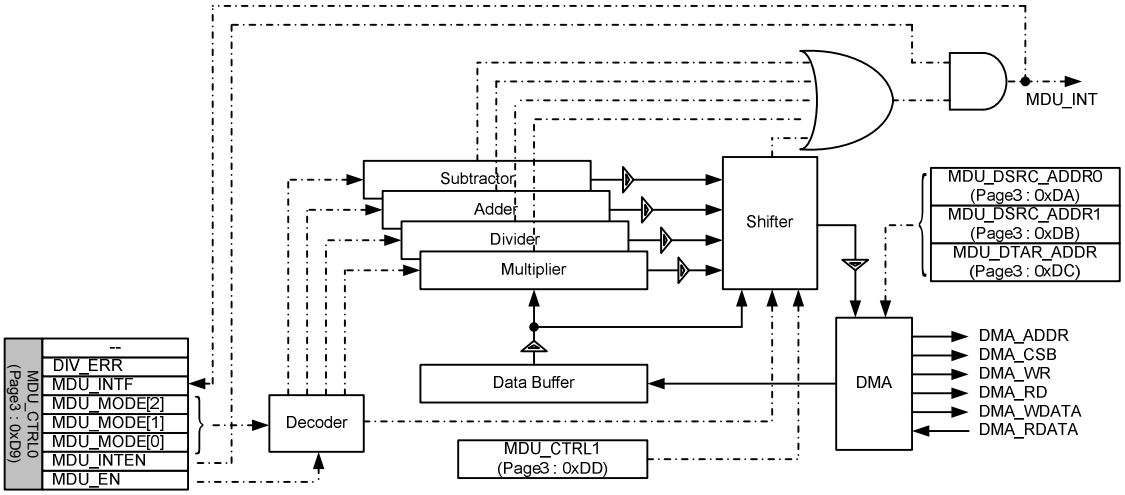


Figure 5.14-1 The block diagram of MDU controller

MDU Related Register

MDU_CTRL0			Page : 3 / Address: 0xD9		MDU Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	DIV_ERR	MDU_INTF	MDU_MODE[2:0]			MDU_INTEN	MDU_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	DIV_ERR	R	Divisor error flag. read : 0 : divisor is a suitable value (non-zero). 1 : divisor is a unsuitable value (zero). This flag will be cleared automatic when divisor is updated to non-zero value.	
5	MDU_INTF	R/W	MDU interrupts flag. read : 0 : idle / busy 1 : MDU interrupt trigger write : 0 : clear this bit 1 : no effect	
4:2	MDU_MODE	R/W	MDU operating mode	

Bit	Function	Type	Description	Condition
			MDU_MODE[2:0] Mode 000 Multiplier 001 Divider with remainder 010 Divider without remainder 011 Adder 100 Subtractor 101 Arithmetic shift 110 Prohibit 111 Prohibit	
1	MDU_INTEN	R/W	MDU interrupt enable control bit. 0 : disable 1 : enable	
0	MDU_EN	R/W	MDU enable control bit. 0 : disable 1 : enable	

Table 5-214 MDU_CTRL0 register

MDU_DSRC_ADR0			Page : 3 / Address: 0xDA		MDU DMA Source Address 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	MDU_DSRC_ADR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	MDU_DSRC_ADR0	R/W	MDU DMA source address register. These address cover all-off internal data memory only. The arrangement of internal content as table 5-216.	

Table 5-215 MDU_DSRC_ADR0 register

MDU_DSRC_ADR0	Multiplicand	Dividend	Adder	Subtracter	Shifter
ADDR	Multiplicant[15 : 8]	Dividend[31 : 24]	Augend[15 : 8]	Minuend[15 : 8]	Shift data[31 : 24]
ADDR+1	Multiplicant[7 : 0]	Dividend[23 : 16]	Augend[7 : 0]	Minuend[7 : 0]	Shift data[23 : 16]
ADDR+2	-	Dividend[15 : 8]			Shift data[15 : 8]
ADDR+3	-	Dividend[7 : 0]			Shift data[7 : 0]

Table 5-216 The arrangement of MDU DMA source address0

MDU_DSRC_ADR1			Page : 3 / Address: 0xDB		MDU DMA Source Address 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	MDU_DSRC_ADR1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	MDU_DSRC_ADR1	R/W	MDU DMA source address register. These address cover all-off internal data memory only. The arrangement of internal content as table 5-218.	

Table 5-217 MDU_DSRC_ADR1 register

MDU_DSRC_ADR1	Multiplier	Divisor	Adder	Subtracter
ADDR	Multiplier[15 : 8]	Divisor [15 : 8]	Addend[15 : 8]	Subtrahend[15 : 8]
ADDR+1	Multiplier[7 : 0]	Divisor [7 : 0]	Addend[7 : 0]	Subtrahend[7 : 0]

Table 5-218 The arrangement of MDU DMA source address1

MDU_DTAR_ADDR			**Page : 3 / Address: 0xDC**		**MDU DMA Target Address Register**			
Bit	7	6	5	4	3	2	1	0
Function	MDU_DTAR_ADDR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	MDU_DTAR_ADDR	R/W	MDU DMA target address register. These address cover all-off internal data memory only. The arrangement of internal content as table 5-220.	

Table 5-219 MDU_DTAR_ADDR register

MDU_DTAR_ADDR	Multipilier	Divider	Adder	Subtracter	Shifter
ADDR	Product[31: 24]	Quotient[31 : 24]	Summation[31 : 24]	Summation[31 : 24]	Shift Result[31 : 24]
ADDR+1	Product[23 : 16]	Quotient[23 : 16]	Summation[23 : 16]	Summation[23 : 16]	Shift Result[23 : 16]
ADDR+2	Product[15 : 8]	Quotient[15 : 8]	Summation[15 : 8]	Summation[15 : 8]	Shift Result[15 : 8]
ADDR+3	Product[7 : 0]	Quotient[7 : 0]	Summation[7 : 0]	Summation[7 : 0]	Shift Result[7 : 0]
ADDR+4	-	Remainder[15 : 8]			
ADDR+5	-	Remainder[7 : 0]			

Table 5-220 The arrangement of MDU DMA target address

MDU_CTRL1			**Page : 3 / Address: 0xDD**		**MDU Control 1 Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	SFT_R_L	A_SHIFT_BIT[4:0]				
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	SFT_R_L	T	MDU left , right shift indication. 0 : right shift 1 : left shift	
4:0	A_SHIFT_BIT[4:0]	R/W	MDU arithmetic shift bit select signal	

A_SHIFT_BIT[4:0]	Shift Bit
0_0000	0-bit
0_0001	1-bit
0_0010	2-bit
0_0011	3-bit
0_0100	4-bit
0_0101	5-bit

Bit	Function	Type	Description		Condition
			0_0110	6-bit	
			0_0111	7-bit	
			0_1000	8-bit	
			0_1001	9-bit	
			0_1010	10-bit	
			0_1011	11-bit	
			0_1100	12-bit	
			0_1101	13-bit	
			0_1110	14-bit	
			0_1111	15-bit	
			1_0000	16-bit	
			1_0001	17-bit	
			1_0010	18-bit	
			1_0011	19-bit	
			1_0100	20-bit	
			1_0101	21-bit	
			1_0110	22-bit	
			1_0111	23-bit	
			1_1000	24-bit	
			1_1001	25-bit	
			1_1010	26-bit	
			1_1011	27-bit	
			1_1100	28-bit	
			1_1101	29-bit	
			1_1110	30-bit	
			1_1111	31-bit	

Table 5-221 MDU_CTRL1 register

P4			Address: 0xC0		Port4 Register			
Bit	7	6	5	4	3	2	1	0
Function	MDU_INTF	--	--	--	--	P42	P41	P40
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Function	Type	Description	Condition
7	MDU_INTF	R	MDU interrupt flag. 0 : idle / busy 1 : MDU interrupt trigger	
6:3	--	R/W	Reserved	
2:0	P4[2:0]	R/W	P4 is used to set IO output data only. Otherwise, that also can be used to configure the Port4 function.	

Table 5-222 P4 register

5.15. Operating Amplifier Unit

The GPM8F3132C family has embedded an operating amplifier and two comparators. The related control register are listed in table 5-223 and table 5-226. These input and output signal are connected to I/O PAD directly. So, user has most flexible in application. Figure 5.15-1 is the block diagram of OP. Figure 5.15-2 is the block diagram of comparators.

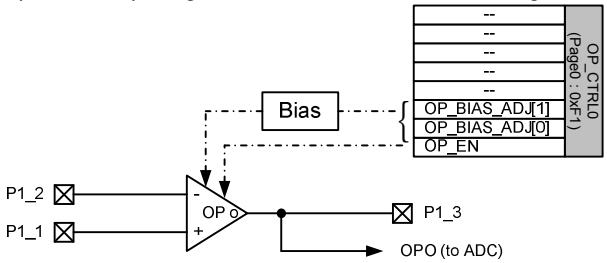


Figure 5.15-1 The block diagram of OP

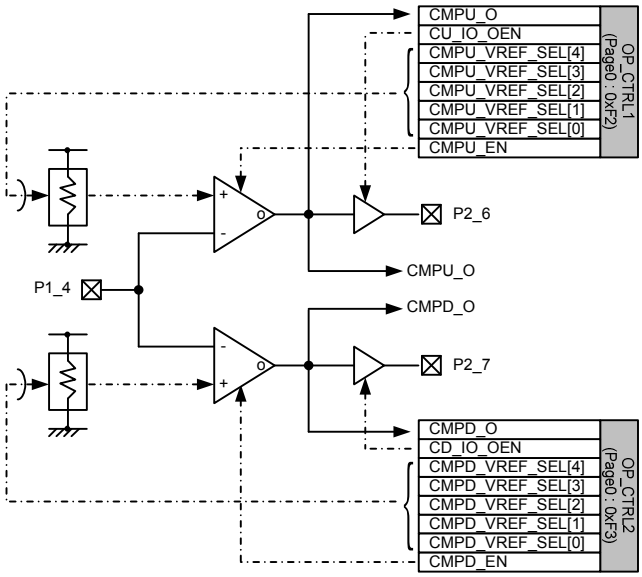


Figure 5.15-2 The block diagram of comparators

OPs Related Register

OP_CTRL0			Page : 0 / Address: 0xF1		Operating Amplifier Control Register - 0			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	OP_BIAS_ADJ[1:0]		OP_EN
Default	0	0	0	0	0		0	0

Bit	Function	Type	Description	Condition
7:3	-	R/W	Reserved	
2:1	OP_BIAS_ADJ	R/W	OP input bias current adjustment bit. 00: Bias Current 5uA 01: Bias Current 15uA 10: Bias Current 25uA 11: Bias Current 35uA	
0	OP_EN	R/W	OP enable control signal	

Bit	Function	Type	Description	Condition
			0 : disable 1 : enable	

Table 5-223 OP_CTRL0 register

OP_CTRL1			Page : 0 / Address: 0xF2		Operating Amplifier Control Register - 1			
Bit	7	6	5	4	3	2	1	0
Function	CMPU_O	CU_IO_OEN	CMPU_VREF_SEL					CMPU_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CMPU_O	R	Up-side comparator output signal without filter 0 : V_{CMP_I} > VREF_U 1 : V_{CMP_I} < VREF_U	
6	CU_IO_OEN	RW	Up-side comparator output to I/O enable 0 : disable 1 : enable	
5:1	CMPU_VREF_SEL	R/W	Up-side comparator reference voltage select signal. The mapping table shown as table 5-226	
0	CMPU_EN	R/W	Up side comparator enable signal 0 : disable 1 : enable	

Table 5-224 OP_CTRL1 register

OP_CTRL2			Page : 0 / Address: 0xF3		Operating Amplifier Control Register - 2			
Bit	7	6	5	4	3	2	1	0
Function	CMPD_O	CD_IO_OEN	CMPD_VREF_SEL					CMPD_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CMPD_O	R	Down-side comparator output signal without filter 0 : V_{CMP_I} > VREF_D 1 : V_{CMP_I} < VREF_D	
6	CD_IO_OEN	RW	Down-side comparator output to I/O enable 0 : disable 1 : enable	
5:1	CMPD_VREF_SEL	R/W	Down-side comparator reference voltage select signal. The mapping table shown as table 226.	
0	CMPD_EN	R/W	Down side comparator enable signal 0 : disable 1 : enable	

Table 5-225 OP_CTRL2 register

VREF_SEL_U / VREF_SEL_D	Vref Voltage	VREF_SEL_U / VREF_SEL_D	Vref Voltage
0_0000	V50_ADC * (0/32)	1_0000	V50_ADC * (16/32)
0_0001	V50_ADC * (1/32)	1_0001	V50_ADC * (17/32)
0_0010	V50_ADC * (2/32)	1_0010	V50_ADC * (18/32)
0_0011	V50_ADC * (3/32)	1_0011	V50_ADC * (19/32)
0_0100	V50_ADC * (4/32)	1_0100	V50_ADC * (20/32)
0_0101	V50_ADC * (5/32)	1_0101	V50_ADC * (21/32)
0_0110	V50_ADC * (6/32)	1_0110	V50_ADC * (22/32)
0_0111	V50_ADC * (7/32)	1_0111	V50_ADC * (23/32)
0_1000	V50_ADC * (8/32)	1_1000	V50_ADC * (24/32)
0_1001	V50_ADC * (9/32)	1_1001	V50_ADC * (25/32)
0_1010	V50_ADC * (10/32)	1_1010	V50_ADC * (26/32)
0_1011	V50_ADC * (11/32)	1_1011	V50_ADC * (27/32)
0_1100	V50_ADC * (12/32)	1_1100	V50_ADC * (28/32)
0_1101	V50_ADC * (13/32)	1_1101	V50_ADC * (29/32)
0_1110	V50_ADC * (14/32)	1_1110	V50_ADC * (30/32)
0_1111	V50_ADC * (15/32)	1_1111	V50_ADC * (31/32)

Table 5-226 The comparator reference voltage mapping table

5.16. Alphabetical List of Instruction Set

5.16.1. Arithmetic Operations

Mnemonic	Description	Code	Bytes	Cycles
ADD A,Rn	Add register to accumulator	0x28-0x2F	1	1
ADD A,direct	Add direct byte to accumulator	0x25	2	2
ADD A,@Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A,#data	Add immediate data to accumulator	0x24	2	2
ADDC A,Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A,direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A,#data	Add immediate data to A with carry flag	0x34	2	2
SUBB A,Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A,direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A,@Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A,#data	Subtract immediate data from A with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	2
INC direct	Increment direct byte	0x05	2	3
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	2
DEC direct	Decrement direct byte	0x15	1	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	2	3
INC DPTR	Increment data pointer	0xA3	1	1
MUL A,B	Multiply A and B	0xA4	1	2
DIV A,B	Divide A by B	0x84	1	6
DA A	Decimal adjust accumulator	0xD4	1	3

5.16.2. Logic Operations

Mnemonic	Description	Code	Bytes	Cycles
ANL A,Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A,direct	AND direct byte to accumulator	0x55	2	2
ANL A,@Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A,#data	AND immediate data to accumulator	0x54	2	2
ANL direct,A	AND accumulator to direct byte	0x52	2	3
ANL direct,#data	AND immediate data to direct byte	0x53	3	3
ORL A,Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A,direct	OR direct byte to accumulator	0x45	2	2
ORL A,@Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A,#data	OR immediate data to accumulator	0x44	2	2
ORL direct,A	OR accumulator to direct byte	0x42	2	3
ORL direct,#data	OR immediate data to direct byte	0x43	3	3
XRL A,Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	0x65	2	2

Mnemonic	Description	Code	Bytes	Cycles
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A,#data	Exclusive OR immediate data to accumulator	0x64	2	2
XRL direct,A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct,#data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	1

5.16.3. Boolean Operations

Mnemonic	Description	Code	Bytes	Cycles
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C,bit	AND direct bit to carry flag	0x82	2	2
ANL C,/bit	AND complement of direct bit to carry	0xB0	2	2
ORL C,bit	OR direct bit to carry flag	0x72	2	2
ORL C,/bit	OR complement of direct bit to carry	0xA0	2	2
MOV C,bit	Move direct bit to carry flag	0xA2	2	2
MOV bit,C	Move carry flag to direct bit	0x92	2	3

5.16.4. Data Transfers

Mnemonic	Description	Code	Bytes	Cycles
MOV A,Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A,direct	Move direct byte to accumulator	0xE5	2	2
MOV A,@Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV A,#data	Move immediate data to accumulator	0x74	2	2
MOV Rn,A	Move accumulator to register	0xF8-0xFF	1	1
MOV Rn,direct	Move direct byte to register	0xA8-0xAF	2	3
MOV Rn,#data	Move immediate data to register	0x78-0x7F	2	2
MOV direct,A	Move accumulator to direct byte	0xF5	2	2
MOV direct,Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1,direct2	Move direct byte to direct byte	0x85	3	3
MOV direct,@Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct,#data	Move immediate data to direct byte	0x75	3	3
MOV @Ri,A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri,direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV @Ri,#data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV DPTR,#data16	Load 16-bit constant into active DPH and DPL in LARGE mode	0x90	3	3

Mnemonic	Description			Code	Bytes	Cycles
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator			0x93	1	5
MOVC A,@A+PC	Move code byte relative to PC to accumulator			0x83	1	4
MOVX A,@Ri	Move external RAM (8-bit address) to A		XDM	0xE2-0xE3	1	3*
			SXDM			3
MOVX A,@DPTR	Move external RAM (16-bit address) to A		XDM	0xE0	1	2*
			SXDM			2
MOVX @Ri,A	Move A to external XDM (8-bit address)	ODE inside ROM/RAM		0xF2-0xF3	1	4*
		Other cases				5*
	Move A to external SXDM (8-bit address)	All cases				3
MOVX @DPTR,A	Move A to external XDM (16-bit address)	CODE inside ROM/RAM		0xF0	1	3*
		Other cases				4*
	Move A to external SXDM (16-bit address)	All cases				2
PUSH direct	Push direct byte onto IDM stack			0xC0	2	3
POP direct	Pop direct byte from IDM stack			0xD0	2	2
XCH A,Rn	Exchange register with accumulator			0xC8-0xCF	1	2
XCH A,direct	Exchange direct byte with accumulator			0xC5	2	3
XCH A,@Ri	Exchange indirect RAM with accumulator			0xC6-0xC7	1	3
XCHD A,@Ri	Exchange low-order nibble indirect RAM with A			0xD6-0xD7	1	3

5.16.5. Program Branches

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	0x11-0xF1	2	4
LCALL addr16	Long subroutine call	0x12	3	4
RET	Return from subroutine	0x22	1	4
RETI	Return from interrupt	0x32	1	4
AJMP addr11	Absolute jump	0x01-0xE1	2	3
LJMP addr16	Long jump	0x02	3	4
SJMP rel	Short jump (relative address)	0x80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	0x73	1	5
JZ rel	Jump if accumulator is zero	0x60	2	4
JNZ rel	Jump if accumulator is not zero	0x70	2	4
JC rel	Jump if carry flag is set	0x40	2	3
JNC	Jump if carry flag is not set	0x50	2	3
JB bit,rel	Jump if direct bit is set	0x20	3	5
JNB bit,rel	Jump if direct bit is not set	0x30	3	5
JBC bit,direct rel	Jump if direct bit is set and clear bit	0x10	3	5
CJNE A,direct rel	Compare direct byte to A and jump if not equal	0xB5	3	5
CJNE A,#data rel	Compare immediate to A and jump if not equal	0xB4	3	4
CJNE Rn,#data rel	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4
CJNE @Ri,#data rel	Compare immediate to ind. and jump if not equal	0xB6-0xB7	3	5
DJNZ Rn,rel	Decrement register and jump if not zero	0xD8-0xDF	2	4
DJNZ direct,rel	Decrement direct byte and jump if not zero	0xD5	3	5
NOP	No operation	0x00	1	1

6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3V ~ 6.0V
Input Voltage Range	V_{IN}	-0.3V to V_+ + 0.3V
Operating Temperature	T_A	-40℃ to +85℃
VDD Total MAX Current	I_{VDDM}	30mA
VSS Total MAX Current	I_{VSSM}	30mA

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
IOSC Frequency	F_{OSC}	8.533×(1-2%)	8.533	8.533×(1+2%)	MHz	±2% at 2.4V~5.5V
PLL Frequency	F_{PLL}	48.0×(1-2%)	48.0	48.0×(1+2%)	MHz	±2% at 2.4V~5.5V

6.3. DC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	V_{LVR}	-	5.5	V	
Operating Current	I_{OP}	-	-	19.0	mA	SYSCLK= 64MHz @ 5.0V, no load
Standby Current	I_{STBY}	-	-	10.0	uA	VDD = 5.5V
Input High Level	V_{IH}	0.7*VDD	-	-	V	VDD = 5.0V(with Schmitt trigger)
Input Low Level	V_{IL}	-	-	0.3*VDD	V	VDD = 5.0V(with Schmitt trigger)
Output High Level	V_{OH}	0.8*VDD	-	-	V	I_{OH} = -8mA at VDD = 5.0V
Output Low Level	V_{OL}	-	-	0.2*VDD	V	I_{OL} = 20mA at VDD = 5.0V
Input Pull High Resistor 1	R_{PH1}	30	50	70	KΩ	VDD = 5.0V
Input Pull High Resistor 1	R_{PL1}	30	50	70	KΩ	VDD = 5.0V
Low Voltage Reset 1	V_{LVR1}	1.9×(1-5%)	2.2	1.9×(1+5%)	V	SYS_CTRL3[2:1]=10
Low Voltage Reset 2	V_{LVR2}	2.4×(1-5%)	2.4	2.4×(1+5%)	V	SYS_CTRL3[2:1]=11
Low Voltage Reset 3	V_{LVR3}	3.2×(1-5%)	3.2	3.2×(1+5%)	V	SYS_CTRL3[2:1]=00
Low Voltage Reset 4	V_{LVR4}	4.2×(1-5%)	4.2	4.2×(1+5%)	V	SYS_CTRL3[2:1]=01

6.4. ADC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	V_{LVR}	-	5.5	V	
ADC Input Voltage Range	V_{ADCIN}	0	-	VDD	V	
ADC Clock Period	T_{AD}	-	-	-	us	Depended on system clock
Input Channel		-	-	16	channel	
Resolution		12			Bit	
No Missing Code		10			bits	
ADC Conversion Time	T_{CON}	-	-	-	us	ADCLK * 15

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Integral Linearity Error	E_{INL}	-	±2	±3	LSB	
Differential Linearity Error	E_{DNL}	-	-1~+2	-1~+3	LSB	

6.5. OP Characteristics (T_A = 25℃)

6.5.1 OP

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	V_{LVR}	-	5.5	V	
OP Input Offset	V_{in_op}	-	10	-	mV	VDD=5.0V

6.6. Comparators Characteristics (T_A = 25℃)

6.5.1 CMPU / CMPD

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	V_{LVR}	-	5.5	V	VDD=5.0V

7. PACKAGE INFORMATION

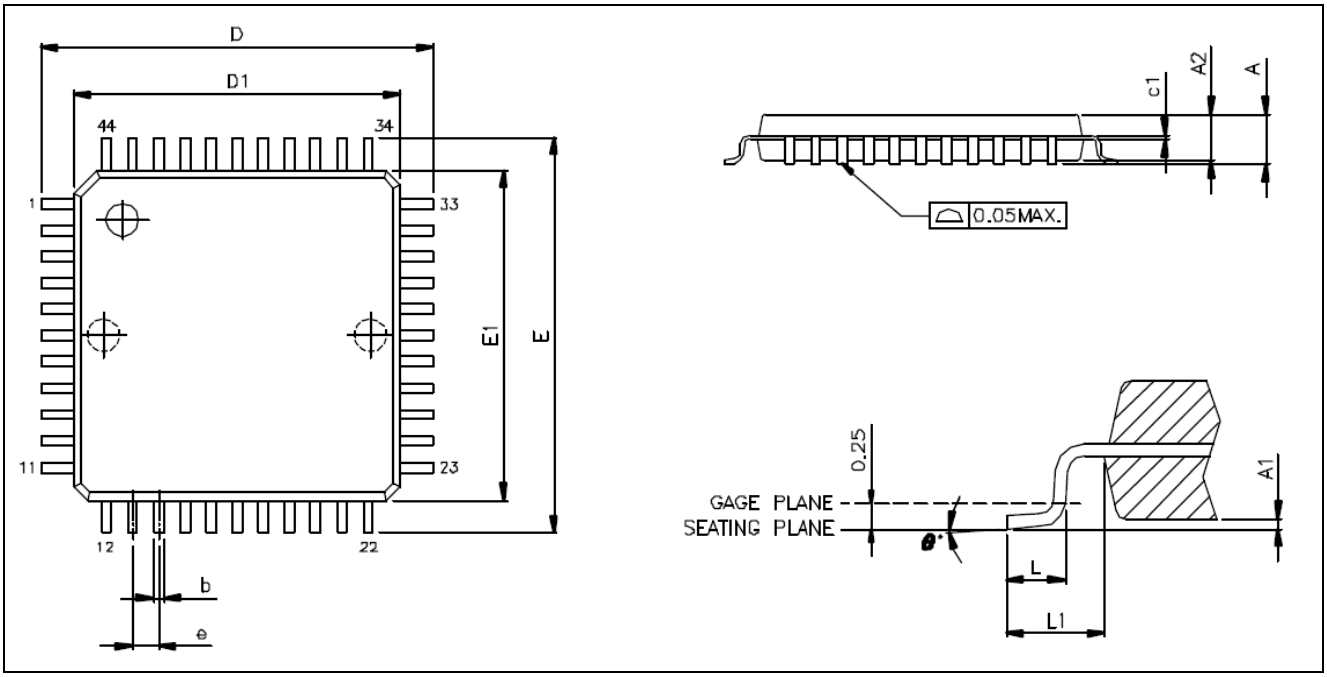
7.1. Ordering Information

Product Number	Package Type
GPM8F3132C – QL01x	Halogen Free Package
GPM8F3132C-QV043	Halogen Free Package

Note1: Package form number (x = 1 - 9, serial number).

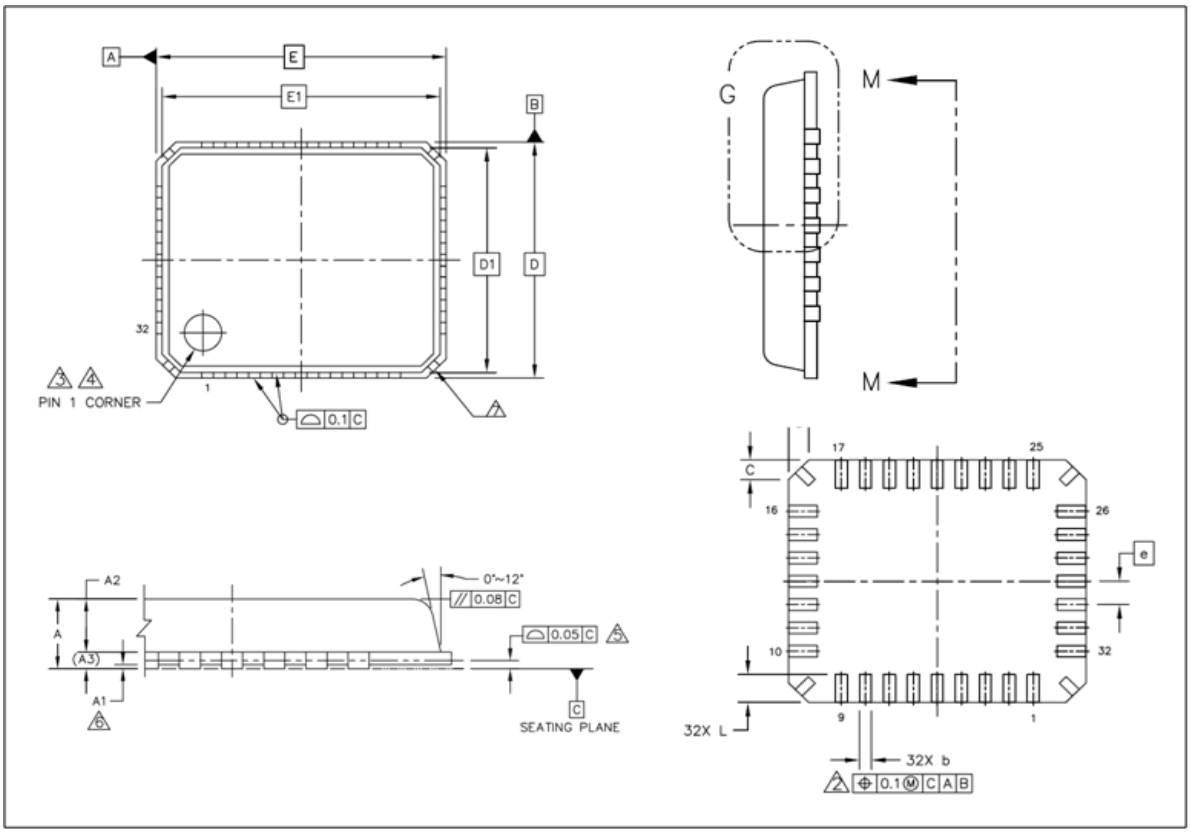
7.2. Package Information

7.2.1. LQFP 44



Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
c1	0.09	-	0.16
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
e		0.80 BSC	
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1		1.00 REF	
θ °	0 °	3.5 °	7 °

7.2.2. QFN32



Symbol	Millimeter		
	Min.	Nom.	Max.
A	0.8	-	0.9
A1	0	0.02	0.05
A2	0.65	-	0.69
A3		0.203 REF.	
b	0.18	0.25	0.3
C	0.24	0.42	0.6
D		5.2 BSC	
D1		4.95 BSC	
E		6.2 BSC	
E1		5.95 BSC	
e		0.5 BSC	
L	0.5	0.6	0.7

Note:

1. DIE THICKNESS ALLLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)

2 DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BE TWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.

3 THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.

4 EXACT SHARE AND SIZE OF THIS FEATURE IS OPTIONAL

5 APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING

6 APPLIED ONLY TO TERMINALS.

7 EXACT SHAPE OF EACH CORNER IS OPTIONAL

8.DISCLAIMER

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9. REVISION HISTORY

Date	Revision #	Description	Page
Mar. 16, 2015	0.1	Original	146
May.11.2016	0.2	Add GPM8F3132C-QV043 pin description and map . Add GPM8F3132C-QV043 program memory allocation description	9,11 14