DATA SHEET

GPM8F3232A
GPM8F3216A
GPM8F3208A

44/28/24 Pin 8-bit Microcontroller with 32/16/8KB Flash

Preliminary

AUG. 03, 2012

Version 0.1

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44/28/24 PIN 8-BIT MICROCONTROLLER WITH 32/16/8KB FLASH

1. GENERAL DESCRIPTION

The GPM8F3232A/3216A/3208A is a highly integrated microcontroller which integrates a pipelined 1T 8051 CPU, 1K/512/256-byte XRAM, 256-byte IDM SRAM and 32/16/8K-byte program Flash. It includes 34/24/20 programmable multi-functional I/Os, Timer0/1/2, UART0, SPI (master), built-in OP, audio and one up to 8-channel of 12-bit ADC for general-purpose application. It operates over a wide voltage range of 2.4V - 5.5V with different clock sources. It has two modes in power management unit. Moreover, there is one on-chip debug circuit with two pins to facilitate full speed in-system debug. The detail is described in the following sections.

2. FEATURES

- **CPU**
  - High speed, high performance 1T 8051
    - 100% software compatible with industry standard 8051
    - Pipeline RISC architecture enables to execute instructions 10 times faster than standard 8051
    - Up to 24.5MHz clock operation
- **Memories**
  - 1K/512/256 bytes XRAM
  - 256 bytes internal Data Memory (IDM) SRAM
  - 32/16/8K bytes Flash with high endurance
    - Minimum 200,000 program/erase cycles
    - Minimum 20 years data retention
  - Programming read only level for software security
- **Clock Management**
  - Internal oscillator: 24.5MHz±2% @ 2.4V~5.5V
  - External clock input max 24.5MHz
  - Crystal input with 32768Hz or 1MHz~25MHz
- **Power Management**
  - 1 STOP mode for power saving
  - 1 IDLE mode for only peripheral operation
- **Interrupt Management**
  - 14 interrupt sources(GPM8F3232A/3216A)
  - Up to 6 external interrupt sources(GPM8F3232A/3216A)
  - 12 interrupt sources(GPM8F3208A)
  - Up to 4 external interrupt sources(GPM8F3208A)
- **Reset Management**
  - Power On Reset (POR)
  - Low Voltage Reset (LVR)
  - Pad Reset (PAD_RST)
  - Watchdog Reset (WDT_RST)
  - Software Reset (S/W_RST)
  - Stop mode Reset (STOP_RST)
  - Miss Clock Reset (MISS_CLK_RST)
  - Flash Related Error Reset (FLASH_ERR_RST)
- **Programmable Watchdog Timer**
  - A time-base generator
  - An event timer
  - System supervisor
- **I/O Ports**
  - Max. 34/24/20 multifunction bi-directional I/Os
  - Each incorporate with pull-up resistor, pull-down resistor, output high, output low or floating input, depending on programmer's settings on the corresponding registers
  - I/O ports with 20mA current sink
  - I/O ports with 8mA current drive
- **Two 16-bit Timer/Counter (Timer 0/1)**
  - Timer mode with clock source selectable
  - Auto reload 8-bit timers
  - Externally gated event counters
- **One Powerful Timer 2 with 16-bit Compare/Capture Unit**
  - Timer mode with clock source selectable
  - Auto-reload 16-bit timers
  - Externally gated event counters
  - Event capturing
  - Pulse width modulation and measurement
- **UART0**
  - One synchronous mode
  - Three asynchronous modes
- **SPI (master mode)**
  - Programmable phase and polarity of master clock
  - Programmable master SPI_CLK clock frequency
  - Max SPI clock: 6.125MHz (F_{OSC} /4) @24.5MHz
- **A/D Converter**
  - One 8-channel 8-bit resolution mode (GPM8F3232A/3216A)
  - One 8-channel 12-bit resolution mode (GPM8F3232A/3216A)
  - One 6-channel 8-bit resolution mode (GPM8F3208A)
  - One 6-channel 12-bit resolution mode (GPM8F3208A)
  - Max conversion clock: 6.125MHz (F_{OSC} /4) @24.5MHz
- **Built-in OP Circuit**
- **Audio Module (available only in GPM8F3232A)**
  - 24KHz output or 32KHz output @24.5MHz
- **Debug Unit**

Product Number	GPM8F3232A	GPM8F3216A	GPM8F3208A
Speed (MHz)	24.5	24.5	24.5
Operating Voltage (V)	2.4~5.5	2.4~5.5	2.4~5.5
Flash (Kbytes)	32	16	8
XRAM (bytes)	1K	512	256
IDM (bytes)	256	256	256
Timer	3	3	3
UART	1	1	1
SPI	1	1	1
12-bit ADC	8-channel	8-channel	6-channel
Built-in OP	Yes	Yes	Yes
IO	34	24	20
Package Type	LQFP44	SOP28	SOP24

3. BLOCK DIAGRAM

3.1. GPM8F3232A

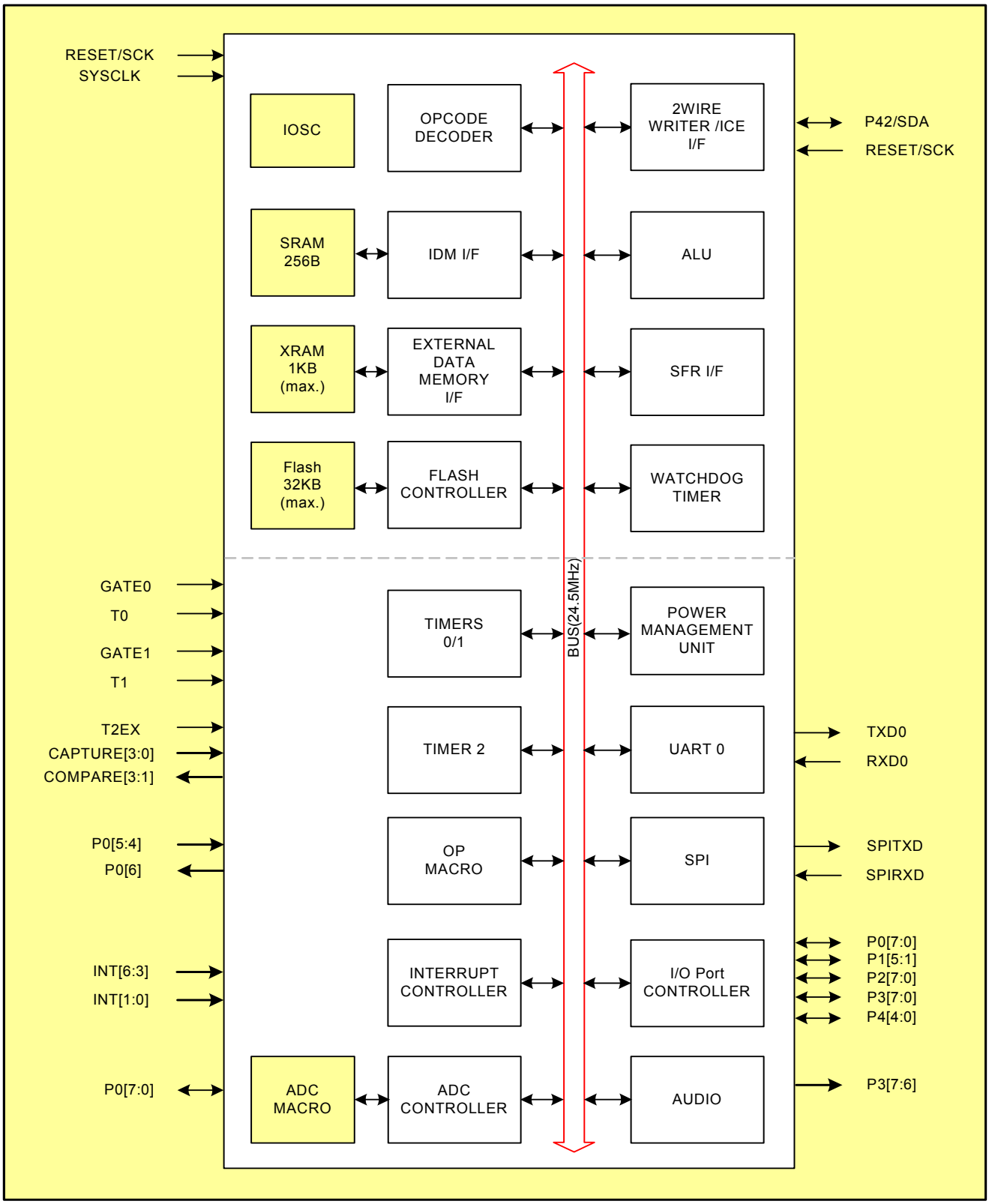


Figure 3-1 Block diagram of GPM8F3232A

3.2. GPM8F3216A

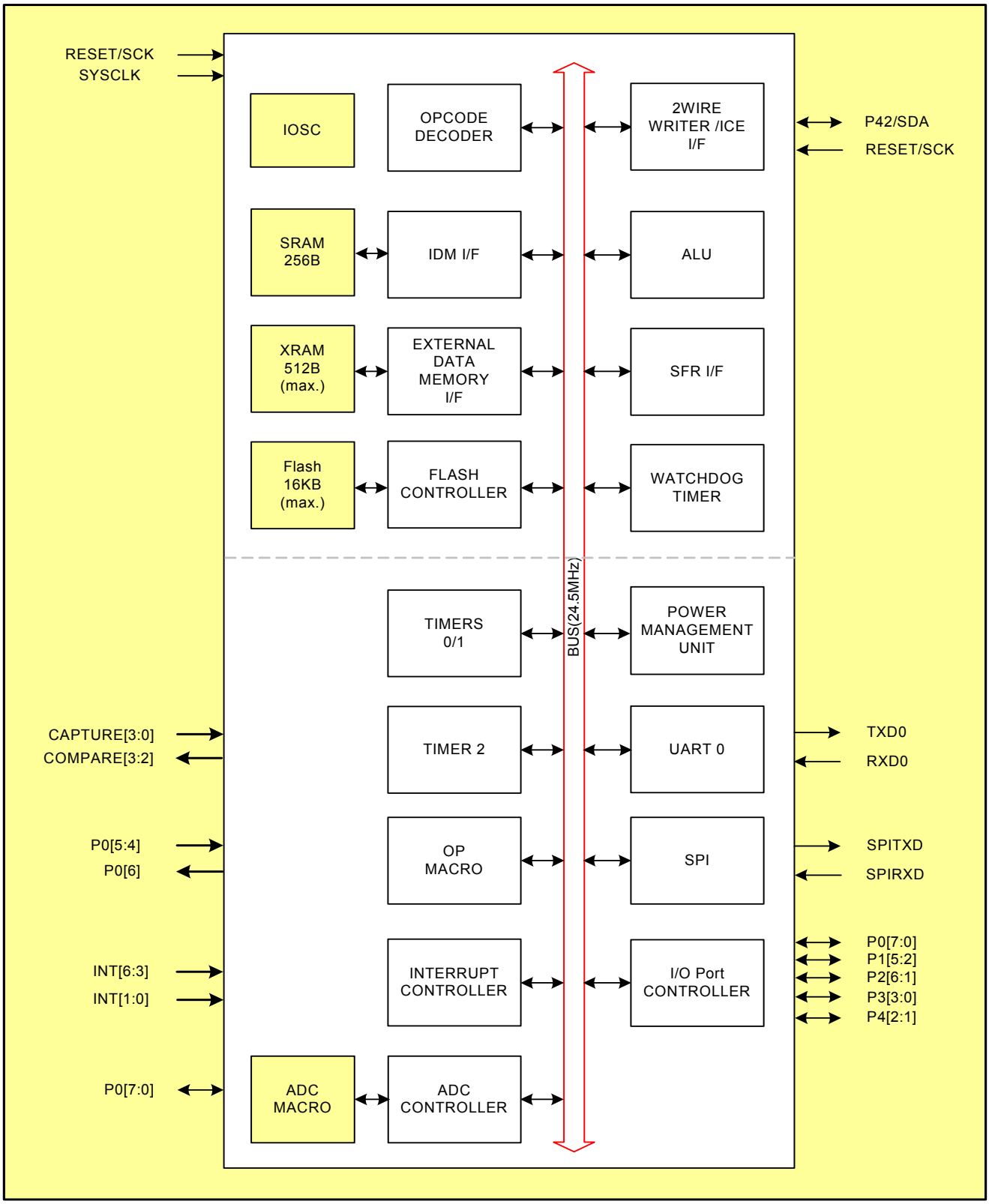


Figure 3-2 Block diagram of GPM8F3216A

3.3. GPM8F3208A

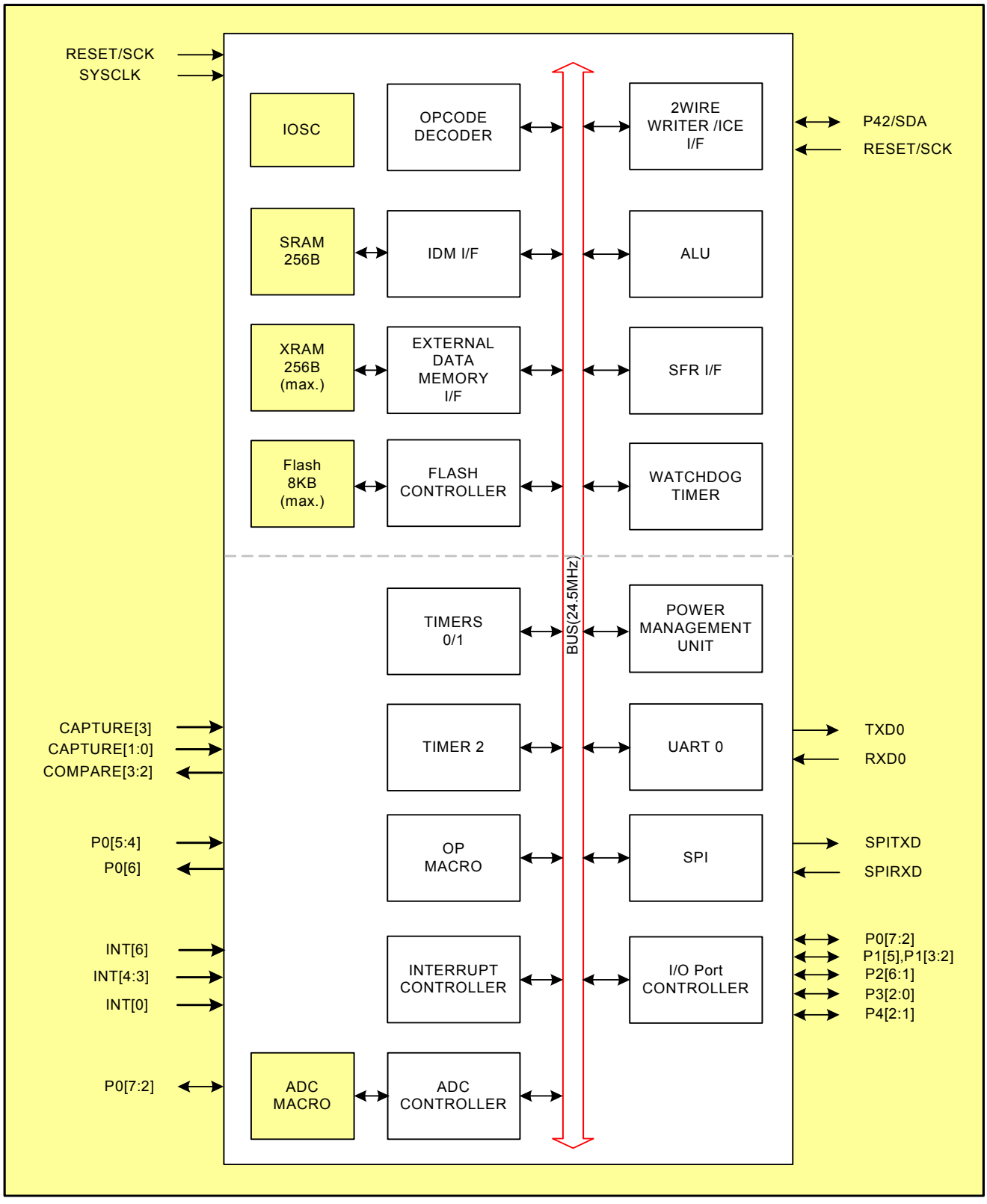


Figure 3-3 Block diagram of GPM8F3208A

4. SIGNAL DESCRIPTIONS

4.1. Pin Descriptions

4.1.1. GPM8F3232A

Type: I = Input, O = Output, S = Supply

Pin Name	LQFP44	Type	Description
P14	1	I/O	Port 1 bit 4 / INT5 / CAPTURE2
P15	2	I/O	Port 1 bit 5 / INT6 / CAPTURE3
RESET	3	I	RESET signal, high active / SCK(2 wire serial bus clock input line)
NC	4		
P30	5	I/O	Port 3 bit 0 / RXD0
P31	6	I/O	Port 3 bit 1 / TXD0
P32	7	I/O	Port 3 bit 2 / INT0
P33	8	I/O	Port 3 bit 3 / INT1
P34	9	I/O	Port 3 bit 4 / T0(Timer 0 input)
P35	10	I/O	Port 3 bit 5 / T1(Timer 1 input)
NC	11		
P36	12	I/O	Port 3 bit 6 / GATE0(Timer 0 gate) / AUDIO_N
P37	13	I/O	Port 3 bit 7 / GATE1(Timer 1 gate) / AUDIO_P
VSS	14	S	Ground
P27	15	I/O	Port 2 bit 7
P20	16	I/O	Port 2 bit 0
P21	17	I/O	Port 2 bit 1
P22	18	I/O	Port 2 bit 2
P23	19	I/O	Port 2 bit 3
P24	20	I/O	Port 2 bit 4
NC	21		
NC	22		
P25	23	I/O	Port 2 bit 5 / XTI
P26	24	I/O	Port 2 bit 6 / XTO
VREG	25	S	Regulator output, needs 2.2uF Cap.
P44	26	I/O	Port 4 bit 4
P43	27	I/O	Port 4 bit 3
P42	28	I/O	Port 4 bit 2 / SDA(2 wire serial bus data input / output line)
P41	29	I/O	Port 4 bit 1
P40	30	I/O	Port 4 bit 0
NC	31		
P07	32	I/O	Port 0 bit 7 / AN7(ADC channel 7 input) / SPI0_RX
P06	33	I/O	Port 0 bit 6 / AN6(ADC channel 6 input) / SPI0_TX / OP_OUT
P05	34	I/O	Port 0 bit 5 / AN5(ADC channel 5 input) / SPI0_CLK / OP V-
P04	35	I/O	Port 0 bit 4 / AN4(ADC channel 4 input) / SPI0_CSB / OP V+
P03	36	I/O	Port 0 bit 3 / AN3(ADC channel 3 input)
P02	37	I/O	Port 0 bit 2 / AN2(ADC channel 2 input)
P01	38	I/O	Port 0 bit 1 / AN1(ADC channel 1 input)
P00	39	I/O	Port 0 bit 0 / AN0(ADC channel 0 input)
VCC	40	S	Power 5V input
NC	41		

Pin Name	LQFP44	Type	Description
P11	42	I/O	Port 1 bit 1 / T2EX / COMPARE1(PWM1)
P12	43	I/O	Port 1 bit 2 / INT3 / CAPTURE0 / COMPARE2(PWM2)
P13	44	I/O	Port 1 bit 3 / INT4 / CAPTURE1 / COMPARE3(PWM3)

4.1.2. GPM8F3216A

Type: I = Input, O = Output, S = Supply

Pin Name	SOP28	Type	Description
P00	1	I/O	Port 0 bit 0 / AN0(ADC channel 0 input)
VCC	2	S	Power 5V input
P12	3	I/O	Port 1 bit 2 / INT3 / CAPTURE0 / COMPARE2(PWM2)
P13	4	I/O	Port 1 bit 3 / INT4 / CAPTURE1 / COMPARE3(PWM3)
P14	5	I/O	Port 1 bit 4 / INT5 / CAPTURE2
P15	6	I/O	Port 1 bit 5 / INT6 / CAPTURE3
RESET	7	I	RESET signal, high active / SCK(2 wire serial bus clock input line)
P30	8	I/O	Port 3 bit 0 / RXD0
P31	9	I/O	Port 3 bit 1 / TXD0
P32	10	I/O	Port 3 bit 2 / INT0
P33	11	I/O	Port 3 bit 3 / INT1
VSS	12	S	Ground
P21	13	I/O	Port 2 bit 1
P22	14	I/O	Port 2 bit 2
P23	15	I/O	Port 2 bit 3
P24	16	I/O	Port 2 bit 4
P25	17	I/O	Port 2 bit 5 / XTI
P26	18	I/O	Port 2 bit 6 / XTO
VREG	19	S	Regulator output, needs 2.2uF Cap.
P42	20	I/O	Port 4 bit 2 / SDA(2 wire serial bus data input / output line)
P41	21	I/O	Port 4 bit 1
P07	22	I/O	Port 0 bit 7 / AN7(ADC channel 7 input) / SPI0_RX
P06	23	I/O	Port 0 bit 6 / AN6(ADC channel 6 input) / SPI0_TX / OP_OUT
P05	24	I/O	Port 0 bit 5 / AN5(ADC channel 5 input) / SPI0_CLK / OP V-
P04	25	I/O	Port 0 bit 4 / AN4(ADC channel 4 input) / SPI0_CSB / OP V+
P03	26	I/O	Port 0 bit 3 / AN3(ADC channel 3 input)
P02	27	I/O	Port 0 bit 2 / AN2(ADC channel 2 input)
P01	28	I/O	Port 0 bit 1 / AN1(ADC channel 1 input)

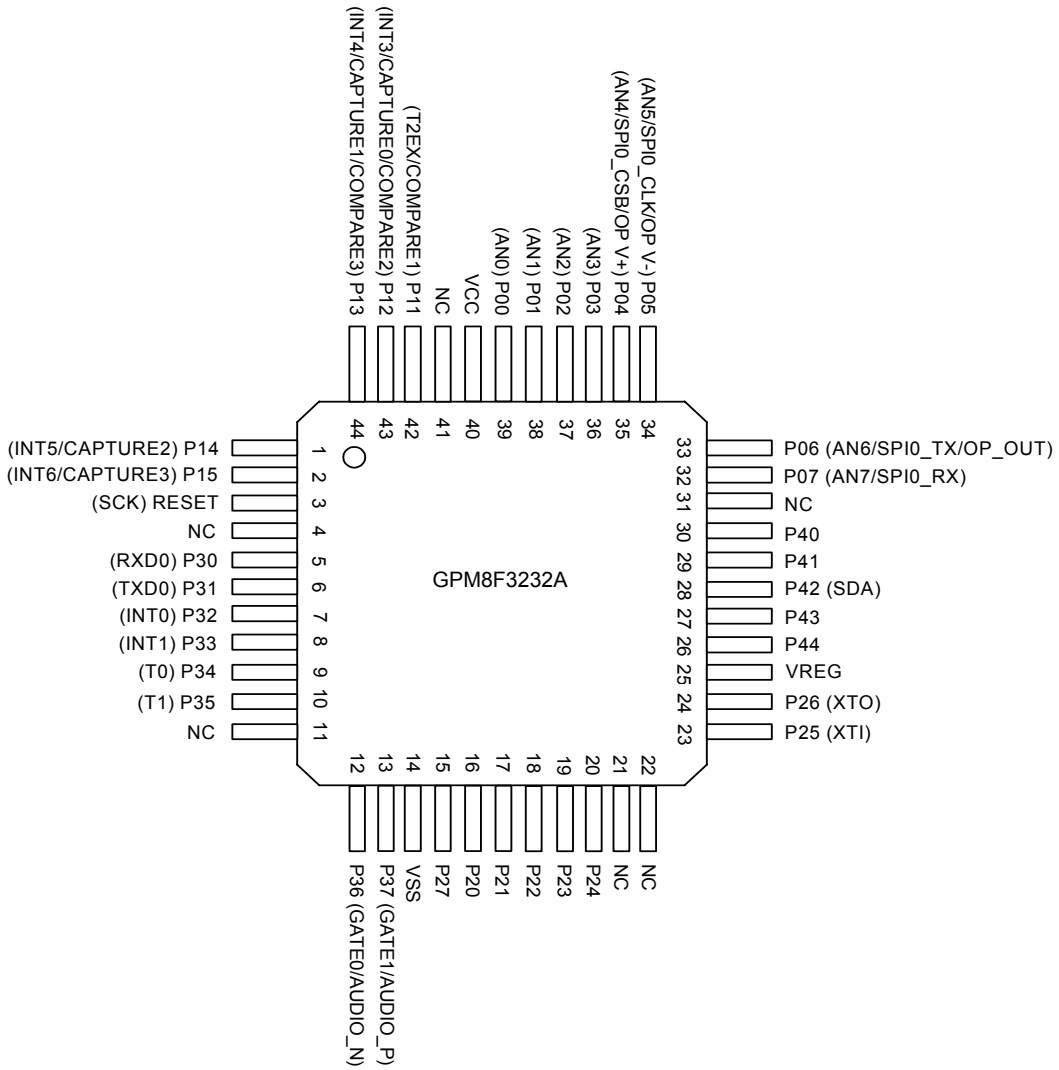
4.1.3. GPM8F3208A

Type: I = Input, O = Output, S = Supply

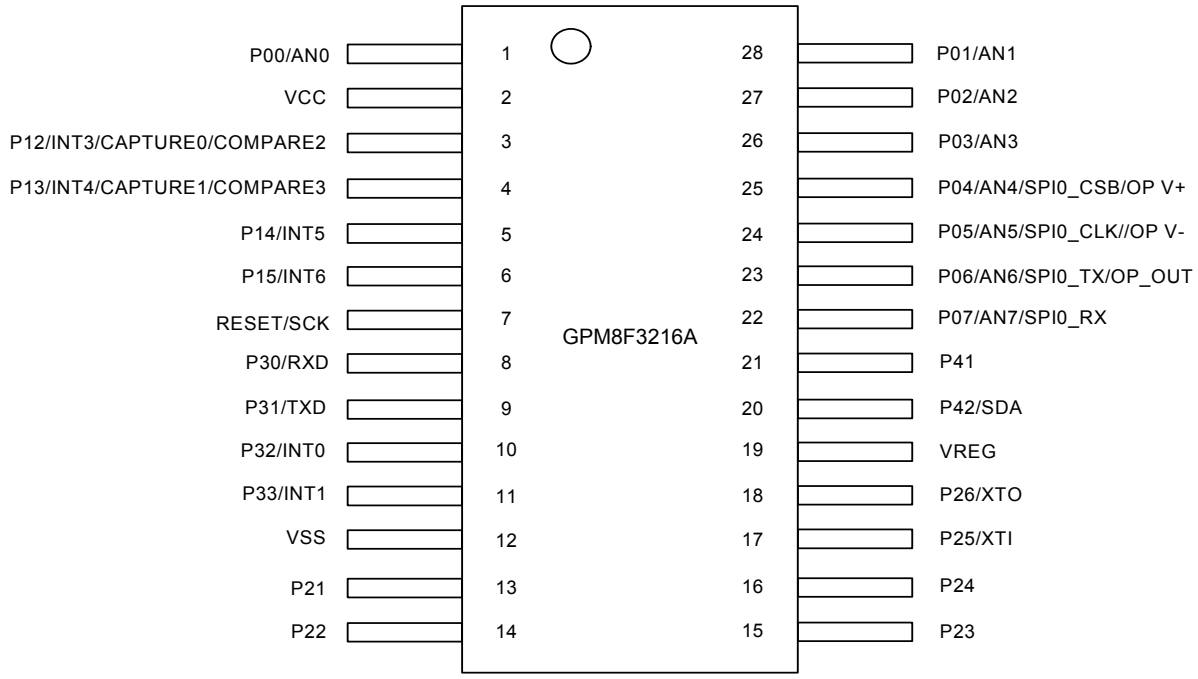
Pin Name	SOP24	Type	Description
P02	1	I/O	Port 0 bit 2 / AN2(ADC channel 2 input)
VCC	2	S	Power 5V input
P12	3	I/O	Port 1 bit 2 / INT3 / CAPTURE0 / COMPARE2(PWM2)
P13	4	I/O	Port 1 bit 3 / INT4 / CAPTURE1 / COMPARE3(PWM3)
P15	5	I/O	Port 1 bit 5 / INT6 / CAPTURE3
RESET	6	I	RESET signal, high active / SCK(2 wire serial bus clock input line)
P30	7	I/O	Port 3 bit 0 / RXD0
P31	8	I/O	Port 3 bit 1 / TXD0
P32	9	I/O	Port 3 bit 2 / INT0
VSS	10	S	Ground
P21	11	I/O	Port 2 bit 1
P22	12	I/O	Port 2 bit 2
P23	13	I/O	Port 2 bit 3
P24	14	I/O	Port 2 bit 4
P25	15	I/O	Port 2 bit 5 / XTI
P26	16	I/O	Port 2 bit 6 / XTO
VREG	17	S	Regulator output, needs 2.2uF Cap.
P42	18	I/O	Port 4 bit 2 / SDA(2 wire serial bus data input/output line)
P41	19	I/O	Port 4 bit 1
P07	20	I/O	Port 0 bit 7 / AN7(ADC channel 7 input) / SPI0_RX
P06	21	I/O	Port 0 bit 6 / AN6(ADC channel 6 input) / SPI0_TX / OP_OUT
P05	22	I/O	Port 0 bit 5 / AN5(ADC channel 5 input) / SPI0_CLK / OP V-
P04	23	I/O	Port 0 bit 4 / AN4(ADC channel 4 input) / SPI0_CSB / OP V+
P03	24	I/O	Port 0 bit 3 / AN3(ADC channel 3 input)

4.2. PIN Map

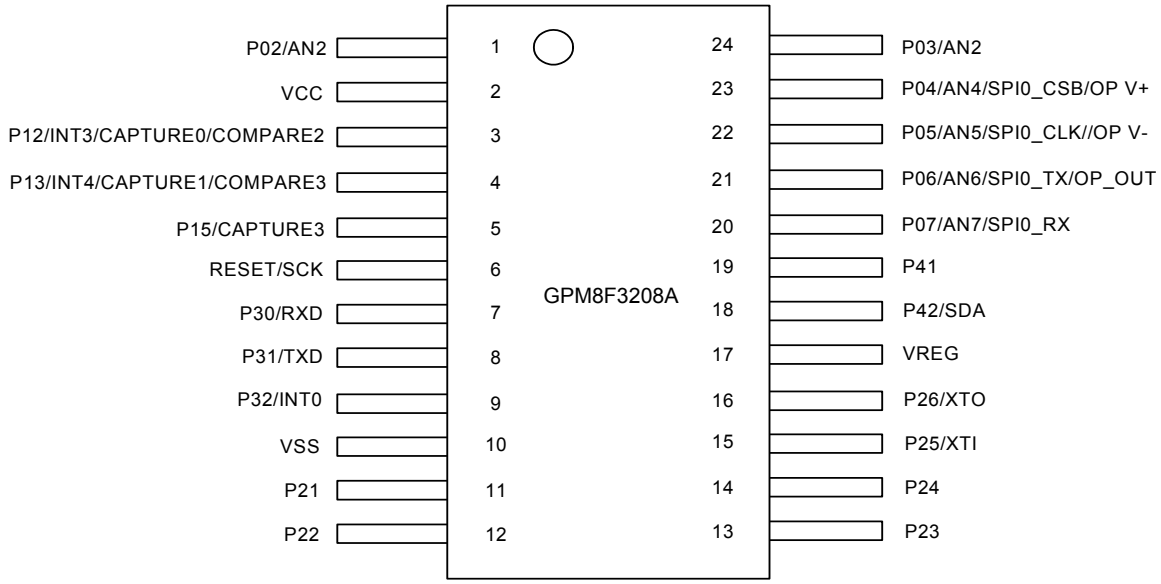
Package Pin Sequence - LQFP 44 Package Top View



Package Pin Sequence – SOP28 Package Top View



Package Pin Sequence – SOP24 Package Top View



5. FUNCTIONAL DESCRIPTIONS

5.1. Central Processing Unit

5.1.1. CPU Introduction

The CPU is an ultra high performance, high speed embedded microcontroller. Pipelined architecture enables the CPU 10 times faster than standard architecture. This performance can also be exploited to great advantage in low power application where the core can be clocked over ten times slower than original implementation for no performance penalty.

5.1.2. CPU Features

- ❑ 100 % software compatible with industry 8051
- ❑ 24 times faster multiplication
- ❑ 12 times faster addition

The CPU is fully compatible with industry standard 8051 microcontroller, maintaining all instruction mnemonics and binary compatibility. It incorporates some great architectural enhancements, allowing the CPU instructions execution with high performance and high speed.

The arithmetic section of the processor performs extensive data manipulation and is comprised of an 8-bit arithmetic logic unit (ALU), an ACC(0xE0) register, B(0xF0) register and PSW(0xD0) register.

5.1.3. Arithmetic Logic Unit (ALU)

The ALU performs the arithmetic and logic operations during one instruction execution. Typical arithmetic operations are addition, subtraction, multiplication and division. Additional operations are such as increment, decrement, BCD-decimal-add-adjust and compare. Within logic unit, operation such as AND, OR, Exclusive OR, complement and rotation are performed. The Boolean processor performs the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry.

5.1.4. Accumulator A Register

The accumulation is the 8-bit general-purpose register, which can be operated with data transfer, temporary saving, condition judgment, etc.

5.1.5. B Register

The B register is used during multiply and divide operations. In other cases, it may be used as normal SFR.

5.1.6. Program Status Word (PSW)

The PSW contains several bits that reflect the current state of the CPU which is similar to the flag-register of general CPU.

5.1.7. Program Counter (PC)

The program counter is a 16-bit wide register. It consists of two 8-bit registers which are PCH and PCL. This register indicates the address of next instruction to be executed. In Reset state, the content of 0x0000 is stored into program counter.

ACC			**Address: 0xE0**		**Accumulator A Register**			
Bit	7	6	5	4	3	2	1	0
Function	ACC[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	**Function**	**Type**	**Description**	**Condition**
7:0	ACC[7:0]	R/W	Accumulator A	

Table 5-1 The ACC register

B			**Address: 0xF0**		**B Register**			
Bit	7	6	5	4	3	2	1	0
Function	B[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	**Function**	**Type**	**Description**	**Condition**
7:0	B[7:0]	R/W	B	

Table 5-2 The B register

PSW			Address: 0xD0		Program Status Word Register			
Bit	7	6	5	4	3	2	1	0
Function	CY	AC	F0	RS1	RS0	OV	F1	P
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CY	R/W	Carry flag	
6	AC	R/W	Auxiliary carry flag	
5	F0	R/W	General purpose flag 0	
4:3	RS[1:0]	R/W	Register bank selection bits RS[1:0] – Function Description 00 – Bank 0, data address 0x00-0x07 01 – Bank 1, data address 0x08-0x0F 10 – Bank 2, data address 0x10-0x17 11 – Bank 3, data address 0x18-0x1F	
2	OV	R/W	Overflow flag	
1	F1	R/W	General purpose flag 1	
0	P	R/W	Parity flag	

Table 5-3 The PSW register

5.2. Memory Organization

5.2.1. Introduction

The GPM8F3232A/3216A/3208A has three separated address spaces for program memory and data memory. The program memory is on-chip, re-programmable Flash memory and contains up to 32/16/8K bytes spaces. The data memory is divided into 1K/512/256 bytes of external RAM, 256 bytes IDM with 128 bytes of SFR which can be read and written. The upper IDM and SFR use the same access address in different access ways which are described in Figure 5-2.

5.2.2. Program Memory Allocation

The program memory allocation is divided into two parts, including code area and last page. The GPM8F3232A/3216A/3208A implements 32/16/8KB memory size. It begins at address 0x0000 and ends at address 0x7FFF/0x3FFF/0x1FFF. The address space between 0x0000 and 0x7BFF/0x3BFF/0x1BFF is used for code area and the address space between 0x7C00/0x3C00/0x1C00 and 0x7FFF/0x3FFF/0x1FFF is called LAST_PAGE which cannot be erased by software. It reserves for constants storage. The last address 0x7FFF/0x3FFF/0x1FFF is used for CONFIG_BYTE whose definition of each bit is described in Table 5-4. This CONFIG_BYTE value can be read from CONFIG_BYTE register(0xB7). User can lock the whole chip by CONFIG_BYTE [0]. If CONFIG_BYTE [0] is programmed to be '0', the whole chip memory is protected and any page erase or program by two wire serial interface is not allowed. The only thing user can do is to erase whole chip. Figure 5-1 shows the program memory map of 32KB/16KB/8KB Flash.

After each reset, CPU starts execution in the program memory at location 0x0000. Each interrupt has its own start address for service routine. The Flash memory can be programmed in-system, through the SCK/SDA interface or by software using the MOVX instruction when PWE= 1. User can refer to the example code in the programming guide for the procedure of write and erase operations. Flash data cannot be programmed from a '0' to a '1', and only erase operation can realize it. Therefore, flash data would typically be erased (set to 0xFF) before being programmed. The write and erase operations are executed by using Pseudo-idle mode to be automatically timed by hardware without data polling to determine the end of the write and erase operation.

For software security consideration, user can set the programmable Flash level by FL_LEVEL register to limit the code area that avoids inadvertently erased or written by software, the protected region is called READONLY_PAGE.

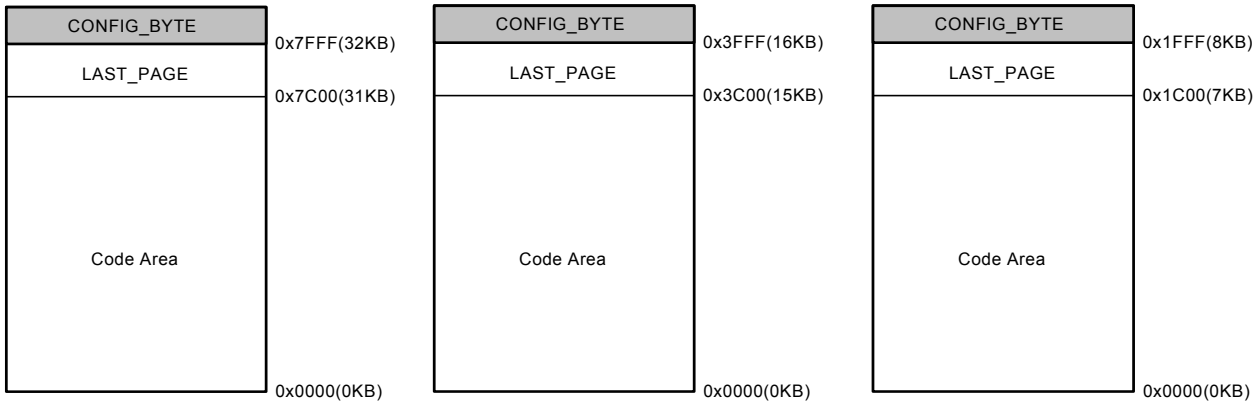


Figure 5-1 Program memory organization

CONFIG_BYTE			Address: 0xB7		CONFIG_BYTE Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	LVRVSEL	--	--	--	IOSEL	CODE Lock
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:6	--	R	Reserved	
5	LVRVSEL	R	LVR voltage level selection 0: 3.9V 1: 2.2V	
4:2	--	R	Reserved	
1	IOSEL	R	IO initial state selection bit 0: Input pull high 1: floating	
0	CODE Lock	R	0 : CODE is locked; 1 : CODE is unlocked	

Table 5-4 The CONFIG_BYTE register

FL_LEVEL			Address: 0xED		Flash Level Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	FLASH_LEVEL[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	FLASH_LEVEL[5:0]	R/W	FLASH_LEVEL, it determines how many 1K pages are read only	

FLASH_LEVEL	Note
0	no page is read only
1	address < 0x400 is read only
2	address < 0x800 is read only
3	address < 0xC00 is read only
4	address < 0x1000 is read only
5	address < 0x1400 is read only
6	address < 0x1800 is read only

Bit	Function	Type	Description		Condition
5:0	FLASH_LEVEL[5:0]	R/W	7	address < 0x1C00 is read only	
			8	address < 0x2000 is read only	
			9	address < 0x2400 is read only	
			10	address < 0x2800 is read only	
			11	address < 0x2C00 is read only	
			12	address < 0x3000 is read only	
			13	address < 0x3400 is read only	
			14	address < 0x3800 is read only	
			15	address < 0x3C00 is read only	
			16	address < 0x4000 is read only	
			17	address < 0x4400 is read only	
			18	address < 0x4800 is read only	
			19	address < 0x4C00 is read only	
			20	address < 0x5000 is read only	
			21	address < 0x5400 is read only	
			22	address < 0x5800 is read only	
			23	address < 0x5C00 is read only	
			24	address < 0x6000 is read only	
			25	address < 0x6400 is read only	
			26	address < 0x6800 is read only	
			27	address < 0x6C00 is read only	
			28	address < 0x7000 is read only	
			29	address < 0x7400 is read only	
			30	address < 0x7800 is read only	
			31	address < 0x7C00 is read only	
			≧32	address < 0x7FFF is read only	
			Note 1. Only FLASH_LEVEL[5:0] is useful in GPM8F3232A Note 2. Only FLASH_LEVEL[4:0] is useful in GPM8F3216A Note 3. Only FLASH_LEVEL[3:0] is useful in GPM8F3208A		

Table 5-5 The FL_LEVEL register

5.2.3. Data Memory Allocation

Data memory address allocations on the GPM8F3232A/3216A/3208A are divided into two parts. The first part is 1K/512/256 bytes of external RAM and the second one is 256 byte IDM as shown in Figure 5-2. The lowest internal data memory (IDM) consists of four register banks with eight registers each. A bit addressable segment with 128 bits (16 bytes) begins at 0x20. The address from 0x30 to 0x7F is not defined and can be utilized freely by user. The last 128 bytes of data memory can be used by different addressing modes. With the indirect addressing mode, address from 0x80 to 0xFF shared with stack space is addressed. With the direct addressing mode, the SFR addressing from 0x80 to 0xFF is accessed. The SFR memory map is shown in Table 5-6.

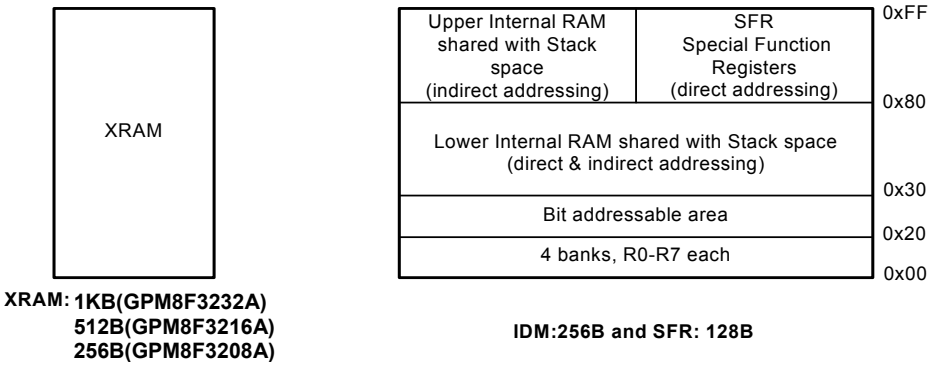


Figure 5-2 Data memory organization

Note1: Black: standard 8051 register; gray: additional register;

0xF8	EIP	IOSCCON	IOSCT0	IOSCT1	SPICON	SPITXD	SPIRXD	
0xF0	B	ADCON	ADCFG	ADAEN	ADOL	ADOH	ADLB	ADUB
0xE8	EIE			TA	FLASHCON	FL_LEVEL		KEYCODE
0xE0	ACC							
0xD8	WDCON							
0xD0	PSW							
0xC8	T2CON	T2IF	CRCL	CRCH	TL2	TH2	CCEN	
0xC0			CCL1	CCH1	CCL2	CCH2	CCL3	CCH3
0xB8	IP							
0xB0	P3			AUDCON	AUDBUF		WKUEN	CONFIG_BYTE
0xA8	IE			OPCON		SRCON	SYSCON0	SYSCON1
0xA0	P2	P4	P3_PU	P3_PD	P4_PU	P4_PD	FLASHERRF	SYSCON2
0x98	SCON0	SBUF0	P0_PU	P0_PD	P1_PU	P1_PD	P2_PU	P2_PD
0x90	P1	EIF			RSTSTS		BIP	BIF
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	RSTCON
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F

Table 5-6 SFR memory map

5.2.4. Memory Related SFR

The following sub-sections describe program, external and internal memories related SFRs of 8051 core and their functionality. For other information about standard SFRs, please refer to appropriate peripheral section.

5.2.4.1. Program Write Enable Bit

The Program Write Enable (PWE) bit, located in PCON register bit 4, is used during MOVX instructions. When PWE bit is set to logic 1, the MOVX @DPTR, An instruction writes data located in accumulator register into program memory addressed by DPTR register. Program memory can be read by MOVC only regardless of PWE bit.

5.2.4.2. Data Pointer Registers

Dual data pointer registers are implemented to speed up data block copying. DPTR0 and DPTR1 are located in four SFR addresses. Active DPTR register is selected by SEL bit (DPS[0]). If SEL=0 then DPTR0 is selected otherwise DPTR1.

5.2.4.3. Stack Pointer

The 8051 has 8-bit stack pointer called SP (0x81) located in the internal RAM space. It is incremented before data is stored during PUSH and CALL execution and decremented after data is popped during POP, RET and RETI execution. In the other words, it always points to the last valid stack byte. The SP is accessed as any other SFRs. Figure 5-3 shows an example when PUSH A is executed and Figure 5-4 shows an example when POP PSW is executed.

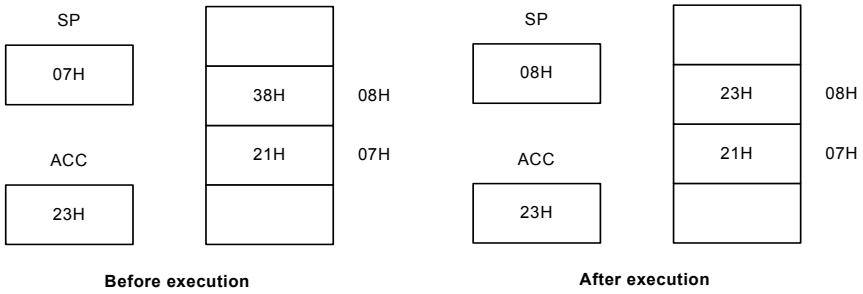


Figure 5-3 Stack byte order for PUSH A instruction

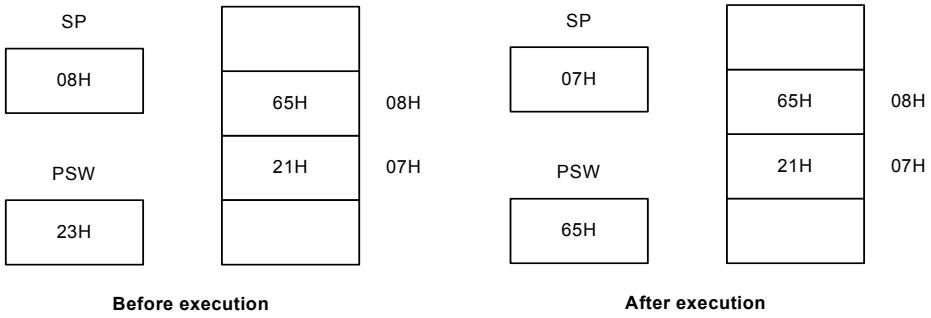


Figure 5-4 Stack byte order for POP PSW instruction

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	--	CPU_IDLE	PWE	STOP_RST_EN	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	--	R/W	Reserved	
5	CPU_IDLE	R/W	IDLE mode enable bit 0: IDLE mode disabled ; 1: IDLE mode entered	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3	STOP_RST_EN	R/W	Wakeup state selection bit 0: Next instruction state after wakeup 1: Reset state afer wakeup	
2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-7 The PCON register

DPH0			Address: 0x83		Data Pointer Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[15:8]	R/W	Data pointer register DPTR0 - high byte	

Table 5-8 The DPH0 register

DPL0			Address: 0x82		Data Pointer Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[7:0]	R/W	Data pointer register DPTR0 - low byte	

Table 5-9 The DPL0 register

DPH1			Address: 0x85		Data Pointer 1 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR1[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[15:8]	R/W	Data pointer 1 register DPTR1 - high byte	

Table 5-10 The DPH1 register

DPL1			Address: 0x84		Data Pointer 1 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[7:0]	R/W	Data pointer 1 register DPTR1 - low byte	

Table 5-11 The DPL1 register

DPS			Address: 0x86		Data Pointer Select Register			
Bit	7	6	5	4	3	2	1	0
Function	ID1	ID0	TSL	--	--	--	--	SEL
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	ID[1:0]	R/W	Increment/decrement function select. See Table 5-13	
5	TSL	R/W	Toggle select enable bit 0: DPTR related instructions do not affect state of SEL bit 1: DPTR related instructions to toggle the SEL bit	
4:1	--	R/W	Reserved	
0	SEL	R/W	Active data pointer select bit See Table 5-13	

Table 5-12 The DPS register

ID1	ID0	SEL=0	SEL=1
0	0	INC DPTR0	INC DPTR1
0	1	DEC DPTR0	INC DPTR1
1	0	INC DPTR0	DEC DPTR1
1	1	DEC DPTR0	DEC DPTR1

Table 5-13 DPTR0/DPTR1 operations

SP			Address: 0x81		Stack Pointer Register			
Bit	7	6	5	4	3	2	1	0
Function	SP[7:0]							
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:0	SP[7:0]	R/W	Stack pointer	

Table 5-14 The SP register

5.3. Special Function Registers(SFR)

GPM8F3232A/3216A/3208A has up to 84 control registers for special function registers. All of the SFRs are used by MCU and peripheral function block for controlling the desired operation. Some of the SFRs contain control and status bits for peripheral module such as Timer unit, Interrupt control unit, etc. Some of bits in SFRs are read only, so write to those bits don't have any effect on corresponding bits. Some SFRs have key code design that KEYCODE register must be written with correct key codes, in sequence, before writing a value to it for software security. The following table shows the summary of the SFRs. The detailed information of each SFRs are explained in each peripheral section.

Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0x80	P0		0xFF	Port 0							
0x81	SP		0x07	Stack Pointer							
0x82	DPL0		0x00	Data pointer register DPTR0 - low byte							
0x83	DPH0		0x00	Data pointer register DPTR0 - high byte							
0x84	DPL1		0x00	Data pointer register DPTR1 - low byte							
0x85	DPH1		0x00	Data pointer register DPTR1 - high byte							
0x86	DPS		0x00	ID1	ID0	TSL	--	--	--	--	SEL

Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0x87	PCON		0x00	SMOD0	--	CPU_ IDLE	PWE	STOP_ RST_EN	--	STOP	--
0x88	TCON		0x00	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
0x89	TMOD		0x00	GATE1	CT1	M11	M10	GATE0	CT0	M01	M00
0x8A	TL0		0x00	Timer 0 Load value – low byte							
0x8B	TL1		0x00	Timer 1 Load value – low byte							
0x8C	TH0		0x00	Timer 0 Load value – high byte							
0x8D	TH1		0x00	Timer 1 Load value – high byte							
0x8E	CKCON		0x01	WD1	WD0	--	T1M	T0M	--	--	--
0x8F	RSTCON	4F,72, 7A	0x10	CB_P_ ENB	LP_E_ ENB	FLASH_ FLOW_ ENB	XADDR_ ENB	--	CHIP_E_ ENB	MISS_CLK_ ENB	FLASH_ERR _ENB
0x90	P1		0xff	Port 1							
0x91	EIF		0x00	--	--	--	INT6F	INT5F	INT4F	INT3F	--
0x94	RSTSTS		0x00	--	MISS_ CLK_RST	STOP_ RST	FLASH_ ERR_RST	S/W_RST	WDT_RST	LVR_RST	RAD_RST
0x96	BIP		0x00	--	--	--	PAUDIO	PADC	--	--	PMERR
0x97	BIF		0x00	--	--	--	AUDIOF	ADCF	--	--	MERRF
0x98	SCON0		0x00	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
0x99	SBUF0		0x00	UART 0 buffer							
0x9A	P0_PU		0xFF	P07_PU	P06_PU	P05_PU	P04_PU	P03_PU	P02_PU	P01_PU	P00_PU
0x9B	P0_PD		0x00	P07_PD	P06_PD	P05_PD	P04_PD	P03_PD	P02_PD	P01_PD	P00_PD
0x9C	P1_PU		0xFF	P17_PU	P16_PU	P15_PU	P14_PU	P13_PU	P12_PU	P11_PU	P10_PU
0x9D	P1_PD		0x00	P17_PD	P16_PD	P15_PD	P14_PD	P13_PD	P12_PD	P11_PD	P10_PD
0x9E	P2_PU		0xFF	P27_PU	P26_PU	P25_PU	P24_PU	P23_PU	P22_PU	P21_PU	P20_PU
0x9F	P2_PD		0x00	P27_PD	P26_PD	P25_PD	P24_PD	P23_PD	P22_PD	P21_PD	P20_PD
0xA0	P2		0xFF	Port 2							
0xA1	P4		0xFF	Port 4							
0xA2	P3_PU		0xFF	P37_PU	P36_PU	P35_PU	P34_PU	P33_PU	P32_PU	P31_PU	P30_PU
0xA3	P3_PD		0x00	P37_PD	P36_PD	P35_PD	P34_PD	P33_PD	P32_PD	P31_PD	P30_PD
0xA4	P4_PU		0xFF	--	P46_PU	P45_PU	P44_PU	P43_PU	P42_PU	P41_PU	P40_PU
0xA5	P4_PD		0x00	--	P46_PD	P45_PD	P44_PD	P43_PD	P42_PD	P41_PD	P40_PD
0xA6	FLASHERRF		0x00	CB_P_F	LP_E_F	FLASH_ FLOW_F	XADDR_F	--	CHIP_E_F	--	--
0xA7	SYSCON2	FF,00	0x00	ADCLKX2	--	INT_filter_ en	GPIO_ SSO	SCHMIT_ DIS_P3	SCHMIT_ DIS_P2	SCHMIT_ DIS_P1	SCHMIT_ DIS_P0
0xA8	IE		0x00	EA	--	ET2	ES0	ET1	EX1	ET0	EX0
0xAB	OPCON		0x00	--	--	--	TRIM_VOSP	TRIM_VOSN	--	--	OP_EN
0xAD	SRCON		0xFF	--	--	--	P4_SR	P3_SR	P2_SR	P1_SR	P0_SR

Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0xAE	SYSCON0	FF,00	0x00	LVRENB	--	--	AUDIO_N_DIS	--	CLKOUT_EN	CCOUTENB	SCHMIT_DIS_P4
0xAF	SYSCON1	FF,00	0x02	T2CLK_SW	--	SPI1_EN	SPI0_EN	--	--	--	--
0xB0	P3		0xFF	Port 3							
0xB3	AUDCON		0x00	--	--	--	--	AUDIO_MODE	AUDIOIE	AUDIO_FREQ_SEL	AUDIO_EN
0xB4	AUDBUF		0x80	AUDBUF[7:0]							
0XB6	WKUEN	AF,50	0x07	--	INT6_WKUEN	INT5_WKUEN	INT4_WKUEN	INT3_WKUEN	--	INT1_WKUEN	INT0_WKUEN
0xB7	CONFIG_BYTE		0xFF	--	--	LVRVSEL	--	--	--	IOSEL	CODE_LOCK
0xB8	IP		0x00	--	--	PT2	PS0	PT1	PX1	PT0	PX0
0xC2	CCL1		0x00	Timer2cc compare/capture 1 low byte							
0xC3	CCH1		0x00	Timer2cc compare/capture 1 high byte							
0xC4	CCL2		0x00	Timer2cc compare/capture 2 low byte							
0xC5	CCH2		0x00	Timer2cc compare/capture 2 high byte							
0xC6	CCL3		0x00	Timer2cc compare/capture 3 low byte							
0xC7	CCH3		0x00	Timer2cc compare/capture 3 high byte							
0xC8	T2CON		0x00	T2PS	I3FR	--	T2R1	T2R0	T2CM	T2I1	T2I0
0xC9	T2IF		0x00	--	--	--	--	--	EXEN2	EXF2	TF2
0xCA	CRCL		0x00	CRC register – Low byte							
0xCB	CRCH		0x00	CRC register – High Byte							
0xCC	TL2		0x00	Timer 2 Load value – low byte							
0xCD	TH2		0x00	Timer 2 Load value – high byte							
0xCE	CCEN		0x00	CMH3	CML3	CMH2	CML2	CMH1	CML1	CMH0	CML0
0xD0	PSW		0x00	CY	AC	F0	RS1	RS0	OV	F1	P
0xD8	WDCON		0x00	--	--	--	--	WDIF	WTRF	EWT	RWT
0xE0	ACC		0x00	ACC register							
0xE8	EIE		0x00	--	--	EWDI	EINT6	EINT5	EINT4	EINT3	--
0xEB	TA		0x00	Timed Access protection register (0xaa➔0x55)							
0xEC	FLASHCON		0x00	--	--	--	--	--	M_ERASE	P_ERASE	PROG
0xED	FL_LEVEL		0x00	--	--	FLASH_LEVEL[5:0]					
0xEF	KEYCODE		0x00	KC7	KC6	KC5	KC4	KC3	KC2	KC1	KC0
0xF0	B		0x00	B register							
0xF1	ADCON		0x00	WINF	READYF	WIN_SEL	WINIE	ADIE	--	PSIDLE	START
0xF2	ADCFG		0x00	AD_BITSEL	CH_SEL[2:0]			SHCLK[1:0]		ADCLK[1:0]	
0xF3	ADAEN		0x00	P07_AEN	P06_AEN	P05_AEN	P04_AEN	P03_AEN	P02_AEN	P01_AEN	P00_AEN
0xF4	ADOL			--	--	--	--	ADO[3:0]			
0xF5	ADOH			ADO[11:4]							
0xF6	ADLB		0x00	ADLB[7:0]							
0xF7	ADUB		0x00	ADUB[7:0]							
0xF8	EIP		0x00	--	--	PWDI	PINT6	PINT5	PINT4	PINT3	--
0xF9	IOSCCON		0x09	XTO_AEN	XTI_AEN	XTAL_PAD_EN	OSC_SEL[1:0]		CLKDIV[2:0]		
0xFA	IOSCT0		0x18	--	--	TEMP_TRIM[2:0]			XFCN[2:0]		

Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0xFB	IOSCT1			OSC_TRIM[2:0]			OSC_TUNE[4:0]				
0xFC	SPICON		0x00	PO-LARITY	PHASE	SPI_CLK_SEL[1:0]		CSB_ KEEP	--	SPI_RD	SPI_ START
0xFD	SPITXD		0x00	SPI TX Data[7:0]							
0xFE	SPIRXD		0x00	SPI RX Data[7:0]							

5.4. Clock Source

GPM8F3232A/3216A/3208A has three clock sources including internal oscillator (24.5MHz), external crystal and external clock source. These three clocks are chosen to be system clock source by controlling OSC_SEL[1:0] bits of IOSCCON register. In addition, a clock divisor for the system clock source is contained to obtain different frequencies. There are eight selections totally and can be controlled by CLKDIV[2:0] bits of IOSCCON register. User can monitor the frequency of SYSCLK on P35 by setting SYSCON0[2]. The block diagram of clock source and detailed description of IOSCCON register are shown in Figure 5-5 and Table 5-15 respectively.

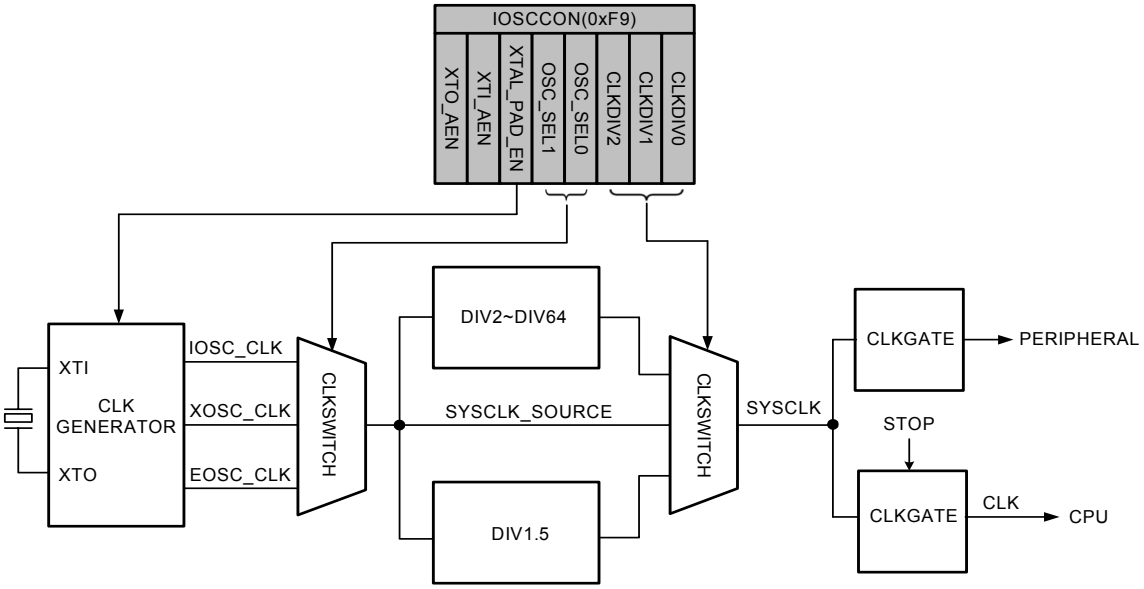


Figure 5-5 The block diagram of clock sources

If crystal mode is utilized, different frequencies can be selected by IOSCT0[2:0] as shown in Table 5-17 and software should delay a period of time according to different crystals for clock stable time. In order to enter stop mode, XTAL_PAD_EN should be turned off before PCON[1] is set to '1'. If internal oscillator mode is utilized, tuning frequencies is possible through IOSCT1[7:0]. If IOSCT1[7:5] is used for trimming bit, each step of frequency is 10%. If IOSCT1[4:0] is used for trimming bit, each step of frequency is 0.4% for fine-tuning. The IOSCT1 register is shown in Table 5-18.

IOSCCON			Address: 0xF9			IOSC Control Register		
Bit	7	6	5	4	3	2	1	0
Function	XTO_AEN	XTI_AEN	XTAL_PAD_EN	OSC_SEL[1:0]		CLKDIV[2:0]		
Default	0	0	0	0	1	0	0	1

Bit	Function	Type	Description
7	XTO_AEN	R/W	XTO analog PAD enable control bit 0: XTO can be I/O PAD 1: XTO can be analog PAD
6	XTI_AEN	R/W	XTI analog PAD enable control bit 0: XTI can be I/O PAD 1: XTI can be analog PAD
5	XTAL_PAD_EN	R/W	If using XTAL or ECLK, XTAL_PAD_EN should be set first for OSC_SEL selection.
4:3	OSC_SEL[1:0]	R/W	00: Internal ROSC 01: Internal ROSC 10: XTAL 11: External CLK If using XTAL, OSC_SEL[1](XTAL_EN) should be set after XOSC_CLK is stable
2:0	CLK_DIV	R/W	System Clock source divider

CLK_DIV	Clock control
000	SYSCLK_SOURCE
001	SYSCLK_SOURCE/2
010	SYSCLK_SOURCE/4
011	SYSCLK_SOURCE/8
100	SYSCLK_SOURCE/16
101	SYSCLK_SOURCE/32
110	SYSCLK_SOURCE/64
111	SYSCLK_SOURCE/1.5

Table 5-15 The IOSCCON register

SYSCON0			Address: 0xAE		SYSTEM control0 Register			
Bit	7	6	5	4	3	2	1	0
Function	LVRENB	--	--	AUDIO_N_DIS	--	CLKOUT_EN	CCOUTENB	SCHMIT_DIS_P4
Default	0	0	0	0	0	0	0	0
Key Code	FF,00							

Bit	Function	Type	Description	Condition
7	LVRENB	R/W	LVR enable control 0: enable LVR function 1: disable LVR function	
6:5	--	--	Reserved	
4	AUDIO_N_DIS	R/W	AUDIO_N disable bit available only if audio function is enabled 0: P36/P37 are output simultaneously as AUDIO_N/P 1: Only P37 is output as AUDIO_P	
3	--	--	Reserved	
2	CLKOUT_EN	R/W	Clock output enable bit (SYSCLK is output on P35)	
1	CCOUTENB	R/W	Disable output function of compare mode in Timer2 0: P1[3:1] = {compare3,compare2,compare1} 1: P1[3:1] is GPIO	
0	SCHMIT_DIS_P4	R/W	P4 Schmitt trigger function disable control bit	

Table 5-16 SYSCON0 register

IOSCT0			Address: 0xFA		IOSC Timing 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TEMP_TRIM[2:0]			XFCN[2:0]		
Default	0	0	0	1	1	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:3	TEMP_TRIM[2:0]	R/W	Temperature coefficient trimming（011: default）	
2:0	XFCN[2:0]	R/W	External XTAL Freq control bit (XTAL_PAD_EN need to be1)	

XFCN	XTAL(HZ)
000	F=32768Hz(weak)
001	F=32768Hz(strong)
010	1MHz<F<4MHz
011	4MHz<F<8MHz
100	8MHz<F<12MHz
101	12MHz<F<16MHz
110	16MHz<F<20MHz
111	25MHz>F>20MHz

Table 5-17 The IOSCT0 register

IOSCT1			Address: 0xFB		IOSC Control Timing 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	OSC_TRIM[2:0]			OSC_TUNE[4:0]				
Default	--	--	--	--	--	--	--	--

Bit	Function	Type	Description	Condition
7:5	OSC_TRIM[2:0]	R/W	Internal OSC frequency trimming bit, 10% each step	
4:0	OSC_TUNE[4:0]	R/W	Internal OSC frequency trimming bit, 0.4% each step	

Table 5-18 The IOSCT1 register

5.5. Power Saving Mode

5.5.1. Introduction

Although GPM8F3232A/3216A/3208A are high-speed microcontrollers designed for maximum performance, it also provides Power Management Unit (PMU) with two advanced power conservation modes. These modes are IDLE mode, and STOP mode. In order to reduce the current consumption when system does not need to be active, STOP mode can be utilized. For more information about these two modes, please see the following two sections.

5.5.2. IDLE Mode

IDLE Mode reduces power consumption by turning off the clock provided to the microcontroller, causing MCU to stop to execute following instruction. By setting CPU_IDLE bit (PCON[5]) is able to enter IDLE mode. In this mode, peripheral clock is not turned off, so peripheral device can still work normally.

5.5.3. STOP Mode

STOP mode is the lowest power states that the microcontroller can enter. It is achieved by cutting-off frequency provided to SYSCLK, resulting in a fully static condition. No processing is possible, timers are stopped, and no serial communication is executed. Processor operation will be postponed on the instruction that sets the STOP bit. STOP mode can be exited in the following ways:

i. A non-clocked interrupt such as the external interrupts INT0-INT6 can be used. Clocked interrupts such as the watchdog timer, internal timers, and serial ports do not operate in STOP mode. Processor operation will resume with the fetching of

the interrupt vector associated with the interrupt that caused the exit from STOP mode. When the interrupt service routine is completed, RETI returns the program to the instruction immediately following the one that invoked the STOP mode. When INT0~INT6 are used for wakeup source, WKUEN register must be set as shown in Table 5-21. There are two selections of the place of instruction execution after wakeup when entering STOP mode and the control bit is in POCN[3]. If STOP_RST_EN is set to '1', reset state will take place after wakeup; otherwise, next instruction will be executed. Table 5-19 shows the three modes in GPM8F3232A/3216A/3208A.

ii. RESET pin cause exit from stop mode and the processor operation will resume execution at address 0x0000.

	System Clock	Peripheral Clock	Wakeup Source	After Wakeup
RUN Mode	Register setting	Register setting	--	--
IDLE Mode	OFF	ON	1. All wakeup sources 2. All interrupt sources	Next instruction state
STOP Mode	OFF	OFF	1. All wakeup sources	Reset state or next instruction state base on PCON[3]

Table 5-19 The three operation modes for GPM8F3232A/3216A/3208A

PCON			**Address: 0x87**		**Power Configuration Register**			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	--	CPU_IDLE	PWE	STOP_RST_EN	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	--	R/W	Reserved	
5	CPU_IDLE	R/W	IDLE mode enable bit 0: IDLE mode disabled ; 1: IDLE mode entered	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3	STOP_RST_EN	R/W	Wakeup state selection bit 0: Next instruction state after wakeup 1: Reset state afer wakeup	
2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-20 The PCON register

WKUEN			**Address: 0xB6**		**Wake Up Enable Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	INT6_WKUEN	INT5_WKUEN	INT4_WKUEN	INT3_WKUEN	--	INT1_WKUEN	INT0_WKUEN
Default	0	0	0	0	0	1	1	1
Key Code	AF, 50							

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	INT6_WKUEN	R/W	INT6 PAD wake up enable control, active high	
5	INT5_WKUEN	R/W	INT5 PAD wake up enable control, active high	
4	INT4_WKUEN	R/W	INT4 PAD wake up enable control, active high	
3	INT3_WKUEN	R/W	INT3 PAD wake up enable control, active high	
2	--	R/W	Reserved	
1	INT1_WKUEN	R/W	INT1 PAD wake up enable control, active high	
0	INT0_WKUEN	R/W	INT0 PAD wake up enable control, active high	

Table 5-21 The WKUEN register

5.6. Interrupt System

5.6.1. Introduction

The GPM8F3232A/3216A/3208A provides 14/14/12 types of interrupt sources (including 11 interrupt sources of standard 8051 and additional 3/3/1 interrupt sources) with two levels interrupt priority control which tabled in Table 5-22. For standard 8051 interrupt sources, each interrupt can be in high or low level priority group by setting or clearing a bit in the IP(0xB8) and EIP(0xF8) registers. INT0 has the top priority in default state and user can choose the related interrupt source to be the top priority by IP register. For additional interrupt sources, high or low level priority group is set or cleared a bit in the BIP(0x96).

Interrupt requests are sampled each system clock at the rising edge of clock control. Each interrupt vector can be individually enabled or disabled by setting or clearing a corresponding bit in the IE(0xA8), EIE(0xE8). The IE contains global interrupt system disable(0) / enable(1) bit called EA. In general, once an interrupt event occurs, the corresponding flag bit will be set. The related registers of interrupt flag are described as below.

If the related interrupt control bit is set to enable interrupt, an interrupt request signal will be generated and then CPU executes service routine. If the related interrupt control bit is disabled, programmer still can observe the corresponding flag bit, but no interrupt request signal will be generated. The interrupt flag bits must be cleared in the interrupt service routine to prevent program from deadlock in interrupt service routine. With any instruction, interrupts pending during the previous instruction is served. Before entering interrupt service routine, the system saves the current PC address into top of stack pointer and jumps to corresponding vector to execute the interrupt service. After finishing the interrupt service, the system abstract the return PC address from the top of the stack to execute the following instruction.

As to additional six interrupt sources, each interrupt vector can be individually enabled or disabled by setting or clearing a corresponding bit in the AUDCON(0xB3), ADCON(0xF1) and RSTCON(0x8F). The corresponding flag can be found in BIF(0x97), and ADCON(0xF1). For more detailed description, please refer to related block.

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Vector number	Priority
IE0	Device pin INT 0	Low/Falling	Hardware	0x03	0	1
TF0	Internal Timer 0	--	Hardware	0x0B	1	2
IE1	Device pin INT 1	Low/Falling	Hardware	0x13	2	3
TF1	Internal Timer 1	--	Hardware	0x1B	3	4
AUDIOF TI0 & RI0	AUDIO interrupt Internal UART0	--	Software(cleared by 1) Software(cleared by 0)	0x23	4	5
TF2 EXF2	Internal Timer2 Timer2 external reload	--	Software(cleared by 0) Software(cleared by 0)	0x2B	5	6
ADCF	ADC interrupt	--	Software(cleared by 1)	0x33	6	7
Reserved	--	--	--	0x3B	7	8
INT3F	Device pin /INT3 Internal Compare 0	Low	Hardware Software(cleared by 1)	0x43	8	9

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Vector number	Priority
INT4F	Device pin /INT4 Internal Compare 1	Low	Hardware Software(cleared by 1)	0x4B	9	10
INT5F	Device pin /INT5 Internal Compare 2	Falling	Software(cleared by 1) Software(cleared by 1)	0x53	10	11
INT6F	Device pin /INT6 Internal Compare 3	Falling	Software(cleared by 1) Software(cleared by 1)	0x5B	11	12
WDIF	Internal Watchdog	--	Software(cleared by 0)	0x63	12	13
MERRF	Memory access Error	--	Software(cleared by 1)	0x6B	13	14

Note1: Interrupt is also generated at falling edge of T2EX pin, while EXEN2 bit is set. This interrupt doesn't set TF2 flag, but EXF2 only and uses 0x2B vector.
Note2: External interrupt pins are activated at low level or by a falling edge.

Table 5-22 Summaries of all interrupt sources

IP			Address: 0xB8		Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	PT2	PS0	PT1	PX1	PT0	PX0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	PT2	R/W	Timer 2 priority level control (1: high level)	
4	PS0	R/W	UART0 priority level control (1: high level)	
3	PT1	R/W	Timer 1 priority level control (1: high level)	
2	PX1	R/W	INT1 priority level control (1: high level)	
1	PT0	R/W	Timer 0 priority level control (1: high level)	
0	PX0	R/W	INT0 priority level control (1: high level)	

Table 5-23 IP register

EIP			Address: 0xF8		Extended Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	PWDI	PINT6	PINT5	PINT4	PINT3	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	--	R/W	Reserved	
5	PWDI	R/W	Watchdog priority level control (1: high level)	
4	PINT6	R/W	INT6/Compare3 priority level control (1: high level)	
3	PINT5	R/W	INT5/Compare2 priority level control (1: high level)	
2	PINT4	R/W	INT4/Compare1 priority level control (1: high level)	
1	PINT3	R/W	INT3/Compare0 priority level control (1: high level)	
0	--	R/W	Reserved	

Table 5-24 EIP register

BIP			Address: 0x96		Additional Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	PAUDIO	PADC	--	--	PMERR
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	--	R/W	Reserved	
5	--	R/W	Reserved	
4	PAUDIO	R/W	AUDIO priority level control (1: high level)	
3	PADC	R/W	ADC priority level control (1: high level)	
2	--	R/W	Reserved	
1	--	R/W	Reserved	
0	PMERR	R/W	MERR priority level control (1: high level)	

Table 5-25 BIP register

IE			Address: 0xA8		Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	EA	--	ET2	ES0	ET1	EX1	ET0	EX0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EA	R/W	Enable global interrupts	
6	--	R/W	Reserved	
5	ET2	R/W	Enable Timer 2 interrupt	
4	ES0	R/W	Enable UART0 interrupt	
3	ET1	R/W	Enable Timer 1 interrupt	
2	EX1	R/W	Enable INT1 interrupt	
1	ET0	R/W	Enable Timer 0 interrupt	
0	EX0	R/W	Enable INT0 interrupt	

Table 5-26 IE register

EIE			Address: 0xE8		Extended Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	EWDI	EINT6	EINT5	EINT4	EINT3	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	--	R/W	Reserved	
5	EWDI	R/W	Enable watchdog interrupt	
4	EINT6	R/W	Enable INT6/Compare3 interrupts	
3	EINT5	R/W	Enable INT5/Compare2 interrupts	
2	EINT4	R/W	Enable INT4/Compare1 interrupts	
1	EINT3	R/W	Enable INT3/Compare0 interrupts	

Bit	Function	Type	Description	Condition
0	--	R/W	Reserved	

Table 5-27 EIE register

TCON			Address: 0x88		Timer0/1 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TF1	R/W	Timer 1 interrupt (overflow) flag	
6	TR1	R/W	Timer 1 run control bit 0: disabled ; 1: enabled	
5	TF0	R/W	Timer 0 interrupt (overflow) flag	
4	TR0	R/W	Timer 0 run control bit 0: disabled ; 1: enabled	
3	IE1	R/W	INT1 interrupt flag	
2	IT1	R/W	INT1 level (at 0) / edge (at 1) sensitivity	
1	IE0	R/W	INT0 interrupt flag	
0	IT0	R/W	INT0 level (at 0) / edge (at 1) sensitivity	

Table 5-28 TCON register

T2IF			Address: 0xC9		Timer 2 Interrupt Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	EXEN2	EXF2	TF2
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2	EXEN2	R/W	Timer 2 external reload interrupt enable 0: external reload interrupt is disabled 1: external reload interrupt is enabled.	
1	EXF2	R/W	Timer 2 external reload flag Cleared by the software	
0	TF2	R/W	Timer 2 overflow flag Cleared by the software	

Table 5-29 T2IF register

WDCON			Address: 0xD8		Watchdog Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	WDIF	WTRF	EWT	RWT
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3	WDIF	R/W	Watchdog interrupt flag	

Bit	Function	Type	Description	Condition
2	WTRF	R/W	Watchdog timer reset flag	
1	EWT	R/W	Watchdog timer reset enable bit 0: Disable; 1: Enable	
0	RWT	R/W	Reset watchdog timer 0: NA; 1: Reset	

Table 5-30 WDCON register

SCON0			Address: 0x98		UART0 configuration register			
Bit	7	6	5	4	3	2	1	0
Function	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	SM0[1:0]	R/W	Mode and baud rate setting	
5	SM02	R/W	Enables a multiprocessor communication feature	
4	REN0	R/W	Enable serial reception.	
3	TB08	R/W	The 9th transmitted data bit in Modes 2 and Mode 3	
2	RB08	R/W	In Mode 0, this bit is not used In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 2 and Mode 3, it is the 9th data bit received.	
1	TI0	R/W	UART0 transmitter interrupt flag	
0	RI0	R/W	UART0 receiver interrupt flag	

Table 5-31 SCON0 register

EIF			Address: 0x91		Extended interrupt flag			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	INT6F	INT5F	INT4F	INT3F	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	INT6F	R/W	INT6 interrupt flag	
3	INT5F	R/W	INT5 interrupt flag	
2	INT4F	R/W	INT4 interrupt flag	
1	INT3F	R/W	INT3 interrupt flag	
0	--	R/W	Reserved	

Table 5-32 EIF register

BIF			Address: 0x97		Additional interrupt flag			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	AUDIOF	ADCF	--	--	MERRF
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	

Bit	Function	Type	Description	Condition
5	--	R/W	Reserved	
4	AUDIOF	R/W	AUDIO interrupt flag, cleared by 1	
3	ADCF	R	ADC interrupt flag, cleared by 1 in ADCON register	
2	--	R/W	Reserved	
1	--	R/W	Reserved	
0	MERRF	R/W	IMemory related error interrupt flag, cleared by 1	

Table 5-33 BIF register

5.7. Reset Sources

5.7.1. Introduction

There are eight types of reset sources for GPM8F3232A/3216A/3208A including Power-On Reset (POR), Low Voltage Reset (LVR), Pad Reset (RAD_RST), Watchdog Timer Reset (WDT_RST), Software Reset (S/W_RST), STOP mode Reset (STOP_RST), Flash Error Reset (FLASH_ERR_RST), and missing system clock Reset (MISS_CLK_RST). Figure 5-6 shows the block diagram of each reset source.

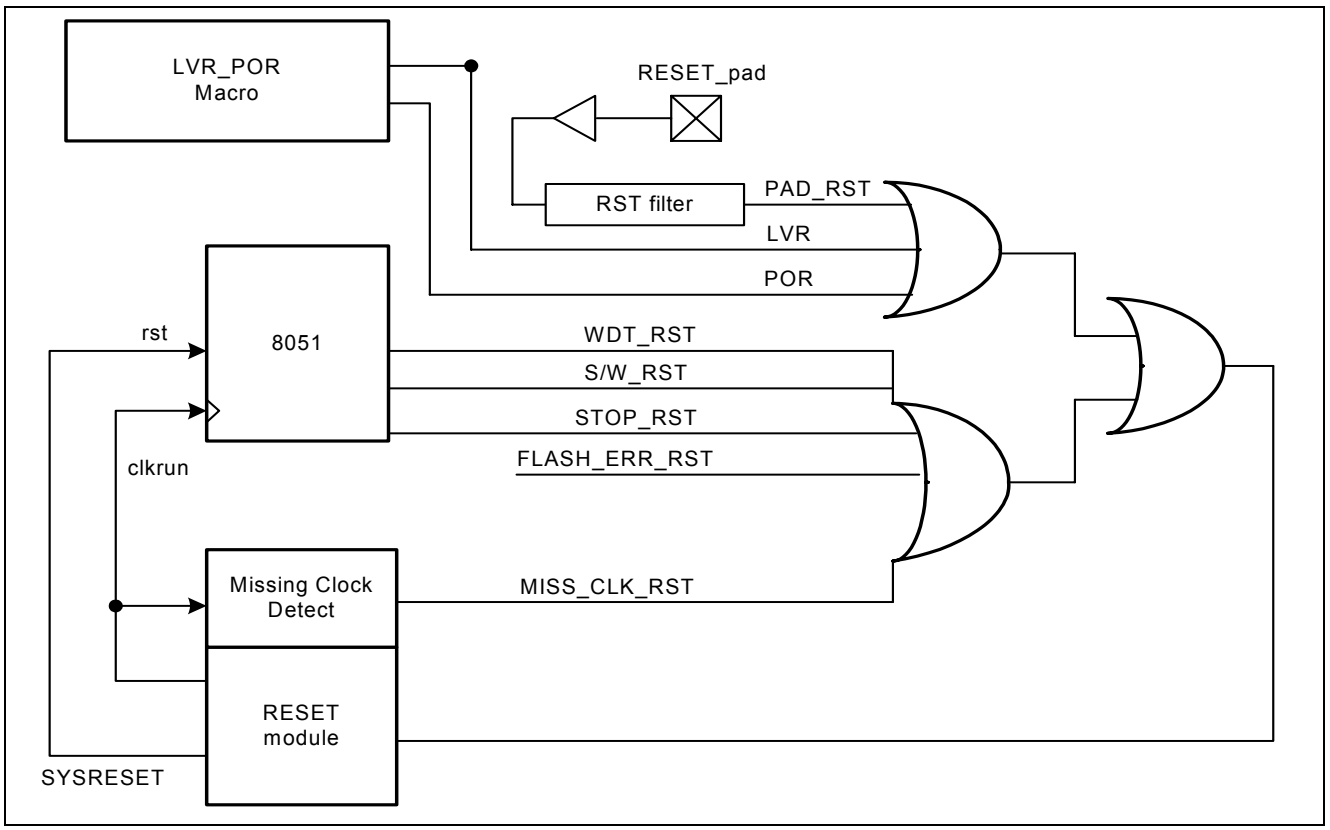


Figure 5-6 Reset sources

5.7.2. Power-On Reset (POR)

A POR is generated when VDD is rising from 0v. When VDD rises to an acceptable level (~1.5V), the power on reset circuit will starts a power-on sequence. After that, the system starts to activate and will operate in target speed. The POR will reset whole chip and registers.

5.7.3. Low Voltage Reset (LVR)

The on-chip Low Voltage Reset (LVR) circuitry forces the system entering reset state when power supplying voltage falls below the specific LVR trigger voltage. This function prevents MCU from working at an invalid operating voltage range.

To enable or disable this function, SYSCON0[7] can be set. If this function is enabled, the LVR circuit will monitor power level while

chip is operating. And the LVR voltage level can be 2.2V or 3.9V by setting CONFIG_BYTE[5] through 2-wire interface. If the power is lower than the specific level for a specific period, the system reset will take place and go to initial state.

5.7.4. Pad Reset (PAD_RST)

The GPM8F3232A/3216A/3208A provides an external pin to force the system returning to its initial status. The RESET pin is high active as shown in Figure 5-7. When the RESET pin equals to VDD, system will be forced to enter reset state, execute instruction from address 0x0000 and all registers go to default state.

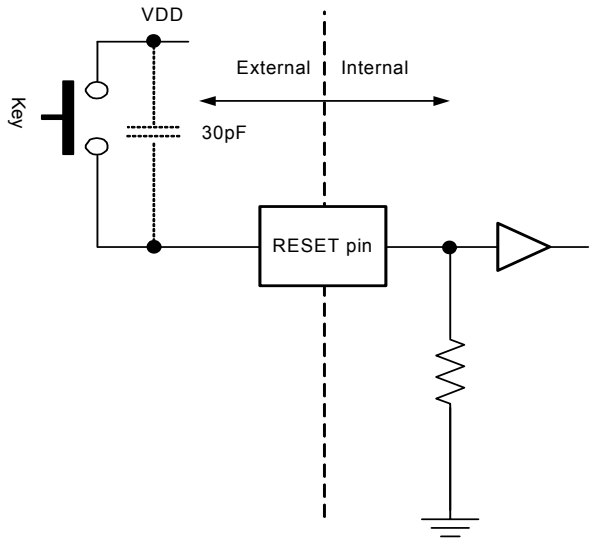


Figure 5-7 Pad reset circuit

5.7.5. Watchdog Timer Reset (WDT_RST)

On-chip watchdog circuitry makes the device entering reset state when MCU goes into unknown state and has no watchdog cleared information. This function prevents the MCU to be stuck in an abnormal condition. The WDT can be enabled or disabled through WDCON register bit 1. At any time prior to reaching its user selected terminal value, software can set the Reset Watchdog Timer (WDCON[0]) bit. If RWT is set before the timeout is reached, the timer will start over. If timeout is reached without RWT being set, the watchdog will reset the CPU. Hardware will automatically clear RWT after software sets it. When the reset occurs, the Watchdog Timer Reset Flag (WDCON[2]) will automatically be set to indicate the cause of the reset, however software must clear this bit manually.

WDCON register is a timed access register that prevent it from accidental writes. TA is located at 0xEB. Correct sequence, 0xAA and 0x55, is required before write to WDCON register. Reading from such register is not protected.

The Watchdog has four timeout selections based on the system clock frequency. The selections are a pre-selected number of clocks and can be set by CKCON[7:6]. Therefore, the actual timeout interval is dependent on the SYSCLK frequency. Figure 5-8 shows the block diagram of Watchdog timer.

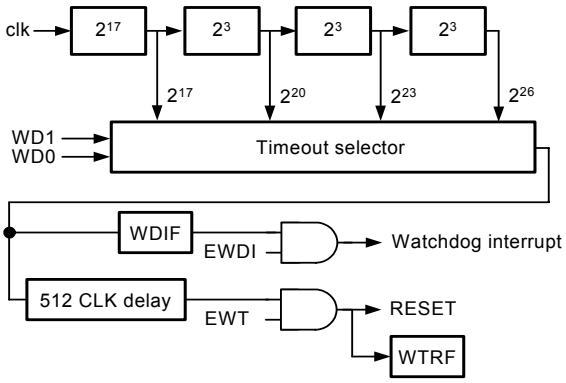


Figure 5-8 The block diagram of Watchdog timer

5.7.6. Other Reset Sources

Other reset sources include Software Reset (S/W_RST), STOP mode Reset (STOP_RST), Flash Error Reset (FLASH_ERR_RST), and missing system clock Reset (MISS_CLK_RST). Software Reset is occurred when writing KEY code to KEYCODE register(0xEF). The key codes are 0x3c and 0xc3. The timing does not matter, but the key codes must be written in order before SW reset is take place. STOP mode Reset is enabled by setting PCON[3] bit. This is the reset when system is reset from STOP mode.

Flash Error Reset is the reset when five flash related errors are arisen. The first error is to execute whole chip erase by software. The second error is to access the wrong address. The third error is when flash is programmed in a wrong way or to program READONLY_PAGE. The forth error is to erase LAST_PAGE and the last error is to program CONFIG_BYTE. Each flash error related reset source can be enabled or disabled by clearing or setting a bit in the RSTCON(0x94) as shown in Table 5-41. The corresponding flag when flash error reset occurs can be observed in FLASHERRF register which is shown in Table 5-42. Missing system clock Reset is the reset when system clock is missed over 4095 IOSC clocks if external crystal is utilized as clock source. There are seven reset status flag can be monitored by RSTSTS register which is shown as Table 5-43.

CONFIG_BYTE			Address: 0xB7		CONFIG_BYTE Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	LVRVSEL	--	--	--	IOSEL	CODE Lock
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:6	--	R	Reserved	
5	LVRVSEL	R	LVR voltage level selection 0: 3.9V 1: 2.2V	
4:2	--	R	Reserved	
1	IOSEL	R	IO initial state selection bit 0: Input pull high 1: floating	
0	CODE Lock	R	0 : CODE is locked; 1 : CODE is unlocked	

Table 5-34 The CONFIG_BYTE register

SYSCON0			Address: 0xAE		SYSTEM control0 Register			
Bit	7	6	5	4	3	2	1	0
Function	LVRENB	--	--	AUDIO_N_DIS	--	CLKOUT_EN	CCOUTENB	SCHMIT_DIS_P4
Default	0	0	0	0	0	0	0	0
Key Code	FF,00							

Bit	Function	Type	Description	Condition
7	LVRENB	R/W	LVR enable control 0: enable LVR function 1: disable LVR function	
6:5	--	--	Reserved	
4	AUDIO_N_DIS	R/W	AUDIO_N disable bit available only if audio function is enabled 0: P36/P37 are output simultaneously as AUDIO_N/P 1: Only P37 is output as AUDIO_P	
3	--	--	Reserved	
2	CLKOUT_EN	R/W	Clock output enable bit (SYSCLK is output on P35)	
1	CCOUTENB	R/W	Disable output function of compare mode in Timer2 0: P1[3:1] = {compare3,compare2,compare1} 1: P1[3:1] is GPIO	
0	SCHMIT_DIS_P4	R/W	P4 Schmitt trigger function disable control bit	

Table 5-35 SYSCON0 register

WDCON			Address: 0xD8		Watchdog Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	WDIF	WTRF	EWT	RWT
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3	WDIF	R/W	Watchdog interrupt flag	
2	WTRF	R/W	Watchdog timer reset flag	
1	EWT	R/W	Watchdog timer reset enable bit 0: Disable 1: Enable	
0	RWT	R/W	Reset watchdog timer 0: NA 1: Reset	

Table 5-36 WDCON register

TA			Address: 0xEB		Timed Access Protection Register			
Bit	7	6	5	4	3	2	1	0
Function	Timed Access protection register (0xaa➔0x55)							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
0	TA[7:0]	R/W	Timed Access protection register (0xaa➔0x55)	

Table 5-37 TA register

CKCON			Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	--	T1M	T0M	--	--	--
Default	0	0	0	0	0	0	0	1

Bit	Function	Type	Description	Condition
7:6	WD[1:0]	R/W	Watchdog timeout selection bits WD[1:0] / Watchdog internal / Number of clocks 00 / 2^{17} / 131072 01 / 2^{20} / 1048576 10 / 2^{23} / 8388608 11 / 2^{26} / 67108864	
5	--	R/W	Reserved	
4	T1M	R/W	Division selection of the system clock that drives Timer 1 0: Timer 1 uses a divided-by-12 of the system clock frequency 1: Timer 1 uses a divided-by-4 of the system clock frequency	
3	T0M	R/W	Division selection of the system clock that drives Timer 0 0: Timer 0 uses a divided-by-12 of the system clock frequency 1: Timer 0 uses a divided-by-4 of the system clock frequency	
2:0	--	R/W	Reserved	

Table 5-38 CKCON register

KEYCODE			Address: 0xEF		KEYCODE Register			
Bit	7	6	5	4	3	2	1	0
Function	KC7	KC6	KC5	KC4	KC3	KC2	KC1	KC0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
0	KEYCODE[7:0]	R/W	KEYCODE register	

Note: Some protected registers are needed to write correct key code to KEYCODE register before write data to them.

Table 5-39 KEYCODE register

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	--	CPU_IDLE	PWE	STOP_RST_EN	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	--	R/W	Reserved	
5	CPU_IDLE	R/W	IDLE mode enable bit 0: IDLE mode disabled ; 1: IDLE mode entered	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3	STOP_RST_EN	R/W	Wakeup state selection bit 0: Next instruction state after wakeup 1: Reset state afer wakeup	
2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-40 PCON register

RSTCON			Address: 0x8F		Flash Error RESET Enable Control Register			
Bit	7	6	5	4	3	2	1	0
Function	CB_P_ENB	LP_E_ENB	FLASH_FLOW_ENB	XADDR_ENB	--	CHIP_E_ENB	MISS_CLK_ENB	FLASH_ERR__ENB
Default	0	0	0	1	0	0	0	0
Key Code	4F,72,7A							

Bit	Function	Type	Description	Condition
7	CB_P_ENB	R/W	CONFIG_BYTE program reset disable control bit	
6	LP_E_ ENB	R/W	LAST_PAGE erase reset disable control bit	
5	FLASH_FLOW_ ENB	R/W	Error flash flow/READONLY_PAGE program reset disable control bit	
4	XADDR_ENB	R/W	Error flash address access reset disable control bit	
3	--	R/W	Reserved	

Bit	Function	Type	Description	Condition
2	CHIP_E_ ENB	R/W	Whole chip erase reset disable control bit	
1	MISS_CLK _ ENB	R/W	Miss clock reset disable control bit	
0	FLASH_ERR _ ENB	R/W	Global Flash related error reset disable control bit	

Table 5-41 RSTCON register

FLASHERRF			Address: 0xA6		Flash Error RESET Status Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	CB_P_F	LP_E_F	FLASH_FLOW_F	XADDR_F	--	CHIP_E_F	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CB_P_F	R/W	Error CONFIG_BYTE program reset flag	
6	LP_E_F	R/W	Error LAST_PAGE erase reset flag	
5	FLASH_FLOW_F	R/W	Error flash flow/ READONLY_PAGE program reset flag	
4	XADDR_F	R/W	Error flash address access reset flag	
3	--	R/W	Reserved	
2	CHIP_E_F	R/W	Error Macro erase reset flag	
1	--	R/W	Reserved	
0	--	R/W	Reserved	

Table 5-42 FLASHERRF register

RSTSTS			Address: 0x94		RESET Status Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	--	MISS_CLK_RST	STOP_RST	FLASH_ERR_RST	S/W_RST	WDT_RST	LVR_RST	RAD_RST
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	MISS_CLK_RST	R/W	RESET from system clock missing clock	
5	STOP_RST	R/W	RESET from STOP mode	
4	FLASH_ERR_RST	R/W	RESET from FLASH error	
3	SW_RST	R/W	RESET from SW RST	
2	WDT_RST	R/W	RESET from WDT	
1	LVR_RST	R/W	RESET from LVR	
0	PAD_RST	R/W	RESET from RESET PAD	

Table 5-43 RSTSTS register

5.8. I/O Ports

5.8.1. Introduction

The GPM8F3232A/3216A/3208A has five ports, including standard Port 0, Port 1, Port 2, Port 3 and additional Port 4. These port pins may be multiplexed with an alternate function for the peripheral features on the device. In general, when an initial reset state occurs, all ports are used as a general purpose input port with open-drain structure and Schmitt trigger function. User can change IO initial state by CONFIG_BYTE[1] through the SCK/SDA interface. The Schmitt trigger function can be controlled by SYSCON2[3:0] and SYSCON0[0]. All the input ports can be programmable pull high/low by PU and PD registers. The PU and PD registers of Port 0 are controlled by 0x9A and 0x9B, the PU and PD registers of Port 1 are controlled by 0x9C and 0x9D, the PU and PD registers of Port 2 are controlled by 0x9E and 0x9F, the PU and PD registers of P3 are controlled by 0xA2 and 0xA3 and the PU and PD registers of P4 are controlled by 0xA4 and 0xA5. Read and write accesses to the I/O port are performed via their corresponding SFRs, P0(0x80), P1(0x90), P2(0xA0), P3(0xB0) and P4(0xA1). When PU and PD are enabled at the same time, the port can output high or low depending on the data. Table 5-44 and Table 5-45 show the truth table of analog pad and digital pad respectively. In GPM8F3232A/3216A/3208A, P0[7:0], and P2[6:5] can be analog pad for special function. P0[7:0] are used for ADC input. P2[6:5] are used for external crystal input and output. The detailed descriptions of analog function are in corresponding sections. The built-in pull high/low resister is 50KΩ. In addition, there is a register, SRCON, for slew rate control (0xAD) of P0~P4. If IO ports are needed to change immediately without slew rate control, the corresponding control bit of each port can be set to '0'. The default state of SRCON register is '0xFF' with 30ns slew rate control. Figure 5-9 and Figure 5-10 show the block diagrams of analog pad and digital pad respectively.

PU	PD	DATA	ADAEN	PAD
0	0	0	0	Driving Low
0	0	1	0	Floating
0	1	0	0	Driving Low
0	1	1	0	Pull low
1	0	0	0	Illegal
1	0	1	0	Pull high
1	1	0	0	Driving Low
1	1	1	0	Driving High
x	x	x	1	Floating

Table 5-44 The truth table of analog pad

PU	PD	DATA	PAD
0	0	0	Driving Low
0	0	1	Floating
0	1	0	Driving Low
0	1	1	Pull low
1	0	0	Illegal
1	0	1	Pull high
1	1	0	Driving Low
1	1	1	Driving High

Table 5-45 The truth table of digital pad

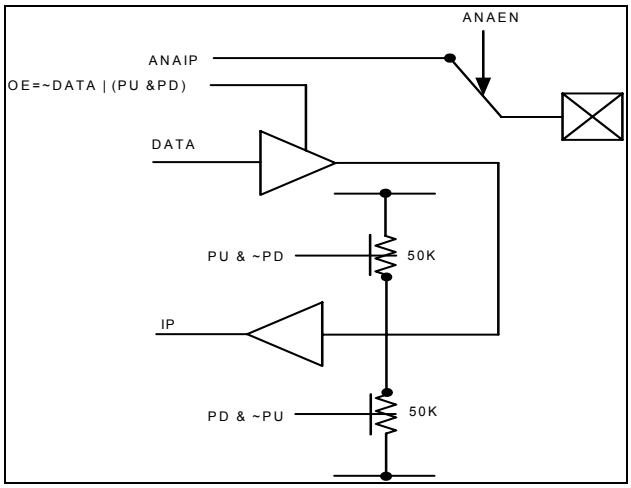


Figure 5-9 The block diagram of analog pad

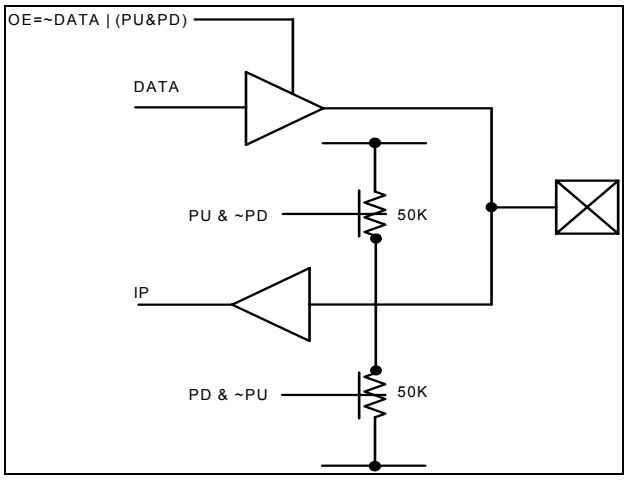


Figure 5-10 The block diagram of digital pad

CONFIG_BYTE			Address: 0xB7		CONFIG_BYTE Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	LVRVSEL	--	--	--	IOSEL	CODE Lock
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:6	--	R	Reserved	
5	LVRVSEL	R	LVR voltage level selection 0: 3.9V 1: 2.2V	
4:2	--	R	Reserved	
1	IOSEL	R	IO initial state selection bit 0: Input pull high 1: floating	
0	CODE Lock	R	0 : CODE is locked; 1 : CODE is unlocked	

Table 5-46 The CONFIG_BYTE register

P0			Address: 0x80		Port0 Register			
Bit	7	6	5	4	3	2	1	0
Function	P07	P06	P05	P04	P03	P02	P01	P00
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P0[7:0]	R/W	Port0	

Table 5-47 P0 register

P1			Address: 0x90		Port1 Register			
Bit	7	6	5	4	3	2	1	0
Function	P17	P16	P15	P14	P13	P12	P11	P10
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P1[7:0]	R/W	Port1	

Table 5-48 P1 register

P2			Address: 0xA0		Port2 Register			
Bit	7	6	5	4	3	2	1	0
Function	P27	P26	P25	P24	P23	P22	P21	P20
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P2[7:0]	R/W	Port2	

Table 5-49 P2 register

P3			Address: 0xB0		Port3 Register			
Bit	7	6	5	4	3	2	1	0
Function	P37	P36	P35	P34	P33	P32	P31	P30
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P3[7:0]	R/W	Port3	

Table 5-50 P3 register

P4			Address: 0xA1		Port4 Register			
Bit	7	6	5	4	3	2	1	0
Function	P47	P46	P45	P44	P43	P42	P41	P40
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P4[7:0]	R/W	Port4	

Table 5-51 P4 register

P0_PU			Address: 0x9A		Port0 pull up configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P07_PU	P06_PU	P05_PU	P04_PU	P03_PU	P02_PU	P01_PU	P00_PU
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P0_PU[7:0]	R/W	Port0 pull up control bits 0: floating; 1: pull up	

Table 5-52 P0_PU register

P0_PD			Address: 0x9B		Port0 pull down configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P07_PD	P06_PD	P05_PD	P04_PD	P03_PD	P02_PD	P01_PD	P00_PD
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_PD[7:0]	R/W	Port0 pull down control bits 0: floating 1: pull down	

Note: If P0_PU and P0_PD are setting to '1' simultaneously, P0 will be output mode

Table 5-53 P0_PD register

P1_PU			Address: 0x9C		Port1 pull up configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P17_PU	P16_PU	P15_PU	P14_PU	P13_PU	P12_PU	P11_PU	P10_PU
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P1_PU[7:0]	R/W	Port1 pull up control bits 0: floating 1: pull up	

Table 5-54 P1_PU register

P1_PD			Address: 0x9D		Port1 pull down configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P17_PD	P16_PD	P15_PD	P14_PD	P13_PD	P12_PD	P11_PD	P10_PD
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P1_PD[7:0]	R/W	Port1 pull down control bits 0: floating 1: pull down	

Note: If P1_PU and P1_PD are setting to '1' simultaneously, P1 will be output mode.

Table 5-55 P1_PD register

P2_PU			Address: 0x9E		Port2 pull up configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P27_PU	P26_PU	P25_PU	P24_PU	P23_PU	P22_PU	P21_PU	P20_PU
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P2_PU[7:0]	R/W	Port2 pull up control bits 0: floating 1: pull up	

Table 5-56 P2_PU register

P2_PD			Address: 0x9F		Port2 pull down configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P27_PD	P26_PD	P25_PD	P24_PD	P23_PD	P22_PD	P21_PD	P20_PD
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_PD[7:0]	R/W	Port2 pull down control bits 0: floating 1: pull down	

Note: If P2_PU and P2_PD are setting to '1' simultaneously, P2 will be output mode

Table 5-57 P2_PD register

P3_PU			Address: 0xA2		Port3 pull up configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P37_PU	P36_PU	P35_PU	P34_PU	P33_PU	P32_PU	P31_PU	P30_PU
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P3_PU[7:0]	R/W	Port3 pull up control bits 0: floating 1: pull up	

Table 5-58 P3_PU register

P3_PD			Address: 0xA3		Port3 pull down configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P37_PD	P36_PD	P35_PD	P34_PD	P33_PD	P32_PD	P31_PD	P30_PD
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P3_PD[7:0]	R/W	Port3 pull down control bits 0: floating 1: pull down	

Note: If P3_PU and P3_PD are setting to '1' simultaneously, P3 will be output mode.

Table 5-59 P3_PD register

P4_PU			Address: 0xA4		Port4 pull up configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P47_PU	P46_PU	P45_PU	P44_PU	P43_PU	P42_PU	P41_PU	P40_PU
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P4_PU[7:0]	R/W	Port4 pull up control bits 0: floating 1: pull up	

Table 5-60 P4_PU register

P4_PD			Address: 0xA5		Port4 pull down configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P47_PD	P46_PD	P45_PD	P44_PD	P43_PD	P42_PD	P41_PD	P40_PD
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P4_PD[7:0]	R/W	Port4 pull down control bits 0: floating; 1: pull down	

Note: If P4_PU and P4_PD are setting to '1' simultaneously, P4 will be output mode.

Table 5-61 P4_PD register

SRCON			Address: 0xAD		Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P4_SR	P3_SR	P2_SR	P1_SR	P0_SR
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	P4_SR	R/W	Port4 slew rate control bit 0: slew rate control disable 1: slew rate control enable 30ns	
3	P3_SR	R/W	Port3 slew rate control bit 0: slew rate control disable 1: slew rate control enable 30ns	
2	P2_SR	R/W	Port2 slew rate control bit 0: slew rate control disable 1: slew rate control enable 30ns	
1	P1_SR	R/W	Port1 slew rate control bit 0: slew rate control disable 1: slew rate control enable 30ns	
0	P0_SR	R/W	Port0 slew rate control bit 0: slew rate control disable 1: slew rate control enable 30ns	

Table 5-62 SRCON register

SYSCON2			Address: 0xA7		SYSTEM control2 Register			
Bit	7	6	5	4	3	2	1	0
Function	ADCLKX2	--	INT_filter_en	GPIO_SSO	SCHMIT_DIS_P3	SCHMIT_DIS_P2	SCHMIT_DIS_P1	SCHMIT_DIS_P0
Default	0	0	0	0	0	0	0	0
Key Code	FF,00							

Bit	Function	Type	Description	Condition
7	ADCLKX2	R/W	ADCLK double enable bit	
6	--	R/W	Reserved	
5	INT_filter_en	R/W	INT0~INT2 pad filter enable bit 0: no filter 1: 2us	
4	GPIO_SSO	R/W	GPIO SSO function enable bit (Avoid GPIO change simultaneously)	
3	SCHMIT_DIS_P3	R/W	P3 Schmitt trigger function disable control bit	
2	SCHMIT_DIS_P2	R/W	P2 Schmitt trigger function disable control bit	
1	SCHMIT_DIS_P1	R/W	P1 Schmitt trigger function disable control bit	
0	SCHMIT_DIS_P0	R/W	P0 Schmitt trigger function disable control bit	

Table 5-63 SYSCON2 register

SYSCON0			Address: 0xAE		SYSTEM control0 Register			
Bit	7	6	5	4	3	2	1	0
Function	LVRENB	--	--	AUDIO_N_DIS	--	CLKOUT_EN	CCOUTENB	SCHMIT_DIS_P4
Default	0	0	0	0	0	0	0	0
Key Code	FF,00							

Bit	Function	Type	Description	Condition
7	LVRENB	R/W	LVR enable control 0: enable LVR function 1: disable LVR function	
6:5	--	--	Reserved	
4	AUDIO_N_DIS	R/W	AUDIO_N disable bit available only if audio function is enabled 0: P36/P37 are output simultaneously 1: Only P37 is output	
3	--	--	Reserved	
2	CLKOUT_EN	R/W	Clock output enable bit (SYSCLK is output on P35)	
1	CCOUTENB	R/W	Disable output function of compare mode in Timer2 0: P1[3:1] = {compare3,compare2,compare1} 1: P1[3:1] is GPIO	
0	SCHMIT_DIS_P4	R/W	P4 Schmitt trigger function disable control bit	

Table 5-64 SYSCON0 register

ADAEN			Address: 0xF3		ADC analog PAD enable Register			
Bit	7	6	5	4	3	2	1	0
Function	P07_AEN	P06_AEN	P05_AEN	P04_AEN	P03_AEN	P02_AEN	P01_AEN	P00_AEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	P07_AEN	R/W	P07 analog PAD enable control bit 0: P07 can be I/O PAD 1: P07 can be analog PAD	
6	P06_AEN	R/W	P06 analog PAD enable control bit 0: P06 can be I/O PAD 1: P06 can be analog PAD	
5	P05_AEN	R/W	P05 analog PAD enable control bit 0: P05 can be I/O PAD 1: P05 can be analog PAD	
4	P04_AEN	R/W	P04 analog PAD enable control bit 0: P04 can be I/O PAD 1: P04 can be analog PAD	
3	P03_AEN	R/W	P03 analog PAD enable control bit 0: P03 can be I/O PAD 1: P03 can be analog PAD	
2	P02_AEN	R/W	P02 analog PAD enable control bit 0: P02 can be I/O PAD 1: P02 can be analog PAD	
1	P01_AEN	R/W	P01 analog PAD enable control bit 0: P01 can be I/O PAD 1: P01 can be analog PAD	
0	P00_AEN	R/W	P00 analog PAD enable control bit 0: P00 can be I/O PAD 1: P00 can be analog PAD	

Table 5-65 ADAEN register

IOSCCON			Address: 0xF9		IOSC Control Register			
Bit	7	6	5	4	3	2	1	0
Function	XTO_AEN	XTI_AEN	XTAL_PAD_EN	OSC_SEL[1:0]		CLKDIV[2:0]		
Default	0	0	0	0	1	0	0	1

Bit	Function	Type	Description
7	XTO_AEN	R/W	XTO analog PAD enable control bit 0: XTO can be I/O PAD 1: XTO can be analog PAD
6	XTI_AEN	R/W	XTI analog PAD enable control bit 0: XTI can be I/O PAD 1: XTI can be analog PAD
5	XTAL_PAD_EN	R/W	If using XTAL or ECLK, XTAL_PAD_EN should be set first for OSC_SEL selection.
4:3	OSC_SEL[1:0]	R/W	00: Internal ROSC 01: Internal ROSC 10: XTAL 11: External CLK If using XTAL, OSC_SEL[1](XTAL_EN) should be set after XOSC_CLK is stable
2:0	CLK_DIV	R/W	System Clock source divider CLK_DIV: Clock control 000: SYSCLK_source 001: SYSCLK_source/2 010: SYSCLK_source/4 011: SYSCLK_source/8 100: SYSCLK_source/16 101: SYSCLK_source/32 110: SYSCLK_source/64 111: SYSCLK_source/1.5

Table 5-66 The IOSCCON register

5.9. Timer Module

5.9.1. Introduction

GPM8F3232A/3216A/3208A is equipped with three timers. They are Timer 0, Timer 1 and Timer 2 respectively. In addition, Timer 2 also features Compare/Capture/Reload function. All of these three timers are up-count timers and 16-bit timer/counters. Each timer's function is described in the following sections.

5.9.2. Timer 0/1

Timer 0 and Timer 1 are fully compatible with the standard 8051 timers. Each timer consists of two 8-bit registers TH0(0x8C), TL0(0x8A), TH1(0x8D), TL1(0x8B). Timers 0 and Timer 1 work in the same three modes except for mode 3 and the related control registers are TMOD(0x89), TCON(0x88) and CKCON(0x8E) registers. In the timer mode, timer registers are incremented every 4/12 SYSCLK periods depends on CKCON(0x8E) setting, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on theirs corresponding input pins: T0 or T1. The input pins are sampled every CLK period.

TH0			Address: 0x8C		Timer0 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH0[7:0]	R/W	Timer 0 Load value – high byte	

Table 5-67 TH0 register

TL0			Address: 0x8A		Timer0 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL0[7:0]	R/W	Timer 0 Load value – low byte	

Table 5-68 TL0 register

TH1			Address: 0x8D		Timer1 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH1[7:0]	R/W	Timer 1 Load value – high byte	

Table 5-69 TH1 register

TL1			Address: 0x8B		Timer1 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL1[7:0]	R/W	Timer 1 Load value – low byte	

Table 5-70 TL1 register

TMOD			Address: 0x89		Timer0/1 Control Mode Register			
Bit	7	6	5	4	3	2	1	0
Function	GATE1	CT1	M11	M10	GATE0	CT0	M01	M00
Default	0	0	0	0	0	1	0	0

Bit	Function	Type	Description	Condition
7	GATE1	R/W	Gating control 0: Timer 1 enabled while TR1 control bit is set 1: Timer 1 enabled while GATE1 pin is high and TR1 control bit is set	
6	CT1	R/W	Counter or timer select bit 0: Timer mode, internally clocked 1: Counter mode, Timer 1 clock source is from T1 pin	
5:4	M1[1:0]	R/W	Mode select bits of timer 1, which is tabled as Table 5-72	
3	GATE0	R/W	Gating control 0: Timer 0 enabled while TR0 control bit is set 1: Timer 0 enabled while GATE0 pin is high and TR0 control bit is set	
2	CT0	R/W	Counter or timer select bit 0: Timer mode, internally clocked 1: Counter mode, Timer 0 clock source is from T0 pin	
1:0	M0[1:0]	R/W	Mode select bits of timer 0, which is tabled as Table 5-72	

Table 5-71 TMOD register

M1	M0	Mode	Function description
0	0	0	TH0/1 operates as 8-bit timer/counter with a divide by 32 pre-scaler served by lower 5-bit of TL0/1.
0	1	1	16-bit timer/counter. TH0/1 and TL0/1 are cascaded
1	0	2	TL0/1 operates as 8-bit timer/counter with 8-bit auto-reload by TH0/1
1	1	3	TL0 is configured as 8-bit timer/counter controlled by the standard Timer 0 bits. TH0 is an 8-bit timer controlled by the Timer 1 controls bits. Timer 1 holds its count.

Table 5-72 Four modes of Timer 0 and Timer 1

TCON			Address: 0x88		Timer0/1 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TF1	R/W	Timer 1 interrupt (overflow) flag	
6	TR1	R/W	Timer 1 run control bit 0: disabled ; 1: enabled	
5	TF0	R/W	Timer 0 interrupt (overflow) flag	
4	TR0	R/W	Timer 0 run control bit 0: disabled ; 1: enabled	
3	IE1	R/W	INT1 interrupt flag	
2	IT1	R/W	INT1 level (at 0)/ edge (at 1) sensitivity	
1	IE0	R/W	INT0 interrupt flag	
0	IT0	R/W	INT0 level (at 0)/ edge (at 1) sensitivity	

Table 5-73 TCON register

CKCON			Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	--	T1M	T0M	MD2	MD1	MD0
Default	0	0	0	0	0	0	0	1

Bit	Function	Type	Description	Condition
7:6	WD[1:0]	R/W	Watchdog timeout selection bits WD[1:0] / Watchdog internal / Number of clocks 00 / 2^{17} / 131072 01 / 2^{20} / 1048576 10 / 2^{23} / 8388608 11 / 2^{26} / 67108864	
5	--	R/W	Reserved	
4	T1M	R/W	Division selection of the system clock that drives Timer 1 0: Timer 1 uses a divide-by-12 of the system clock frequency 1: Timer 1 uses a divide-by-4 of the system clock frequency	
3	T0M	R/W	Division selection of the system clock that drives Timer 0 0: Timer 0 uses a divide-by-12 of the system clock frequency 1: Timer 0 uses a divide-by-4 of the system clock frequency	
2:0	--	R/W	Reserved	

Table 5-74 CKCON register

5.9.2.1. Timer 0: Mode 0 (13-Bit Timer/Counter)

In this mode, Timer 0 is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer 0 interrupt flag TF0 is set. The counted input is enabled to the Timer 0 when TR0(TCON[4]) = 1 and either GATE0(TMOD[3]) = 0 or GATE0 input pin(P36)= 1. (Setting GATE0(TMOD[3]) = 1 allows the Timer 0 to be controlled by external input GATE0(P36), to facilitate pulse width measurements). The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Figure 5-11 shows the block diagram of Timer 0 for Mode 0.

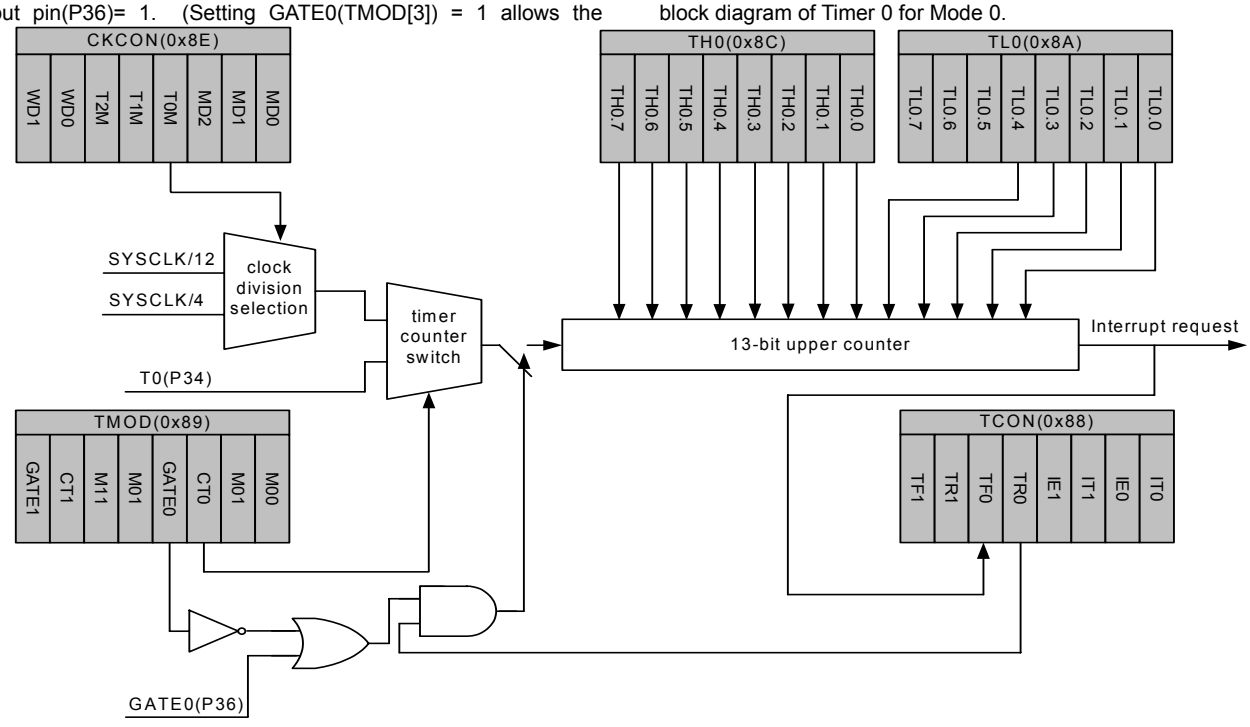


Figure 5-11 The block diagram of Timer 0 for Mode 0

5.9.2.2. Timer 0: Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. The block diagram of Mode 1 is shown in Figure 5-12.

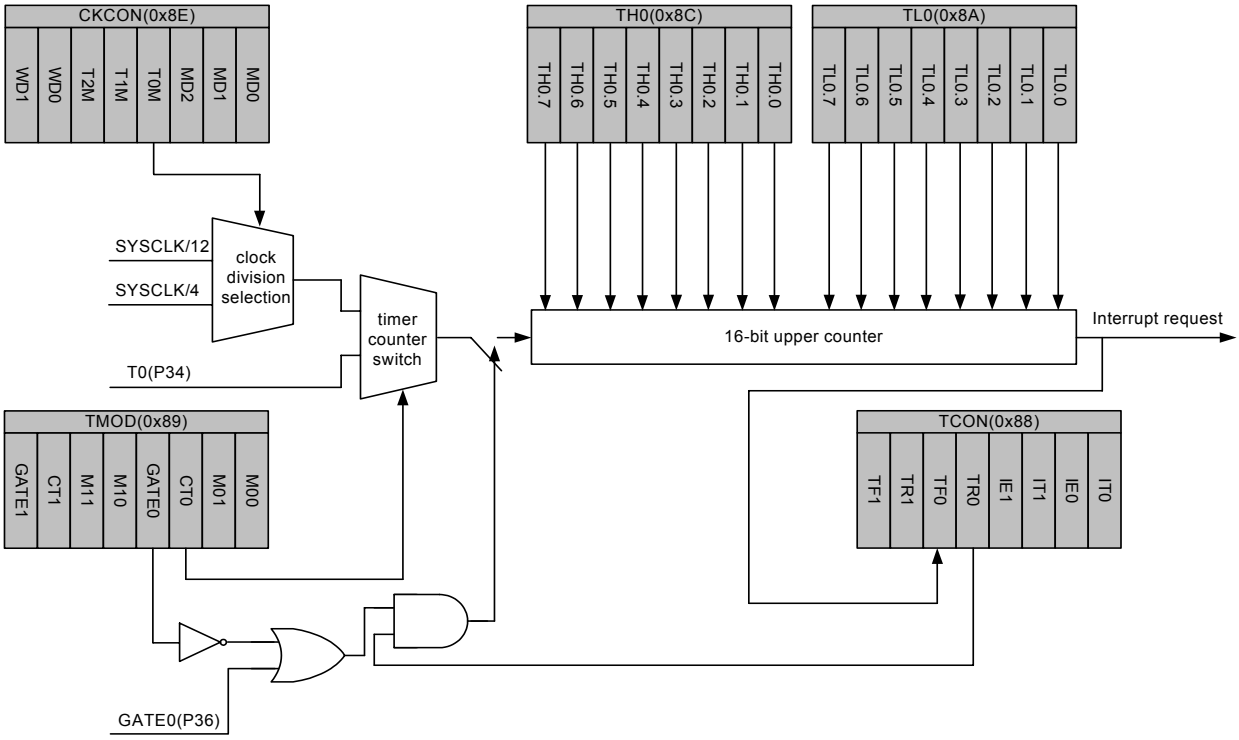


Figure 5-12 The block diagram of Timer 0 for Mode 1

5.9.2.3. Timer 0: Mode 2 (8-bit Timer/Counter with Auto-reloadable Function)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reloads, as shown in Figure 5-13. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is loaded by software. The reload leaves TH0 unchanged.

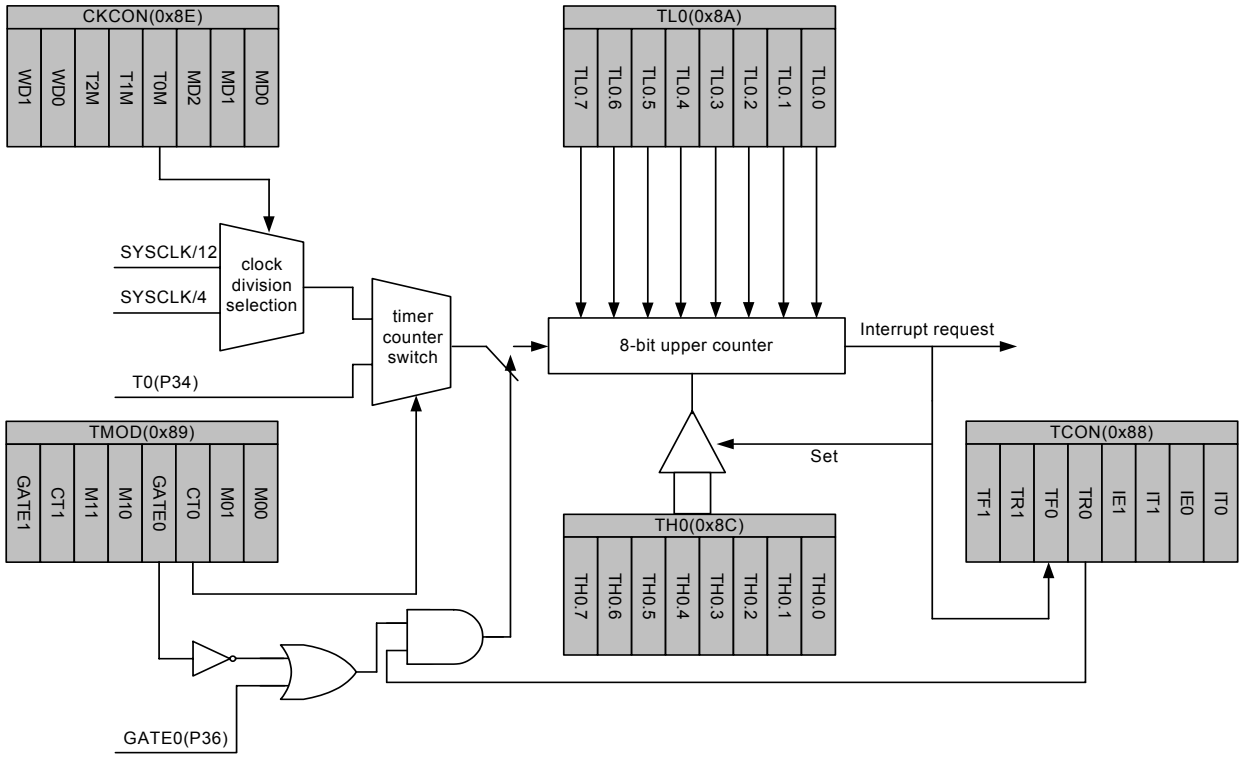


Figure 5-13 The block diagram of Timer 0 for Mode 2

5.9.2.4. Timer 0: Mode 3 (Two 8-Bit Timers/Counters)

Timer 0 in Mode 3 establishes TL0 and TH0 as two separated counters. The block diagram for Mode 3 on Timer 0 is shown in Figure 5-14. TL0 uses the Timer 0 control bits: CT0, GATE0, TR0, and TF0. TH0 is locked into a timer function and uses the TR1 and TF1 flags from Timer 1 and controls Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer/counter. When Timer 0 is in Mode 3, Timer 1 can be turned off by switching it into its own Mode 3, or can still be used by the serial channel as a baud rate generator, or in any application where interrupt from Timer 1 is not required.

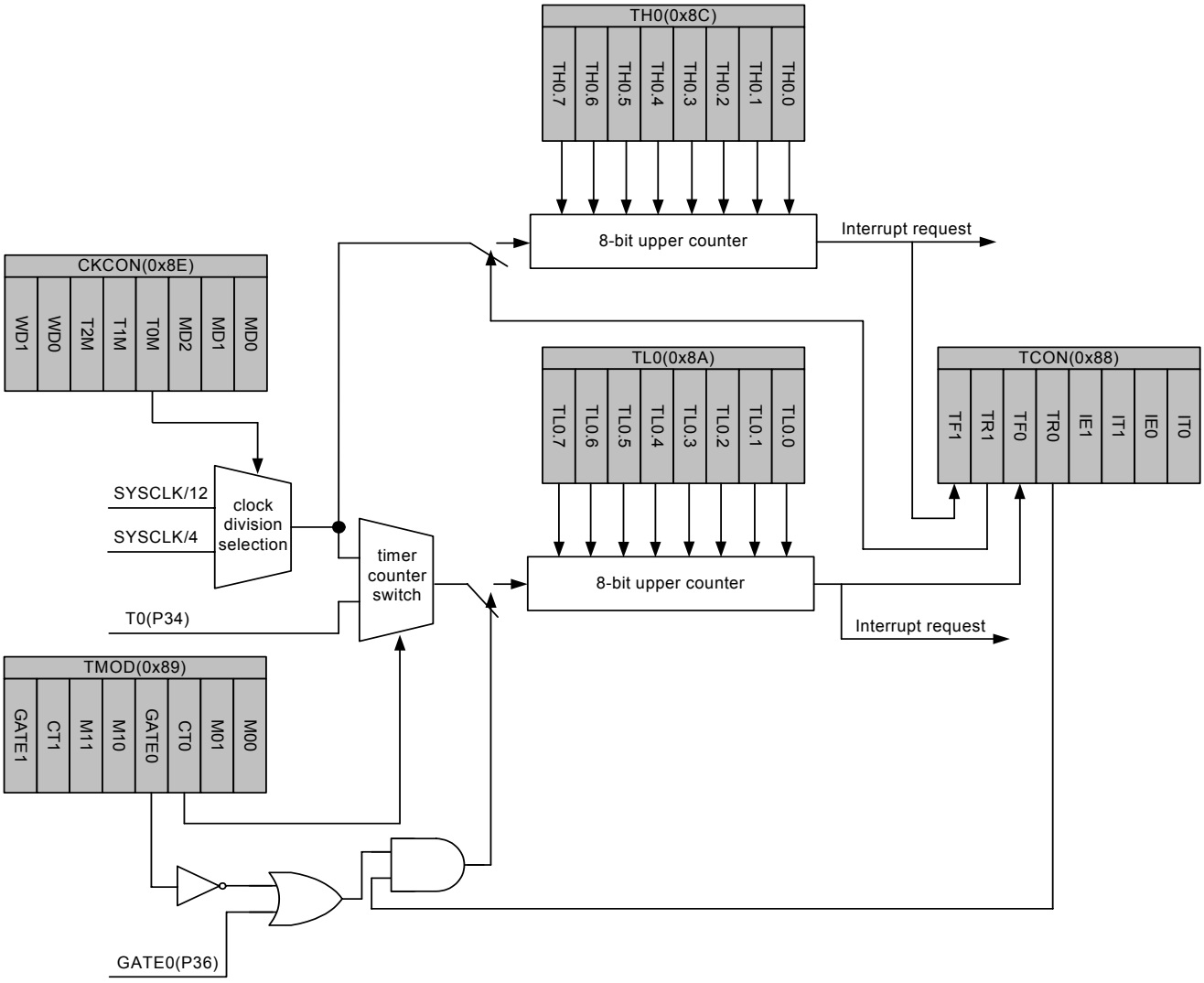


Figure 5-14 The block diagram of Timer 0 for Mode 3

5.9.2.5. Timer 1: Mode 0 (13-Bit Timer/Counter)

In this mode, the Timer 1 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer 1 interrupt flag TF1 is set. The counted input is enabled to the Timer1 when TR1(TCON[6]) = 1 and either GATE1(TMOD[7]) = 0 or GATE1 input pin(P37)= 1. (Setting GATE1(TMOD[7]) = 1 allows the Timer1 to be controlled by external input GATE1(P37), to facilitate pulse width measurements). The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Figure 5-15 shows the block diagram of Timer1 for Mode 0.

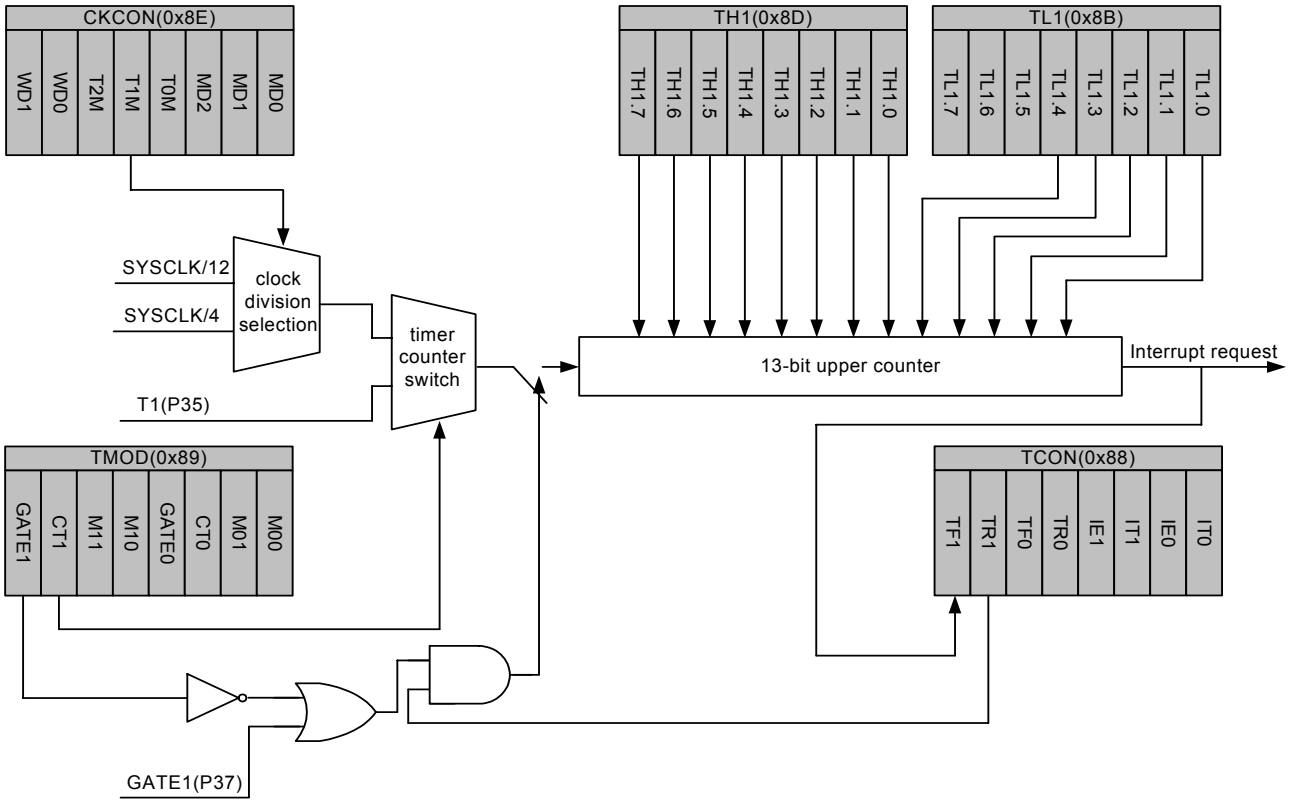


Figure 5-15 The block diagram of Timer 1 for Mode 0

5.9.2.6. Timer 1: Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. The block diagram of Mode 1 is shown in Figure 5-16.

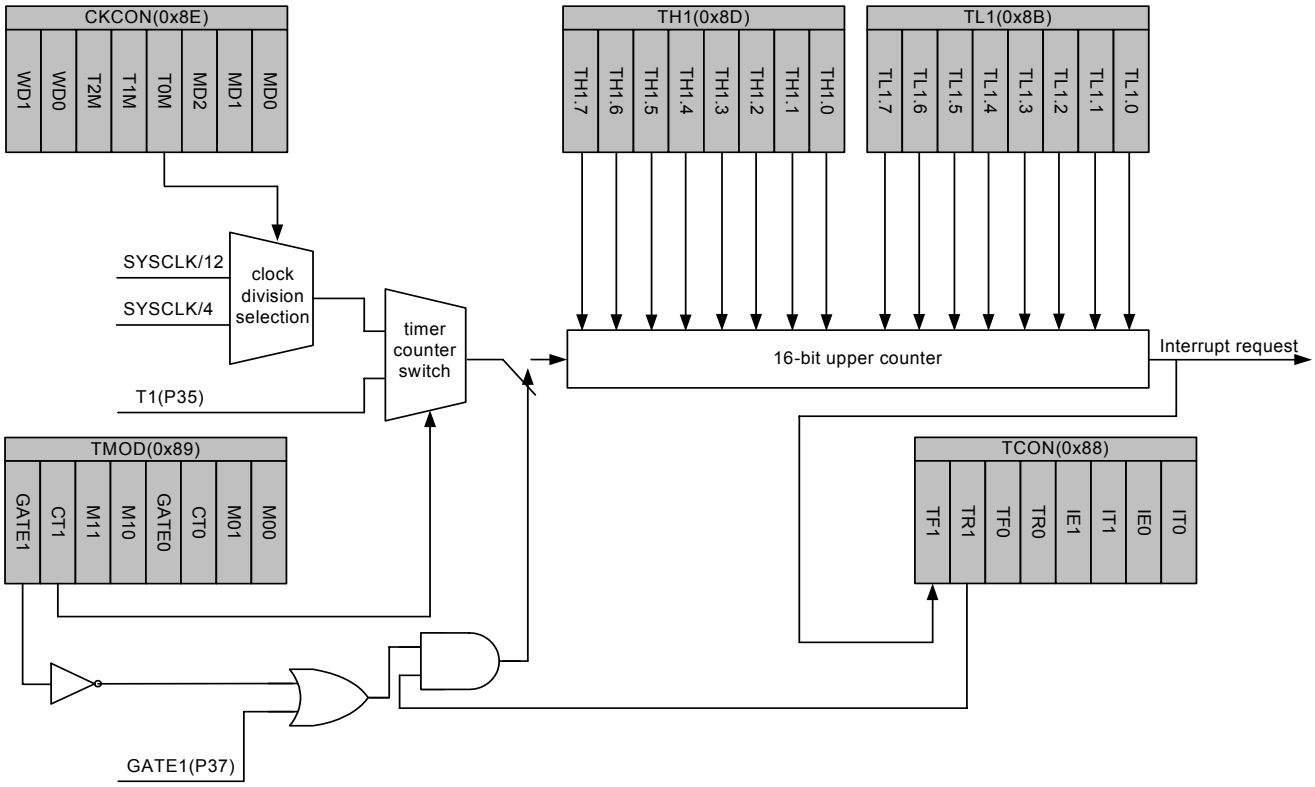


Figure 5-16 The block diagram of Timer 1 for Mode 1

5.9.2.7. Timer 1: Mode 2 (8-Bit Timer/Counter with Auto-reloadable Function)

Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic reloads, as shown in Figure 5-17. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is loaded by software. The reload leaves TH1 unchanged.

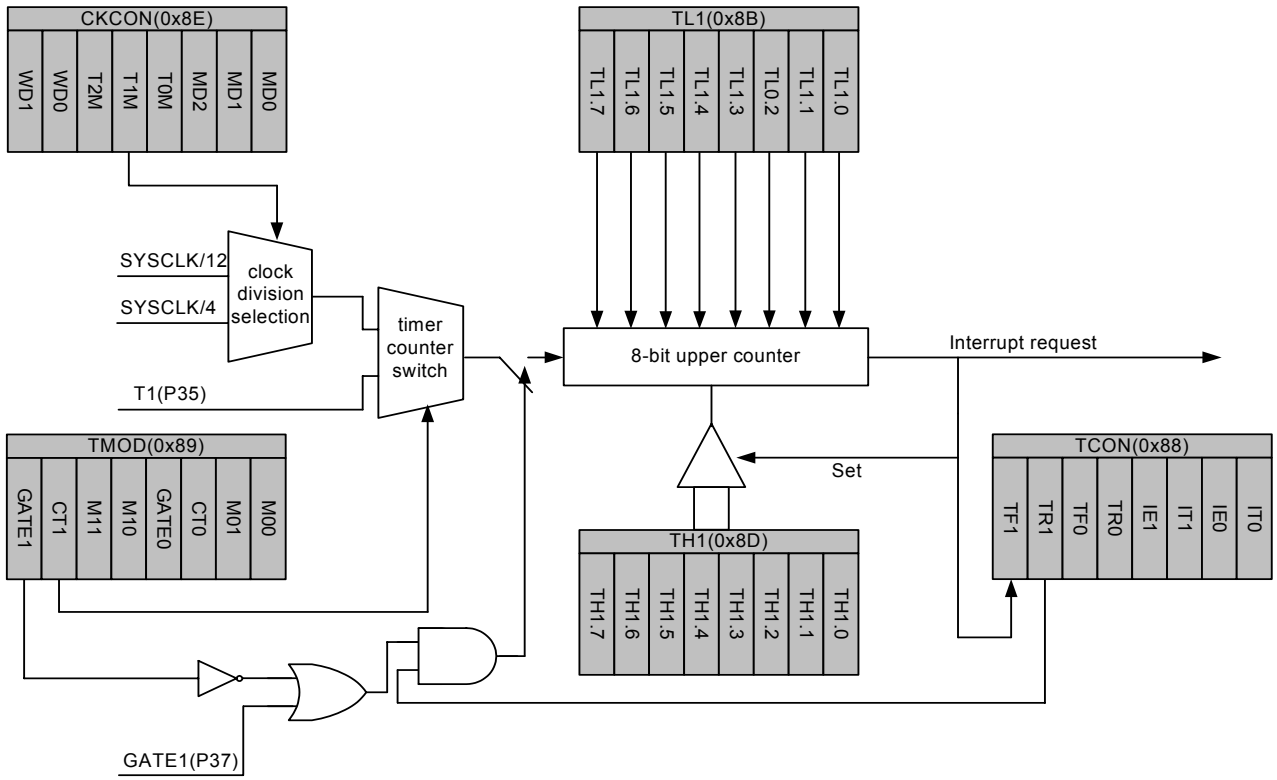


Figure 5-17 The block diagram of Timer 1 for Mode 2

5.9.2.8. Timer 1: Mode 3

Timer 1 in Mode 3 is has no timer function. The effect is the same as setting TR1=0.

5.9.3. Timer 2

Timer 2, which is a 16-bit-wide register, can operate as timer. The additional Compare/Capture/Reload feature is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc. Figure 5-18 shows the block diagram of compare/capture function for Timer 2.

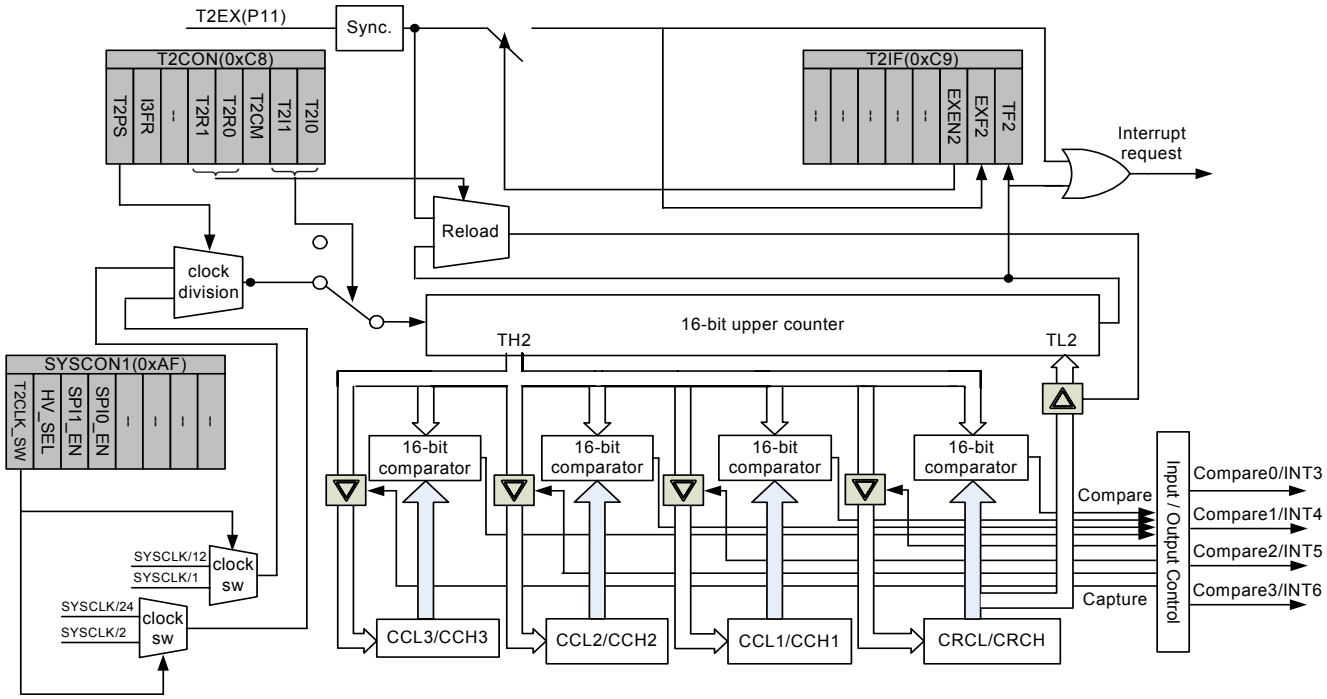


Figure 5-18 The block diagram of compare/capture function for Timer 2

5.9.3.1. Timer Mode

In timer function, the count rate is derived from the oscillator frequency. A 2:1 pre-scaler offers the possibility of selecting a count rate of 1/12(1/1) or 1/24(1/2) of an oscillator frequency. Thus, the 16-bit timer register (consisted of TH2 and TL2) is either incremented in every 1/12(1/1) clock periods or in every 1/24(1/2) clock periods. The pre-scaler is selected by bit T2PS of T2CON and the clock switch is selected by bit T2CLK_SW of SYSCON1.

5.9.3.2. Reload of Timer 2

The reload mode for Timer 2 is selected by T2R0 and T2R1 bits of T2CON. In mode 0, when Timer2 rolls over from all 1's to all 0's, not only TF2 is set but also Timer 2 registers is loaded with the 16-bit value from CRC register. Required CRC value can be preset by software. The reload occurs in the same clock cycle in which TF2 is set, thus overwriting the count value 0x0000. In mode 1, a 16-bit reload from the CRC register is caused by a negative transition at the corresponding T2EX input pin(P11). In addition, this transition sets EXF2 flag, if bit EXEN2 is set. Setting EXF2 will generate an interrupt, if Timer 2 interrupt is enabled.

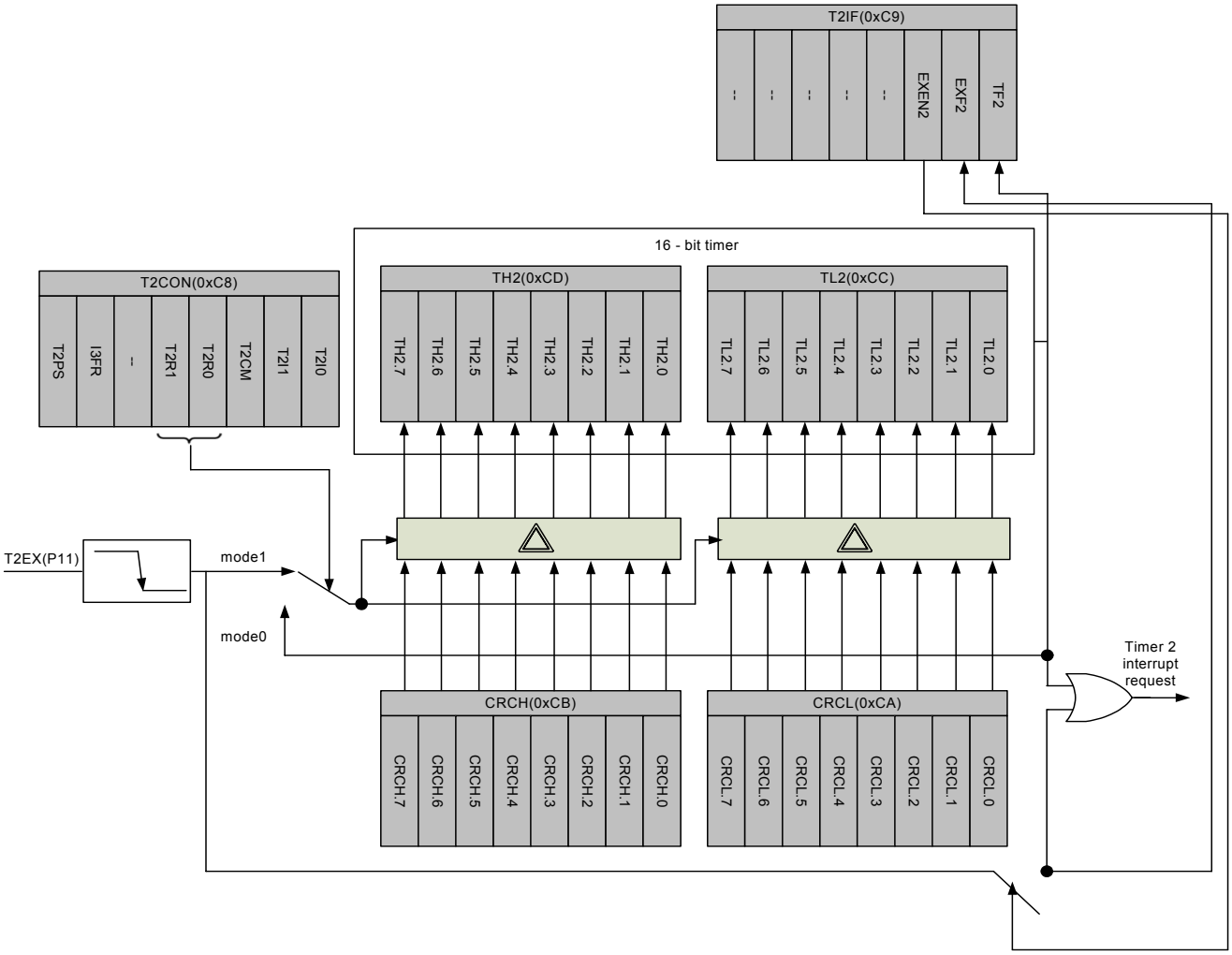


Figure 5-19 The block diagram of reload function for Timer 2

5.9.3.3. Compare Functions (PWM output)

The 16-bit value stored in a compare/capture register is compared with the contents of the timer register. If the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin, and an interrupt is requested. The contents of a compare register can be considered as time stamp at which a dedicated output reacts in a predefined way (either with a positive or negative transition). Variation of this time stamp somehow changes the wave of a rectangular output signal at a port pin. This may - as a variation of the duty cycle of a periodic signal - be used for pulse width modulation as well as for a continually controlled generation of any kind of square waveforms. Two compare modes are implemented to cover a wide range of possible applications. The compare modes 0 and 1 are selected by bit T2CM in special function register T2CON. In both compare modes, the new value arrives at certain pin of P1[3:1] within the same clock cycle in which the internal compare signal is activated.

❑ Compare mode 0

In mode 0, upon matching the timer and compare register contents, an output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit exclusively. It means that instructions writing to the P1 pin will have no effect. Figure 5-20 shows a functional diagram of a port register in compare mode 0. The port register is directly controlled by the two signals: timer overflow and compare.

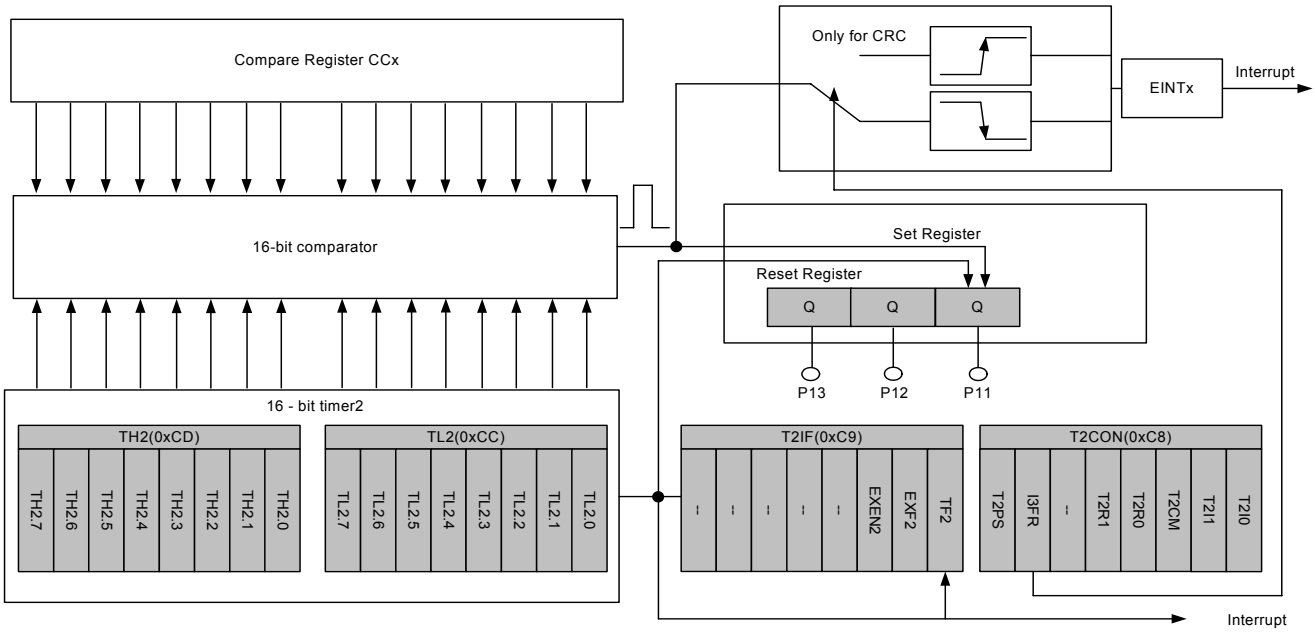


Figure 5-20 The block diagram of compare mode 0 for Timer 2

❑ Compare mode 1

In compare mode 1, the software adaptively determines the transition of the output signal. It is commonly used when output signals are not related to a constant signal period. In compare mode 1, both transitions of a signal can be controlled. If mode 1 is enabled, and the software writes to an appropriate output register of P1, a new value will not appear at the output pin until the next compare match occurs. User can select this way whether the output signal should make a new transition or should keep its old value, until the Timer 2 counter matches the stored compare value. Figure 5-21 shows a functional diagram of Timer 2 in compare mode 1.

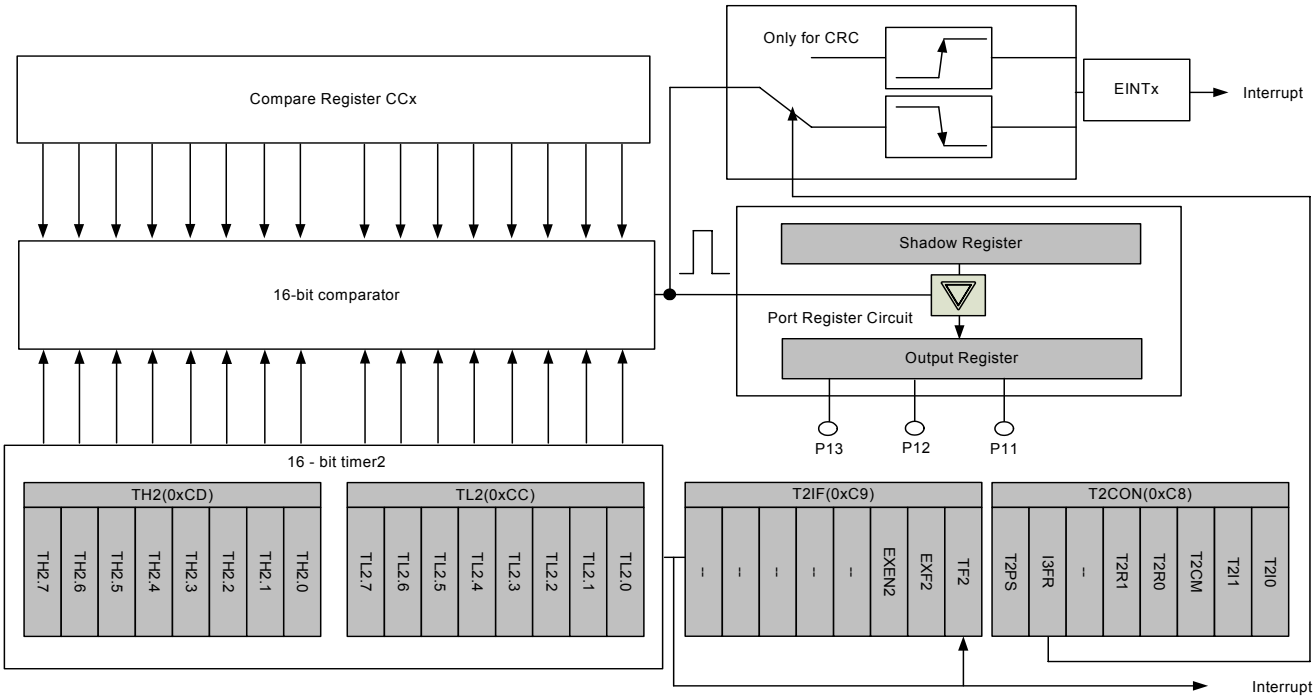


Figure 5-21 The block diagram of compare mode 1 for Timer 2

5.9.3.4. Capture Functions

Each of compare/capture registers from CC1, CC2 and CC3 to CRC register can be used to latch the current 16-bit value of the Timer 2 registers TL2 and TH2. Two different modes are provided for this function.

❑ Capture mode 0

In mode 0, an external event latches Timer 2 contents to a dedicated capture register. The external event causing a capture is

- for the CC registers 1 to 3: a positive transition on pins CAPTURE1 to CAPTURE3
- for the CRC register: a positive or negative transition on the CAPTURE0 pin, depending on the bit I3FR of T2CON. If the I3FR flag is cleared, a capture occurs in response to a negative transition; otherwise, a capture occurs in response to a positive transition on compare0 pin.

❑ Capture mode 1

In mode 1, a capture will occur upon writing to the low order byte of the dedicated 16-bit capture register. This mode is provided to allow software reading of Timer 2 contents on-the fly. The capture occurs in response to a write instruction to the low order byte of a capture register. The write-to-register signal (e.g. write-to-CRCL) is used to initiate a capture. The value written to the dedicated capture register is irrelevant for this function. The Timer 2 contents will be latched into the appropriate capture register in the cycle following the write instruction. In this mode, no interrupt request will be generated.

Figure 5-22 and Figure 5-23 show functional diagrams of the Timer 2 capture function.

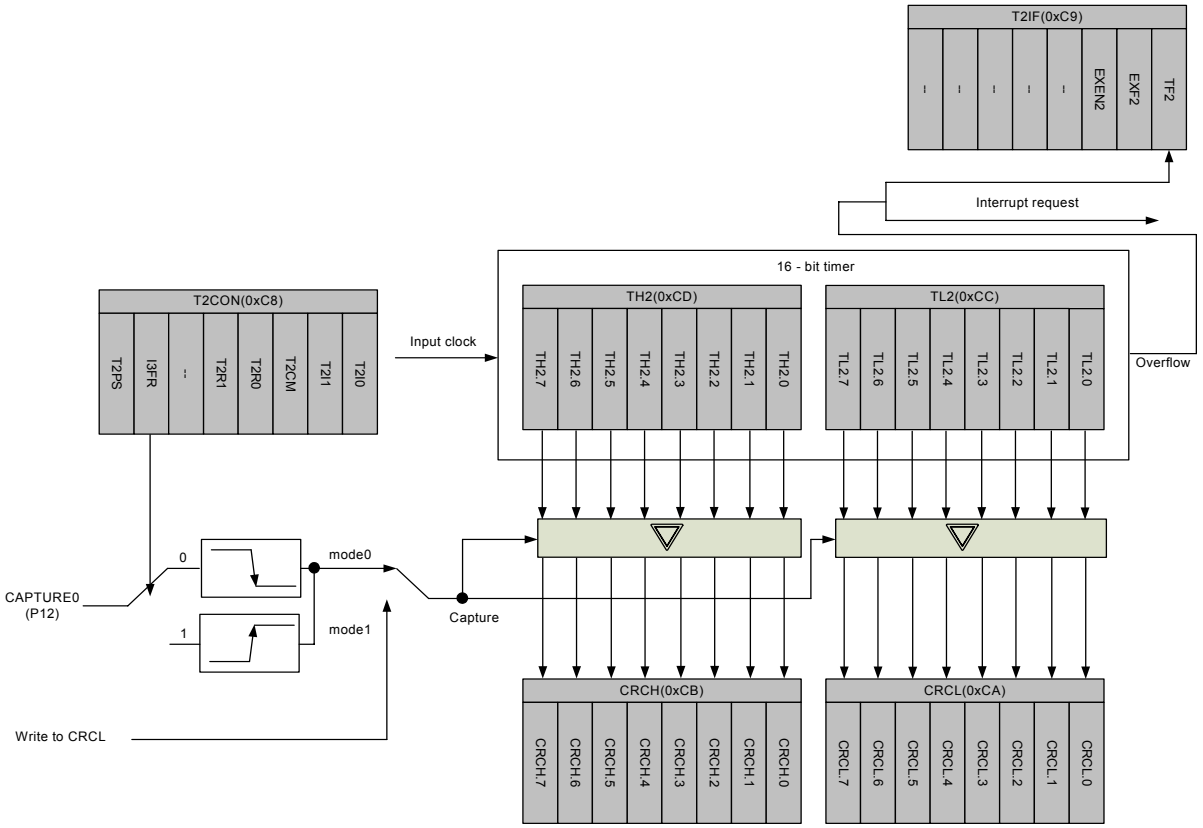


Figure 5-22 The block diagram of Timer 2 capture mode 0 for CRCL and CRCH

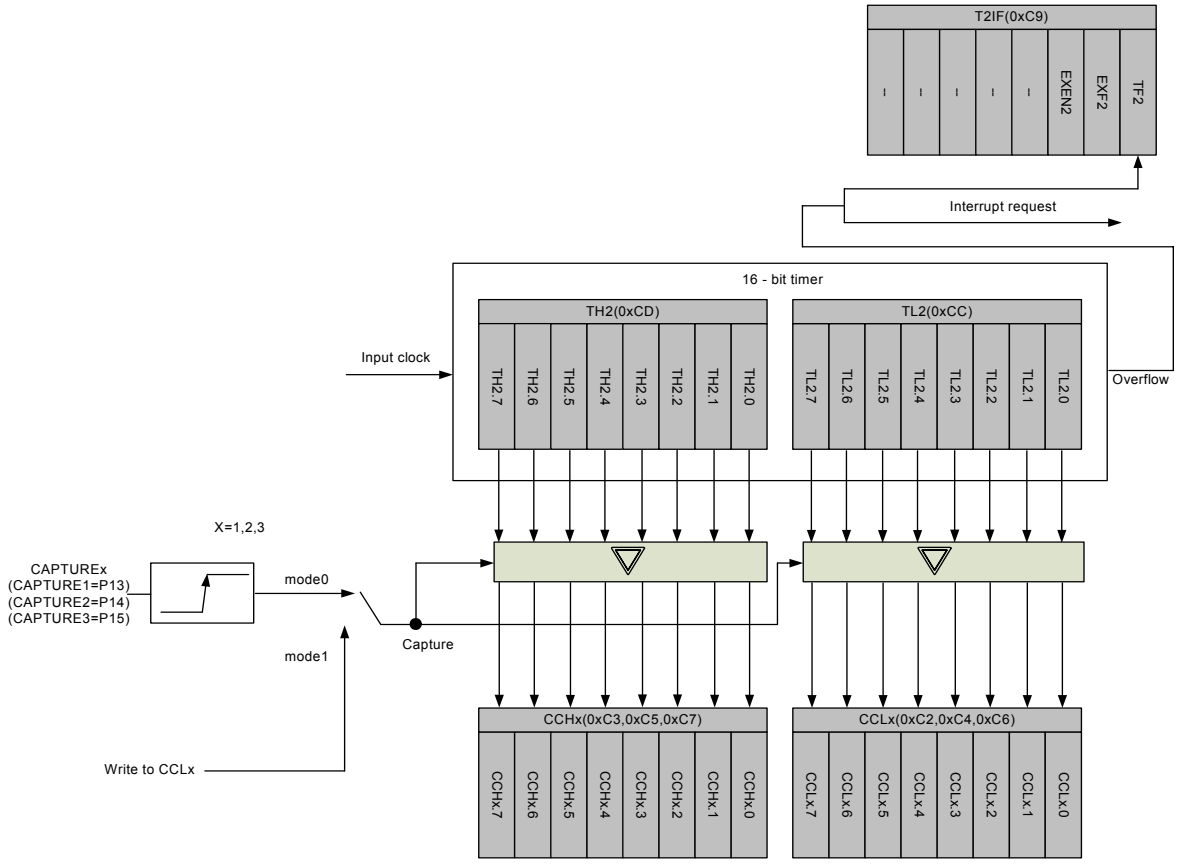


Figure 5-23 The block diagram of Timer 2 capture mode 0 for CCLx and CCHx (x=1,2,3)

5.9.3.5. Timer 2 Related Registers

SYSCON1			Address: 0xAF		SYSTEM Control1 Register			
Bit	7	6	5	4	3	2	1	0
Function	T2CLK_SW	--	SPI1_EN	SPI0_EN	--	--	--	--
Default	0	0	0	0	0	0	1	0
Key Code	FF,00							

Bit	Function	Type	Description	Condition
7	T2CLK_SW	R/W	Timer 2 timer function input frequency switch 0: SYSCLK/12 (T2PS=0) or SYSCLK/24 (T2PS=1) 1: SYSCLK/1 (T2PS=0) or SYSCLK/2 (T2PS=1)	
6	--	R/W	Reserved	
5	SPI1_EN	R/W	SPI signals forward to P3[6:4] enable P3[4]: SPI_CLK P3[5]: SPI_TX P3[6]: SPI_RX	
4	SPI0_EN	R/W	SPI signals forward to P0[7:4] enable P0[4]: SPI_CSB P0[5]: SPI_CLK P0[6]: SPI_TX P0[7]: SPI_RX	
3:0	--	R/W	Reserved	

Table 5-75 SYSCON1 register

T2CON			Address: 0xC8		Timer2 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	T2PS	I3FR	--	T2R1	T2R0	T2CM	T2I1	T2I0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	T2PS	R/W	Pre-scaler selection bit 0: SYSCLK/12 or SYSCLK/1 1: SYSCLK/24 or SYSCLK/2	
6	I3FR	R/W	Interrupt edge activity selection bit of compare 0 function in combination with capture 0 function and register CRC Compare 0: 0: a negative transition on compare0 output can generate interrupt 1: a positive transition on compare0 output can generate interrupt Capture 0: 0: capture to CRC register occurs on a positive transition of CAPTURE0 pin 1: capture to CRC register occurs on a positive transition of CAPTURE0 pin	
5	--	R/W	Reserved	
4:3	T2R[1:0]	R/W	Timer 2 reload mode selection bit T2R1 / T2R0 / Function 0 / X / Reload disabled 1 / 0 / Mode 0: auto-reload upon Timer 2 overflow 1 / 1 / Mode 1: reload upon falling edge at pin T2EX	

Bit	Function	Type	Description	Condition
2	T2CM	R/W	Compare mode select bit for registers CRC, CC1, CC2, and CC3 0: compare mode 0 is selected 1: compare mode 1 is selected	
1:0	T2I[1:0]	R/W	Timer 2 input selection bit	

T2I1	T2I0	Function
0	0	No input selected, Timer 2 is stopped
0	1	Timer function input frequency SYSCLK/12 or SYSCLK/1(T2PS=0) SYSCLK/24 or SYSCLK/2(T2PS=1)
1	0	No input selected, Timer 2 is stopped
1	1	No input selected, Timer 2 is stopped

Table 5-76 T2CON register

CCEN			Address: 0xCE		Compare/Capture Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	CMH3	CML3	CMH2	CML2	CMH1	CML1	CMH0	CML0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	CM3[1:0]	R/W	Compare/capture mode for CC3 register	

CMH3	CML3	Function
0	0	Compare/capture disabled
0	1	Capture on rising edge of CAPTURE3 pin
1	0	Compare enabled
1	1	Capture on write operation into register CCL3

Bit	Function	Type	Description	Condition
5:4	CM2[1:0]	R/W	Compare/capture mode for CC2 register	

CMH2	CML2	Function
0	0	Compare/capture disabled
0	1	Capture on rising edge of CAPTURE2 pin
1	0	Compare enabled
1	1	Capture on write operation into register CCL2

Bit	Function	Type	Description	Condition
3:2	CM1[1:0]	R/W	Compare/capture mode for CC1 register	

CMH1	CML1	Function
0	0	Compare/capture disabled
0	1	Capture on rising edge of CAPTURE1 pin
1	0	Compare enabled
1	1	Capture on write operation into register CCL1

Bit	Function	Type	Description	Condition
1:0	CM0[1:0]	R/W	Compare/capture mode for CRC register	

CMH2	CML2	Function
0	0	Compare/capture disabled
0	1	Capture on falling/rising edge of CAPTURE0 pin
1	0	Compare enabled
1	1	Capture on write operation into register CRCL

Table 5-77 CCEN register

T2IF			Address: 0xC9		Timer 2 Interrupt Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	EXEN2	EXF2	TF2
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2	EXEN2	R/W	Timer 2 external reload interrupt enable 0: external reload interrupt is disabled 1: external reload interrupt is enabled	
1	EXF2	R/W	Timer 2 external reload flag Cleared by the software	
0	TF2	R/W	Timer 2 overflow flag Cleared by the software	

Table 5-78 T2IF register

CCH1			Address: 0xC3		Timer 2 CC1 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	CC1[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC1[15:8]	R/W	Timer2 compare/capture 1 - high byte	

Table 5-79 The CCH1 register

CCL1			Address: 0xC2		Timer 2 CC1 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	CC1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC1[7:0]	R/W	Timer2 compare/capture 1 - low byte	

Table 5-80 The CCL1 register

CCH2			Address: 0xC5		Timer 2 CC2 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	CC2[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC2[15:8]	R/W	Timer2 compare/capture 2 - high byte	

Table 5-81 The CCH2 register

CCL2			Address: 0xC4		Timer 2 CC2 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	CC2[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC2[7:0]	R/W	Timer2 compare/capture 2 - low byte	

Table 5-82 The CCL2 register

CCH3			Address: 0xC7		Timer 2 CC3 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	CC3[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC3[15:8]	R/W	Timer2 compare/capture 3 - high byte	

Table 5-83 The CCH3 register

CCL3			Address: 0xC6		Timer 2 CC3 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	CC3[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC3[7:0]	R/W	Timer2 compare/capture 3 - low byte	

Table 5-84 The CCL3 register

CRCH			Address: 0xCB		CRC Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	CRC[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CRC[15:8]	R/W	CRC - high byte	

Table 5-85 The CRCH register

CRCL			Address: 0xCA		CRC Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	CRC[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CRC[7:0]	R/W	CRC - low byte	

Table 5-86 The CRCL register

TH2			Address: 0xCD		Timer 2 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH2[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH2[7:0]	R/W	Timer 2 Load value – high byte	

Table 5-87 TH2 register

TL2			Address: 0xCC		Timer 2 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL2[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL2[7:0]	R/W	Timer 2 Load value – low byte	

Table 5-88 TL2 register

5.10. UART0

UART0 has the same functionality as a standard 8051 UART. The serial port is full duplex, meaning it can transmit and receive concurrently. It is receive double-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0 reads a physically separate receive register. The serial port can operate in 4 modes: one synchronous and three asynchronous modes. Mode 2 and Mode 3 have a special feature for multiprocessor communications. This feature is enabled by setting SM02 bit in SCON0 register. The master processor first sends out an address byte, which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM02 = 1, no slave will be interrupted by a data byte. An address byte will interrupt all slaves. The addressed slave will clear its SM02 bit and prepare to receive the data bytes that will be coming. The slaves that were not being addressed leave their SM02 set and ignoring the incoming data.

5.10.1. UART0: Mode 0 (Synchronous Shift Register)

This mode is used as shift register IO control, and not for real communication application. The baud rate is fixed at 1/12 of the system clock frequency and TXD0(P31) output is a shift clock. Eight bits are transmitted with LSB first. Reception is initialized by setting the flags in SCON0 as follows: RI0 =0 and REN0 =1. Figure 5-24 shows the timing diagram of UART0 transmission mode 0.

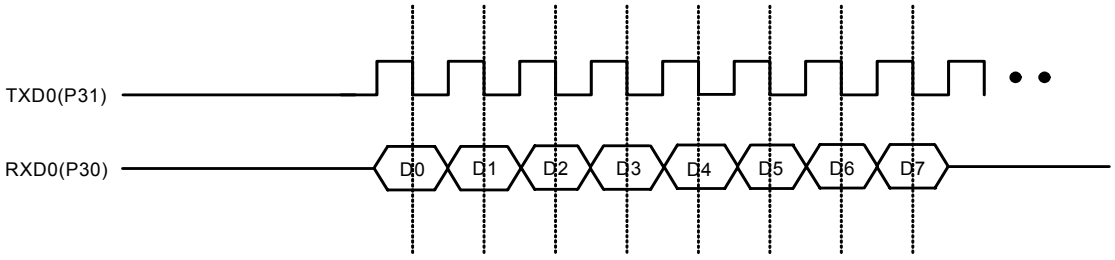


Figure 5-24 The timing diagram of UART0 transmission mode 0

5.10.2. UART0: Mode 1 (8-Bit UART, Variable Baud Rate, Timer1 Clock Source)

In mode 1, TXD0 serves as serial output. 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the reception, 8 data bits are available by reading SBUF0 and stop bit sets the flag RB08 in the SFR SCON0. The baud rate is variable and depends from Timer 1 mode. Figure 5-25 shows the timing diagram of UART0 transmission mode 1.

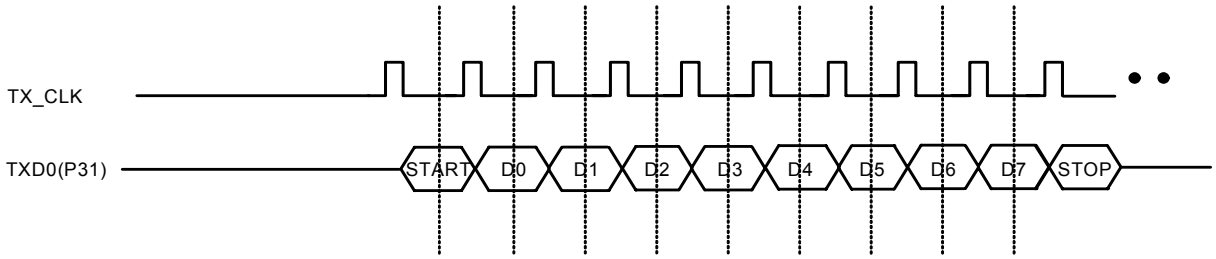


Figure 5-25 The timing diagram of UART0 transmission mode 1

5.10.3. UART0: Mode 2 (9-Bit UART, Fixed Baud Rate)

This mode is similar to Mode 1 with two differences. The baud rate is fixed at 1/32 or 1/64 of system clock frequency, and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the UART0 interface: at transmission, bit TB08 in SCON0 is output as the 9th bit, and at receive, the 9th bit affects RB08 in SCON0. Figure 5-26 shows the timing diagram of UART0 transmission mode 2.

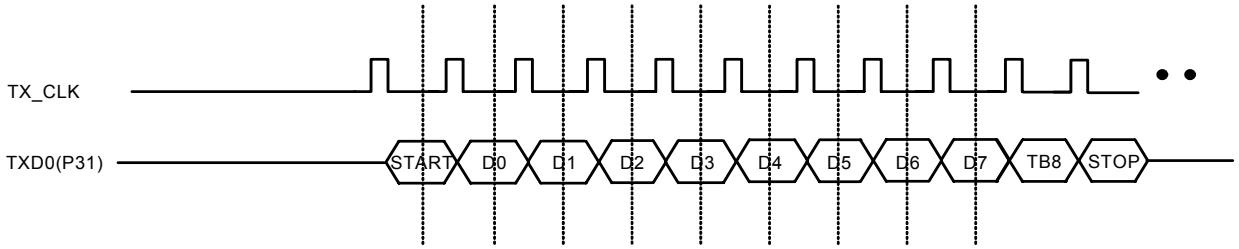


Figure 5-26 The timing diagram of UART0 transmission mode 2

5.10.4. UART0: Mode 3 (9-Bit UART, Variable Baud Rate, Timer1 Clock Source)

The only difference between Mode 2 and Mode 3 is that the baud rate is a variable in Mode 3. When REN0 =1 data receiving is enabled. The baud rate is variable and depends from Timer 1 mode.

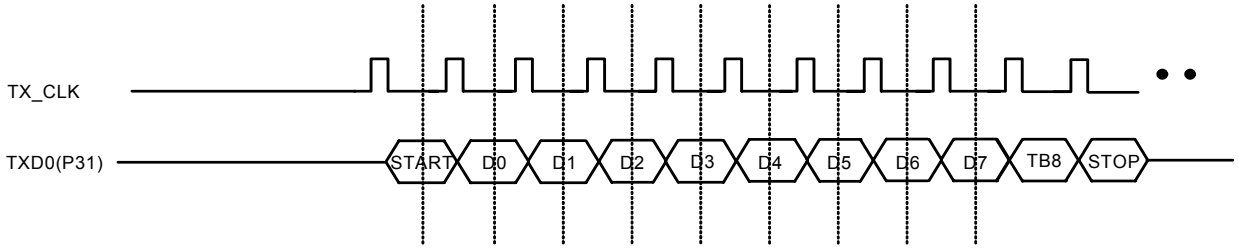


Figure 5-27 The timing diagram of UART0 transmission mode 3

5.10.5. UART0 Related Registers

The UART0 related registers are: SBUF0(0x99), SCON0(0x98), PCON(0x87), IE(0xA8) and IP(0xB8). The UART0 data buffer (SBUF0) consists of two separate registers: transmit and receive registers. A data written into SBUF0 sets this data in UART0 output register and starts a transmission. A data read from SBUF0, reads data from the UART0 receive register.

SBUF0			Address: 0x99		UART0 Buffer Register			
Bit	7	6	5	4	3	2	1	0
Function	SBUF0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
2:0	SBUF0[7:0]	R/W	UART0 buffer	

Table 5-89 SBUF0 register

SCON0			Address: 0x98		UART0 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	SM0[1:0]	R/W	Mode and baud rate setting which described as below table	
5	SM02	R/W	Enables a multiprocessor communication feature	
4	REN0	R/W	Enable serial reception.	
3	TB08	R/W	The 9th transmitted data bit in Modes 2 and Mode 3	
2	RB08	R/W	In Mode 0, this bit is not used In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 2 and Mode 3, it is the 9th data bit received	
1	TI0	R/W	UART0 transmitter interrupt flag	
0	RI0	R/W	UART0 receiver interrupt flag	

Table 5-90 SCON0 register

SM00	SM01	Mode	Function	Baud Rate
0	0	0	Shift register	SYSCLK/12
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	SYSCLK/32(SMOD0=0) SYSCLK/64(SMOD0=1)
1	1	3	9-bit UART	Variable

Variable: in Mode1 and Mode 3

Timer	Baud Rate
Timer 1 overflow rate	$T1_{ov}/32$ (SMOD0=0)
Timer 1 overflow rate	$T1_{ov}/16$ (SMOD0=1)

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	--	CPU_IDLE	PWE	STOP_RST_EN	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	--	R/W	Reserved	
5	CPU_IDLE	R/W	IDLE mode enable bit 0: IDLE mode disabled; 1: IDLE mode entered	

Bit	Function	Type	Description	Condition
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3	STOP_RST_EN	R/W	Wakeup state selection bit 0: Next instruction state after wakeup 1: Reset state afer wakeup	
2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-91 PCON register

IE			Address: 0xA8		Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	EA	--	ET2	ES0	ET1	EX1	ET0	EX0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EA	R/W	Enable global interrupts	
6	--	R/W	Reserved	
5	ET2	R/W	Enable Timer 2 interrupt	
4	ES0	R/W	Enable UART0 interrupt	
3	ET1	R/W	Enable Timer 1 interrupt	
2	EX1	R/W	Enable INT1 interrupt	
1	ET0	R/W	Enable Timer 0 interrupt	
0	EX0	R/W	Enable INT0 interrupt	

Table 5-92 IE register

IP			Address: 0xB8		Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	--	PS1	PT2	PS0	PT1	PX1	PT0	PX0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	PT2	R/W	Timer 2 priority level control (1: high level)	
4	PS0	R/W	UART0 priority level control (1: high level)	
3	PT1	R/W	Timer 1 priority level control (1: high level)	
2	PX1	R/W	INT1 priority level control (1: high level)	
1	PT0	R/W	Timer 0 priority level control (1: high level)	
0	PX0	R/W	INT0 priority level control (1: high level)	

Table 5-93 IP register

5.11. SPI

A Serial Peripheral Interface (SPI) controller is built in GPM8F3232A/3216A/3208A to facilitate communicating with other devices and components. The SPI controller includes four master modes. There are four control signals on SPI including SPI_CSB, SPI_CLK, SPI_TX, and SPI_RX, these four signals are shared with P0[7:4] or {PXX, P3[6:4]} (PXX is used for SPICSN and can be a random pin as long as it is not utilized for any other function) based on SPI0 or SPI1 is chosen. The control share I/O is set by SYSCON1[5:4]. While SPI module is enabled by corresponding control bit, these four pins cannot be GPIOs. In other words, any setting on corresponding GPIO control register will have no effect. The SPI provides following features.

- ❑ Programmable phase and polarity of master clock
- ❑ Programmable master SPI_CLK clock frequency

In master mode, the shifting clock (SPI_CLK) is generated by SPI block. There are two control bits to control the clock phase and polarity. The transmission starts immediately after SPI_START is set(SPICON[0]=1,0xFC). The SPI shifts the 8-bit data from MSB to LSB through the SPI_TX pin during 8 SCK cycles. Programmer can read SPI data from SPIRXD control register by setting SPI_RD =1. The following four diagrams depict the timing scheme on SPI master mode for different operation types (polarity control bit equals “1” or “0”, phase control bit equals “1” or “0”). The related registers are SYSCON1 register, SPICON register, SPITXD register and SPIRXD registers which are tabled as Table 5-94 to Table 5-97.

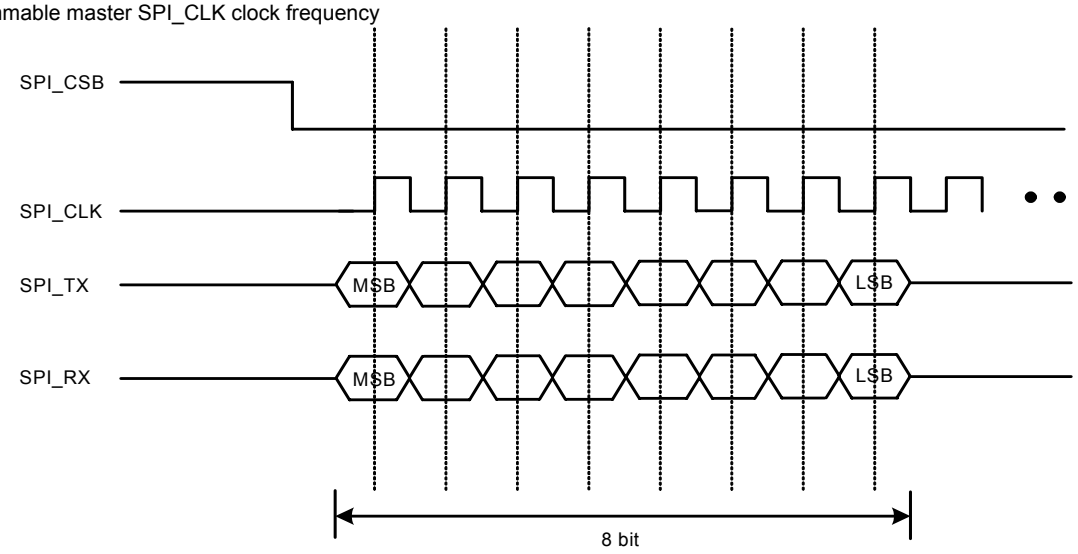


Figure 5-28 Master Mode, POLARITY=0, PHASE=0

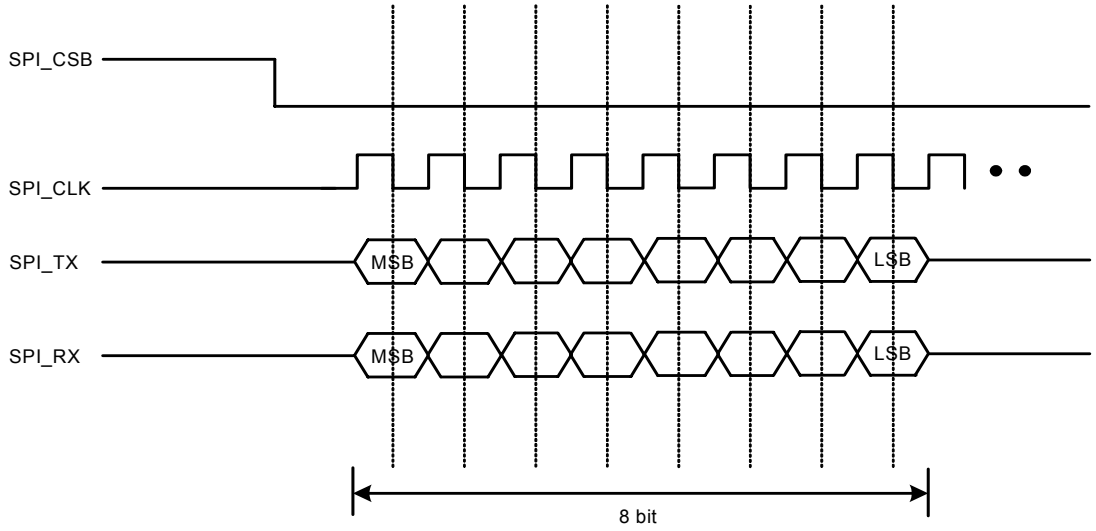


Figure 5-29 Master Mode, POLARITY=0, PHASE=1

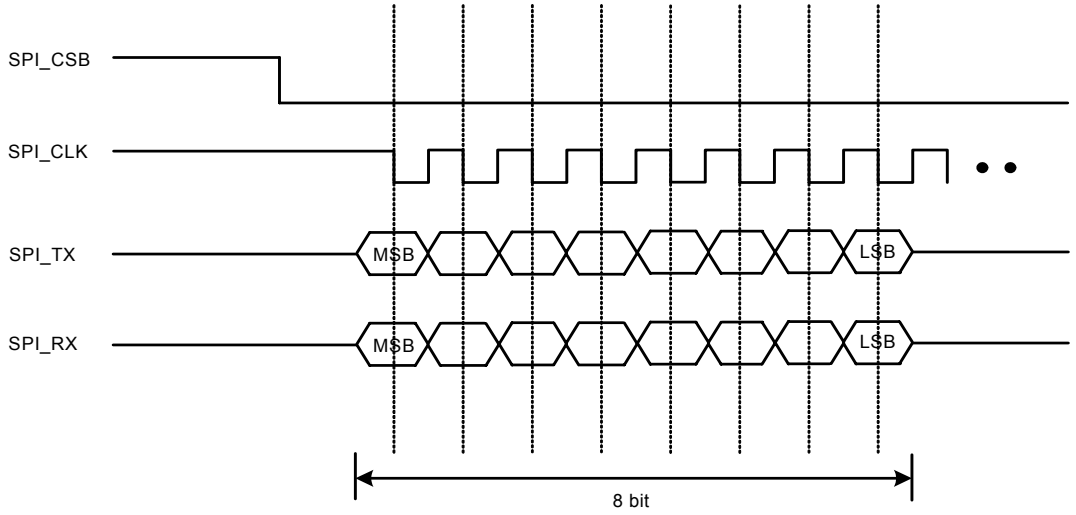


Figure 5-30 Master Mode, POLARITY=1, PHASE=0

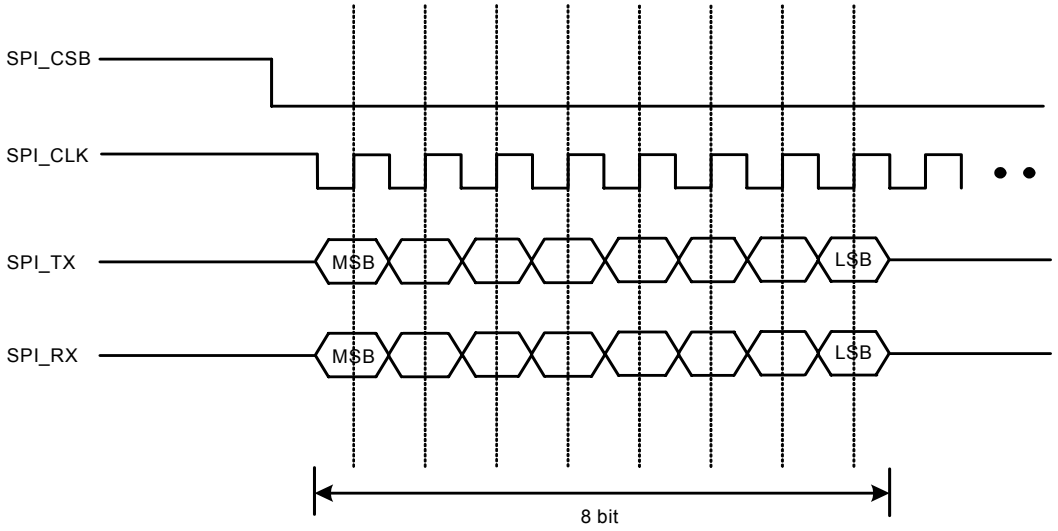


Figure 5-31 Master Mode, POLARITY=1, PHASE=1

SYSCON1			Address: 0xAF		SYSTEM Control1 Register			
Bit	7	6	5	4	3	2	1	0
Function	T2CLK_SW	--	SPI1_EN	SPI0_EN	--	--	--	--
Default	0	0	0	0	0	0	1	0
Key Code	FF,00							

Bit	Function	Type	Description	Condition
7	T2CLK_SW	R/W	Timer 2 timer function input frequency switch 0: SYSCLK/12 (T2PS=0) or SYSCLK/24 (T2PS=1) 1: SYSCLK/1 (T2PS=0) or SYSCLK/2 (T2PS=1)	
6	--	R/W	Reserved	
5	SPI1_EN	R/W	SPI signals forward to P3[6:4] enable P3[4]: SPI_CLK P3[5]: SPI_TX P3[6]: SPI_RX	

Bit	Function	Type	Description	Condition
4	SPI0_EN	R/W	SPI signals forward to P0[7:4] enable P0[4]: SPI_CSB P0[5]: SPI_CLK P0[6]: SPI_TX P0[7]: SPI_RX	
3:0	--	R/W	Reserved	

Table 5-94 SYSCON1 register

SPICON			Address: 0xFC		SPI Control Register			
Bit	7	6	5	4	3	2	1	0
Function	POLARITY	PHASE	SPI_CLK_SEL[1:0]		CSB_KEEP	--	SPI_RD	SPI_START
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	POLARITY	R/W	SPI CLK initial state 0: low state; 1: high state	
6	PHASE	R/W	SPI CLK type control 0: rising sample; 1: falling sample	
5:4	SPI_CLK_SEL[1:0]	R/W	SPI Clock output selection: 00: SYSCLK/2 01: SYSCLK/4 10: SYSCLK/8 11: SYSCLK/16	
3	CSB_KEEP	R/W	SPI CSB keep low control, high active	
2	--	R/W	Reserved	
1	SPI_RD	R/W	SPI read command	
0	SPI_START	R/W	SPI enable(W)/SPI busy flag(R)	

Table 5-95 SPICON register

SPITXD			Address: 0xFD		SPI Output Buffer Register			
Bit	7	6	5	4	3	2	1	0
Function	SPITXD[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	SPITXD	R/W	SPI output buffer	

Table 5-96 SPITXD register

SPIRXD			Address: 0xFE		SPI Input Buffer Register			
Bit	7	6	5	4	3	2	1	0
Function	SPIRXD[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	SPIRXD	R/W	SPI input buffer	

Table 5-97 SPIRXD register

5.12. ADC

There is one Analog-to-Digital-Converter (ADC) in GPM8F3232A/3216A/3208A. It provides general purpose usages such as voice record feature and any other analog functions.

- ❑ 8 Channels, 12-bit resolution (11-bit no-missing code) ADC
- ❑ Supports programming sample hold and ADC clock function

5.12.1. ADC Control

Eight channels of 12-bit SAR ADC are built in GPM8F3232A/3216A/3208A. They are defined as general-purpose line input P00, P01 … P07. These eight channels are very suitable for system voltage detection and other general-purpose usages. In addition, there is an AD_BITSEL control pin which can choose 8-bit ADC or 12-bit ADC to be used. Figure 5-32 and Figure 5-33 show the related timing and block diagrams.

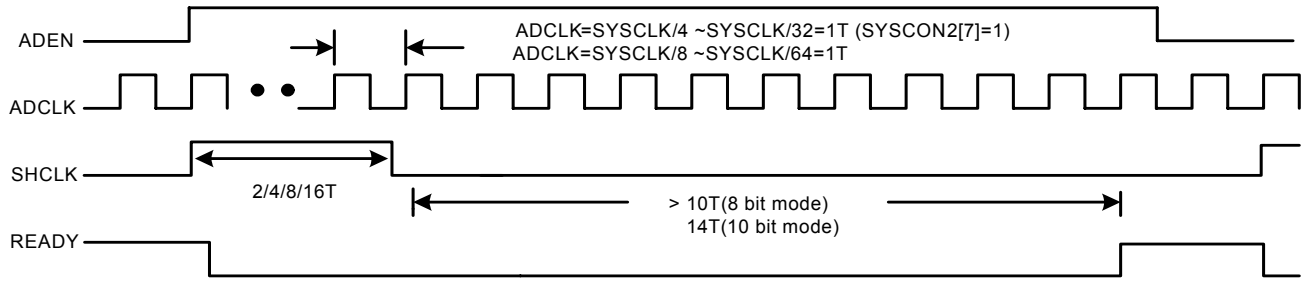


Figure 5-32 The timing diagram of ADC control

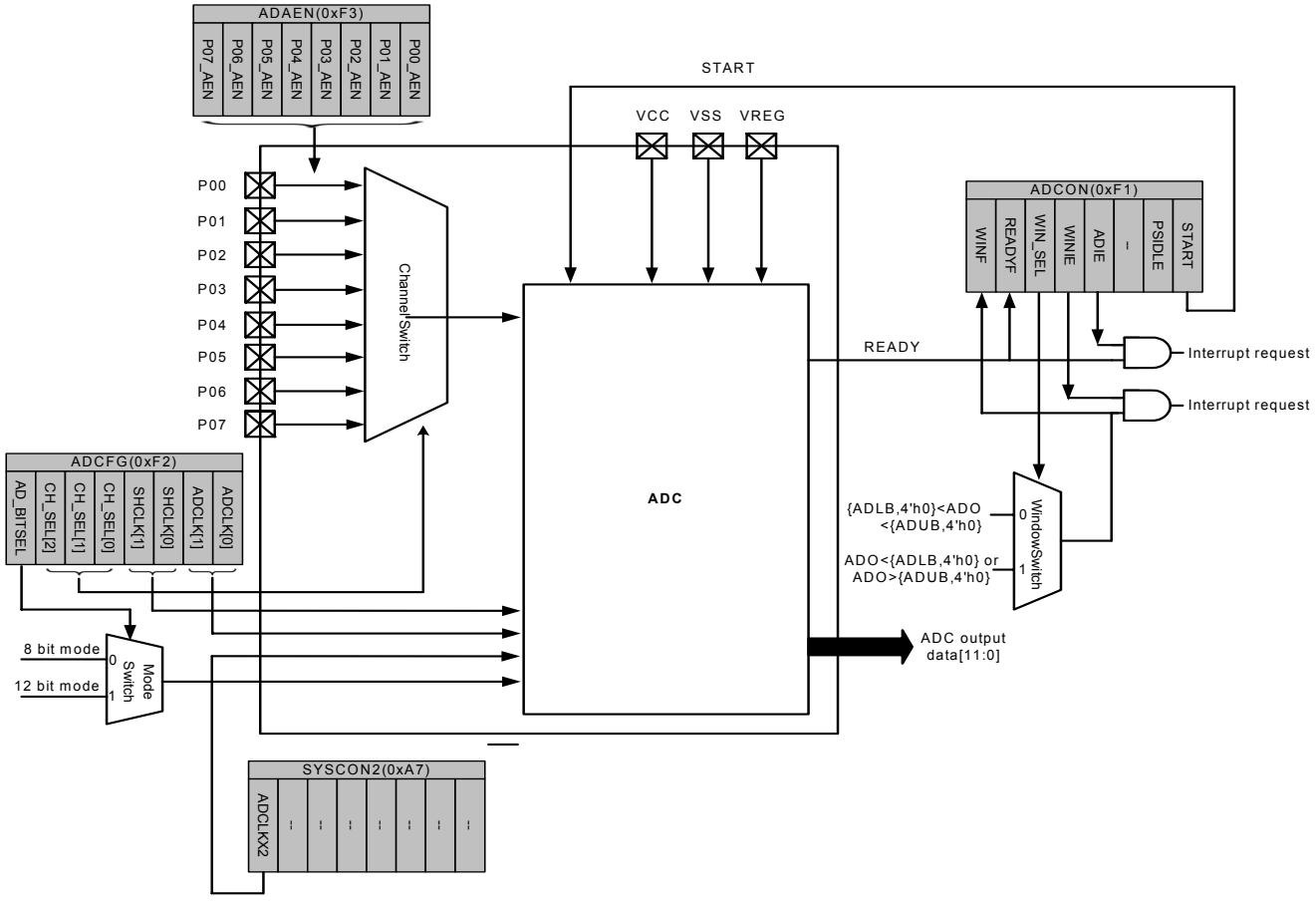


Figure 5-33 The block diagram of ADC

ADC Related Register

ADCON			Address: 0xF1		ADC Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WINF	READYF	WIN_SEL	WINIE	ADIE	--	PSIDLE	START
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	WINF	R/W	Window detect flag, cleared by 1.	
6	READYF	R/W	ADC transfer ready flag, cleared by 1.	
5	WIN_SEL	R/W	ADC output window selection 0: ADC output is between ADLB and ADUB 1: ADC output isn't between ADLB and ADUB	
4	WINIE	R/W	ADC window interrupt enable	
3	ADIE	R/W	ADC transfer ready interrupt enable	
2	--	R/W	Reserved	
1	PSIDLE	R/W	IDLE mode enable bit (ADC start transfer with suspending CPU clock)	
0	START	R/W	ADC start transfer control	

Table 5-98 ADCON register

ADCFG			Address: 0xF2		ADC Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	AD_BITSEL	CH_SEL[2:0]			SHCLK[1:0]		ADCLK[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	AD_BITSEL	R/W	0: 8-bit ADC; 1: 12-bit ADC	
6:4	CH_SEL[2:0]	R/W	ADC channel selection 0: P00 is selected 1: P01 is selected 2: P02 is selected 3: P03 is selected 4: P04 is selected 5: P05 is selected 6: P06 is selected 7: P07 is selected	
3:2	SHCLK[1:0]	R/W	ADC sample and hold period 0: 2T of ADCLK 1: 4T of ADCLK 2: 8T of ADCLK 3: 16T of ADCLK	
1:0	ADCLK	R/W	ADC clock selection 0: ADC conversion clock = 3.0625MHz (F_{OSC} /8) 1: ADC conversion clock = 1.53MHz (F_{OSC} /16) 2: ADC conversion clock = 765.625KHz (F_{OSC} /32) 3: ADC conversion clock = 382.81KHz (F_{OSC} /64)	

Table 5-99 ADCFG register

ADAEN			Address: 0xF3		ADC Analog PAD Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	P07_AEN	P06_AEN	P05_AEN	P04_AEN	P03_AEN	P02_AEN	P01_AEN	P00_AEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	P07_AEN	R/W	P07 analog PAD enable control bit 0: P07 can be I/O PAD 1: P07 can be analog PAD	
6	P06_AEN	R/W	P06 analog PAD enable control bit 0: P06 can be I/O PAD 1: P06 can be analog PAD	
5	P05_AEN	R/W	P05 analog PAD enable control bit 0: P05 can be I/O PAD 1: P05 can be analog PAD	
4	P04_AEN	R/W	P04 analog PAD enable control bit 0: P04 can be I/O PAD 1: P04 can be analog PAD	
3	P03_AEN	R/W	P03 analog PAD enable control bit 0: P03 can be I/O PAD 1: P03 can be analog PAD	
2	P02_AEN	R/W	P02 analog PAD enable control bit 0: P02 can be I/O PAD 1: P02 can be analog PAD	
1	P01_AEN	R/W	P01 analog PAD enable control bit 0: P01 can be I/O PAD 1: P01 can be analog PAD	
0	P00_AEN	R/W	P00 analog PAD enable control bit 0: P00 can be I/O PAD 1: P00 can be analog PAD	

Table 5-100 ADAEN register

ADOL			Address: 0xF4		ADC Output Low Data Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	ADO[3:0]			
Default	0	0	0	0	--	--	--	--

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	ADO[3:0]	R/W	ADC output data[3:0]	

Table 5-101 ADOL register

ADOH			Address: 0xF5		ADC Output High Data Register			
Bit	7	6	5	4	3	2	1	0
Function	ADO[11:4]							
Default	--	--	--	--	--	--	--	--

Bit	Function	Type	Description	Condition
7:0	ADO[11:4]	R/W	ADC output data[11:4]	

Table 5-102 ADOH register

ADLB			Address: 0xF6		ADC Low Boundary register			
Bit	7	6	5	4	3	2	1	0
Function	ADLB[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	ADLB	R/W	ADC low boundary, compare to ADC[11:4]	

Table 5-103 ADLB register

ADUB			Address: 0xF7		ADC UP Boundary register			
Bit	7	6	5	4	3	2	1	0
Function	ADUB[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	ADUB	R/W	ADC up boundary, compare to ADC[11:4]	

Table 5-104 ADUB register

SYSCON2			Address: 0xA7		SYSTEM control2 Register			
Bit	7	6	5	4	3	2	1	0
Function	ADCLKX2	--	INT_filter_en	GPIO_SSO	SCHMIT_DIS_P3	SCHMIT_DIS_P2	SCHMIT_DIS_P1	SCHMIT_DIS_P0
Default	0	0	0	0	0	0	0	0
Key Code	FF,00							

Bit	Function	Type	Description	Condition
7	ADCLKX2	R/W	ADCLK double enable bit	
6	--	R/W	Reserved	
5	INT_filter_en	R/W	INT0~INT2 pad filter enable bit 0: no filter 1: 2us	
4	GPIO_SSO	R/W	GPIO SSO function enable bit (Avoid GPIO change simultaneously)	
3	SCHMIT_DIS_P3	R/W	P3 Schmitt trigger function disable control bit	
2	SCHMIT_DIS_P2	R/W	P2 Schmitt trigger function disable control bit	
1	SCHMIT_DIS_P1	R/W	P1 Schmitt trigger function disable control bit	
0	SCHMIT_DIS_P0	R/W	P0 Schmitt trigger function disable control bit	

Table 5-105 SYSCON2 register

5.13. Built-in OP Circuits

In GPM8F3232/3216/3208A, there is one built-in OP circuit. The related control registers are OPCO. Figure 5-34 shows the diagram of the built-in OP circuit.

OPCON			Address: 0xAB		OP Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	TRIM_VOSP	TRIM_VOSN	--	--	OP_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	TRIM_VOSP	R/W	Trimming bit for OP offset (V+)	
3	TRIM_VOSN	R/W	Trimming bit for OP offset (V+)	
2	--	R/W	Reserved	
1	--	R/W	Reserved	
0	OP_EN	R/W	Enable OP function	

Table 5-106 OPCON register

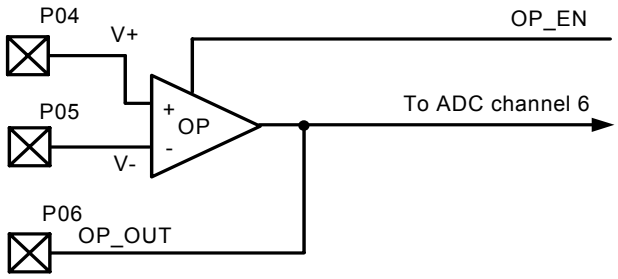


Figure 5-34 Built-in OP circuit

5.14. Audio Unit

In GPM8F3232A/3216A/3208A, there is one audio control unit utilized for audio application. The related control registers are AUDCON and AUDBUF. When audio function is enabled, P36 and P37 are used as AUDIO_N and AUDIO_P in default setting, user can disable the output of AUDIO_N and leave P36 as GPIO by setting SYSCON0[4]. Figure 5-35 shows the diagram of P36 and P37 output for different AUDCON settings.

AUDCON			Address: 0xB3		Audio Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	AUDIO_MODE	AUDIOIE	AUDIO_FREQ_SEL	AUDIO_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3	AUDIO_MODE	R/W	Audio mode selection 0: x 1: PWM mode	
2	AUDIOIE	R/W	Enable audio interrupt	
1	AUDIO_FREQ_SEL	R/W	Audio output frequency selection 0: AUDIO_24KHz output 1: AUDIO_32KHz output	
0	AUDIO_EN	R/W	Enable audio function	

Table 5-107 AUDCON register

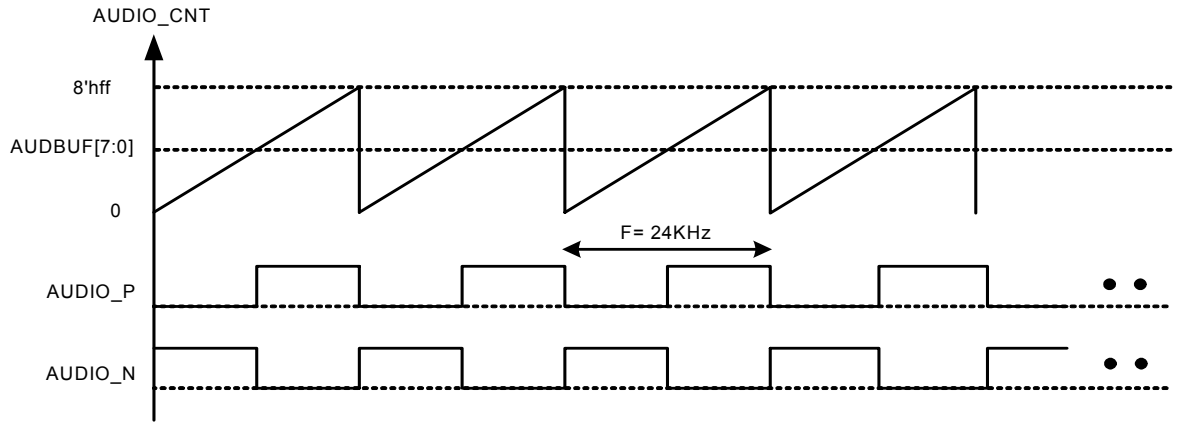
AUDBUF			Address: 0xB4		Audio Buffer Register			
Bit	7	6	5	4	3	2	1	0
Function	AUDBUF[7:0]							
Default	1	0	0	0	0	0	0	0

Table 5-108 AUDBUF register

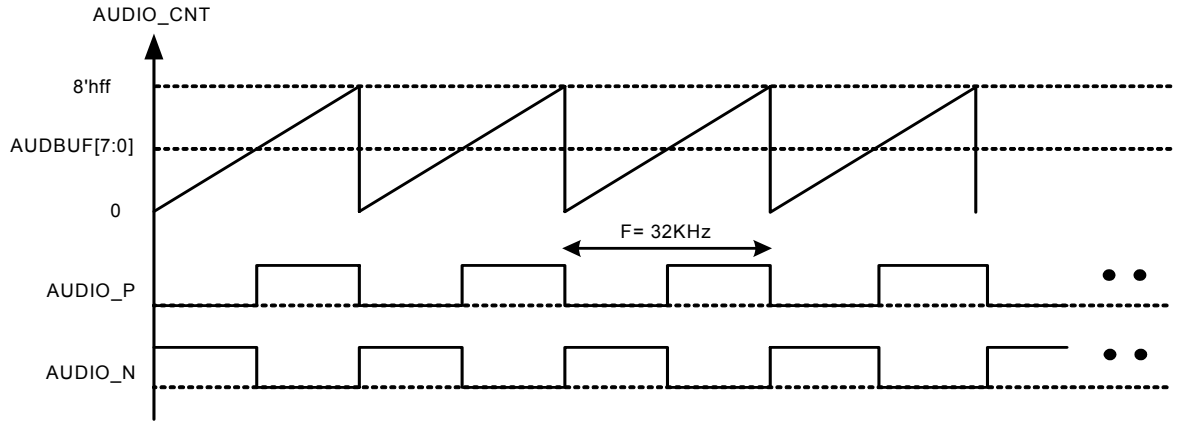
SYSCON0			Address: 0xAE		SYSTEM control0 Register			
Bit	7	6	5	4	3	2	1	0
Function	LVRENB	--	--	AUDIO_N_DIS	--	CLKOUT_EN	CCOUTENB	SCHMIT_DIS_P4
Default	0	0	0	0	0	0	0	0
Key Code	FF,00							

Bit	Function	Type	Description	Condition
7	LVRENB	R/W	LVR enable control 0: enable LVR function 1: disable LVR function	
6:5	--	--	Reserved	
4	AUDIO_N_DIS	R/W	AUDIO_N disable bit available only if audio function is enabled 0: P36/P37 are output simultaneously as AUDIO_N/P 1: Only P37 is output as AUDIO_P	
3	--	--	Reserved	
2	CLKOUT_EN	R/W	Clock output enable bit (SYSCLK is output on P35)	
1	CCOUTENB	R/W	Disable output function of compare mode in Timer2 0: P1[3:1] = {compare3,compare2,compare1} 1: P1[3:1] is GPIO	
0	SCHMIT_DIS_P4	R/W	P4 Schmitt trigger function disable control bit	

Table 5-109 SYSCON0 register



If AUDCON[7:0]=8'h09 (Audio 24KHz output)



If AUDCON[7:0]=8'h0A (Audio 32KHz output)

Figure 5-35 The diagram of P36(AUDIO_N) and P37(AUDIO_P) output for audio application

5.15. Alphabetical List of Instruction Set

5.15.1. Arithmetic Operations

Mnemonic	Description	Code	Bytes	Cycles
ADD A,Rn	Add register to accumulator	0x28-0x2F	1	1
ADD A,direct	Add direct byte to accumulator	0x25	2	2
ADD A,@Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A,#data	Add immediate data to accumulator	0x24	2	2
ADDC A,Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A,direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A,#data	Add immediate data to A with carry flag	0x34	2	2
SUBB A,Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A,direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A,@Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A,#data	Subtract immediate data from A with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	2
INC direct	Increment direct byte	0x05	2	3
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	2
DEC direct	Decrement direct byte	0x15	1	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	2	3
INC DPTR	Increment data pointer	0xA3	1	1
MUL A,B	Multiply A and B	0xA4	1	2
DIV A,B	Divide A by B	0x84	1	6
DA A	Decimal adjust accumulator	0xD4	1	3

5.15.2. Logic Operations

Mnemonic	Description	Code	Bytes	Cycles
ANL A,Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A,direct	AND direct byte to accumulator	0x55	2	2
ANL A,@Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A,#data	AND immediate data to accumulator	0x54	2	2
ANL direct,A	AND accumulator to direct byte	0x52	2	3
ANL direct,#data	AND immediate data to direct byte	0x53	3	3
ORL A,Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A,direct	OR direct byte to accumulator	0x45	2	2
ORL A,@Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A,#data	OR immediate data to accumulator	0x44	2	2
ORL direct,A	OR accumulator to direct byte	0x42	2	3
ORL direct,#data	OR immediate data to direct byte	0x43	3	3
XRL A,Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A,#data	Exclusive OR immediate data to accumulator	0x64	2	2

Mnemonic	Description	Code	Bytes	Cycles
XRL direct,A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct,#data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	1

5.15.3. Boolean Operations

Mnemonic	Description	Code	Bytes	Cycles
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C,bit	AND direct bit to carry flag	0x82	2	2
ANL C,/bit	AND complement of direct bit to carry	0xB0	2	2
ORL C,bit	OR direct bit to carry flag	0x72	2	2
ORL C,/bit	OR complement of direct bit to carry	0xA0	2	2
MOV C,bit	Move direct bit to carry flag	0xA2	2	2
MOV bit,C	Move carry flag to direct bit	0x92	2	3

5.15.4. Data Transfers

Mnemonic	Description	Code	Bytes	Cycles
MOV A,Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A,direct	Move direct byte to accumulator	0xE5	2	2
MOV A,@Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV A,#data	Move immediate data to accumulator	0x74	2	2
MOV Rn,A	Move accumulator to register	0xF8-0xFF	1	1
MOV Rn,direct	Move direct byte to register	0xA8-0xAF	2	3
MOV Rn,#data	Move immediate data to register	0x78-0x7F	2	2
MOV direct,A	Move accumulator to direct byte	0xF5	2	2
MOV direct,Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1,direct2	Move direct byte to direct byte	0x85	3	3
MOV direct,@Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct,#data	Move immediate data to direct byte	0x75	3	3
MOV @Ri,A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri,direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV @Ri,#data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV DPTR,#data16	Load 16-bit constant into active DPH and DPL in LARGE mode	0x90	3	3
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator	0x93	1	5
MOVC A,@A+PC	Move code byte relative to PC to accumulator	0x83	1	4

Mnemonic	Description		Code	Bytes	Cycles
MOVX A,@Ri	Move external RAM (8-bit address) to A	XDM	0xE2-0xE3	1	3*
		SXDM			3
MOVX A,@DPTR	Move external RAM (16-bit address) to A	XDM	0xE0	1	2*
		SXDM			2
MOVX @Ri,A	Move A to external XDM (8-bit address)	ODE inside ROM/RAM	0xF2-0xF3	1	4*
		Other cases			5*
	Move A to external SXDM (8-bit address)	All cases			3
MOVX @DPTR,A	Move A to external XDM (16-bit address)	CODE inside ROM/RAM	0xF0	1	3*
		Other cases			4*
	Move A to external SXDM (16-bit address)	All cases			2
PUSH direct	Push direct byte onto IDM stack		0xC0	2	3
POP direct	Pop direct byte from IDM stack		0xD0	2	2
XCH A,Rn	Exchange register with accumulator		0xC8-0xCF	1	2
XCH A,direct	Exchange direct byte with accumulator		0xC5	2	3
XCH A,@Ri	Exchange indirect RAM with accumulator		0xC6-0xC7	1	3
XCHD A,@Ri	Exchange low-order nibble indirect RAM with A		0xD6-0xD7	1	3

5.15.5. Program Branches

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	0x11-0xF1	2	4
LCALL addr16	Long subroutine call	0x12	3	4
RET	Return from subroutine	0x22	1	4
RETI	Return from interrupt	0x32	1	4
AJMP addr11	Absolute jump	0x01-0xE1	2	3
LJMP addr16	Long jump	0x02	3	4
SJMP rel	Short jump (relative address)	0x80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	0x73	1	5
JZ rel	Jump if accumulator is zero	0x60	2	4
JNZ rel	Jump if accumulator is not zero	0x70	2	4
JC rel	Jump if carry flag is set	0x40	2	3
JNC	Jump if carry flag is not set	0x50	2	3
JB bit,rel	Jump if direct bit is set	0x20	3	5
JNB bit,rel	Jump if direct bit is not set	0x30	3	5
JBC bit,direct rel	Jump if direct bit is set and clear bit	0x10	3	5
CJNE A,direct rel	Compare direct byte to A and jump if not equal	0xB5	3	5
CJNE A,#data rel	Compare immediate to A and jump if not equal	0xB4	3	4
CJNE Rn,#data rel	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4
CJNE @Ri,#data rel	Compare immediate to ind. and jump if not equal	0xB6-0xB7	3	5
DJNZ Rn,rel	Decrement register and jump if not zero	0xD8-0xDF	2	4
DJNZ direct,rel	Decrement direct byte and jump if not zero	0xD5	3	5
NOP	No operation	0x00	1	1

6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3V ~ 6.0V
Input Voltage Range	V_{IN}	-0.3V to V_+ + 0.3V
Operating Temperature	T_A	-40℃ to +85℃
VDD Total MAX Current	I_{VDDM}	100mA
VSS Total MAX Current	I_{VSSM}	150mA

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
IOSC Frequency	F_{OSC}	24.5×(1-2%)	24.5	24.5×(1+2%)	MHz	±2% at 2.4V~5.5V

6.3. DC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	V_{LVR}	-	5.5	V	-
Operating Current	I_{OP}	-	-	10.0	mA	SYSCLK= 24.5MHz @ 5.0V, no load
Standby Current	I_{STBY}	-	-	5.0	uA	VDD = 5.5V
Input High Level	V_{IH}	0.7*VDD	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.3*VDD	V	VDD = 5.0V
Output High Level	V_{OH}	0.8*VDD	-	-	V	I_{OH} = -8mA at VDD = 5.0V
Output Low Level	V_{OL}	-	-	0.2*VDD	V	I_{OL} = 20mA at VDD = 5.0V
Input Pull High Resistor 1	R_{PH1}	30	50	70	KΩ	VDD = 5.0V
Input Pull High Resistor 1	R_{PL1}	30	50	70	KΩ	VDD = 5.0V
Low Voltage Reset 1	V_{LVR1}	2.2×(1-5%)	2.2	2.2×(1+5%)	V	CONGIF_BYTE[5]=1
Low Voltage Reset 2	V_{LVR2}	3.9×(1-5%)	3.9	3.9×(1+5%)	V	CONGIF_BYTE[5]=0

6.4. ADC Characteristics (T_A = 25℃)

6.4.1. 12 bit Mode

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	V_{LVR}	-	5.5	V	-
ADC Input Voltage Range	V_{ADCIN}	0	-	VDD	V	-
ADC Clock Period	T_{AD}	0.3265	-	-	us	ADCLKmax=24.5MHz/8
Input Channel	-	-	-	8	channel	-
Resolution	-	12			Bit	-
No Missing Code	-	10			bits	-
ADC Conversion Time	T_{CON}	5.224	-	-	us	ADCLK*16@ADCFG[1:0]=2'b00
Integral Linearity Error	E_{INL}	-	±2	±3	LSB	-
Differential Linearity Error	E_{DNL}	-	-1~+2	-1~+3	LSB	-

6.4.2. 8 bit Mode

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	V_{LVR}	-	5.5	V	-
ADC Input Voltage Range	V_{ADCIN}	0	-	VDD	V	-
ADC Clock Period	T_{AD}	0.3265	-	-	us	ADCLKmax=24.5MHz/8
Input Channel	-	-	-	8	channel	-
Resolution	-	8			Bit	-
No Missing Code	-	8			bits	-
ADC Conversion Time	T_{CON}	3.918	-	-	us	ADCLK*12@ADCFG[1:0]=2'b00
Integral Linearity Error	E_{INL}	-	±0.5	±1	LSB	-
Differential Linearity Error	E_{DNL}	-	±0.25	±0.5	LSB	-

6.5. OP Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	V_{LVR}	-	5.5	V	-
OP Input Offset	V_{in_op}	-	7	-	mV	VDD=5.0V

7. PACKAGE INFORMATION

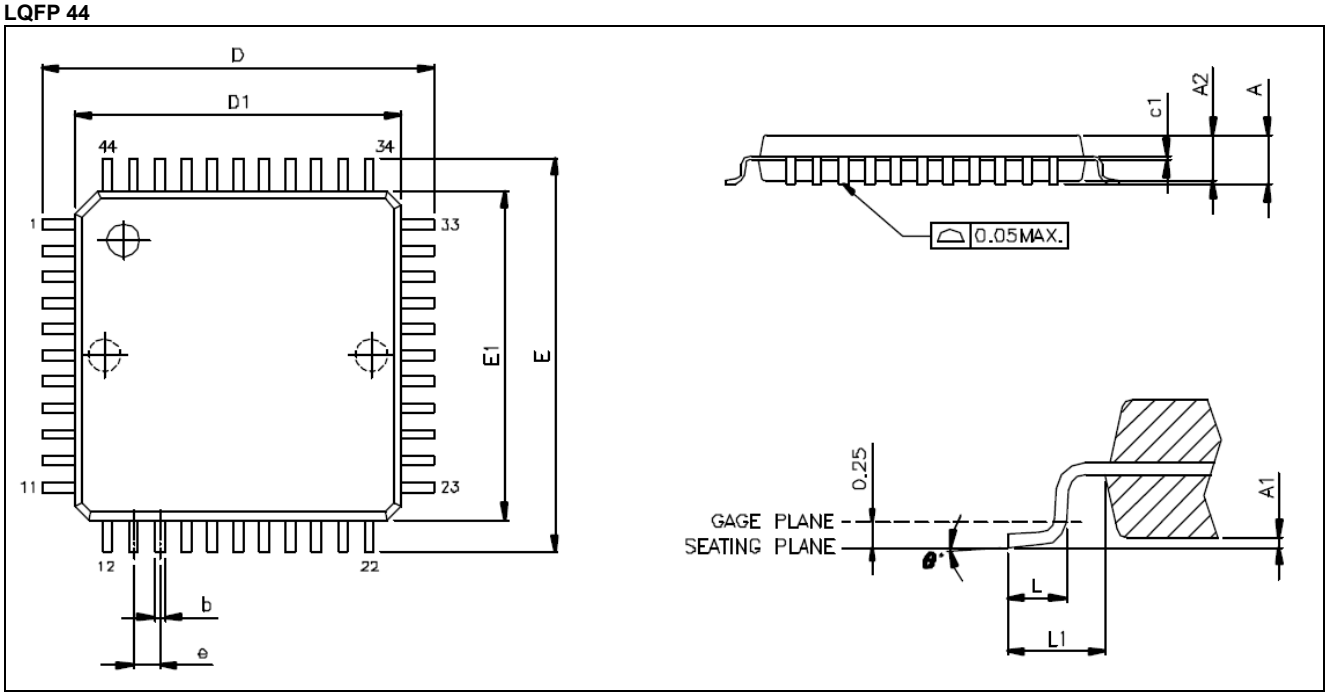
7.1. Ordering Information

Product Number	Package Type
GPM8F3232A – QL01x	Halogen Free Package
GPM8F3216A – HS05x	Halogen Free Package
GPM8F3208A – HS10x	Halogen Free Package

Note1: Package form number (x = 1 - 9, serial number).

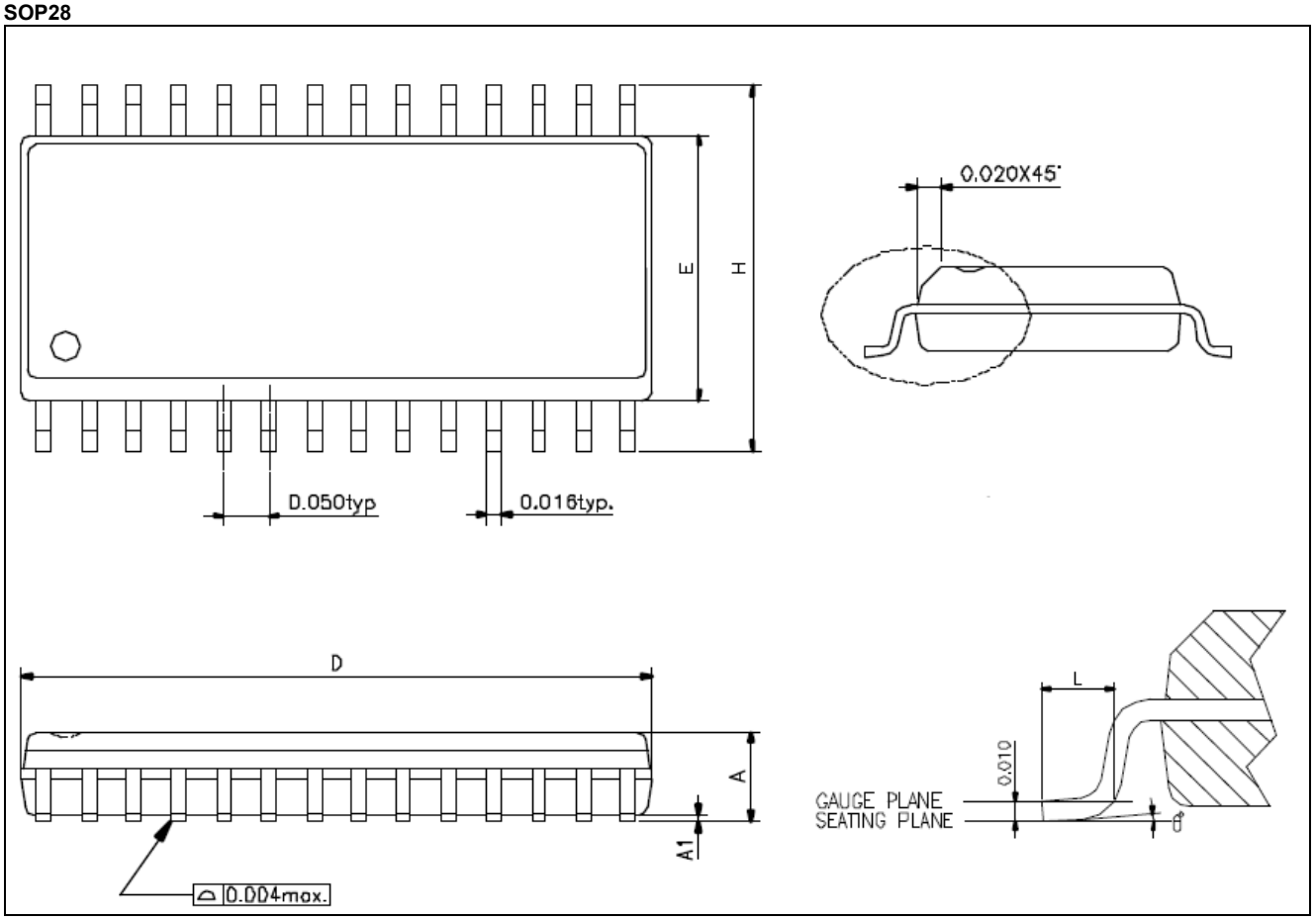
7.2. Package Information

LQFP 44



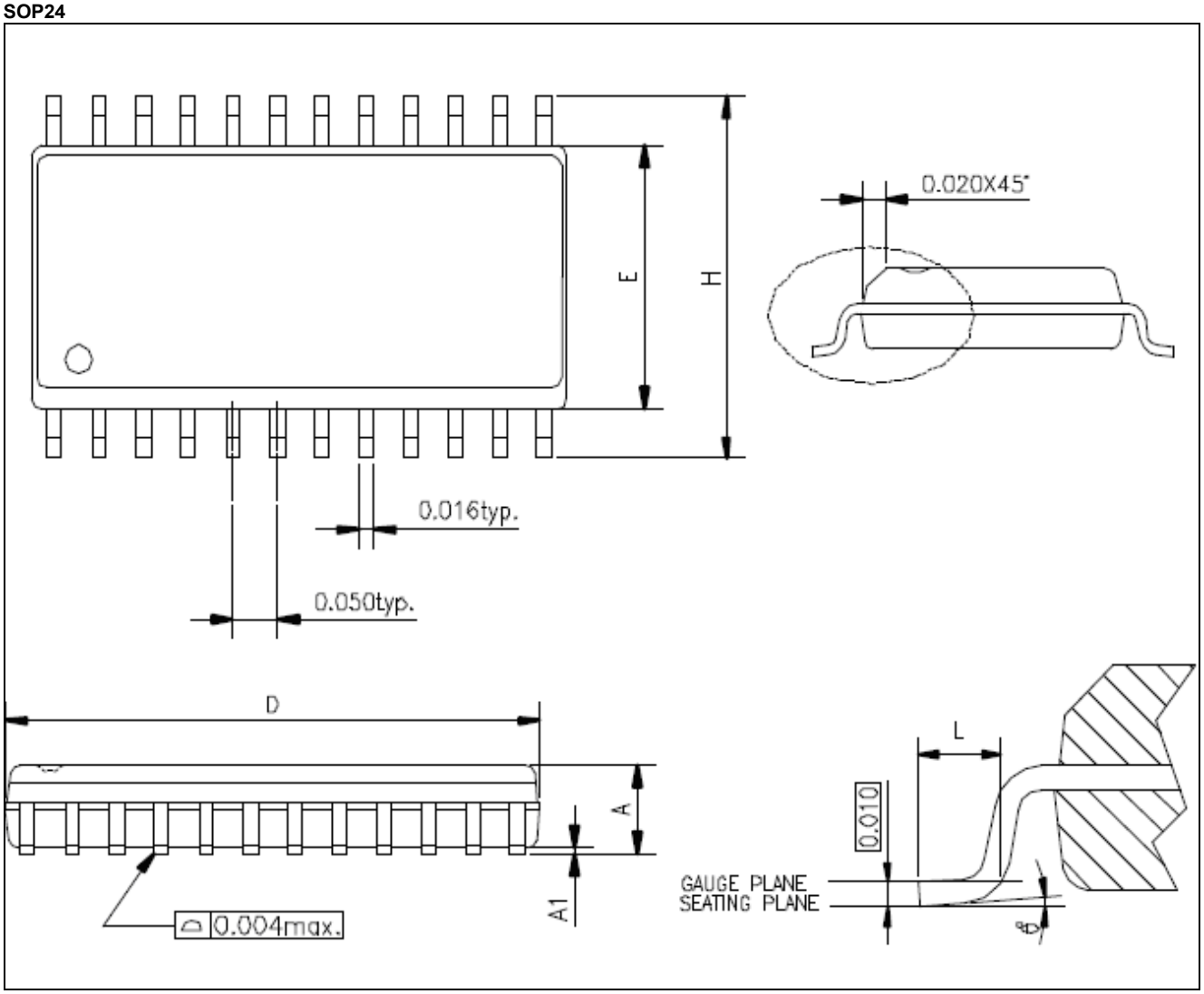
Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
c1	0.09	-	0.16
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
e		0.80 BSC	
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1		1.00 REF	
θ °	0 °	3.5 °	7 °

SOP28



Symbol	Millimeter		
	Min.	Nom.	Max.
A	0.093	-	0.104
A1	0.004	-	0.012
D	0.697	-	0.713
E	0.291	-	0.299
H	0.394	-	0.419
L	0.016	-	0.050
θ °	0 °	-	8 °

SOP24



Symbol	Millimeter		
	Min.	Nom.	Max.
A	0.093	0.099	0.104
A1	0.004	-	0.012
D	0.599	0.600	0.614
E	0.291	0.295	0.299
H	0.394	0.406	0.419
L	0.016	0.035	0.050
θ °	0 °	-	8 °

8. DISCLAIMER

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9. REVISION HISTORY

Date	Revision #	Description	Page
AUG. 03, 2012	0.1	Original	90