DATA SHEET

GPMD2130A

Synchronous MOSFET Drivers

Preliminary

May 08, 2014

Version 0.1

Table of Contents

PAGE

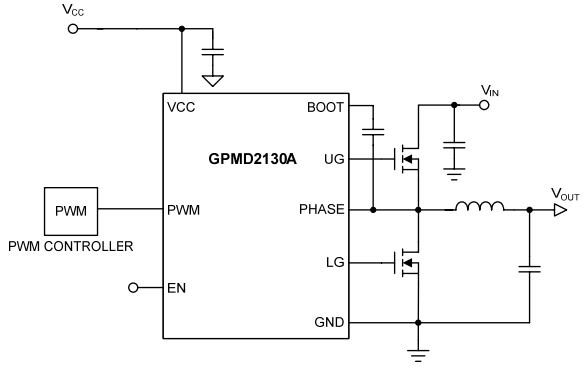
Synchronous MOSFET Drivers

1. GENERAL DESCRIPTION

The GPMD2130A is designed to drive dual N-channel MOSFETs with adaptive dead-time control. The device integrated bootstrap forward P-CH MOSFET. It's not necessary to use external Schottky barrier diode (SBD) to save cost.

The GPMD2130A has a built-in tri-state PWM input function which can support a number of PWM controllers. When the PWM input signal stays within tri-state shutdown window for the 160ns (typ.) shutdown hold-off time, the tri-state function shuts off the drivers. The device is also equipped with Power-On-Reset (POR), enable control, thermal warning and thermal shutdown functions into a single package. The POR circuit with hysteresis monitors VCC supply voltage to start up/shut down the IC at power-on/off. This thermal warning feature is the indication of the high temperature status. The thermal shutdown function shuts down the drivers when the junction temperature rises beyond 160°C and will automatically turns on the drivers when the temperature drops by 20°C. The GPMD2130A is enabled by other power system. Pulling and holding the EN pin below 0.8V shuts off the drivers.

2. SIMPLIFIED APPLICATION CIRCUIT



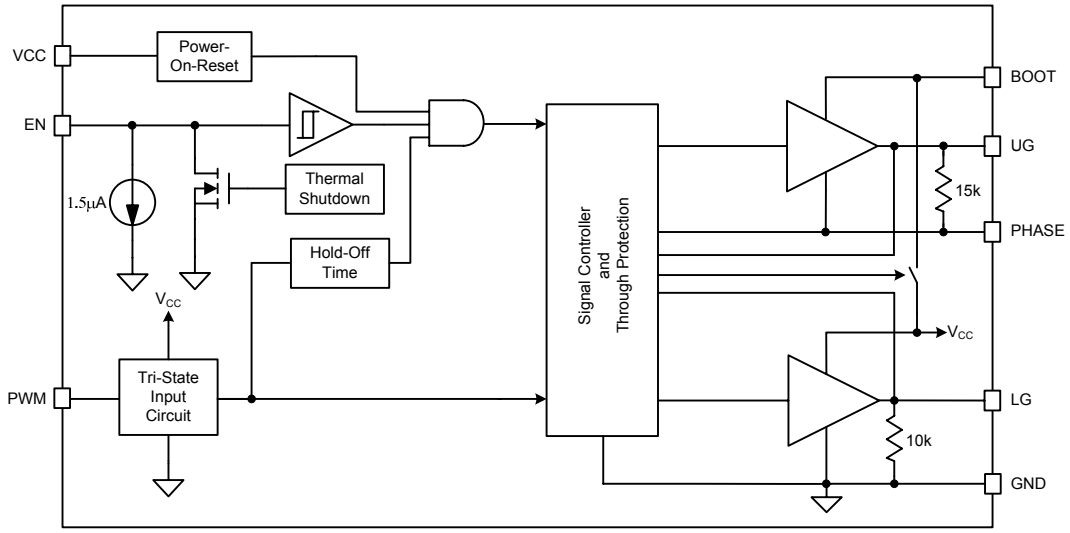
3. FEATURES

- Drives Dual N-Channel MOSFETs with 20ns Dead Time
- Built-in bootstrapping switch
- Built-in Tri-State PWM Input Function for Power Stage Shutdown
- Power-On-Reset Monitoring on VCC Pin
- Enable/Shutdown Control Function
- Over-Temperature Protection with Hysteresis
- SOP-8Package
- Lead Free and Green Devices Available (RoHS Compliant)

4. APPLICATIONS

- Desktops
- Graphics Cards
- Severs
- Portable/Notebook Regulators

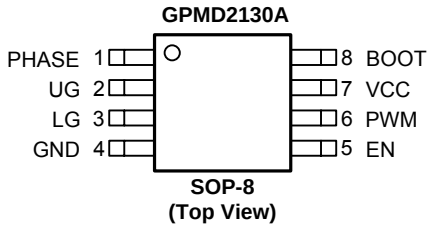
5. BLOCK DIAGRAM



6. PIN DESCRIPTIONS

Pin		Function
No.	Name	
1	PHASE	Junction point of the high-side MOSFET source, output filter inductor and the low-side MOSFET drain. Connect this pin to the source of the high-side MOSFET. This pin is used as sink for UG driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off. An Schottky diode between this pin and the ground is recommended to reduce negative transient voltage that is common in a power supply system.
2	UG	Output of the high-side MOSFET driver. Connect this pin to gate of the high-side MOSFET.
3	LG	Output of the low-side MOSFET Driver. Connect this pin to gate of the low-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the low-side MOSFET has turned off.
4	GND	Power ground for the low-side gate drivers. Connect this pin to the source of low-side MOSFET. This pin is used as sink for LG drivers. All voltage levels are measured with respect to this pin. Tie this pin to the ground island/plane through the lowest impedance connection available.
5	EN	Enable pin of the MOSFET drivers. Applying and holding the voltage on this pin above the enable voltage threshold enables the drivers. When leave this pin open, an internal pull-low current (1.5μA typical) pulls the EN voltage and shuts down the drivers. The pin is pulled low when the junction temperature rises beyond thermal shutdown level.
6	PWM	PWM drive logic input.
7	VCC	Supply voltage input pin for control circuitry. Connect +5V from the VCC pin to the AGND pin. Decoupling at least 1μF of a MLCC capacitor from the VCC pin to the AGND pin.
8	BOOT	Supply input for the UG gate driver and an internal level-shift circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.

6.1. Pin Configuration



7. FUNCTION DESCRIPTIONS

VCC Power-On-Reset (POR)

A Power-On-Reset (POR) function is designed to prevent incorrect logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the VCC supply voltage exceeds the rising POR threshold, the POR enables the device. The POR circuit has a hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the VCC pin.

Enable Control

Pulling the V_{EN} above 2V will enable the driver output, and pulling V_{EN} below 0.8V will disable the driver output. When leave this pin open, an internal pull-low current (1.5μA typical) pulls the EN voltage and shuts down the drivers. If enable function is not used, connect EN to VIN for normal operation.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of GPMD2130A. When the junction temperature exceeds +160°C, a thermal sensor turns off the drivers, allowing the device to cool down. When the device's junction temperature cools by 20°C, the internal thermal sense circuit will enable the drivers. For normal operation, the device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

8. ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC to AGND Voltage	-0.3 ~ 7	V
V_{DRV}	DRV to PGND Voltage	-0.3 ~ 7	V
V_{BOOT}	BOOT to PHASE Voltage	-0.3 ~ 7	V
V_{BOOT}	BOOT to AGND Voltage	-0.3 ~ 35	V
V_{PHASE}	PHASE to AGND Voltage >20ns Pulse Width <20ns Pulse Width	 -0.3 ~ 28 -5 ~ 35	V
V_{UG}	UG to PHASE Voltage >20ns Pulse Width <20ns Pulse Width	 -0.3 ~ V_{BOOT}+0.3 -5 ~ V_{BOOT}+0.3	V
V_{LG}	LG to PGND Voltage >20ns Pulse Width <20ns Pulse Width	 -0.3 ~ V_{CC}+0.3 -5 ~ V_{CC}+0.3	V
V_{PGND}	PGND to AGND Voltage	-0.3 ~ +0.3	V
V_{EN}, V_{PWM}, V_{THWN}, V_{LSDBL}	EN, PWM, THWN, LSDBL to AGND Voltage	-0.3 ~ V_{CC}+0.3	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 seconds)	260	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9. THERMAL CHARACTERISTICS

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2) SOP-8	110	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

10. RECOMMENDED OPERATION CONDITIONS (Note 3)

Symbol	Parameter	Range	Unit
V_{CC}, V_{DRV}	VCC, DRV to AGND Voltage	4.5 ~ 5.5	V
V_{ENH}	EN Logic High Input Voltage	2 ~ 5.5	V
V_{ENL}	EN Logic Low Input Voltage	0 ~ 0.8	V
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit

11. ELECTRICAL CHARACTERISTICS

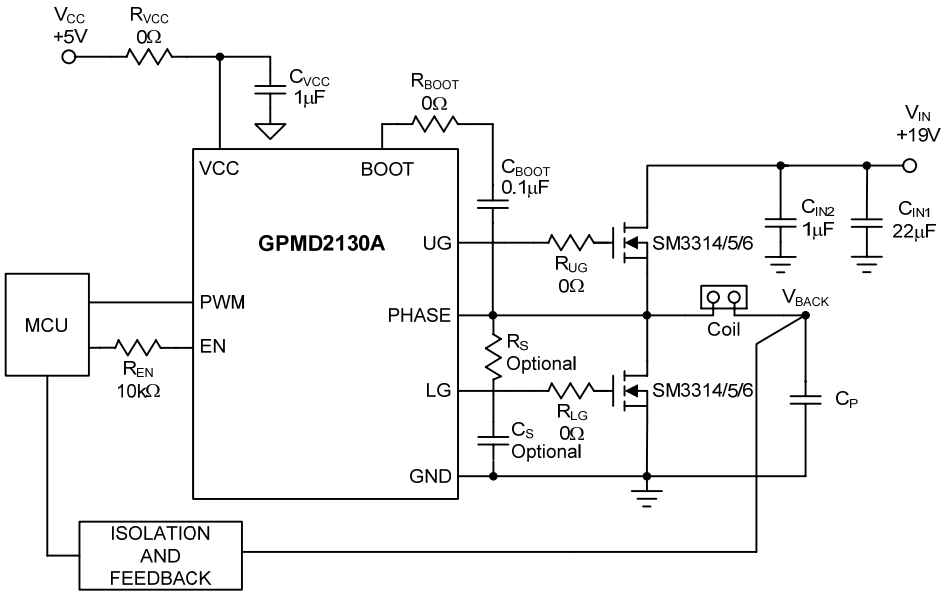
Unless otherwise specified, these specifications apply over VCC=VDRV=VBOOT=5V, VEN=5V, and TA= -40 to 85 oC. Typical values are at TA=25oC.

Symbol	Parameter	Test Conditions	GPMD2130A			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
	VCC Supply Current	LSDBL pin floating	-	0.46	-	mA
	VCC Shutdown Current	V_{EN}=0V, LSDBL pin floating	-	0.2	-	mA
POWER-ON-RESET (POR)						
	VCC Rising POR Threshold		3.5	3.7	3.9	V
	VCC POR Hysteresis		-	0.2	-	V
PWM INPUT PIN						
V_{PWM_H}	PWM Rising Threshold		3.8	-	-	V
V_{PWM_L}	PWM Falling Threshold		-	-	0.9	V
	Tri-State Shutdown Window		1.6	-	2.9	V
	Shutdown Hold-Off Time	(Note 4)	100	160	-	ns
	PWM Input Resistance	V_{PWM}=1V	-	20	-	kΩ
EN INPUT PIN						
V_{EN_H}	EN Input Logic High		2	-	-	V
V_{EN_L}	EN Input Logic Low		-	-	0.8	V
	EN Input Current			1.5	5	μA
LSDBL INPUT PIN						
V_{LD_H}	Low-Side Activation Threshold		2	-	-	V
V_{LD_L}	Low-Side Disable Threshold		-	-	0.8	V
	LSDBL Input Current	V_{LSDBL}=1V	-60	-30	-15	μA
BOOTSTRAP SWITCH						
V_F	Bootstrap Switch Resistance	$V_{DRV} - V_{BOOT-GND}$, I_F=10mA	-	0.5	0.8	V
I_R	Reverse Leakage	$V_{BOOT-GND}$=30V, V_{PHASE}=25V, V_{DRV}=5V	-	-	0.5	μA
GATE DRIVER						
	UG Pull-Up Resistance		-	1.7	2.5	Ω
	UG Sink Resistance		-	1.3	2.5	Ω
	LG Pull-Up Resistance		-	2.1	3	Ω
	LG Sink Resistance		-	0.6	1	Ω
	UG to LG Dead Time	(Note 4)	-	20	-	ns
	LG to UG Dead Time	(Note 4)	-	20	-	ns
	UG Rising Time	(Note 4)	-	20	-	ns
	UG Falling Time	(Note 4)	-	20	-	ns
	LG Rising Time	(Note 4)	-	20	-	ns
	LG Falling Time	(Note 4)	-	20	-	ns
PROTECTION						
	Thermal Shutdown Temperature	(Note 4)	-	160	-	°C
	Thermal Shutdown Hysteresis	(Note 4)	-	20	-	°C

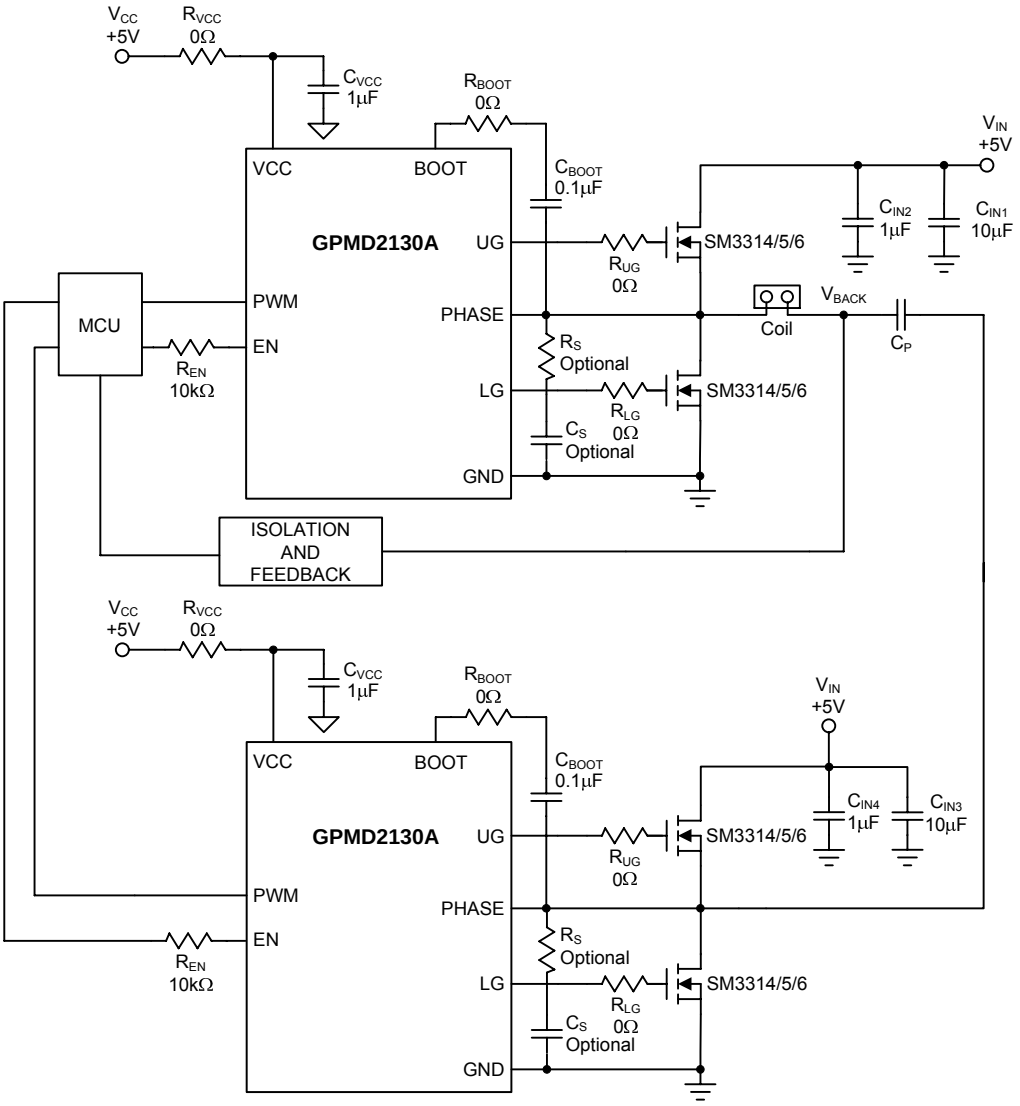
Note4: Not tested in production.

12. TYPICAL APPLICATION CIRCUIT

12.1. 19V Half Bridge Test Circuit:

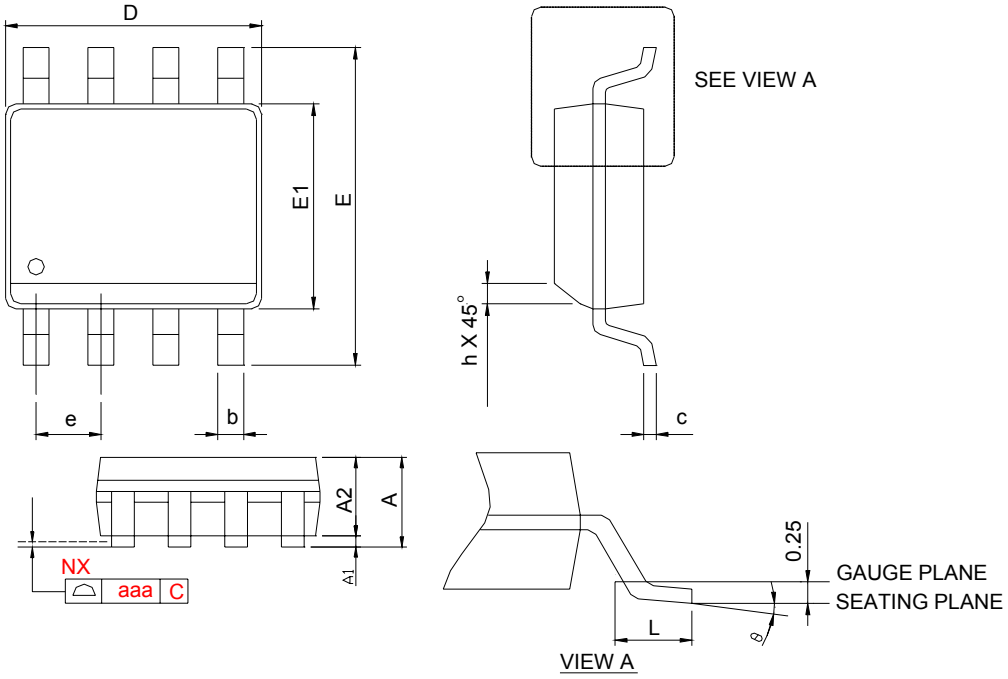


12.2. 5V Full Bridge Test Circuit:



13. PACKAGE INFORMATION

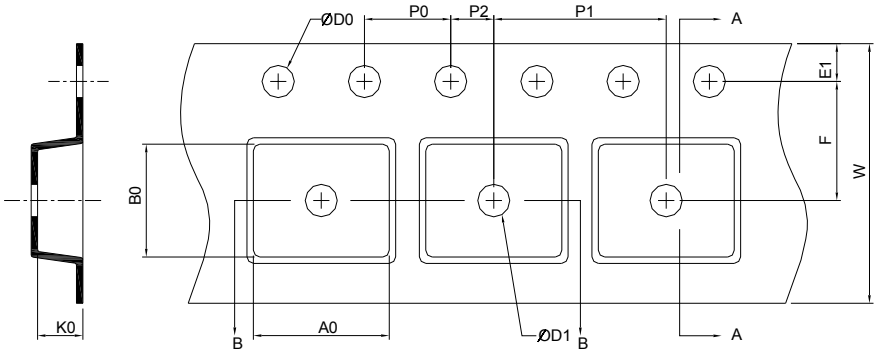
SOP-8

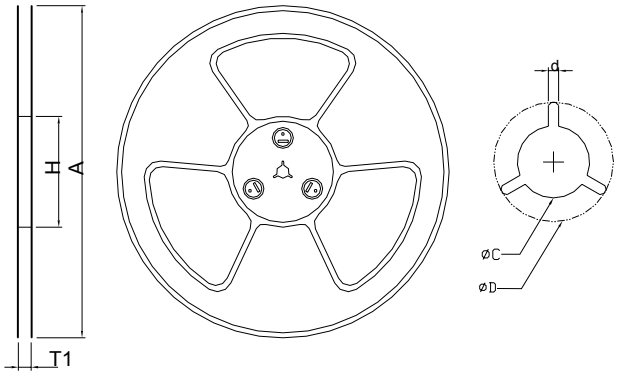


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
aaa	0.10		0.004	

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

14. CARRIER TAPE & REEL DIMENSIONS



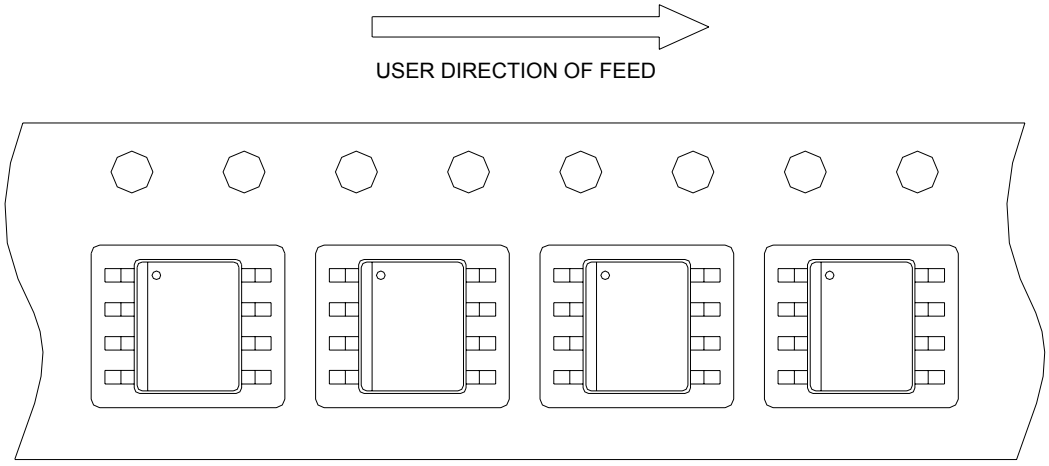


Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.55±0.20	5.25±0.20	2.10±0.20

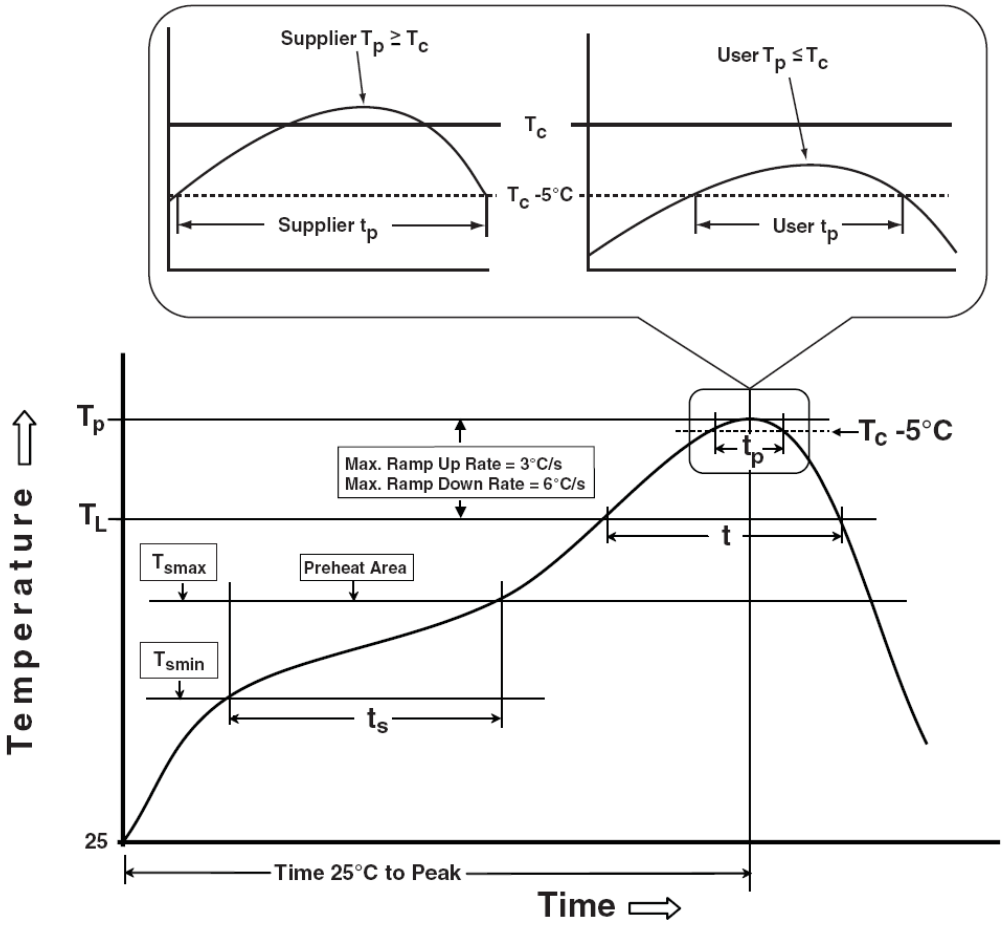
15. DEVICES PER UNIT

Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500

16. TAPING DIRECTION INFORMATION



17. CLASSIFICATION PROFILE



18. CLASSIFICATION REFLOW PROFILES

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

19. RELIABILITY TEST PROGRAM

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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21. REVISION HISTORY

Date	Revision #	Description	Page
May 08, 2014	0.1	Preliminary version	16