DATA SHEET

GPR23L1611D

3.3 Volt 16-Mbit (2M x 8 / 1M x 16)

Mask ROM with Page Mode

OCT. 15, 2009

Version 1.2

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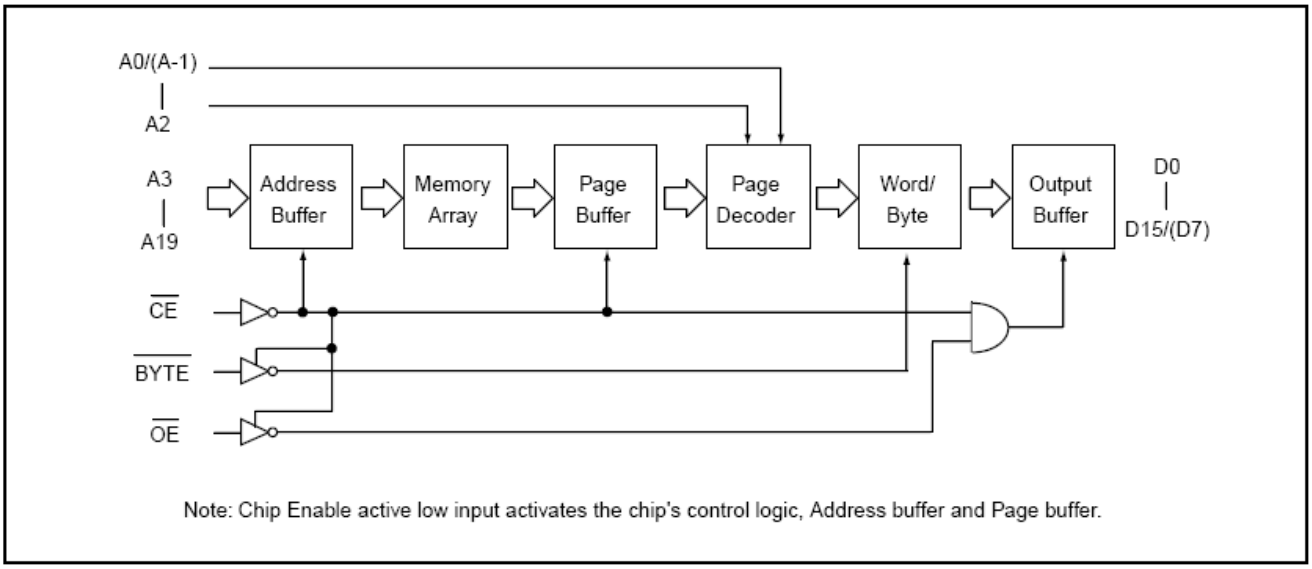
3.3 VOLT 16-MBIT (2M x 8 / 1M x 16) MASK ROM WITH PAGE MODE

1. FEATURES

- Bit organization
  - 2M x 8 (byte mode)
  - 1M x 16 (word mode)
- Fast access time
  - Random access: 100ns (max.)
  - Page access: 30ns (max.)
- Page size
  - 8 words per page
- Current
  - Operating: 40mA
  - Standby: 15uA
- Supply voltage
  - 3.0V ~ 3.6V

2. BLOCK DIAGRAM

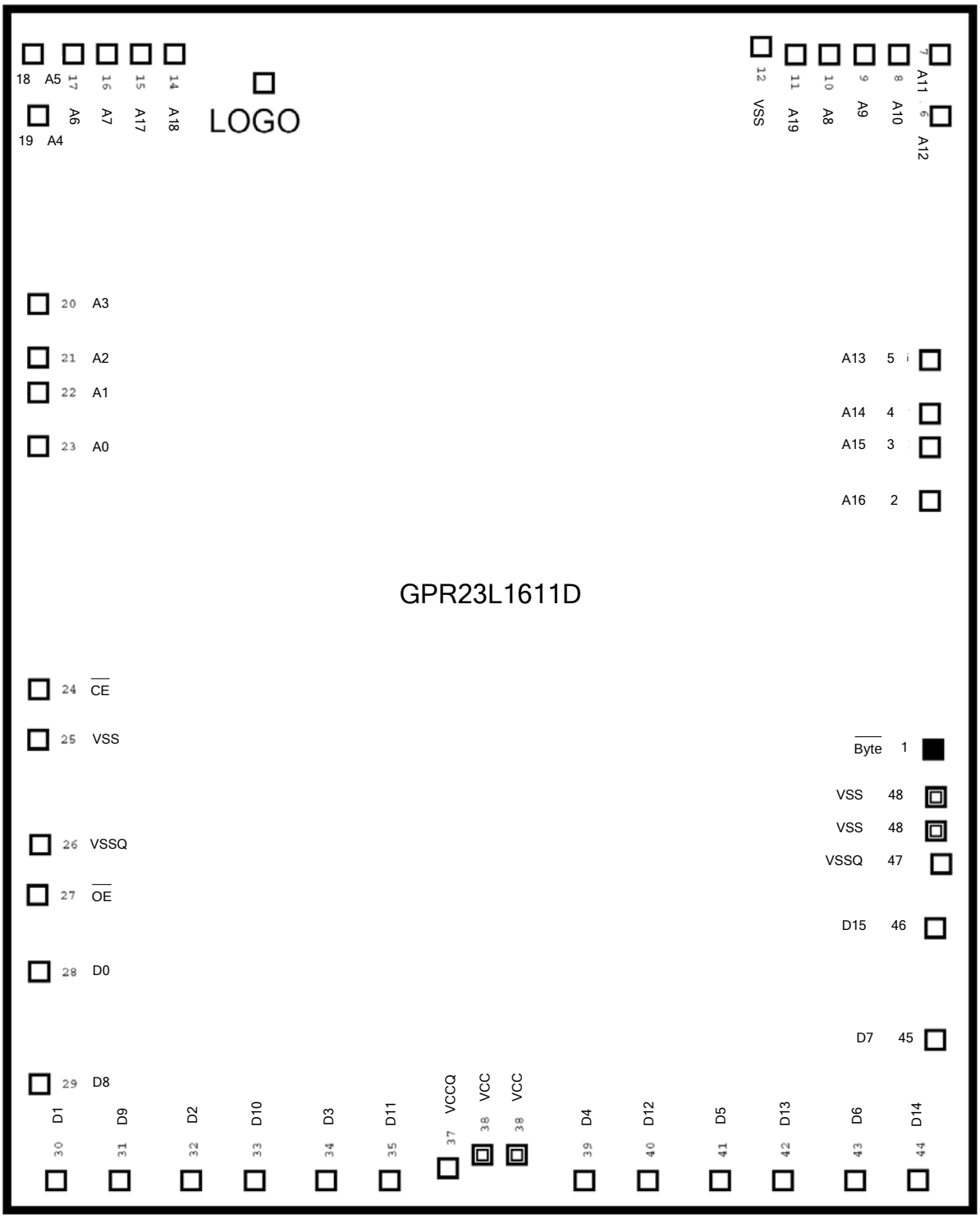


Note: Chip Enable active low input activates the chip's control logic, Address buffer and Page buffer.

3. PIN DESCRIPTION

Symbol	Pin Function
A0~A19	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode)/LSB Address (Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{Byte}$	Word/Byte Mode Selection
VCC, VCCQ	Power Supply Pin
VSS, VSSQ	Ground Pin
NC	No Connection

3.1. Pad Assignment



4. MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{Byte}$	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 3.9V
Ambient Operating Temperature	Topr	0°C to 70°C
Storage Temperature	Tstg	-65°C to 125°C

5.2. DC Characteristics (Ta = 0℃ ~ 70℃, VCC = 3.0V~3.6V)

Item	Symbol	Min.	Max.	Conditions
Output High Voltage	VOH	2.3V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.1V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.2 x VCC	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	40mA	tRC = 200ns, all outputs open, $\overline{CE}$ =VIL, $\overline{OE}$ =VIH
Standby Current (CMOS)	ISTB	-	15uA	$\overline{CE}$ >VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

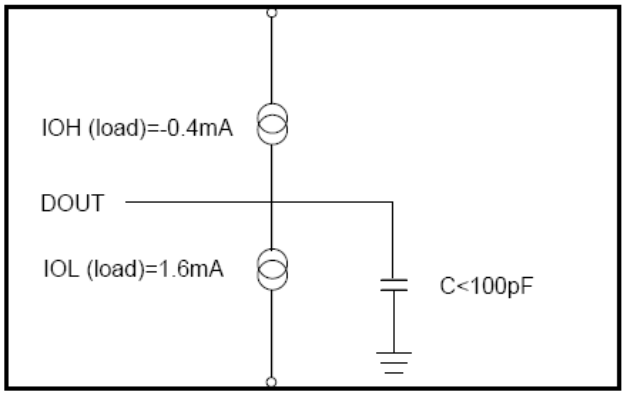
5.3. AC Characteristics (Ta = 0℃ ~ 70℃, VCC = 3.0V~3.6V)

Item	Symbol	Min.	Max.
Read Cycle Time	tRC	100ns	-
Address Access Time	tAA	-	100ns
Chip Enable Access Time	tACE	-	100ns
Page Mode Access Time	tPA	-	30ns
Output Enable Time	tOE	-	30ns
Output Hold After Address	tOH	0ns	-
Output High Z Delay	tHZ	-	20ns

Note: Output high-impedance delay (tHZ) is measured from OE or CE going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

5.4. AC Test Conditions

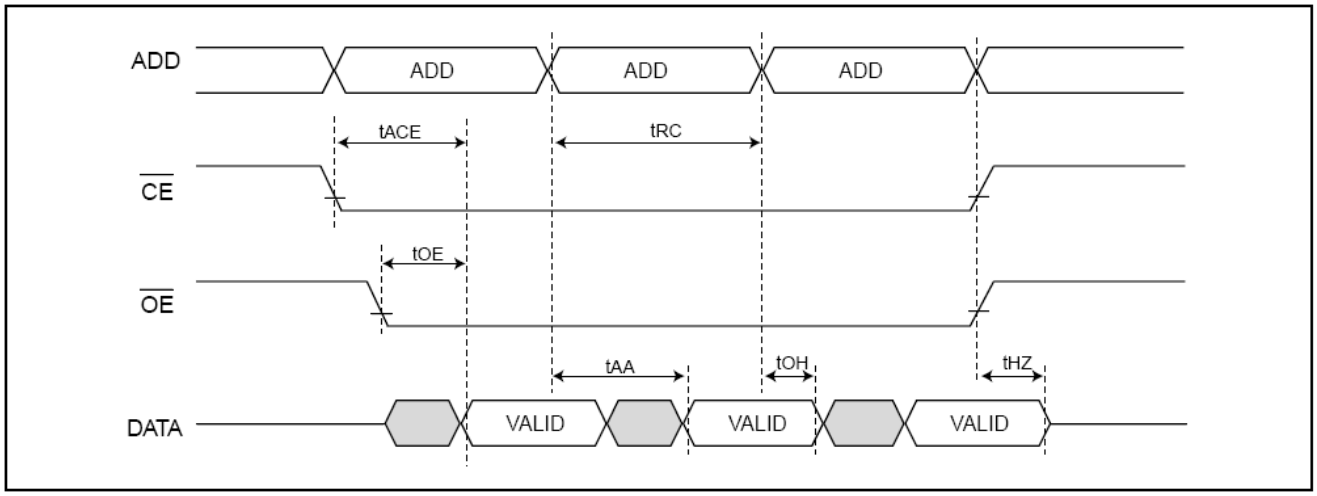
Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



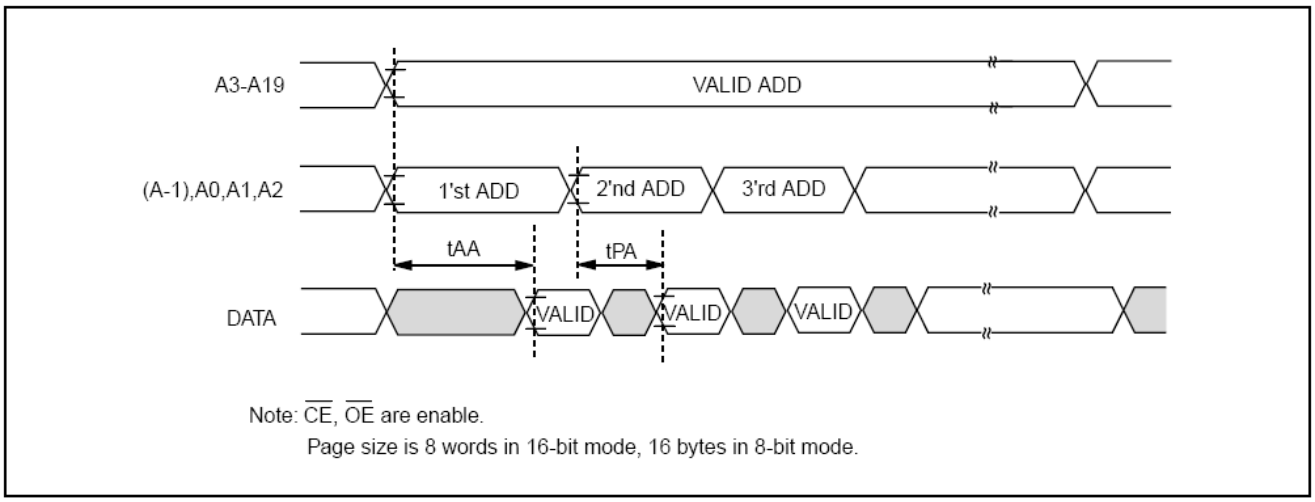
Note: No output loading is present in tester load board. Active loading is used and under software programming control. Output loading capacitance includes load board's and all stray capacitance.

6. TIMING DIAGRAM

6.1. Random Read



6.2. Page Read



Note: $\overline{CE}$, $\overline{OE}$ are enable.
Page size is 8 words in 16-bit mode, 16 bytes in 8-bit mode.

7. APPLICATION NOTE

7.1. Power Pad Bonding Guideline

1. Except NC pads, all the other Power pads should be wire bonded, please do not keep them floating.
2. Please keep the PCB layout width ε 20 mil for the VCC/VCCQ and VSS/VSSQ.(Figure 1)
3. For better noise immunity, it is recommended to add Bead (300mA minimum) and Bypass capacitor near to the VCC/VCCQ pins. (Figure 2)

7.2. PCB Layout Suggestion

1. The Substrate should be floating, not connected to GROUND.
2. Each Power pad (VCC/VCCQ, VSS/VSSQ) should be wire bonded to a dedicated power pin, then keep one centimeter distance at least before the user want to merge the PCB layout for those pins , can not be just bonded each Power pad to the same power pin.(Figure 3)
3. The Address and Data bus lines of MROM should be separated away in PCB layout.
4. Each Control pin ($\overline{CE}$ or $\overline{OE}$) should be shielded by GROUND lines.
5. If the Connector is adopted in the PCB, it is recommended to connect more sets of connections to VSS/VSSQ and VCC/VCCQ for both the PCB and the system.

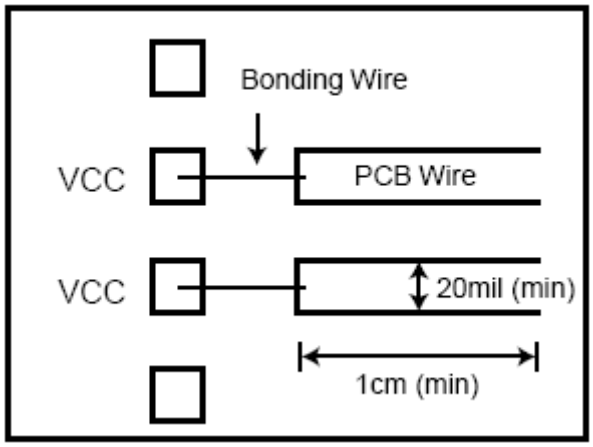


Figure 1 Power Pin Pitch

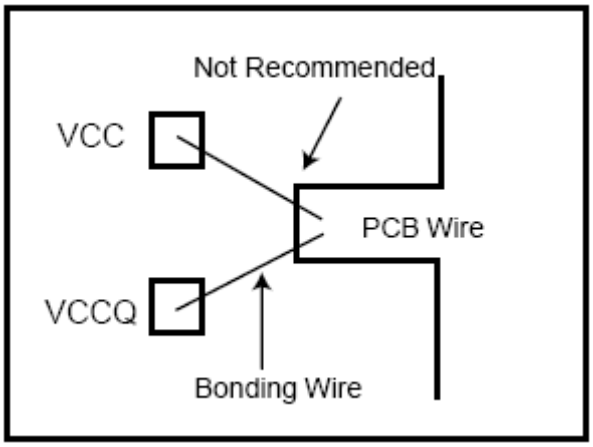


Figure 3 Dedicated Power Pin

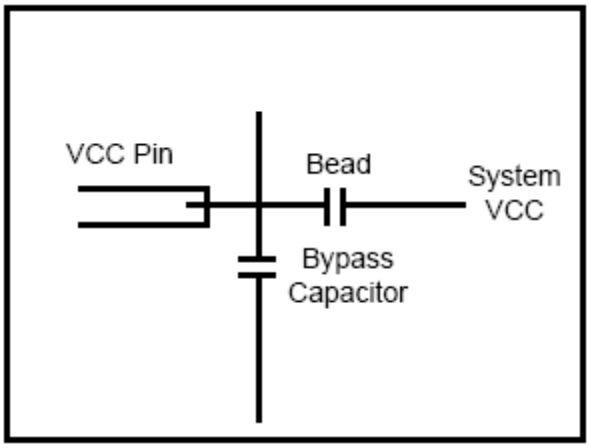


Figure 2 Bead and Bypass Capacitor to Power Pin

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPR23L1611D - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

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10. REVISION HISTORY

Date	Revision #	Description	Page
OCT. 15, 2009	1.2	1. Modify 1. FEATURES. 2. Modify 3. PIN DESCRIPTION. 3. Modify 3.1. Pad Assignment. 4. Modify 5.2. DC Characteristics. 5. Modify 5.3. AC Characteristics. 6. Modify 5.4 AC Test Conditions. 7. Modify 7. APPLICATION NOTES.	3 4 5 6 6 7 8
APR. 01, 2008	1.1	Add APPLICATION NOTE in section 7.	8
FEB. 26, 2008	1.0	Original	10