DATA SHEET

GPR23L3200E

32M-BIT MASK ROM

AUG. 16, 2010

Version 1.7

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32M-BIT MASK ROM

1. GENERAL DESCRIPTION

This device is a fully static mask programmable ROM fabricated by advance technology. It is organized either as 4M x 8 (byte mode) or as 2M x 16 (word mode) depending on the voltage level of $\overline{\text{BYTE}}$ pin. (See mode selection table). This device operates with low power supply voltage, 2.7V - 3.6V. It requires no external clock, which assure extremely easy operation.

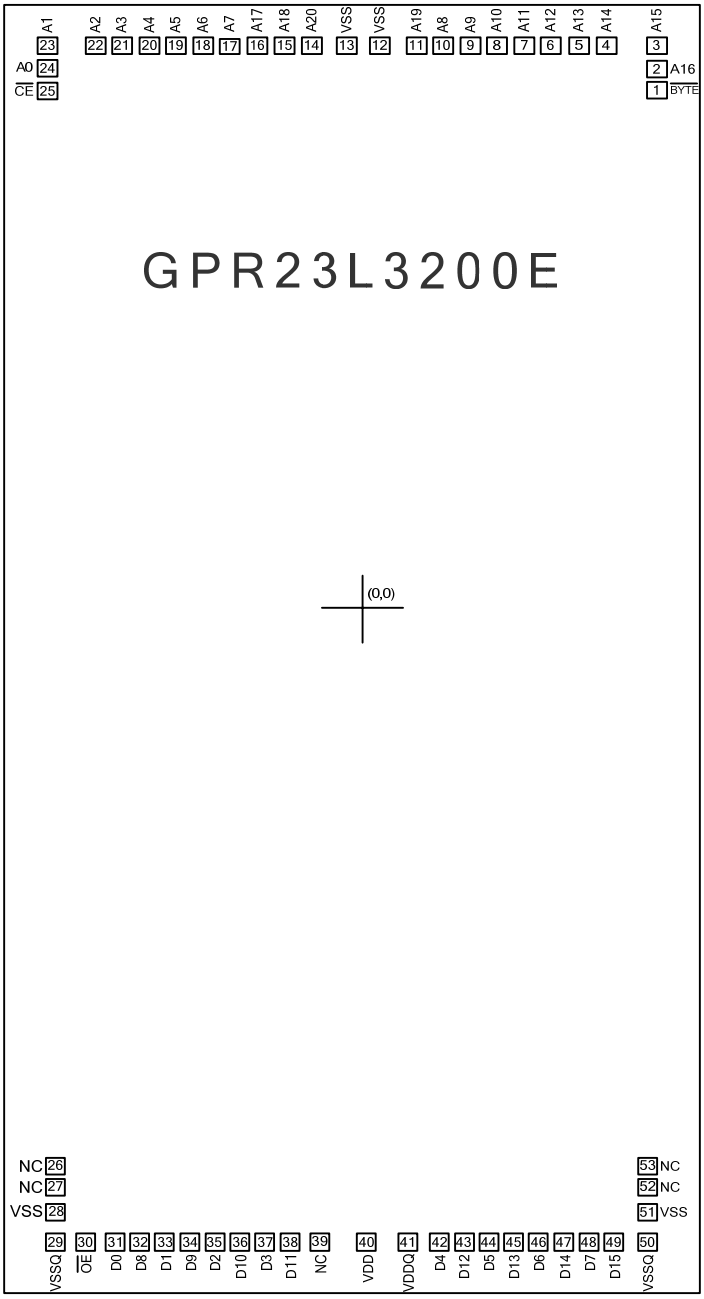
2. FEATURES

- Bit organization
  - 4M x 8 (byte mode)
  - 2M x 16 (word mode)
- Fast access time
  - Random access: 70ns
- Current
  - Operating: 40mA
  - Standby: 15μA
- Supply voltage
  - 2.7V ~ 3.6V

3. SIGNAL DESCRIPTIONS

Symbol	PIN Function
A0 ~ A20	Address Inputs
D0 ~ D14	Data Outputs
D15 / A-1	D15 (Word Mode) / LSB Address (Byte Mode)
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{BYTE}}$	Word / Byte Mode Selection
VDD	Power Supply Pin(For Internal Core)
VDDQ	Power Supply Pin(For I/O)
VSS	Ground Pin(For Internal Core)
VSSQ	Ground Pin(For I/O)
NC	No Connection

3.1. PAD Assignment



4. MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	V_{IN}	-0.3V to 3.9V
Ambient Operating Temperature	T_{OPR}	0℃ to 70℃
Storage Temperature	T_{STG}	-65℃ to 125℃

5.2. DC Characteristics (VDD = 2.7V ~ 3.6V, T_A = 0℃ ~ 70℃)

Item	Symbol	Min.	Max.	Conditions
Output High Voltage	VOH	2.3V	-	IOH = -400μA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.1V	VDD + 0.3V	-
Input Low Voltage	VIL	-0.3V	0.2XVDD	-
Input Leakage Current	ILI	-	5.0μA	0V, VDD
Output Leakage Current	ILO	-	5.0μA	0V, VDD
Operating Current	ICC	-	40mA	f = 5.0MHz, $\overline{CE}$ = VIL, $\overline{OE}$ = VIH, all output open
Standby Current (TTC)	ISTB1	-	1.0mA	$\overline{CE}$ = VIH
Standby Current (CMOS)	ISTB2	-	15μA	$\overline{CE}$ > VDD-0.2V
Input Capacitance	CIN	-	10pF	T_A = 25°C, f = 1.0MHZ
Output Capacitance	COUT	-	10pF	T_A = 25°C, f = 1.0MHZ

5.3. AC Characteristics (VDD = 2.7V ~ 3.6V, T_A = 0℃ ~ 70℃)

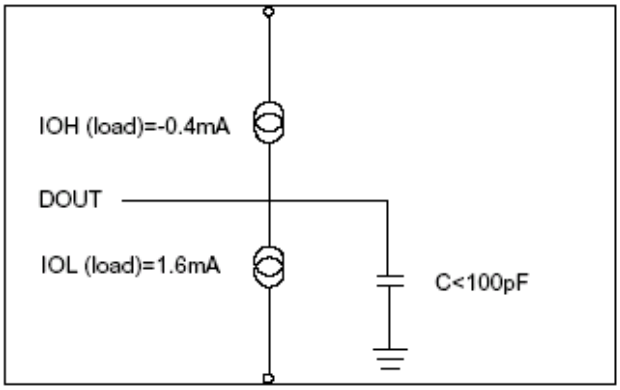
Item	Symbol	Min.	Max.
Read Cycle Time	tRC	70ns	-
Address Access Time	tAA	-	70ns
Chip Enable Access Time	tACE	-	70ns
Output Enable Time	tOE	-	35ns
Output Hold After Address	tOH	0ns	-
Output High Z Delay	tHZ	-	20ns

Note: Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guar-anteed by design over the full voltage and temperature operating range - not tested.

5.4. AC Test Conditions

Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure

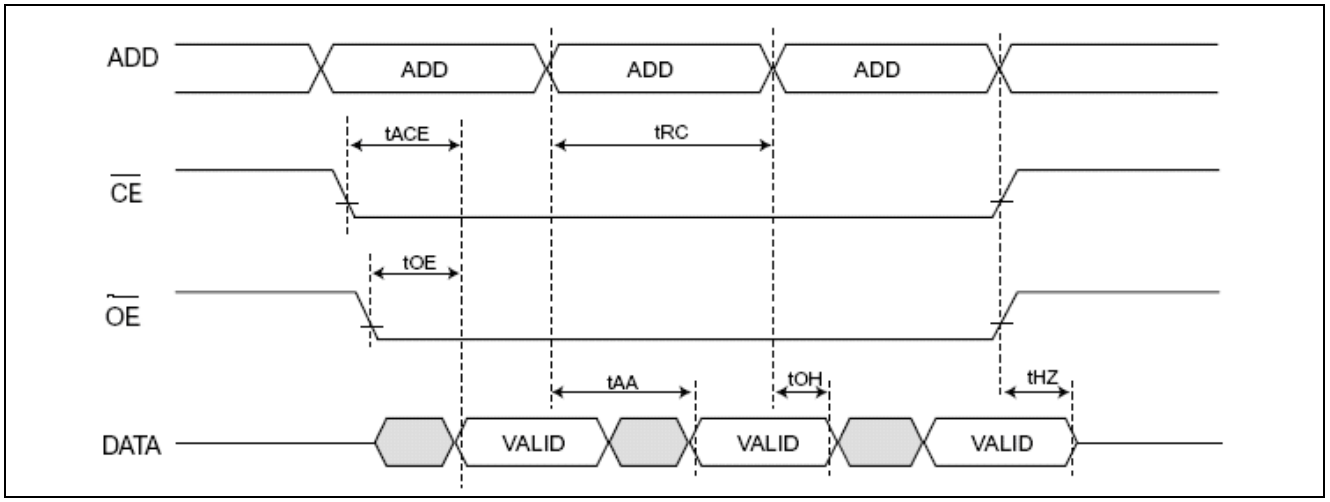
Note: 30pF output load capacitance for 70ns speed grade



Note: No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

5.5. Timing Diagram

5.5.1. Random read



Important Note: It will fail to read 1st data from GPR23L3200E after power on if $\overline{CE}$ is always set to ground level. Please refer the application note for further details.

6. APPLICATION NOTE

6.1. Power Pad Bonding Guideline

1. Except NC pads, all the other Power pads should be wire bonded, please do not keep them floating.
2. Please keep the PCB layout width ε 20 mil for the VDD/VDDQ and VSS/VSSQ.(Figure 2)
3. For better noise immunity, it is recommended to add Bead (300mA minimum) and Bypass capacitor near to the VDD/VDDQ pins. (Figure 3)

6.2. PCB Layout Suggestion

1. The Substrate should be floating, not connected to GROUND.
2. Each Power pad (VDD/VDDQ, VSS/VSSQ) should be wire bonded to a dedicated power pin, then keep one centimeter distance at least before the user want to merge the PCB layout for those pins , can not be just bonded each Power pad to the same power pin.(Figure 4)
3. The Address and Data bus lines of MROM should be separated away in PCB layout.
4. Each Control pin ($\overline{CE}$ or $\overline{OE}$) should be shielded by GROUND lines.
5. If the Connector is adopted in the PCB, it is recommended to connect more sets of connections to VSS/VSSQ and VDD/VDDQ for both the PCB and the system.

Figure 2. Power Pin Pitch

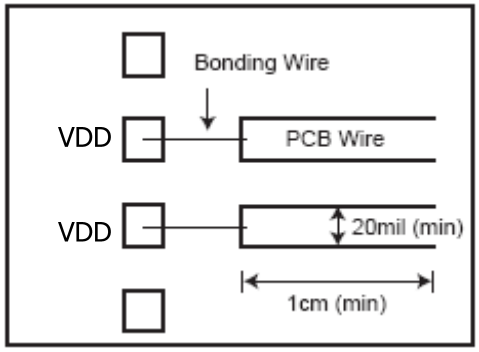


Figure 3. Bead and Bypass Capacitor to Power Pin

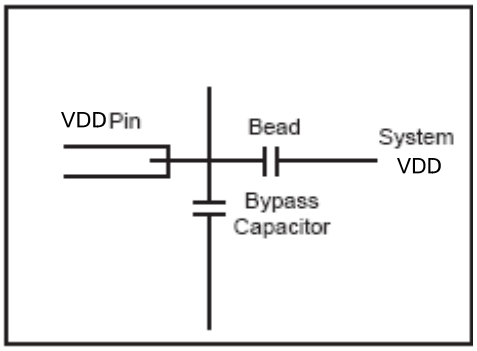
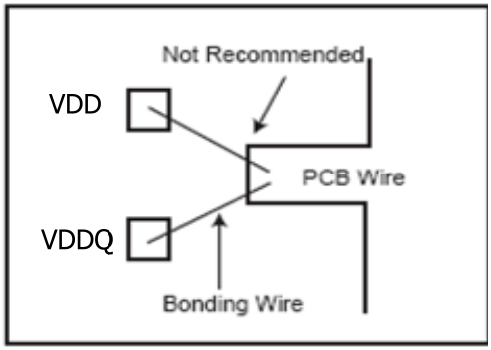


Figure 4. Dedicated Power Pin



7. ORDERING INFORMATION

Product Number	Package Type
GPR23L3200E - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

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9. REVISION HISTORY

Date	Revision #	Description	Page
AUG. 16, 2010	1.7	Modify 3.1 Pad Assignment.	4
DEC. 25, 2009	1.6	1. Modify 2. SIGNAL DESCRIPTION. 2. Modify 3. PIN DESCRIPTION. 3. Modify 3.1. Pad Assignment. 4. Modify 5.2. DC Characteristics. 5. Add section 6. APPLICATION NOTE.	3 3 4 5 7
JAN. 03, 2008	1.5	1. Delete section 3.1.1 “48 TSOP”. 2. Delete section 5 “PACKAGE INFORMATION”. 3. Modify “Ordering information” in section 6.	4 7 7
AUG. 21, 2007	1.4	1. Modify the “PIN Configuration” in section 3.1. 2. Add footnote to section 4.5.1.	4 6
MAR. 29, 2007	1.3	Modify the “Ordering Information” in section 3.2.	4
MAR. 01, 2006	1.2	1. Add the note to section 3.1.	4
JAN. 10, 2006	1.1	2. Add the “GENERAL DESCRIPTION” to section 1. 3. Add the “PIN Configuration” to section 3.1. 4. Modify the “Ordering Information” and “Mode Selection” in section 3.2 and 3.3. 5. Modify the “48-PIN plastic TSOP” in section 5.1.	3 4 4 7
APR. 28, 2005	1.0	Original Note: The GPR23L3200E data sheet v1.0 is a continued version of SPR23L3200E data sheet v1.0.	7