DATA SHEET

GPR23L6411E

64M-Bit Page Mode Mask ROM

AUG. 16, 2010

Version 1.2

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64M-BIT PAGE MODE MASK ROM

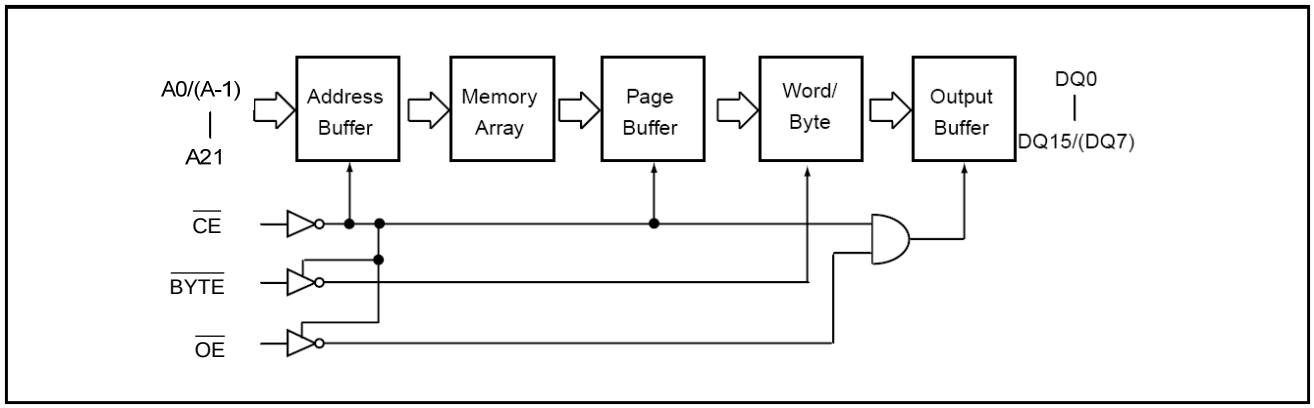
1. FEATURES

- Bit organization
  - 8M x 8 (byte mode)
  - 4M x 16 (word mode)
- Fast access time
  - Random access: 70ns (max.)
  - Page access: 25ns (max.)
- Page size
  - 8 words per page
- Current
  - Operating: 20mA
  - Standby: 15uA
- Supply voltage
  - 2.7V ~ 3.6V

2. PIN DESCRIPTION

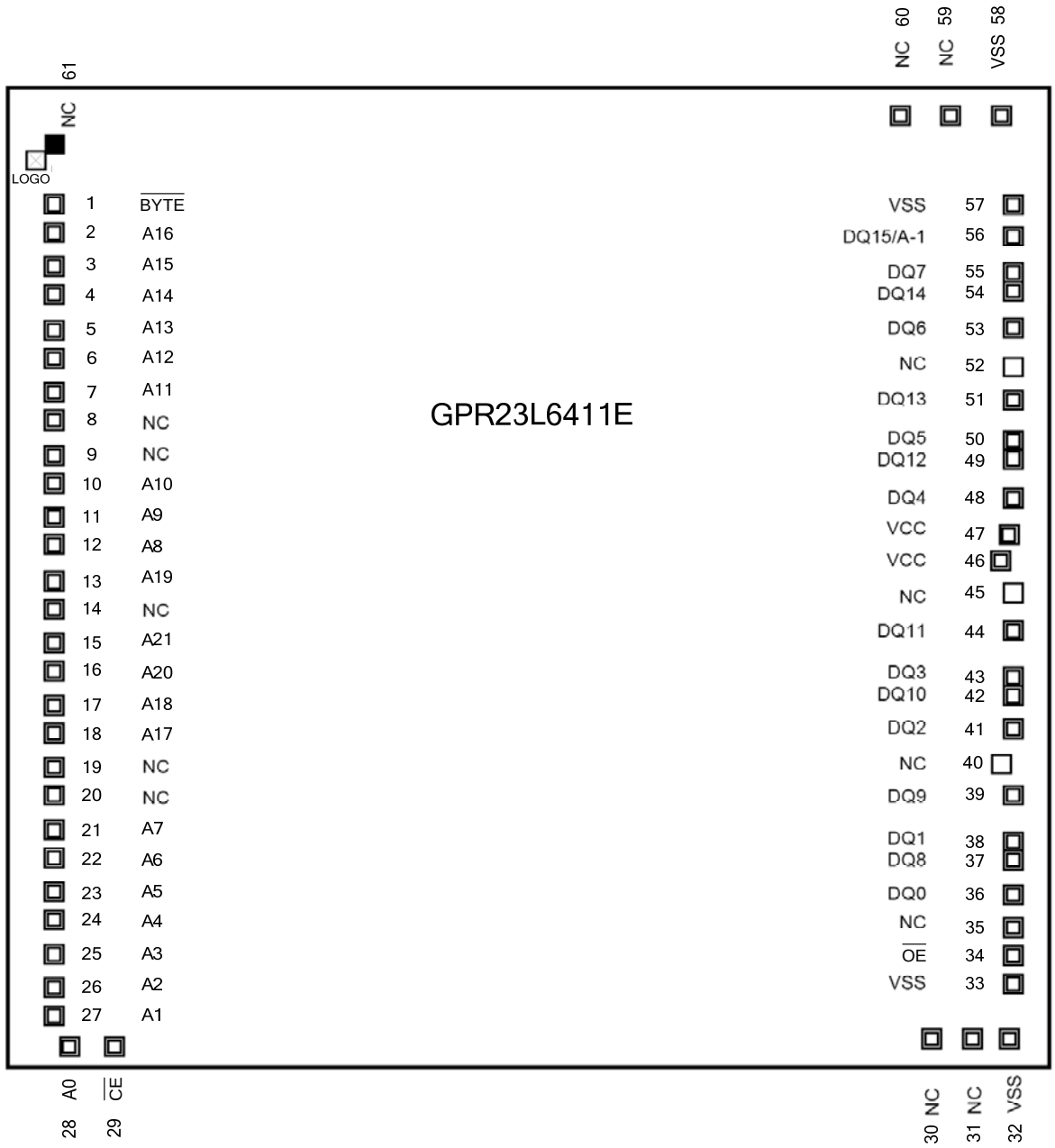
Symbol	PIN Function
A0~A21	Address Input
DQ0~DQ14	Data Outputs
DQ15/A-1	D15 (Word Mode)/ LSB Address(Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$	Word/ Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

3. LOCK DIAGRAM



4. PIN CONFIGURATION

4.1. PAD Assignment



5. MODES SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	DQ15/A-1	DQ0~DQ7	DQ8~DQ15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	DQ0~DQ7	DQ8~DQ15	Word	Active
L	L	L	Input	DQ0~DQ7	High Z	Byte	Active

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to Vcc+1.4V
Ambient Operating Temperature	Topr	0°C to 70°C
Storage Temperature	Tstg	-65°C to 125°C

6.2. DC Characteristics (Ta = 0℃ ~ 70℃, VCC = 2.7V~3.6V)

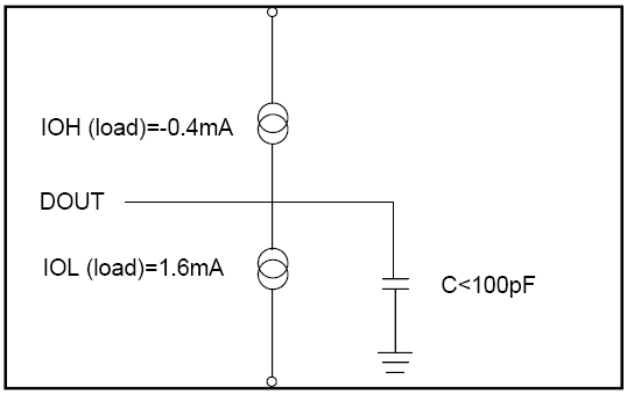
Item	Symbol	Min.	Max.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -400uA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	0.7xVCC	VCC+0.3	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC	-	20mA	f=5MHz, $\overline{CE}$ =VIL, $\overline{OE}$ =VIH all output open
Standby Current (CMOS)	ISTB	-	15uA	$\overline{CE}$ >VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

6.3. AC Characteristics (Ta = 0℃ ~ 70℃, VCC = 2.7V~3.6V)

Item	Symbol	Min.	Max.
Read Cycle Time	tRC	70ns	-
Address Access Time	tAA	-	70ns
Chip Enable Access Time	tCE	-	70ns
Page Access Time	tPA	-	25ns
Output Enable Time	tOE	-	25ns
Output Hold After Address	tOH	0ns	-
Output High Z Delay	tHZ	-	20ns

6.4. AC Test Conditions

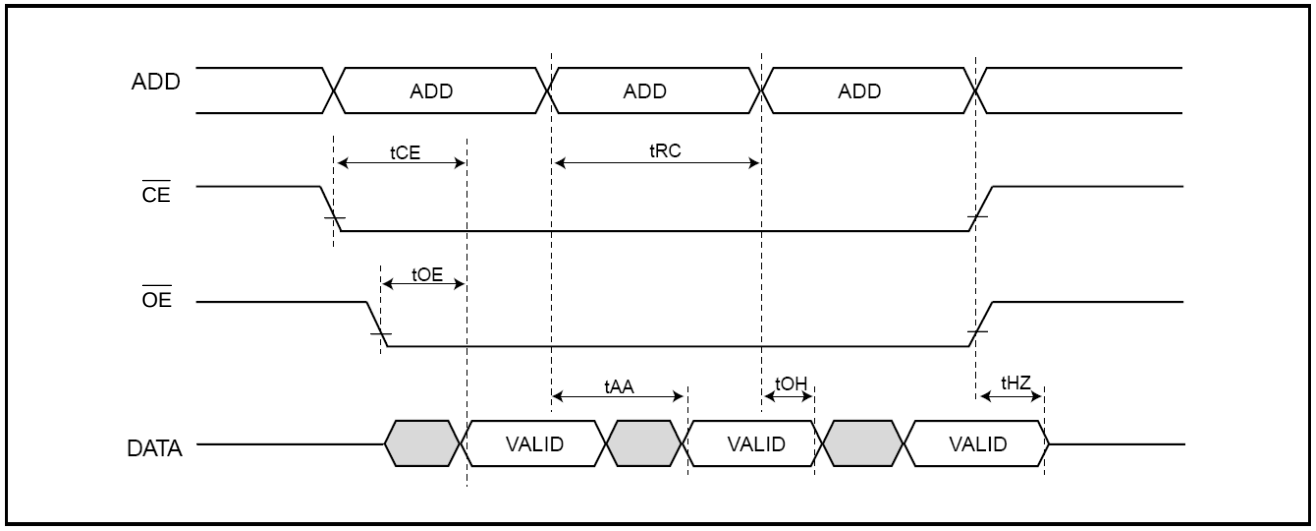
Input Pulse Levels	0V~ 3.0V
Input Rise and Fall Times	5ns
Input Timing Level	1.5V
Output Timing Level	1.5V
Output Load	See Figure



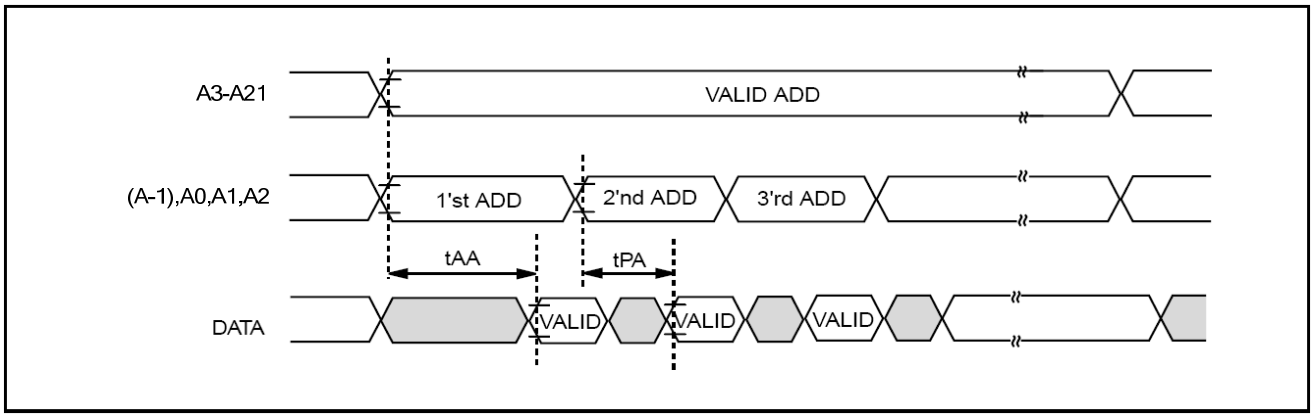
Note: No output loading is present in tester load board. Active loading is used and under software programming control. Output loading capacitance includes load board's and all stray capacitance.

7. TIMING DIAGRAM

7.1. Random Read



7.2. Page Read



8. APPLICATION NOTE

8.1. Power Pad Bonding Guideline

1. Except NC pads, all the other Power pads should be wire bonded, please do not keep them floating.
2. Please keep the PCB layout width ε 20 mil for the VCC/VCCQ and VSS/VSSQ.(Figure 1)
3. For better noise immunity, it is recommended to add Bead (300mA minimum) and Bypass capacitor near to the VCC/VCCQ pins. (Figure 2)

8.2. PCB Layout Suggestion

1. The Substrate should be floating, not connected to GROUND.
2. Each Power pad (VCC/VCCQ, VSS/VSSQ) should be wire bonded to a dedicated power pin, then keep one centimeter distance at least before the user want to merge the PCB layout for those pins , can not be just bonded each Power pad to the same power pin.(Figure 3)
3. The Address and Data bus lines of MROM should be separated away in PCB layout.
4. Each Control pin (PCEB or POEB) should be shielded by GROUND lines.
5. If the Connector is adopted in the PCB, it is recommended to connect more sets of connections to VSS/VSSQ and VCC/VCCQ for both the PCB and the system.

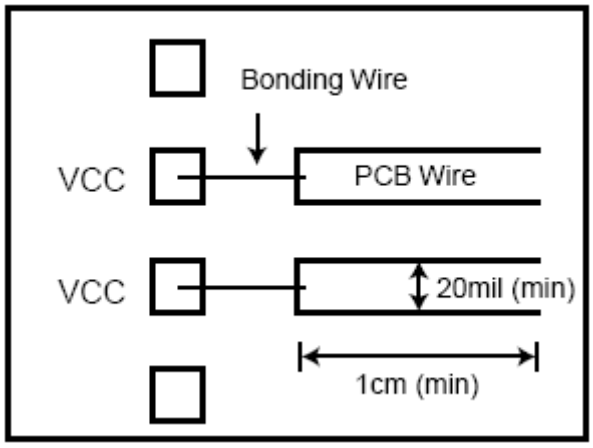


Figure 1 Power Pin Pitch

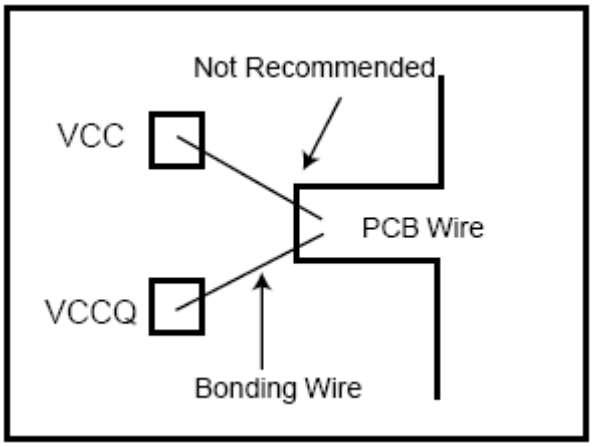


Figure 3 Dedicated Power Pin

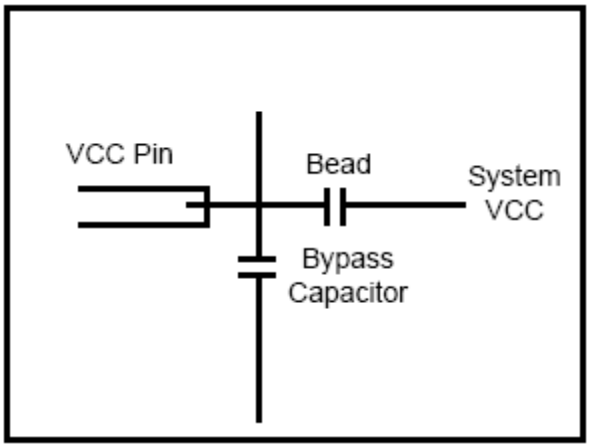


Figure 2 Bead and Bypass Capacitor to Power Pin

9. ORDERING INFORMATION

Product Number	Package Type
GPR23L6411E - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision#	Description	Page
AUG. 16, 2010	1.2	Modify 4.1 Pad Assignment and Locations.	4
APR. 01, 2008	1.1	Add APPLICATION NOTE in section 8.	7
NOV. 20, 2007	1.0	Original	9