DATA SHEET

GPR23L800D

8M-BIT MASK ROM

DEC. 25, 2009

Version 1.5

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8M-BIT MASK ROM

1. FEATURES

- Bit organization
  - 1M x 8 (byte mode)
  - 512K x 16 (word mode)
- Fast access time
  - Random access: 70ns(max.)
- Current
  - Operating: 15mA
  - Standby: 5μA
- Supply voltage
  - 2.7V ~ 3.6V

2. SIGNAL DESCRIPTIONS

Symbol	PIN Function
A0~A18	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode)/ LSB Address (Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$	Word/ Byte Mode Selection
VDD	Power Supply Pin
VSS	Ground Pin
NC	No Connection

2.1. PAD Assignment

3. MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

4. ELECTRICAL SPECIFICATIONS

4.1. Absolute Maximum Ratings

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	V_{IN}	-0.3V to 3.9V
Ambient Operating Temperature	T_{OPR}	-0℃ to 70℃
Storage Temperature	T_{STG}	-65℃ to 125℃

4.2. DC Characteristics (VDD = 2.7V ~ 3.6V, T_A = 0°C ~ 70°C)

Item	Symbol	Min.	Max.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -400μA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.1V	VCC+0.3V	-
Input Low Voltage	VIL	-0.3V	0.8V	-
Input Leakage Current	ILI	-	5.0μA	0V, VCC
Output Leakage Current	ILO	-	5.0μA	0V, VCC
Operating Current	ICC	-	15mA	f = 5.0MHz, $\overline{CE}$ = VIL, $\overline{OE}$ = VIH, all output open
Standby Current (CMOS)	ISTB	-	5.0μA	$\overline{CE}$ > VCC - 0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1.0MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1.0MHZ

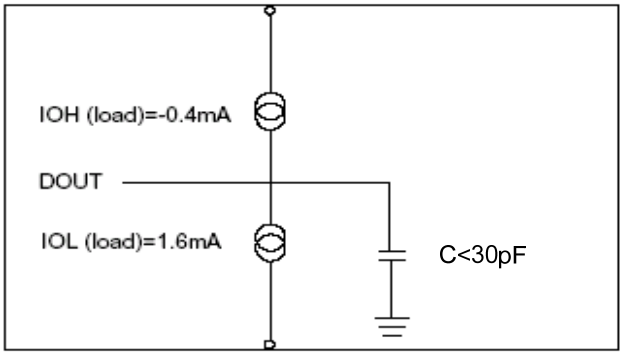
4.3. AC Characteristics (VDD = 2.7V ~ 3.6V, T_A = 0°C ~ 70°C)

Item	Symbol	Min.	Max.
Read Cycle Time	tRC	70ns	-
Address Access Time	tAA	-	70ns
Chip Enable Access Time	tACE	-	70ns
Output Enable Time	tOE	-	30ns
Output Hold After Address	tOH	0ns	-
Output High Z Delay	tHZ	-	20ns

Note: Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guar-anteed by design over the full voltage and temperature operating range - not tested.

4.4. AC Test Conditions

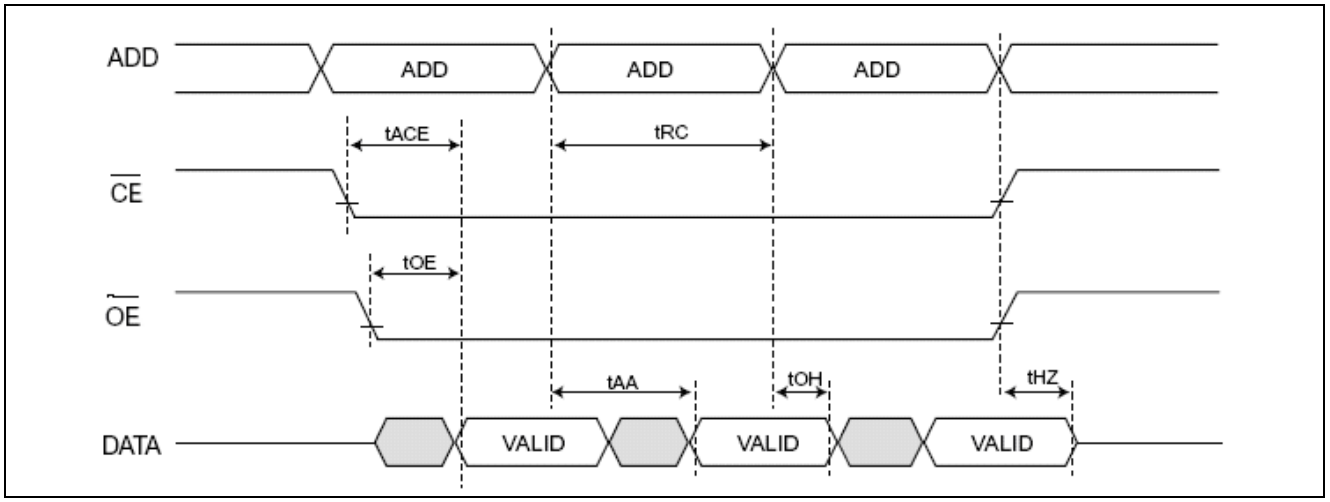
Input Pulse Levels	0V~ 3.0V
Input Rise and Fall Times	5ns
Input Timing Level	1.5V
Output Timing Level	1.5V
Output Load	See Figure



Note: No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

4.5. Timing Diagram

4.5.1. Random Read



Important Note: It will fail to read 1st data from GPR23L800D after power on if** $\overline{CE}$ **is always set to ground level. Please refer the application note for further details.

5. PACKAGE/PAD LOCATIONS

5.1. Ordering Information

Product Number	Package Type
GPR23L800D - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

6. DISCLAIMER

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7. REVISION HISTORY

Date	Revision #	Description	Page
DEC. 25, 2009	1.5	Modify 4.4. AC Test Conditions.	5
JAN. 03, 2008	1.4	1. Delete section 2.1 “Pin Configuration”. 2. Modify “Ordering Information” in section 5.1.	3 6
AUG. 21, 2007	1.3	1. Modify the “PIN Configuration” in section 2.1. 2. Add footnote to section 4.5.1.	3 5
JAN. 08, 2007	1.2	1. Modify the “PIN Configuration” in section 2.1. 2. Modify the “Absolute Maximum Ratings” in section 4.1. 3. Modify the “Ordering Information” in section 5.2.	3 4 6
FEB. 27, 2006	1.1	Add the “PIN Configuration” to section 2.1.	3
JUL. 04, 2005	1.0	Original Note: The GPR23L800D data sheet v1.0 is a continued version of SPR23L800D data sheet v1.0.	7