DATA SHEET

Generalplus

GPR25L162B

16M-BIT [x1 / x2] CMOS SERIAL FLASH

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Version 1.4

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16M-BIT [x 1/ x 2] CMOS SERIAL FLASH

1. FEATURES

1.1. GENERAL

- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 16,777,216 x 1 bit structure or 8,388,608 x 2 bits (Dual Output mode) structure
- 512 Equal Sectors with 4K byte each
  - Any Sector can be erased individually
- 32 Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Program Capability
  - Byte base
  - Page base (256 bytes)
- Latch-up protected to 100mA from -1V to V_{CC} +1V
- **GPR25L162B is compatible with MX25L1606E**

1.2. Performance

- High Performance
  - Fast access time: 86MHz serial clock
  - Serial clock of Dual Output mode : 80MHz
  - Fast program time: 1.4ms(typ.) and 5ms(max.)/page
  - Byte program time: 9us (typical)
  - Fast erase time: 60ms(typ.) /sector ; 0.7s(typ.) /block
- Low Power Consumption
  - Low active read current: 25mA(max.) at 86MHz
  - Low active programming current: 20mA (max.)
  - Low active erase current: 20mA (max.)
  - Low standby current: 25uA (max.)
  - Deep power-down mode 5uA (typical)
- Typical 100,000 erase/program cycles
- 20 years of data retention

1.3. Software Features

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
  - The BP3-BP0 status bit defines the size of the area to be software protection against program and erase instructions
  - Additional 512 bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programmed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS commands for 1-byte manufacturer ID and 1-byte device ID

1.4. Hardware Features

- PACKAGE
  - 8-pin SOP (150mil)
  - 8-pin SOP (200mil)

2. GENERAL DESCRIPTION

The device feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in Dual Output read mode, the SI and SO pins become SIO0 and SIO1 pins for data output.

The device provides sequential read operation on whole chip.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page basis, or word basis for erase command is executes on sector, or block, or whole chip basis.

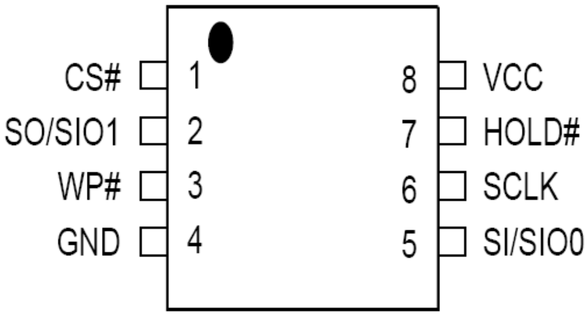
To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details. When the device is not in operation and CS# is high, it is put in standby mode.

The GPR25L162B reliably stores memory contents even after typical 100,000 program and erase cycles.

3. PIN CONFIGURATIONS

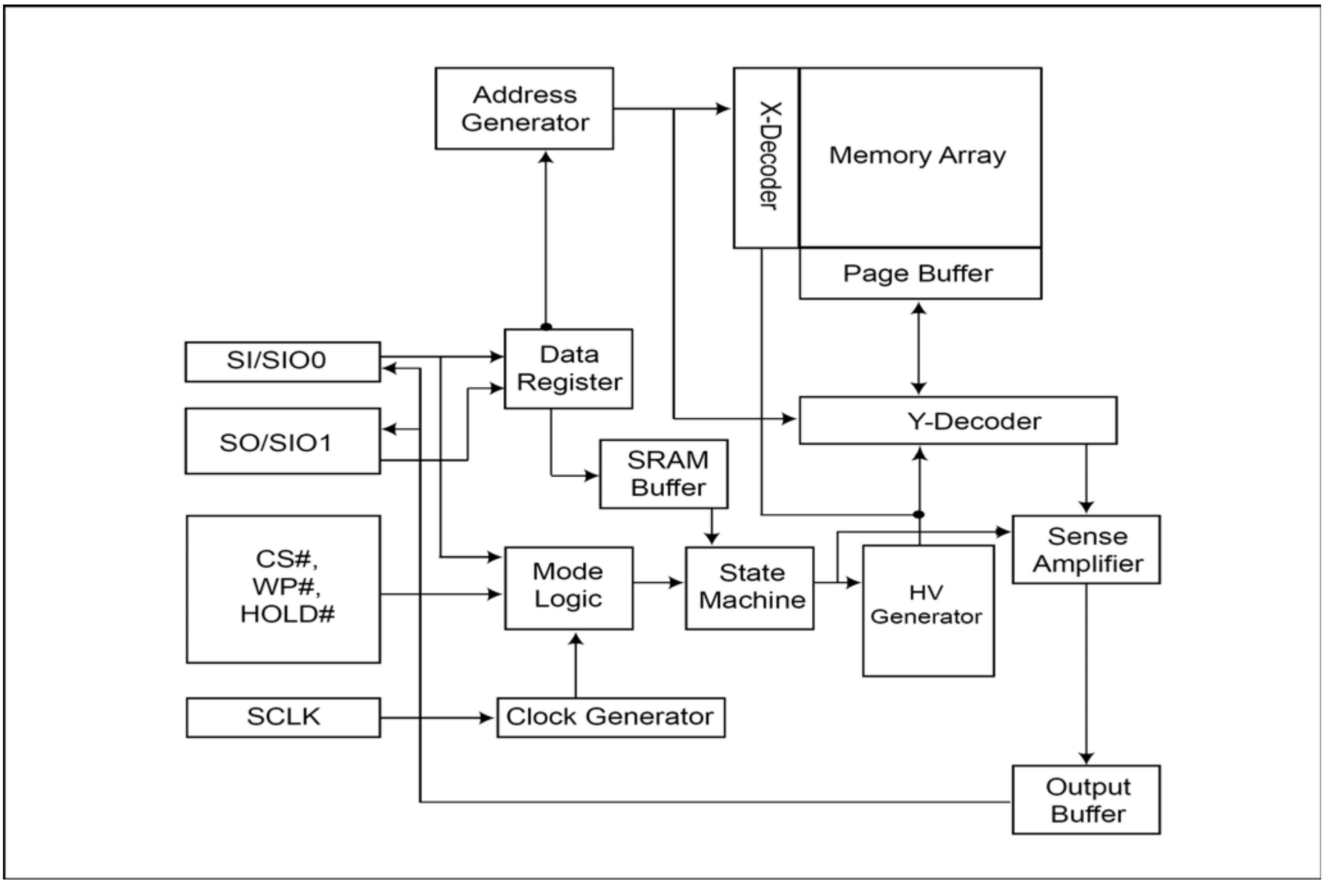
3.1. 8-PIN SOP (150mil, 200mil)



4. PIN DESCRIPTION

Symbol	Description
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for Dual Output mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Output (for Dual Output mode)
SCLK	Clock Input
WP#	Write protection
HOLD#	Hold, to pause the device without deselecting the device
VCC	+ 3.3V Power Supply
GND	Ground

5. BLOCK DIAGRAM



6. MEMORY ORGANIZATION

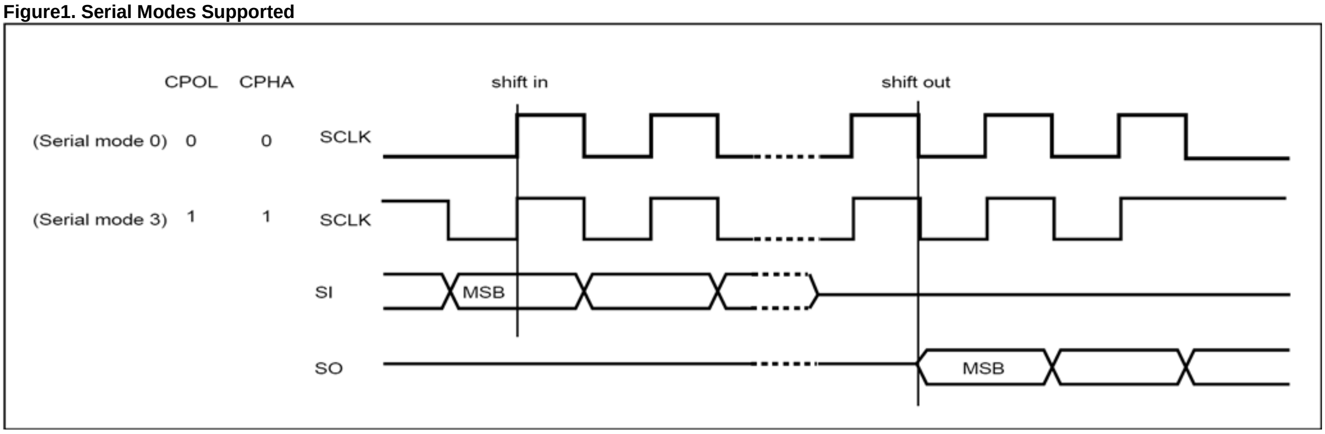
Table 1. Memory Organization

Block	Sector	Address Range	
31	511	1FF000h	1FFFFFh
	:	:	:
	496	1F0000h	1F0FFFh
30	495	1EF000h	1EFFFFh
	:	:	:
	480	1E0000h	1E0FFFh
: :	: :	: :	: :
0	15	00F000h	00FFFFh
	:	:	:
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

7. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z. The CS# falling time needs to follow tCHCL spec.
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown in Figure 1.
5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, DREAD, RES, and REMS the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, CE, PP, RDP, DP, ENSO, EXSO, and WRSCUR, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure1. Serial Modes Supported



Note:

CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

8. DATA PROTECTION

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the standby mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP) command completion
  - Sector Erase (SE) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES).
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM):

Use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of "Protected Area Sizes", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.

Please refer to table of "protected area sizes".

- The Hardware Protected Mode (HPM) uses WP# to protect the BP3-BP0 bits and SRWD bit.

Table2. Protected Area Sizes

Status bit				Protect Level
BP3	BP2	BP1	BP0	
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 31th)
0	0	1	0	2 (2blocks, block 30th-31th)
0	0	1	1	3 (4blocks, block 28th-31th)
0	1	0	0	4 (8blocks, block 24th-31th)
0	1	0	1	5 (16blocks, block 16th-31th)
0	1	1	0	6 (32blocks, all)
0	1	1	1	7 (32blocks, all)
1	0	0	0	8 (32blocks, all)
1	0	0	1	9 (32blocks, all)
1	0	1	0	10 (16blocks, block 0th-15th)
1	0	1	1	11 (24blocks, block 0th-23th)
1	1	0	0	12 (28blocks, block 0th-27th)
1	1	0	1	13 (30blocks, block 0th-29th)
1	1	1	0	14 (31blocks, block 0th-30th)
1	1	1	1	15 (32blocks, all)

II. Additional 512 bit secured OTP for unique identifier: to provide 512 bit one-time program area for setting device unique serial number - Which may be set by factory or system customer. Please refer to table 3. 512 bit secured OTP definition.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 512 bit secured OTP by entering 512 bit secured OTP mode (with ENSO command), and going

through normal program procedure, and then exiting 512 bit secured OTP mode by writing EXSO command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of "security register definition" for security register bit definition and table of "512 bit secured OTP definition" for address range definition.

Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 512 bit secured OTP mode, array access is not allowed.

Table3. 512 bit Secured OTP Definition

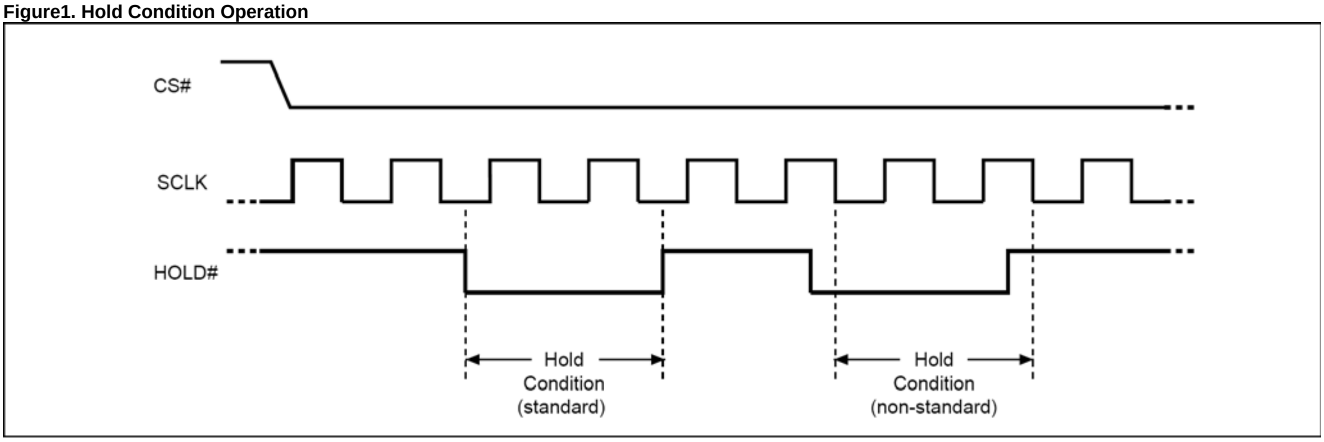
Address range	Size	Standard Factory Lock	Customer Lock
xxxx00~xxxx0F	128-bit	ESN (electrical serial number)	Determined by customer
xxxx10~xxxx3F	384-bit	N/A	

9. HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low), see Figure 2.

Figure1. Hold Condition Operation



The Serial Data Output (SO) is high impedance, both Serial Data Input (SI) and Serial Clock (SCLK) are don't care during the HOLD operation. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

10. COMMAND DESCRIPTION

Table4. Command Definition

Command (byte)	**WREN (write enable)**	**WRDI (write disable)**	**WRSR (write status register)**	**RDID (read identification)**	**RDSR (read status register)**	**READ (read data)**	**FAST READ (fast read data)**
1st byte	06 (hex)	04 (hex)	01 (hex)	9F (hex)	05 (hex)	03 (hex)	0B (hex)
2nd byte	-	-	-	-	-	AD1	AD1
3rd byte	-	-	-	-	-	AD2	AD2
4th byte	-	-	-	-	-	AD3	AD3
5th byte	-	-	-	-	-	-	Dummy
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to write new values to the status register	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out the values of the status register	n bytes read out until CS# goes high	n bytes read out until CS# goes high

Command (byte)	**RES (read electronic ID)**	**REMS (read electronic manufacturer & device ID)**	**DREAD (Double Output Mode command)**	**SE (sector erase)**	**BE (block erase)**	**CE (chip erase)**	**PP (page program)**
1st byte	AB (hex)	90 (hex)	3B (hex)	20 (hex)	52 or D8 (hex)	60 or C7 (hex)	02 (hex)
2nd byte	x	x	AD1	AD1	AD1		AD1
3rd byte	x	x	AD2	AD2	AD2		AD2
4th byte	x	ADD (Note 1)	AD3	AD3	AD3		AD3
5th byte			Dummy				
Action	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	n bytes read out by Dual Output until CS# goes high	to erase the selected sector	to erase the selected block	to erase whole chip	to program the selected page

Command (byte)	**RDSCUR (read security register)**	**WRSCUR (write security register)**	**ENSO (enter secured OTP)**	**EXSO (exit secured OTP)**	**DP (Deep power down)**	**RDP (Release from deep power down)**
1st byte	2B (hex)	2F (hex)	B1 (hex)	C1 (hex)	B9 (hex)	AB (hex)
2nd byte						
3rd byte						
4th byte						
5th byte						
Action	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	to enter the 512 bit secured OTP mode	to exit the 512 bit secured OTP mode	enters deep power down mode	release from deep power down mode

Note1: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

10.1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, SE, BE, CE, and WRSR, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.
The sequence is shown as Figure 11.

10.2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.
The sequence is shown as Figure 12.
The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion

10.3. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.
The sequence is shown as Figure 13.
The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and not affect value of WEL bit if it is applied to a protected memory area.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3-BP0) bits, non-volatile bits, indicate the protected area(as defined in table 2) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3-BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase(CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed).

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP# pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3-BP0) are read only.

Status Register for GPR25L162B

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	0	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	0	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	0	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note1: see the table "Protected Area Size".

10.4. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3-BP0) bits to define the protected area of memory (as shown in table 1). The WRSR also can set or reset the Status Register Write Disable

(SRWD) bit in accordance with Write Protection (WP#) pin signal. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence is shown as Figure 14.

The WRSR instruction has no effect on b6, b1, b0 of the status register.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 5. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP3-BP0 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP3-BP0 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:
1. As defined by the values in the Block Protect (BP3-BP0) bits of the Status Register, as shown in Table 1.
As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):
- When SRWD bit=0, no matter WP# is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3-BP0. The protected area, which is defined by BP3-BP0 is at software protected mode (SPM).
- When SRWD bit=1 and WP# is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3-BP0. The protected area, which is defined by BP3-BP0, is at software protected mode (SPM)

Note: If SRWD bit=1 but WP# is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):
- When SRWD bit=1, and then WP# is low (or WP# is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3-BP0 and hardware protected mode by the WP# to against data modification.

Note: to exit the hardware protected mode requires WP# driving high once the hardware protected mode is entered. If the WP# pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3-BP0.

10.5. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence is shown as Figure 15.

10.6. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence is shown as Figure 16.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

10.7. Dual Output Mode (DREAD)

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits(interleave on 1I/2O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the data out will perform as 2-bit instead of previous 1-bit.

The sequence is shown as Figure 17.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

The DREAD only perform read operation. Program/Erase /Read ID/Read status....operation do not support DREAD throughputs.

10.8. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see table 3) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence is shown as Figure 18.

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3-BP0 bits, the Sector Erase (SE) instruction will not be executed on the page.

10.9. Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte sector erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see table 3) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence is shown as Figure 19.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3-BP0 bits, the Block Erase (BE) instruction will not be executed on the page.

10.10. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). Any address of the sector (see table 3) is a valid address for Chip Erase (CE) instruction. The CS# must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence is shown as Figure 20.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP3-BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3-BP0 all set to "0".

10.11. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). If the eight least significant address bits (A7-A0) are not all 0, all transmitted data which goes beyond the end of the current page are programmed from the start address if the same page (from the address whose 8 least significant address bits (A7-A0) are all 0). The CS# must keep during the whole Page Program cycle. The CS# must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed. If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the request address of the page without effect on other address of the same page.

The sequence is shown as Figure 21.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3-BP0 bits, the Page Program (PP) instruction will not be executed.

10.12. Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence is shown as Figure 22.

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (those instructions allow the ID being reading out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

10.13. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in Table 9. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The sequence is shown in Figure 23 and Figure 24.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power Down Mode.

10.14. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Manufacturer ID and Device ID are listed as table of "ID Definitions".

The sequence is shown as Figure 25.

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

10.15. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 26. The Device ID values are listed in Table of ID Definitions. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Table6. ID Definitions

Command Type	GPR25L162B		
RDID Command	manufacturer ID	memory type	memory density
	C2	20	15
RES Command	electronic ID		
	14		
REMS	manufacturer ID	device ID	
	C2	14	

10.16. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 512 bit secured OTP mode. The additional 512 bit secured OTP is independent from main array, which may use to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

Please note that WRSR/WRSCUR commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

10.17. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 512 bit secured OTP mode.

10.18. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The definition of the Security Register bits is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex- factory or not. When it is "0", it indicates non- factory lock; "1" indicates factory- lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 512 bit Secured OTP area cannot be update any more. While it is in 512 bit secured OTP mode, array access is not allowed.

Table7. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	x	x	x	x	x	LDSO (indicate if lock-down)	Secured OTP indicator bit
reserved	reserved	reserved	reserved	reserved	reserved	0 = not lockdown 1 = lock-down (cannot program/erase OTP)	0 = non-factory lock 1 = factory lock
volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	non-volatile bit	non-volatile bit

10.19. Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. Unlike write status register, the WREN instruction is not required before sending WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 512 bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

11. POWER-ON STATE

The device is at below states when power-up:

- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:

- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the below time delay:

- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.

Please refer to the figure of "power-up timing".

Note:

To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended.(generally around 0.1uF)

11.1. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

12. ELECTRICAL SPECIFICATIONS

12.1. Absolute Maximum Ratings

Rating		Value
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-55°C to 125°C
Applied Input Voltage		-0.5V to 4.6V
Applied Output Voltage		-0.5V to 4.6V
VCC to Ground Potential		-0.5V to 4.6V

Notice:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot V_{SS} to -2.0V and V_{CC} to +2.0V for periods up to 20ns, see Figure 3 and 4.

Figure 3.Maximum Negative Overshoot Waveform

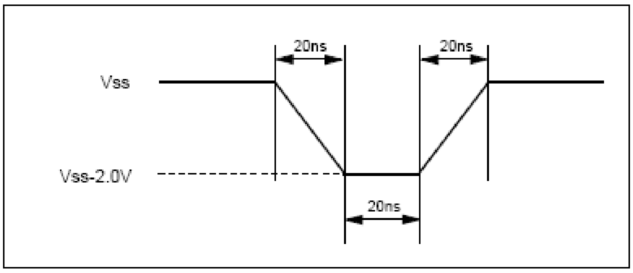
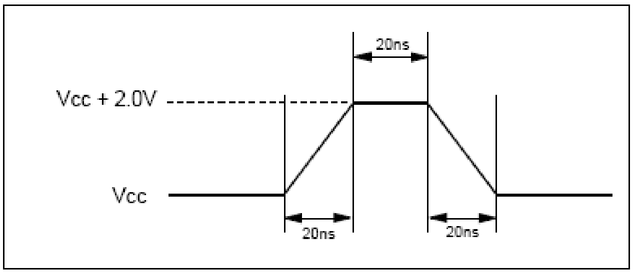


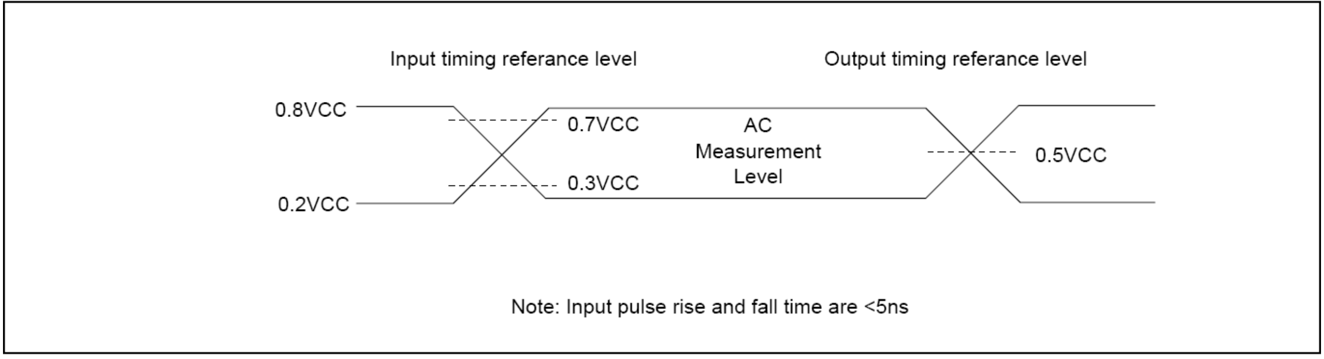
Figure 4. Maximum Positive Overshoot Waveform



12.2. Capacitance TA = 25°C, f = 1.0 MHz

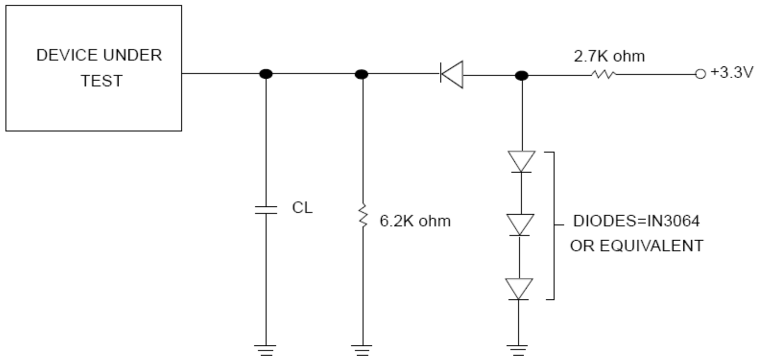
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance	-	-	6	pF	VIN = 0V
COUT	Output Capacitance	-	-	8	pF	VOUT = 0V

Figure5. Input Test Waveforms and Measurement Level



Note: Input pulse rise and fall time are <5ns

Figure6. Output Loading



CL=30pF/15pF Including jig capacitance

12.3. DC Characteristics

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1	-	-	± 2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1	-	-	± 2	uA	VCC = VCC Max, VIN = VCC or GND
ISB1	VCC Standby Current	1	-	-	25	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current	-	-	5	20	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1	-	-	25	mA	f=86MHz fT=80MHz (2 x I/O read)SCLK=0.1VCC/0.9VCC, SO=Open
		1	-	-	20	mA	f=66MHz, SCLK=0.1VCC/0.9VCC, SO=Open
		1	-	-	10	mA	f=33MHz, SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1	-	-	20	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current	1	-	-	20	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1	-	-	20	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1	-	-	20	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage	-	-0.5	-	0.3VCC	V	
VIH	Input High Voltage	-	0.7VCC	-	VCC+0.4	V	
VOL	Output Low Voltage	-	-	-	0.4	V	IOL = 1.6mA
VOH	Output High Voltage	-	VCC-0.2	-	-	V	IOH = -100uA

Notes:

1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Not 100% tested.

12.4. AC Characteristics

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, CE, DP, RES, RDP, WREN, WRDI, RDID, RDSR, WRSR		DC	-	86	MHz
fRSCLK	fR	Clock Frequency for READ instructions		DC	-	33	MHz
fTSCLK	fT	Clock Frequency for DREAD instructions		DC	-	80	MHz
tCH(1)	tCLH	Clock High Time	fC=86MHz	5.5	-	-	ns
			fR=33MHz	13	-	-	ns
tCL(1)	tCLL	Clock Low Time	fC=86MHz	5.5	-	-	ns
			fR=33MHz	13	-	-	ns
tCLCH(2)		Clock Rise Time (3) (peak to peak)		0.1	-	-	V/ns

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
tCHCL(2)		Clock Fall Time (3) (peak to peak)		0.1	-	-	V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		5	-	-	ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		5	-	-	ns
tDVCH	tDSU	Data In Setup Time		2	-	-	ns
tCHDX	tDH	Data In Hold Time		5	-	-	ns
tCHSH		CS# Active Hold Time (relative to SCLK)		5	-	-	ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		5	-	-	ns
tSHSL	tCSH	CS# Deselect Time	Read	15	-	-	ns
			Write	40	-	-	ns
tSHQZ(2)	tDIS	Output Disable Time		-	-	6	ns
tCLQV	tV	Clock Low to Output Valid, Loading 30pF/15pF		-	-	8/6	ns
tCLQX	tHO	Output Hold Time		0	-	-	ns
tHLCH		HOLD# Setup Time (relative to SCLK)		5	-	-	ns
tCHHH		HOLD# Hold Time (relative to SCLK)		5	-	-	ns
tHHCH		HOLD Setup Time (relative to SCLK)		5	-	-	ns
tCHHL		HOLD Hold Time (relative to SCLK)		5	-	-	ns
tHHQX(2)	tLZ	HOLD to Output Low-Z		-	-	6	ns
tHLQZ(2)	tHZ	HOLD# to Output High-Z		-	-	6	ns
tWHSL(4)		Write Protect Setup Time		20	-	-	ns
tSHWL (4)		Write Protect Hold Time		100	-	-	ns
tDP(2)		CS# High to Deep Power-down Mode		-	-	10	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read		-	-	8.8	us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read		-	-	8.8	us
tW		Write Status Register Cycle Time		-	5	40	ms
tBP		Byte-Program		-	9	300	us
tPP		Page Program Cycle Time		-	1.4	5	ms
tSE		Sector Erase Cycle Time		-	60	300	ms
tBE		Block Erase Cycle Time		-	0.7	2	s
tCE		Chip Erase Cycle Time		-	14	30	s

Notes:

1. tCH + tCL must be greater than or equal to 1/ fC. For Fast Read, tCL/tCH=5.5/5.5.
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
5. Test condition is shown as Figure 5.
6. The CS# rising time needs to follow tCHCL spec and CS# falling time needs to follow tCHCL spec.

12.5. Timing Analysis

Figure7. Serial Input Timing

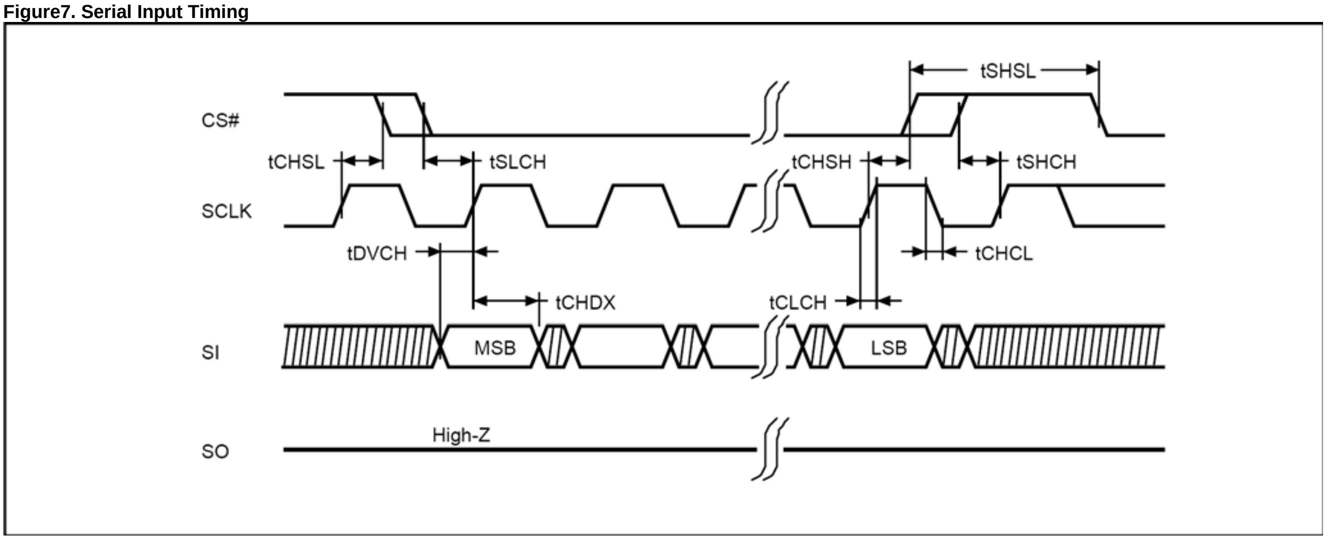


Figure8. Output Timing

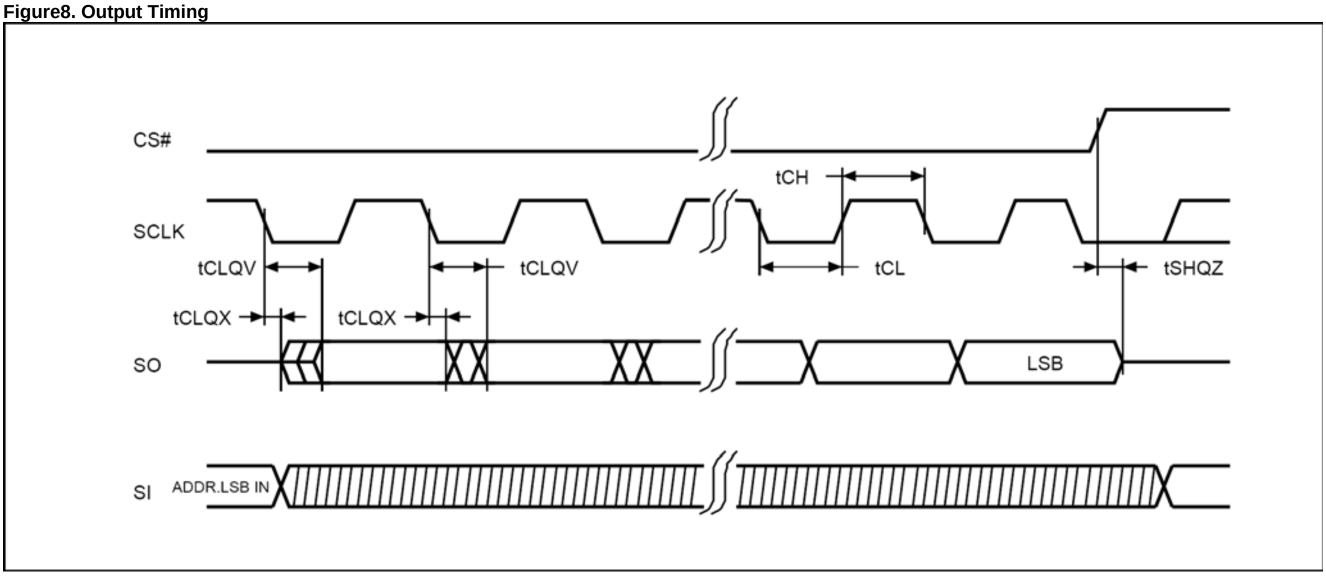
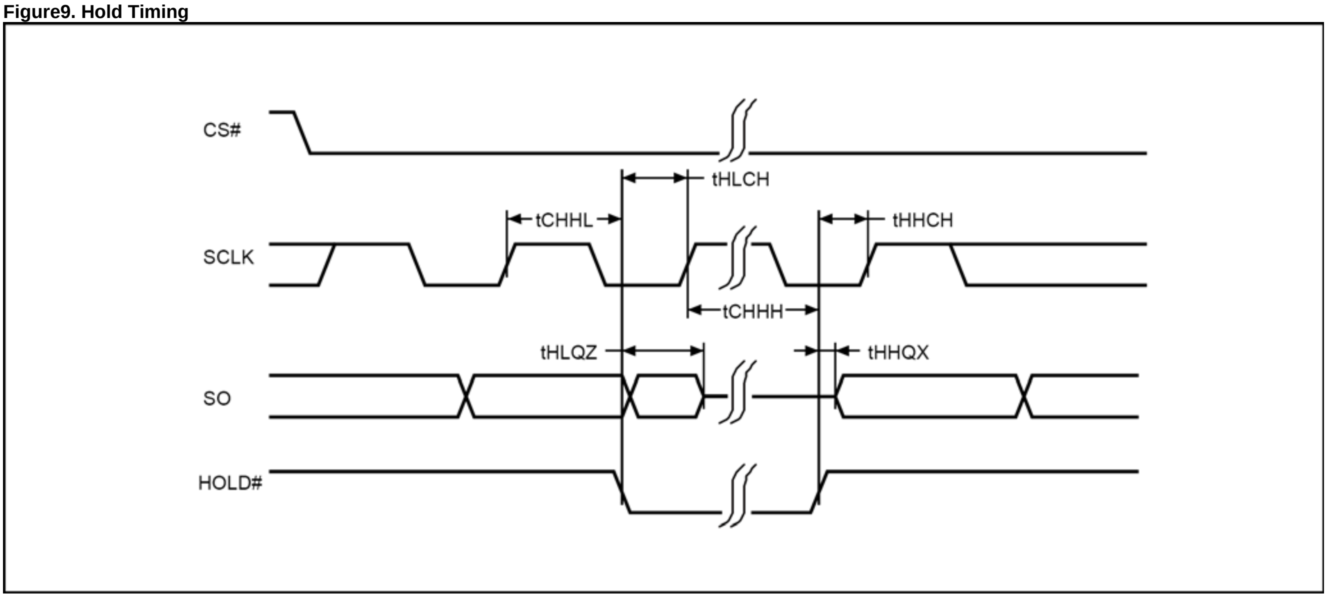


Figure9. Hold Timing



* SI is "don't care" during HOLD operation.

Figure10. WP# Disable Setup and Hold Timing during WRSR when SRWD=1

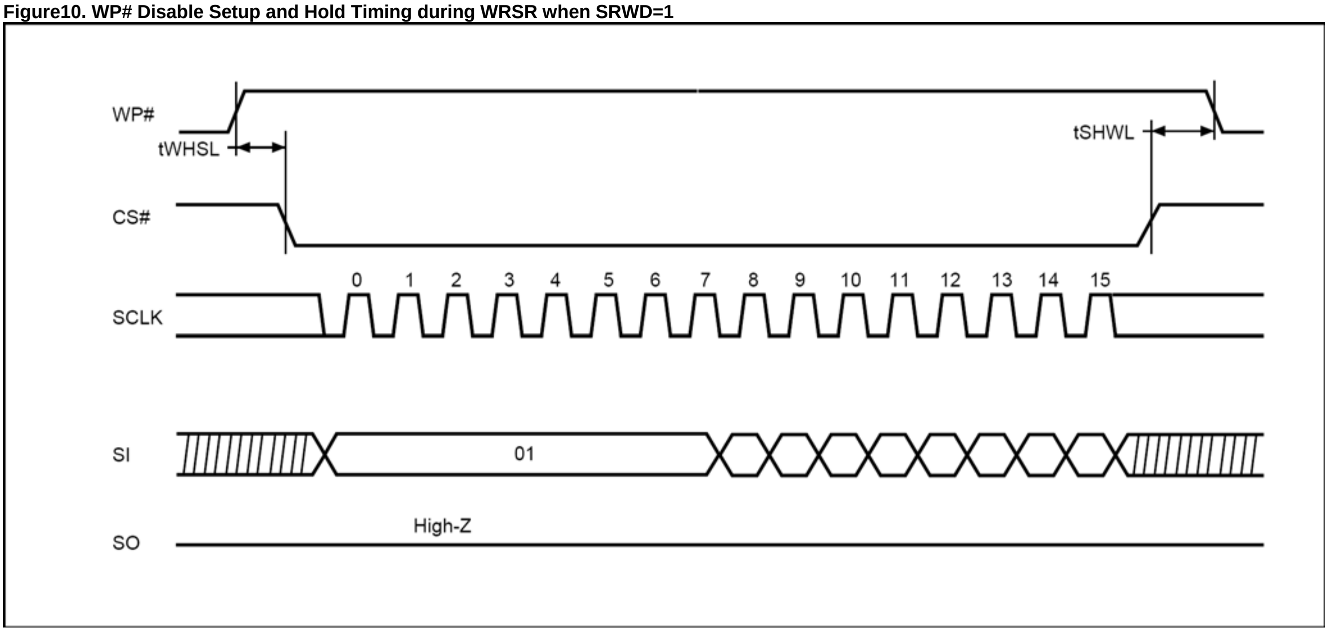


Figure11. Write Enable (WREN) Sequence (Command 06)

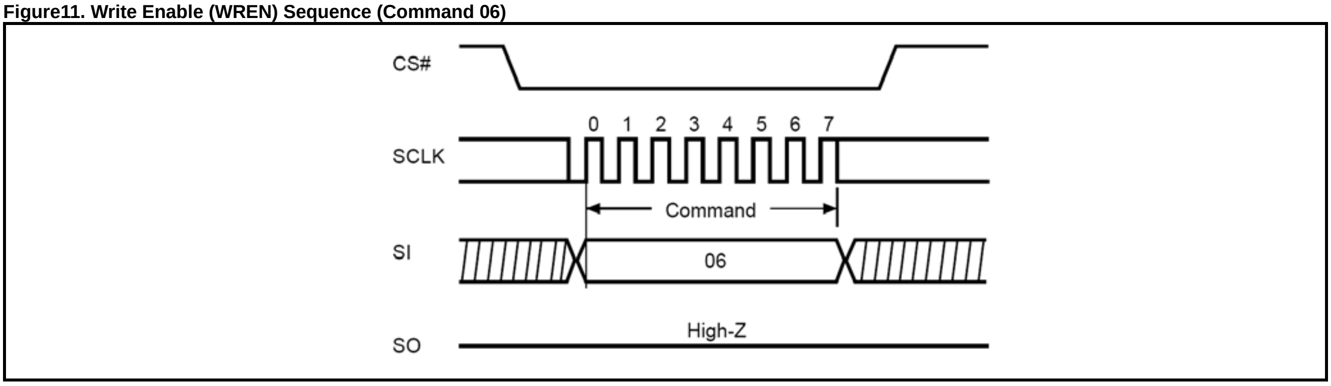


Figure12. Write Disable (WRDI) Sequence (Command 04)

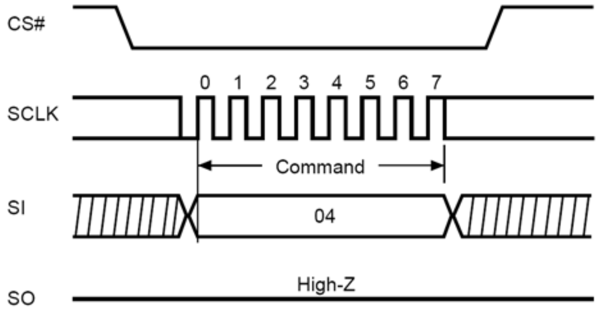


Figure13. Read Status Register (RDSR) Sequence (Command 05)

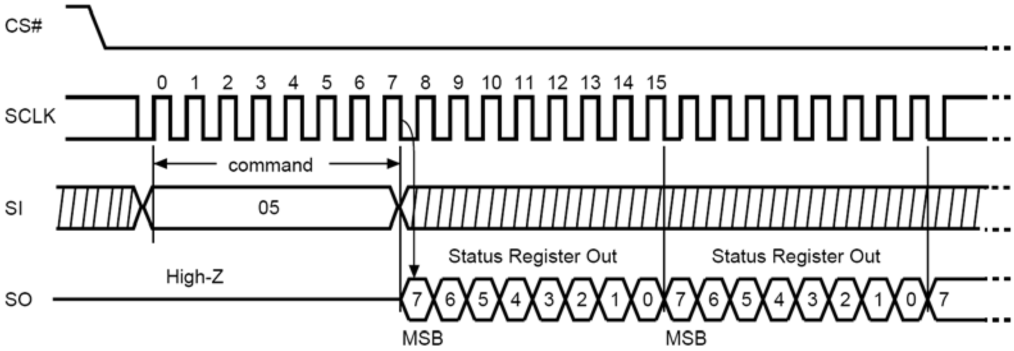


Figure14. Write Status Register (WRSR) Sequence (Command 01)

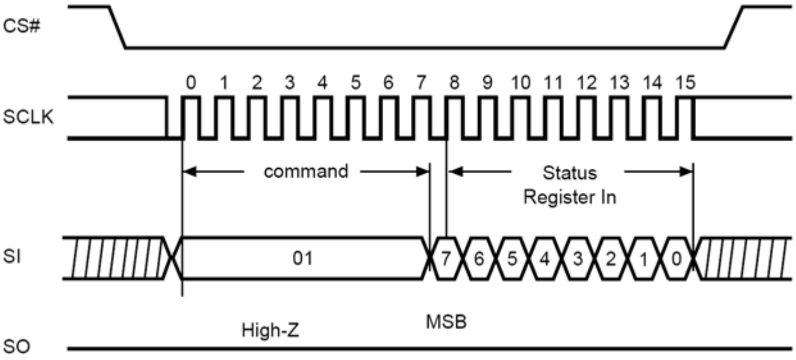


Figure15. Read Data Bytes (READ) Sequence (Command 03)

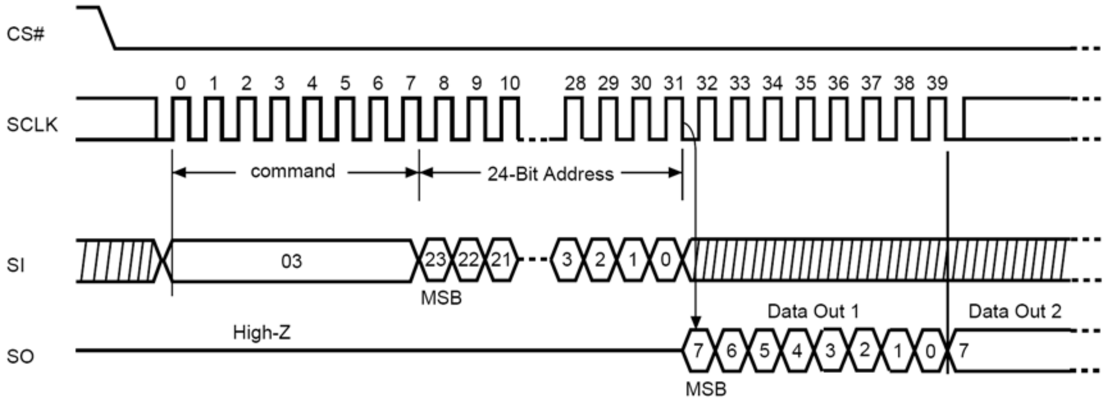


Figure16. Read at Higher Speed (FAST_READ) Sequence (Command 0B)

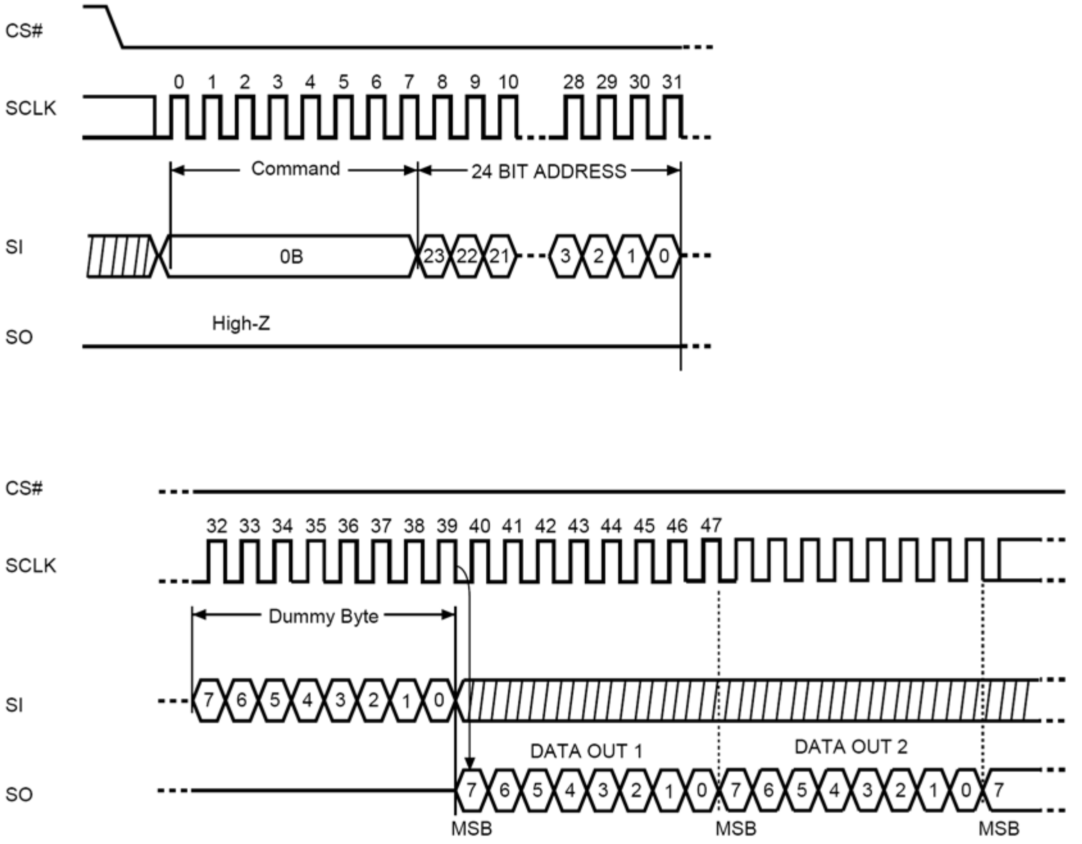


Figure17. Dual Output Read Mode Sequence (Command 3B)

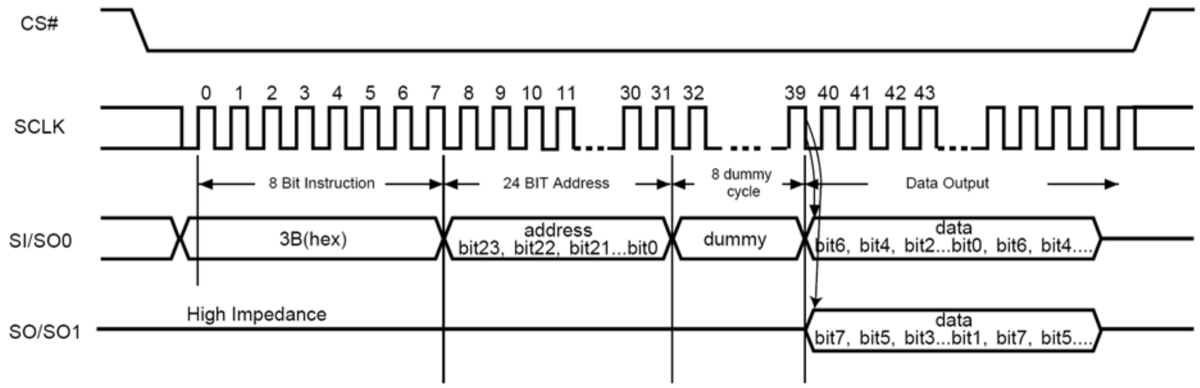
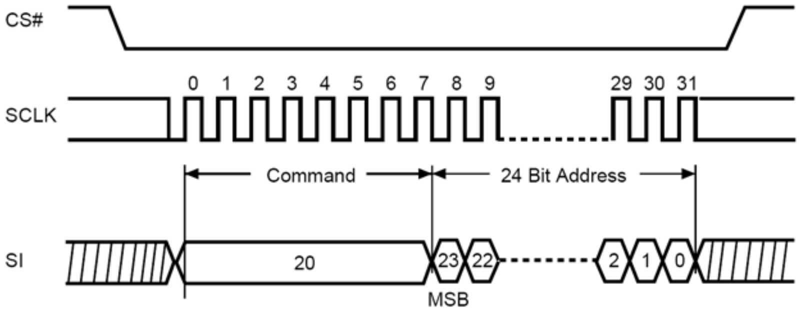
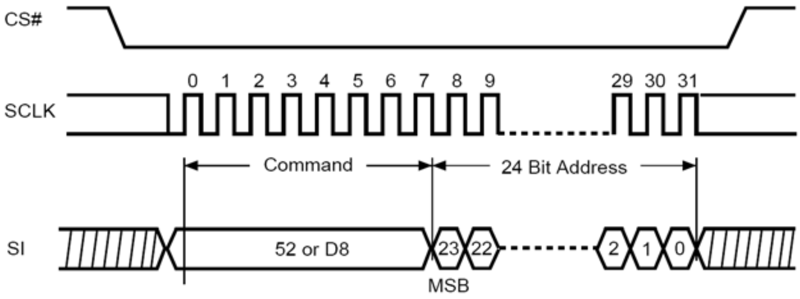


Figure18. Sector Erase (SE) Sequence (Command 20)



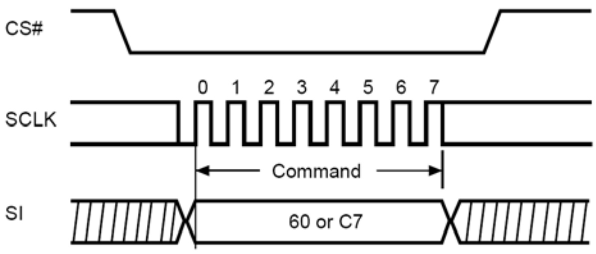
Note: SE command is 20(hex).

Figure19. Block Erase (BE) Sequence (Command 52 or D8)



Note: BE command is 52 or D8(hex).

Figure20. Chip Erase (CE) Sequence (Command 60 or C7)



Note: CE command is 60(hex) or C7(hex).

Figure21. Page Program (PP) Sequence (Command 02)

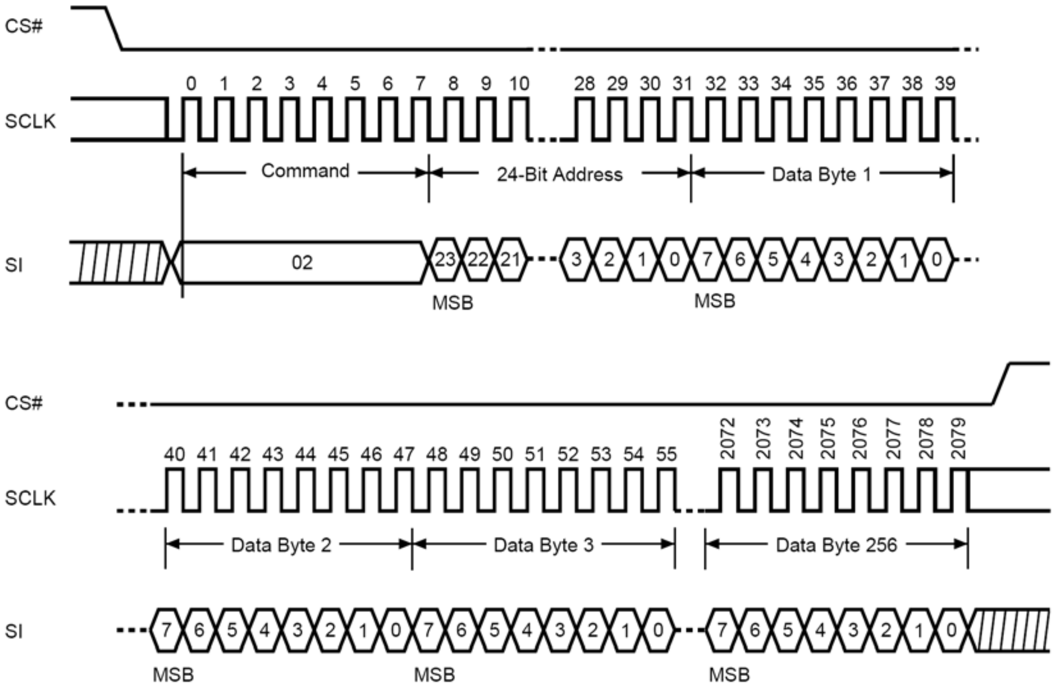


Figure22. Deep Power-down (DP) Sequence (Command B9)

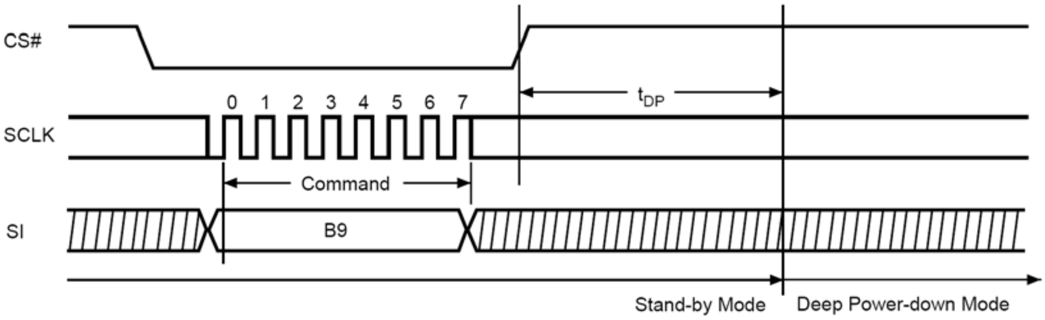


Figure23. Release from Deep Power-down (RDP) Sequence (Command AB)

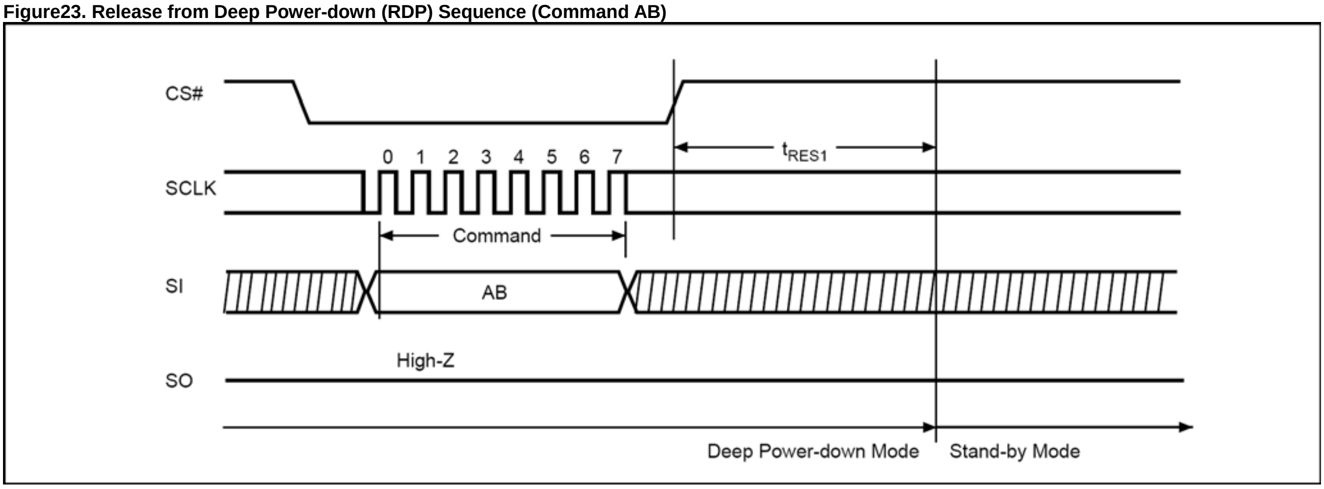


Figure24. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB)

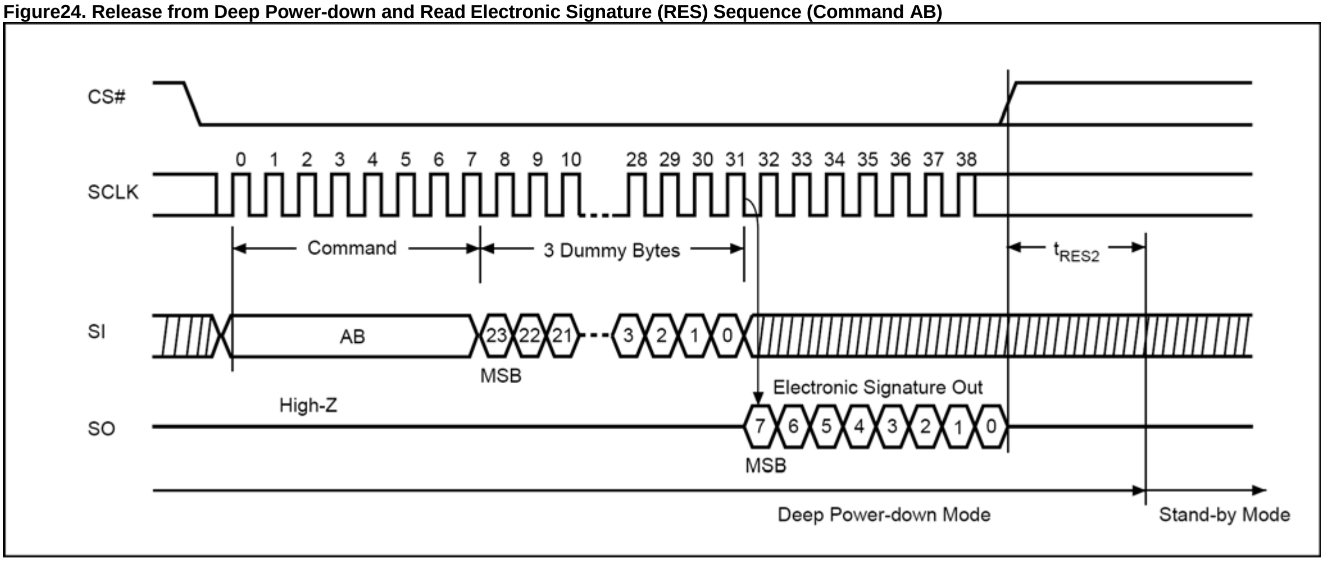


Figure25. Read Identification (RDID) Sequence (Command 9F)

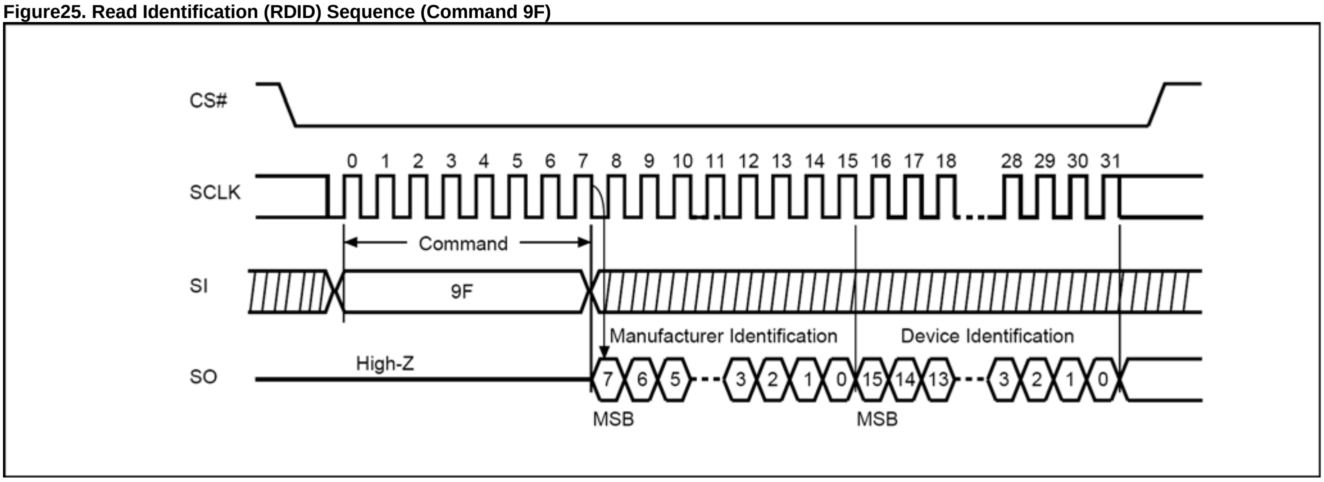
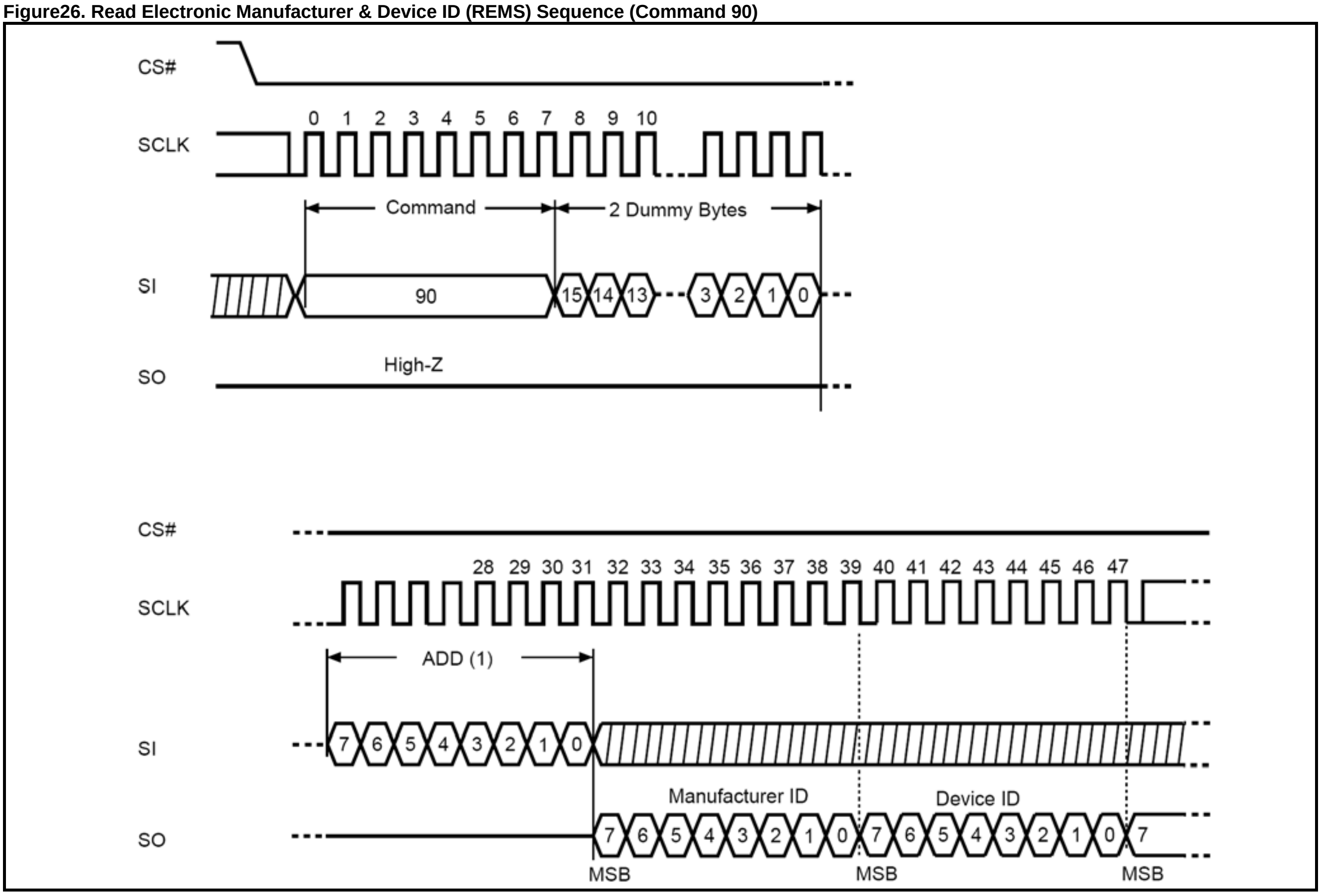


Figure26. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90)



Notes:

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first

(2) Instruction is either 90(hex).

Figure 27. Read Security Register (RDSCUR) Sequence (Command 2B)

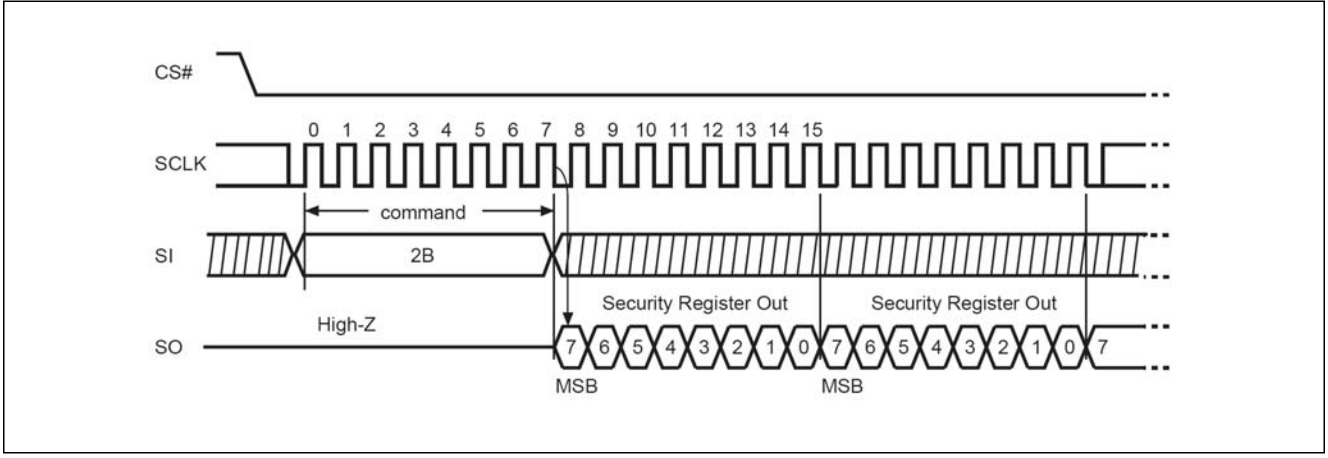


Figure 28. Write Security Register (WRSCUR) Sequence (Command 2F)

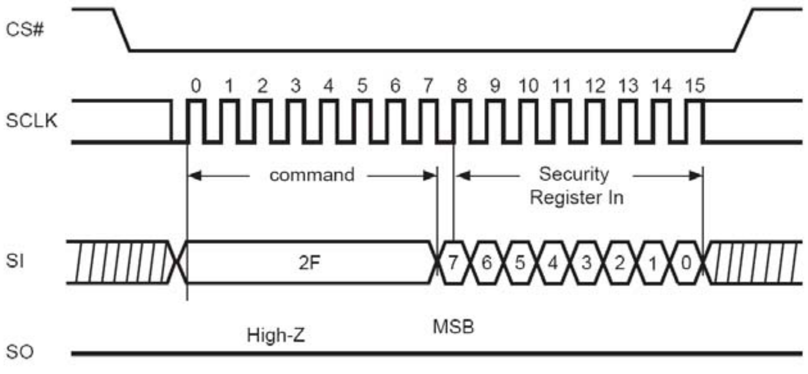
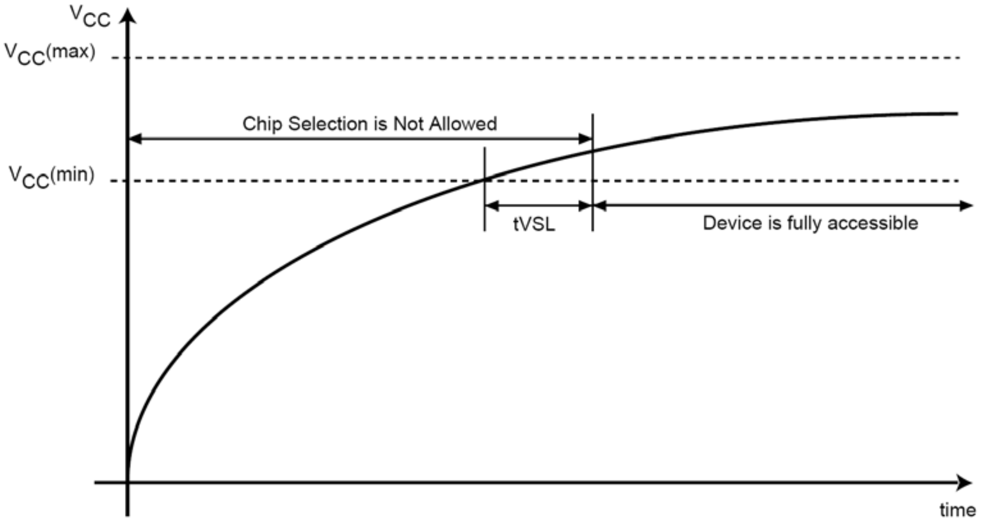


Figure29. Power-up Timing



Note: VCC (max.) is 3.6V and VCC (min.) is 2.7V.

Table10. Power-Up Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL(1)	VCC(min) to CS# low	200	-	us

Note: 1.The parameter is characterized only.

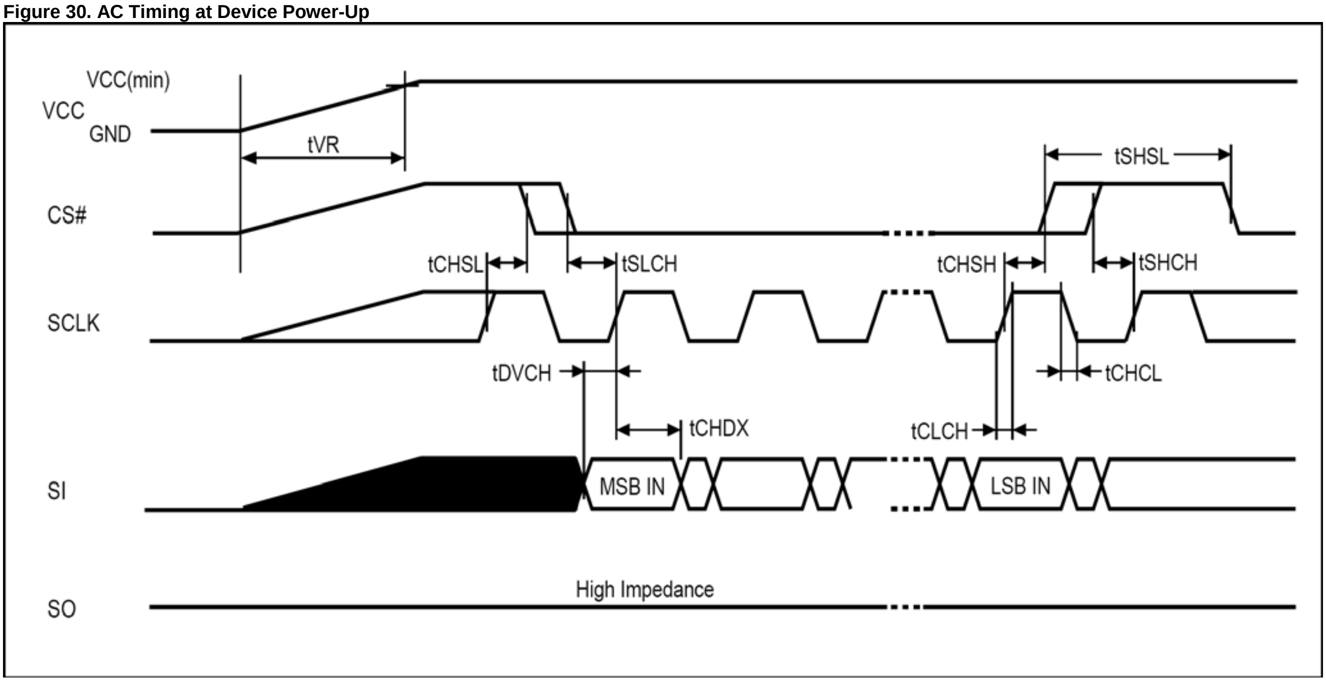
13. RECOMMENDED OPERATING CONDITIONS

13.1. At Device Power-Up and Power-down

AC timing illustrated in Figure 28 and Figure 29 are the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power down, CS# need to follow the voltage applied on VCC to keep the device not be selected. The CS# can be driven low when VCC reach V_{CC}(min.) and wait a period of tVSL.

Figure 30. AC Timing at Device Power-Up



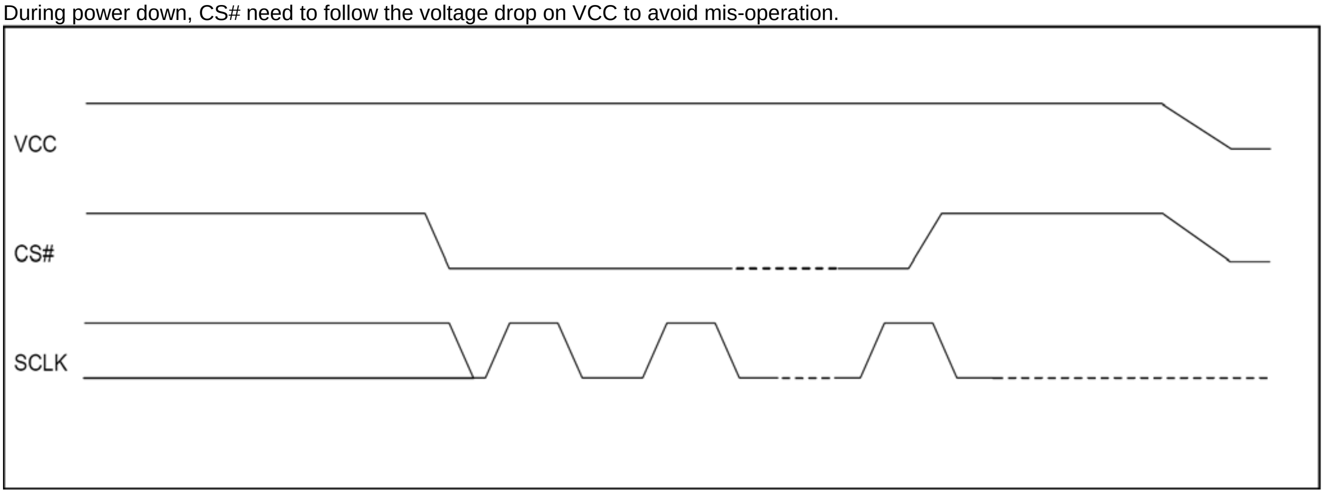
Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes:

1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "AC CHARACTERISTICS" table.

Figure 31. Power-Down Sequence

During power down, CS# need to follow the voltage drop on VCC to avoid mis-operation.



14. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Min.	Typ. (1)	Max. (2)	Unit
Write Status Register Time	-	5	40	ms
Sector Erase Time	-	60	300	ms
Block Erase Time	-	0.7	2	s
Chip Erase Time	-	14	30	s
Byte Program Time (via page program command)	-	9	300	us
Page Program Time	-	1.4	5	ms
Erase/Program Cycle	-	100,000	-	cycles

Note:

1. Typical program and erase time assumes the following conditions: 25℃, 3.3V, and checker board pattern.
2. Under worst conditions of 85℃ and 2.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. Erase/Program cycles comply with JEDEC JESD-47 & JESD22-A117A standard.

14.1. Data Retention

Parameter	Condition	Min.	Max.	UNIT
Data retention	55°C	20	-	years

15. LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

16. PACKAGE/PAD LOCATIONS

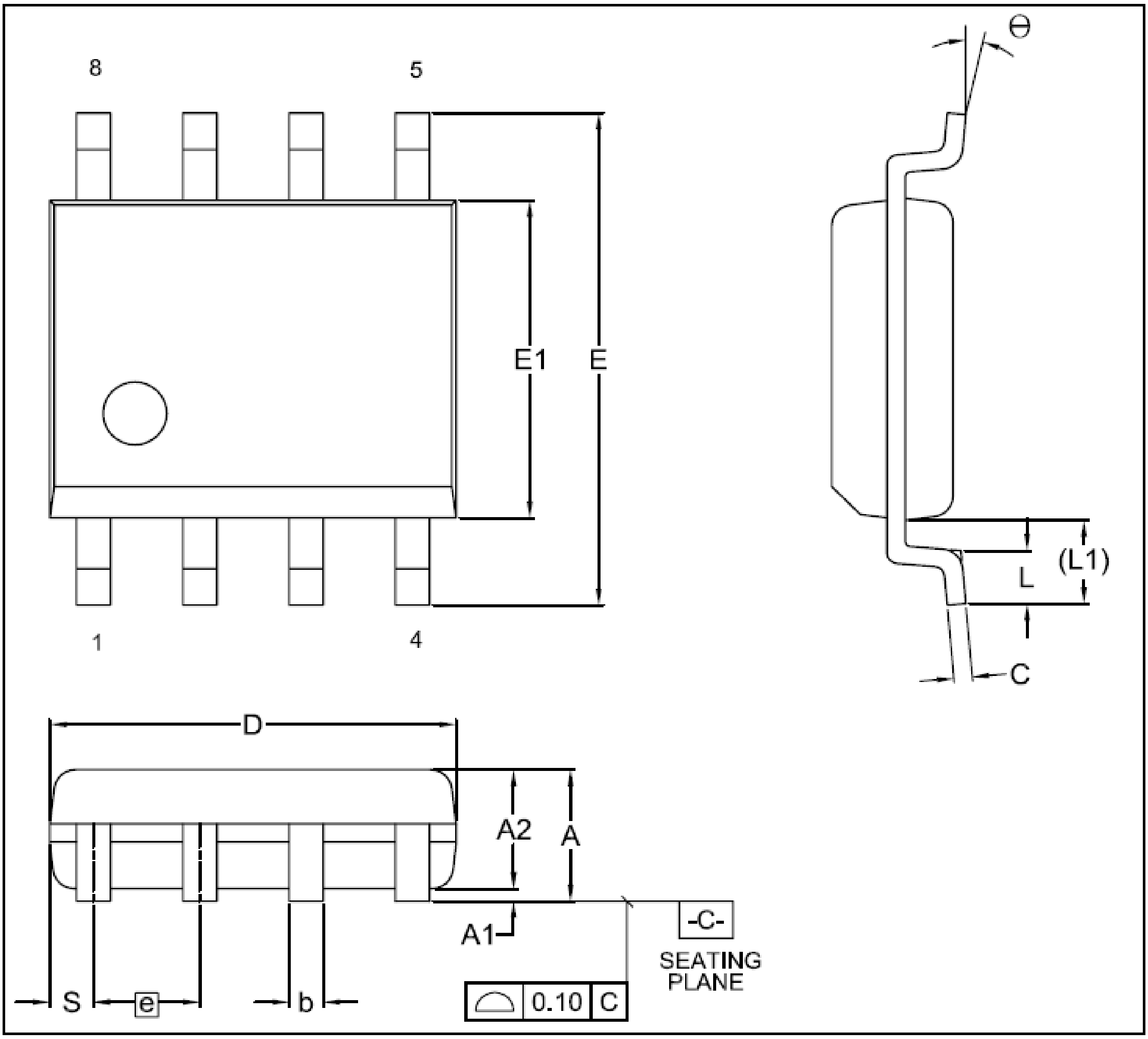
16.1. Ordering Information

Product Number	Package Type
GPR25L162B-QS01x	SOP 8L 150mil-Halogen Free Package
GPR25L162B-QS13x	SOP 8L 200mil-Halogen Free Package

Note: x = 1 - 9, serial number.

16.2. Package Information

16.2.1. Package Outline for SOP 8L (150MIL)

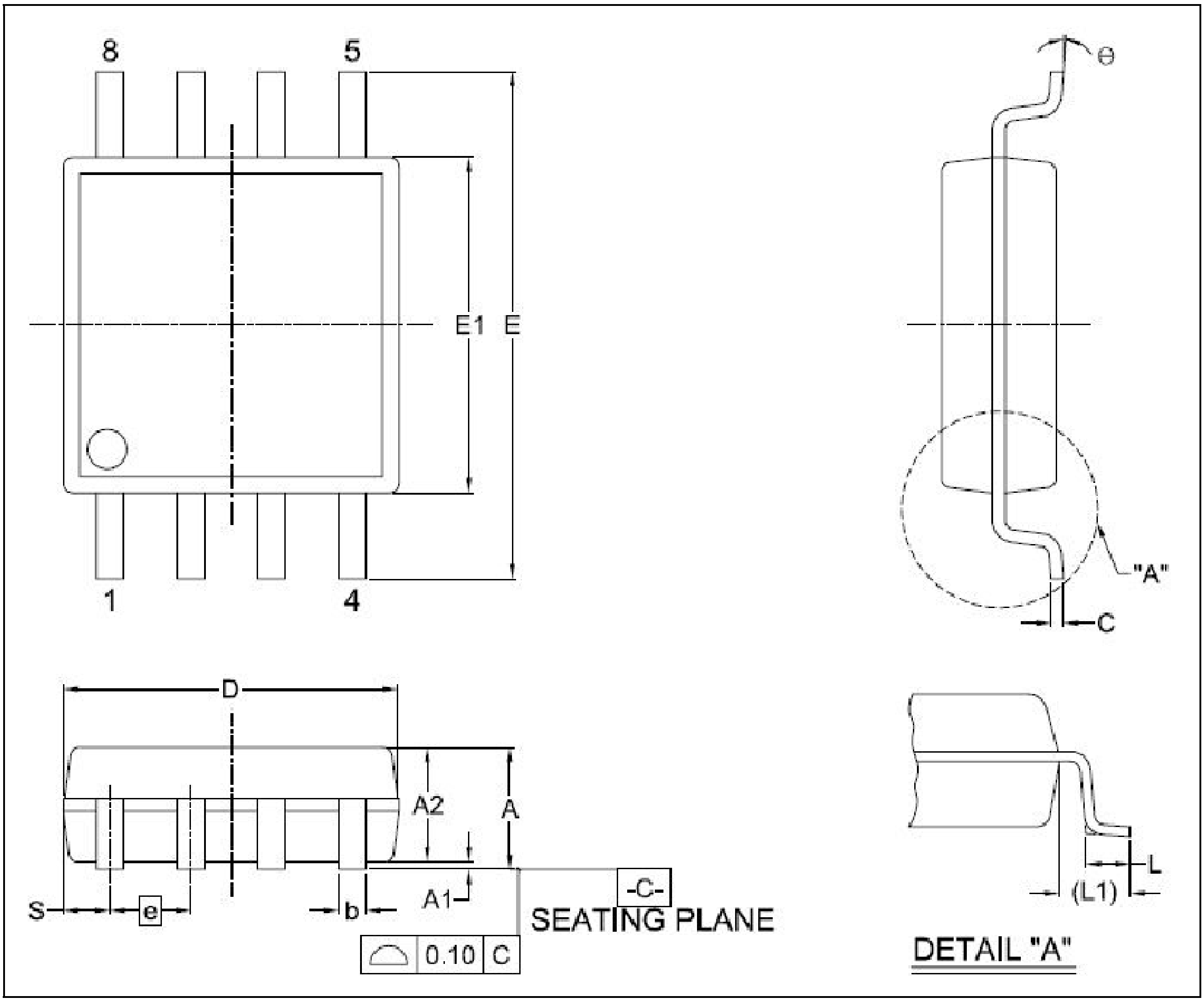


16.2.1.1. Dimensions (Inch dimensions are derived from the original mm dimensions)

Symbol Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
mm	**Min.**	-	0.10	1.35	0.36	0.15	4.77	5.80	3.80	-	0.46	0.85	0.41	0
	Nom.	-	0.15	1.45	0.41	0.20	4.90	5.99	3.90	1.27	0.66	1.05	0.54	5
	Max.	1.75	0.20	1.55	0.51	0.25	5.03	6.20	4.00	-	0.86	1.25	0.67	8
inch	**Min.**	-	0.004	0.053	0.014	0.006	0.188	0.228	0.150	-	0.018	0.033	0.016	0
	Nom.	-	0.006	0.057	0.016	0.008	0.193	0.236	0.154	0.050	0.026	0.041	0.021	5
	Max.	0.069	0.008	0.061	0.020	0.010	0.198	0.244	0.158	-	0.034	0.049	0.026	8

DWG. NO.	Revision	Reference		Issue Date
		JEDEC	EIAJ	
6110-1401	6	MS-012	-	11-26-03

16.2.2. Package Outline for SOP 8L (200MIL)



16.2.2.1. Dimensions (Inch dimensions are derived from the original mm dimensions)

Unit \ Symbol		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	-	0.05	1.70	0.36	0.19	5.13	7.70	5.18	-	0.50	1.21	0.62	0
	Nom.	-	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5
	Max.	2.16	0.20	1.91	0.51	0.25	5.33	8.10	5.38	-	0.80	1.41	0.88	8
inch	Min.	-	0.002	0.067	0.014	0.007	0.202	0.303	0.204	-	0.020	0.048	0.024	0
	Nom.	-	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5
	Max.	0.085	0.008	0.075	0.020	0.010	0.210	0.319	0.212	-	0.031	0.056	0.035	8

DWG. NO.	Revision	Reference		Issue Date
		JEDEC	EIAJ	
6110-1406	3			

17. DISCLAIMER

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18. REVISION HISTORY

Date	Revision	Description	Page
Apr. 09, 2014	1.4	Add 200mi; SOP8 information.	
Oct. 20, 2011	1.3	1. Added RDSCUR & WRSCUR diagram form. 2. Added CS# rising and falling time description. 3. Modified tW from 40(typ.)/100(max.) to 5(typ.)/40(max.).	30,31 8,22 22,32
Feb. 10, 2011	1.2	1. Changed ISB1(MAX.) from 50uA to 25uA. 2. Modified GENERAL DESCRIPTION. 3. Modified COMMAND DESCRIPTION. 4. Changed Min. of fC, fR, fT from 10KHz to DC. 5. Modified Figure 8,19,26,28. 6. Add Figure 29.	4,21 5 12~17 21 23,27,30,31 31
Dec. 14, 2010	1.1	Add writer compatible information in section 1.1	4
Mar. 22, 2010	1.0	Original	38