DATA SHEET

Generalplus

GPR323816A

4M x 16 bit Synchronous DRAM (SDRAM)

OCT. 08, 2008

Version 1.0

Table of Contents

PAGE

4M x 16 bit Synchronous DRAM (SDRAM)

1. GENERAL DESCRIPTION

The GPR323816A SDRAM is a high-speed CMOS synchronous DRAM containing 64 Mbits. It is internally configured as 4 Banks of 1M word x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command.

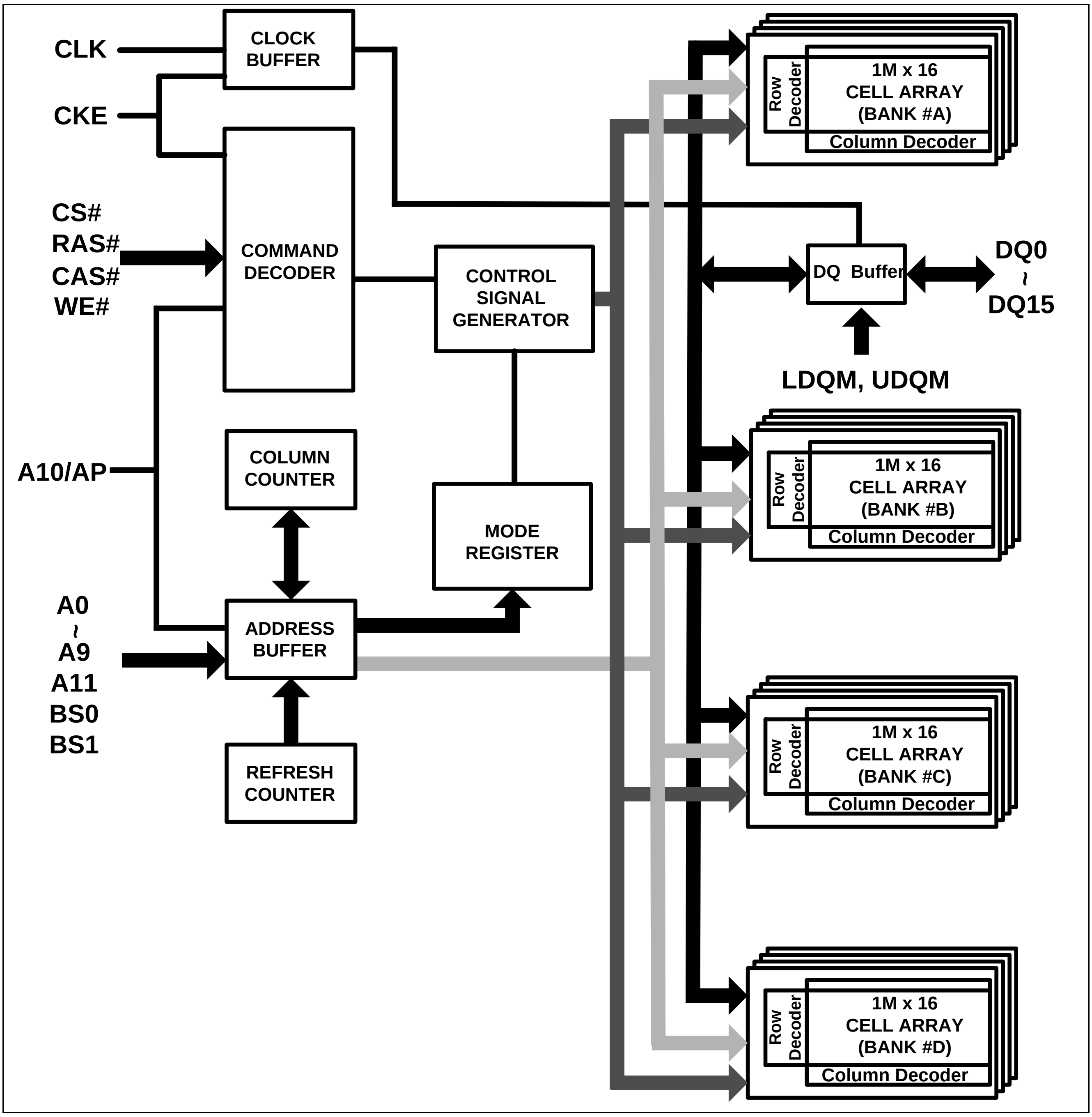
The GPR323816A provides for programmable Read or Write burst lengths of 1, 2, 4, 8, or full page, with a burst termination option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. By having a programmable mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth and particularly well suited to high performance PC applications.

2. FEATURES

- Fast access time from clock: 5 ns
- Fast clock rate: 166 MHz
- Fully synchronous operation
- Internal pipelined architecture
- 1M word x 16-bit x 4-bank
- Programmable Mode registers
  - CAS Latency: 2, or 3
  - Burst Length: 1, 2, 4, 8, or full page
  - Burst Type: interleaved or linear burst
  - Burst stop function
- Auto Refresh and Self Refresh
- 4096 refresh cycles/64ms
- CKE power down mode
- Single +3.3V ± 0.3V power supply
- Interface: LVTTL
- 54-pin 400 mil plastic TSOP II package
  - Pb free and Halogen free
- Key Specifications

GPR323816A		
tCK3	Clock Cycle time(min.)	6 ns
tAC3	Access time from CLK(max.)	5 ns
tRAS	Row Active time(min.)	42 ns
tRC	Row Cycle time(min.)	60 ns

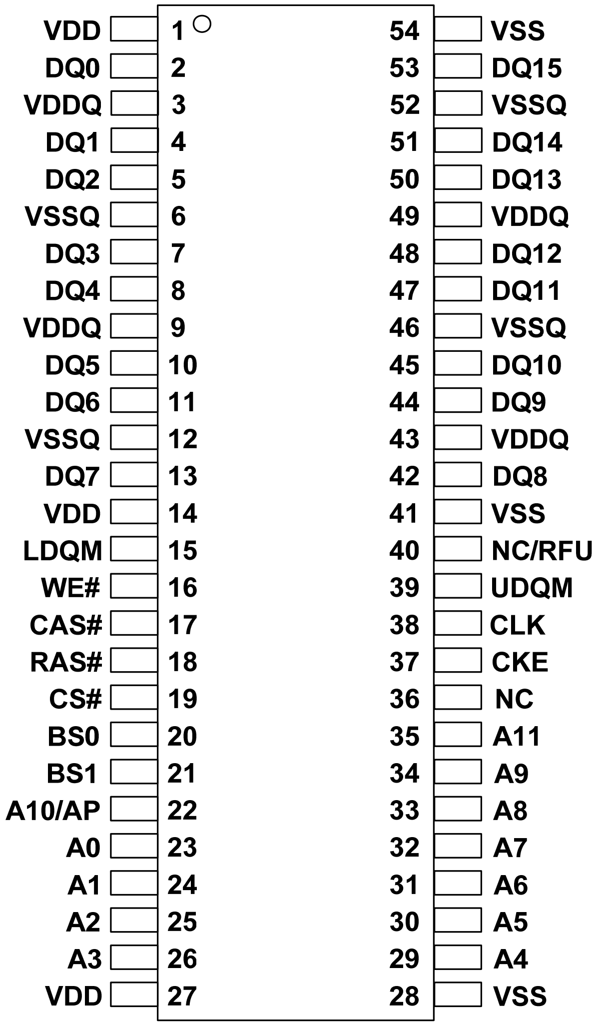
3. BLOCK DIAGRAM



4. PIN DESCRIPTIONS

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>CLK</td><td>Input</td><td>Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.</td></tr>
<tr><td>CKE</td><td>Input</td><td>Clock Enable: CKE activates(HIGH) and deactivates(LOW) the CLK signal. If CKE goes low synchronously with clock(set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes. CKE is synchronous except after the device enters Power Down and Self Refresh modes, where CKE becomes asynchronous until exiting the same mode. The input buffers, including CLK, are disabled during Power Down and Self Refresh modes, providing low standby power.</td></tr>
<tr><td>BS0,BS1</td><td>Input</td><td>Bank Activate: BS0, BS1 input select the bank for operation.
<table>
<tr><td>BS1</td><td>BS0</td><td>Select Bank</td></tr>
<tr><td>0</td><td>0</td><td>BANK #A</td></tr>
<tr><td>0</td><td>1</td><td>BANK #B</td></tr>
<tr><td>1</td><td>0</td><td>BANK #C</td></tr>
<tr><td>1</td><td>1</td><td>BANK #D</td></tr>
</table></td></tr>
<tr><td>A0-A11</td><td>Input</td><td>Address Inputs: A0-A11 are sampled during the BankActivate command (row address A0-A11) and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 1M available in the respective bank. During a Precharge command, A10 is sampled to determine if all banks are to be precharged (A10 = HIGH). The address inputs also provide the op-code during a Mode Register Set command.</td></tr>
<tr><td>CS#</td><td>Input</td><td>Chip Select: CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.</td></tr>
<tr><td>RAS#</td><td>Input</td><td>Row Address Strobe: The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the positive edges of CLK. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BS is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BS is switched to the idle state after the precharge operation.</td></tr>
<tr><td>CAS#</td><td>Input</td><td>Column Address Strobe: The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the positive edges of CLK. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS# "LOW." Then, the Read or Write command is selected by asserting WE# "LOW" or "HIGH."</td></tr>
<tr><td>WE#</td><td>Input</td><td>Write Enable: The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the positive edges of CLK. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.</td></tr>
<tr><td>LDQM, UDQM</td><td>Input</td><td>Data Input/Output Mask: Controls output buffers in read mode and masks Input data in write mode.</td></tr>
<tr><td>DQ0-DQ15</td><td>Input / Output</td><td>Data I/O: The DQ0-15 input and output data are synchronized with the positive edges of CLK. The I/Os are maskable during Reads and Writes.</td></tr>
<tr><td>NC/RFU</td><td>-</td><td>No Connect: These pins should be left unconnected.</td></tr>
<tr><td>VDDQ</td><td>Supply</td><td>DQ Power: Provide isolated power to DQs for improved noise immunity. (3.3V± 0.3V)</td></tr>
<tr><td>VSSQ</td><td>Supply</td><td>DQ Ground: Provide isolated ground to DQs for improved noise immunity. (0 V)</td></tr>
<tr><td>VDD</td><td>Supply</td><td>Power Supply: +3.3V ± 0.3V</td></tr>
<tr><td>VSS</td><td>Supply</td><td>Ground</td></tr>
</table>

4.1. Pin Assignment (TSOP II Top View)



5. OPERATION MODE

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 2 shows the truth table for the operation commands.

Table 2. Truth Table (Note (1), (2))

Command	State	CKEn-1	CKEn	DQM	BS0,1	A10	A0-9,11	CS#	RAS#	CAS#	WE#
BankActivate	Idle(3)	H	X	X	V	Row address		L	L	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	X	V	L	Column address (A0 ~ A7)	L	H	L	L
Write and AutoPrecharge	Active(3)	H	X	X	V	H		L	H	L	L
Read	Active(3)	H	X	X	V	L	Column address (A0 ~ A7)	L	H	L	H
Read and Autoprecharge	Active(3)	H	X	X	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	OP code			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (SelfRefresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Mode Entry	Any(5)	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (PowerDown)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Mask/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

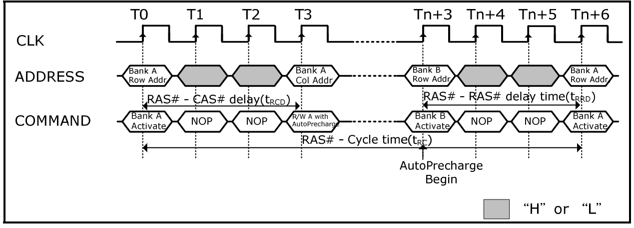
Note:

1. V=Valid X=Don't Care L=Low level H=High level
2. CKEn signal is input level when commands are provided.
   CKEn-1 signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BS signal.
4. Device state is 1, 2, 4, 8, and full page burst operation.
5. Power Down Mode can not enter in the burst operation.
   When this command is asserted in the burst cycle, device state is clock suspend mode.

6. COMMANDS

6.1. BankActivate (RAS# = "L", CAS# = "H", WE# = "H", BSs = Bank, A0-A11 = Row Address)

The BankActivate command activates the idle bank designated by the BS0, 1 signals. By latching the row address on A0 to A11 at the time of this command, the selected row access is initiated. The read or write operation in the same bank can occur after a time delay of tRCD(min.) from the time of bank activation. A subsequent BankActivate command to a different row in the same bank can only be issued after the previous active row has been precharged (refer to the following figure). The minimum time interval between successive BankActivate commands to the same bank is defined by tRC(min.). The SDRAM has four internal banks on the same chip and shares part of the internal circuitry to reduce chip area; therefore it restricts the back-to-back activation of the four banks. tRRD(min.) specifies the minimum time required between activating different banks. After this command is used, the Write command and the Block Write command perform the no mask write operation.



BankActivate Command Cycle (Burst Length = n, CAS# Latency = 3)

6.2. BankPrecharge Command(RAS# = "L", CAS# = "H", WE# = "L", BSs = Bank, A10 = "L", A0-A9 and A11 = Don't care)

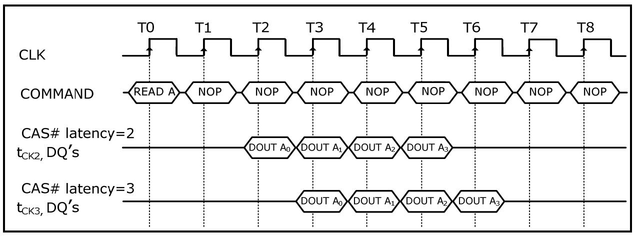
The BankPrecharge command precharges the bank disignated by BS signal. The precharged bank is switched from the active state to the idle state. This command can be asserted anytime after tRAS(min.) is satisfied from the BankActivate command in the desired bank. The maximum time any bank can be active is specified by tRAS(max.). Therefore, the precharge function must be performed in any active bank within tRAS(max.). At the end of precharge, the precharged bank is still in the idle state and is ready to be activated again.

6.3. PrechargeAll Command (RAS# = "L", CAS# = "H", WE# = "L", BSs = Don't care, A10 = "H", A0-A9 and A11 = Don't care)

The PrechargeAll command precharges all banks simultaneously and can be issued even if all banks are not in the active state. All banks are then switched to the idle state.

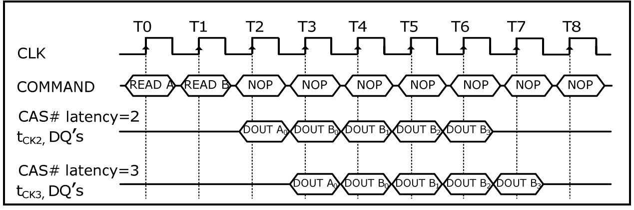
6.4. Read Command (RAS# = "H", CAS# = "L", WE# = "H", BSs = Bank, A10 = "L", A0-A7 = Column Address)

The Read command is used to read a burst of data on consecutive clock cycles from an active row in an active bank. The bank must be active for at least tRCD(min.) before the Read command is issued. During read bursts, the valid data-out element from the starting column address will be available following the CAS# latency after the issue of the Read command. Each subsequent data-out element will be valid by the next positive clock edge (refer to the following figure). The DQs go into high-impedance at the end of the burst unless other command is initiated. The burst length, burst sequence, and CAS# latency are determined by the mode register, which is already programmed. A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue.



Burst Read Operation(Burst Length = 4, CAS# Latency = 2, 3)

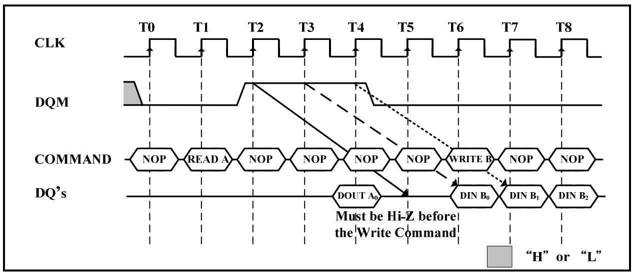
The read data appears on the DQs subject to the values on the DQM inputs two clocks earlier (i.e. DQM latency is two clocks for output buffers). A read burst without the auto precharge function may be interrupted by a subsequent Read or Write command to the same bank or the other active bank before the end of the burst length. It may be interrupted by a BankPrecharge/ PrechargeAll command to the same bank too. The interrupt coming from the Read command can occur on any clock cycle following a previous Read command (refer to the following figure).



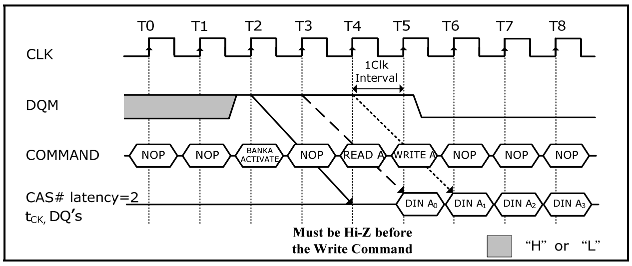
Read Interrupted by a Read (Burst Length = 4, CAS# Latency = 2, 3)

The DQM inputs are used to avoid I/O contention on the DQ pins when the interrupt comes from a Write command. The DQMs must be asserted (HIGH) at least two clocks prior to the Write command to suppress data-out on the DQ pins. To guarantee the DQ pins against I/O contention, a single cycle with high-impedance on the DQ pins must occur between the last read data and the Write command (refer to the following three figures).

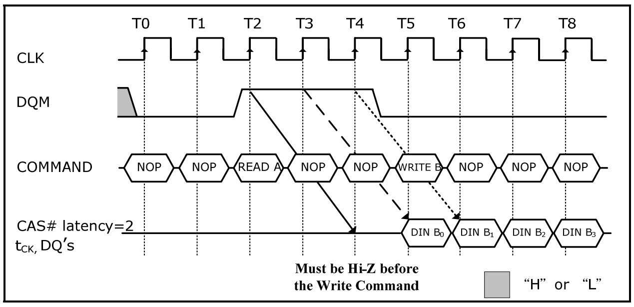
If the data output of the burst read occurs at the second clock of the burst write, the DQMs must be asserted (HIGH) at least one clock prior to the Write command to avoid internal bus contention.



Read to Write Interval (Burst Length ≥ 4, CAS# Latency = 3)

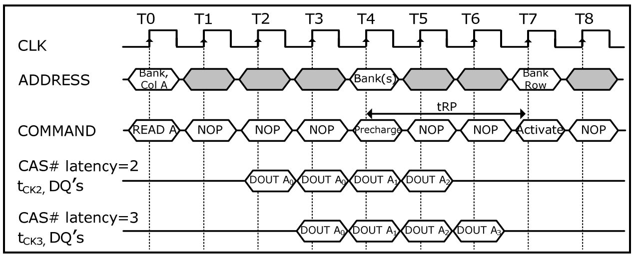


Read to Write Interval (Burst Length ≥ 4, CAS# Latency = 2)



Read to Write Interval (Burst Length ≥ 4, CAS# Latency = 2)

A read burst without the auto precharge function may be interrupted by a BankPrecharge/ PrechargeAll command to the same bank. The following figure shows the optimum time that BankPrecharge/ PrechargeAll command is issued in different CAS latency.



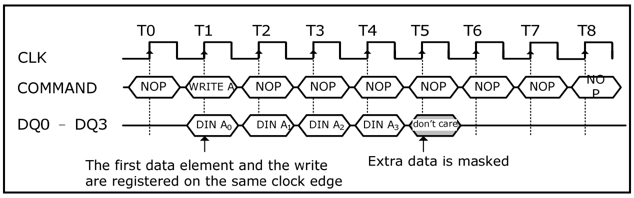
Read to Precharge (CAS# Latency = 2, 3)

6.5. Read and AutoPrecharge Command (RAS# = "H", CAS# = "L", WE# = "H", BSs = Bank, A10 = "H", A0-A7 = Column Address)

The Read and AutoPrecharge command automatically performs the precharge operation after the read operation. Once this command is given, any subsequent command cannot occur within a time delay of {tRP(min.) + burst length}. At full-page burst, only the read operation is performed in this command and the auto precharge function is ignored.

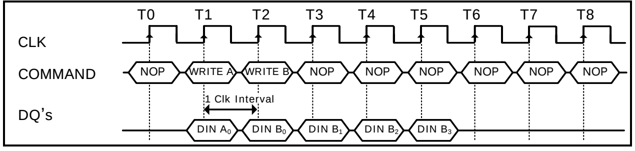
6.6. 6 Write Command(RAS# = "H", CAS# = "L", WE# = "L", BSs = Bank, A10 = "L", A0-A7 = Column Address)

The Write command is used to write a burst of data on consecutive clock cycles from an active row in an active bank. The bank must be active for at least tRCD(min.) before the Write command is issued. During write bursts, the first valid data-in element will be registered coincident with the Write command. Subsequent data elements will be registered on each successive positive clock edge (refer to the following figure). The DQs remain with high-impedance at the end of the burst unless another command is initiated. The burst length and burst sequence are determined by the mode register, which is already programmed. A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).



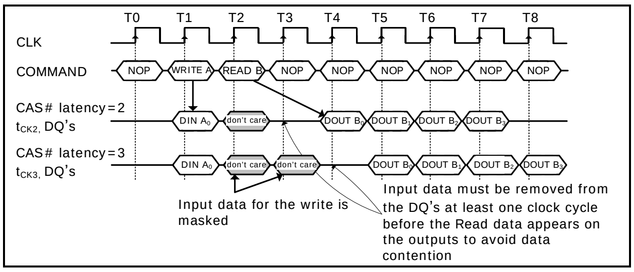
Burst Write Operation (Burst Length = 4)

A write burst without the auto precharge function may be interrupted by a subsequent Write, BankPrecharge/PrechargeAll, or Read command before the end of the burst length. An interrupt coming from Write command can occur on any clock cycle following the previous Write command (refer to the following figure).



Write Interrupted by a Write (Burst Length = 4)

The Read command that interrupts a write burst without auto precharge function should be issued one cycle after the clock edge in which the last data-in element is registered. In order to avoid data contention, input data must be removed from the DQs at least one clock cycle before the first read data appears on the outputs (refer to the following figure). Once the Read command is registered, the data inputs will be ignored and writes will not be executed.

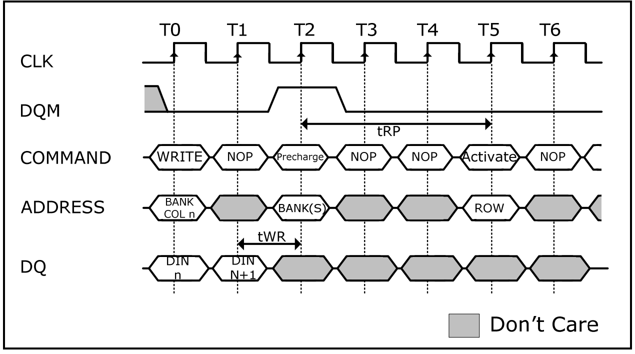


Input data for the write is masked

Input data must be removed from the DQ's at least one clock cycle before the Read data appears on the outputs to avoid data contention

Write Interrupted by a Read (Burst Length = 4, CAS# Latency = 2, 3)

The BankPrecharge/PrechargeAll command that interrupts a write burst without the auto precharge function should be issued *m* cycles after the clock edge in which the last data-in element is registered, where *m* equals tWR/tCK rounded up to the next whole number. In addition, the DQM signals must be used to mask input data, starting with the clock edge following the last data-in element and ending with the clock edge on which the BankPrecharge/PrechargeAll command is entered (refer to the following figure).

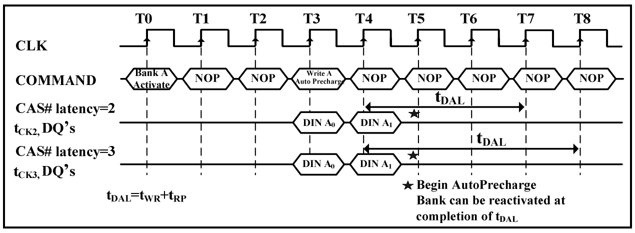


Note: The DQMs can remain low in this example if the length of the write burst is 1 or 2.

Write to Precharge

6.7. Write and AutoPrecharge Command (RAS# = "H", CAS# = "L", WE# = "L", BSs = Bank, A10 = "H", A0-A7 = Column Address)

The Write and AutoPrecharge command performs the precharge operation automatically after the write operation. Once this command is given, any subsequent command can not occur within a time delay of {(burst length -1) + tWR + tRP(min.)}. At full-page burst, only the write operation is performed in this command and the auto precharge function is ignored.



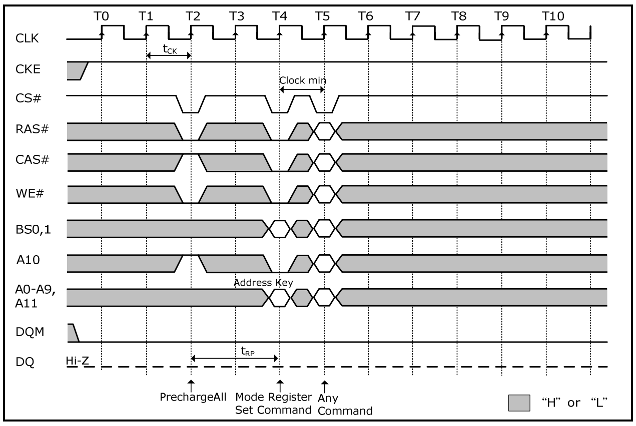
$t_{DAL}=t_{WR}+t_{RP}$

★ Begin AutoPrecharge
Bank can be reactivated at completion of t_{DAL}

Burst Write with Auto-Precharge (Burst Length = 2, CAS# Latency = 2, 3)

6.8. Mode Register Set Command (RAS# = "L", CAS# = "L", WE# = "L", A0-A11 = Register Data)

The mode register stores the data for controlling the various operating modes of SDRAM. The Mode Register Set command programs the values of CAS# latency, Addressing Mode and Burst Length in the Mode register to make SDRAM useful for a variety of different applications. The default values of the Mode Register after power-up are undefined; therefore this command must be issued at the power-up sequence. The state of pins A0~A9 and A11 in the same cycle is the data written to the mode register. One clock cycle is required to complete the write in the mode register (refer to the following figure). The contents of the mode register can be changed using the same command and the clock cycle requirements during operation as long as all banks are in the idle state.



Mode Register Set Cycle

The mode register is divided into various fields depending on functionality.

Function	Address
RFU*	BS0, 1
RFU*	A11, 10
WBL	A9
Test Mode	A8
	A7
CAS Latency	A6
	A5
	A4
BT	A3
Burst Length	A2
	A1
	A0

***Note:** RFU (Reserved for future use) should stay “0” during MRS cycle.

6.8.1. Burst Length Field (A2~A0)

This field specifies the data length of column access using the A2~A0 pins and selects the Burst Length to be 2, 4, 8, or full page.

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full Page

6.8.2. Burst Type Field (A3)

The Burst Type can be one of two modes, Interleave Mode or Sequential Mode.

A3	Burst Type
0	Sequential
1	Interleave

6.8.3. Burst Definition, Addressing Sequence of Sequential and Interleave Mode

Burst Length	Start Address			Sequential	Interleave
	A2	A1	A0		
2	X	X	0	0, 1	0, 1
	X	X	1	1, 0	1, 0
4	X	0	0	0, 1, 2, 3	0, 1, 2, 3
	X	0	1	1, 2, 3, 0	1, 0, 3, 2
	X	1	0	2, 3, 0, 1	2, 3, 0, 1
	X	1	1	3, 0, 1, 2	3, 2, 1, 0
8	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
Full page	location = 0-255			n, n+1, n+2, n+3, …255, 0, 1, 2, … n-1, n, …	Not Support

6.8.4. CAS# Latency Field (A6~A4)

This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS# Latency depends on the frequency of CLK. The minimum whole value satisfying the following formula must be programmed into this field.

$t_{CAC}(min) \le$ CAS# Latency X t_{CK}

A6	A5	A4	CAS# Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 clocks
0	1	1	3 clocks
1	X	X	Reserved

6.8.5. Test Mode Field (A8~A7)

These two bits are used to enter the test mode and must be programmed to "00" in normal operation.

A8	A7	Test Mode
0	0	Normal mode
0	1	Vendor Use Only
1	X	Vendor Use Only

6.8.6. Write Burst Length (A9)

This bit is used to select the write burst mode. When the A9 bit is "0", the Burst-Read-Burst-Write mode is selected. When the A9 bit is "1", the Burst-Read-Single-Write mode is selected.

A9	Write Burst Mode
0	Burst-Read-Burst-Write
1	Burst-Read-Single-Write

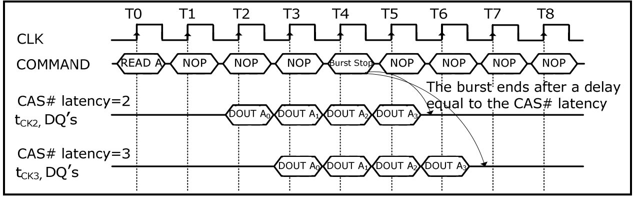
Note: A10 and BS should stay “L” during mode set cycle.

6.9. No-Operation Command(RAS# = "H", CAS# = "H", WE# = "H")

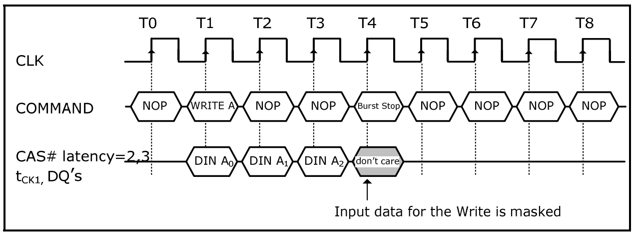
The No-Operation command is used to perform a NOP to the SDRAM which is selected (CS# is Low). This prevents unwanted commands from being registered during idle or wait states.

6.10. Burst Stop Command (RAS# = "H", CAS# = "H", WE# = "L")

The Burst Stop command is used to terminate either fixed-length or full-page bursts. This command is only effective in a read/write burst without the auto precharge function. The terminated read burst ends after a delay equal to the CAS# latency (refer to the following figure). The termination of a write burst is shown in the following figure.



Termination of a Burst Read Operation (Burst Length ＞ 4, CAS# Latency = 2, 3)



Termination of a Burst Write Operation (Burst Length = X, CAS# Latency = 2, 3)

6.11. Device Deselect Command (CS# = "H")

The Device Deselect command disables the command decoder so that the RAS#, CAS#, WE# and Address inputs are ignored, regardless of whether the CLK is enabled. This command is similar to the No Operation command.

6.12. AutoRefresh Command (RAS# = "L", CAS# = "L", WE# = "H", CKE = "H", A11 = “Don‘t care, A0-A9 = Don't care)

The AutoRefresh command is used during normal operation of the SDRAM and is analogous to CAS#-before-RAS# (CBR) Refresh in conventional DRAMs. This command is non-persistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "don't care" during an AutoRefresh command. The internal refresh counter increments automatically on every auto refresh cycle to all of the rows. The refresh operation must be performed 4096 times within 64ms. The time required to complete the auto refresh operation is specified by tXSR(min.). To provide the AutoRefresh command, all banks need to be in the idle state and the device must not be in power down mode (CKE is high in the previous cycle). This command must be followed by NOPs until the auto refresh operation is completed. The precharge time requirement, tRP(min), must be met before successive auto refresh operations are performed.

6.13. SelfRefresh Entry Command(RAS# = "L", CAS# = "L", WE# = "H", CKE = "L", A0-A9 = Don't care)

The SelfRefresh is another refresh mode available in the SDRAM. It is the preferred refresh mode for data retention and low power operation. Once the SelfRefresh command is registered, all the inputs to the SDRAM become "don't care" with the exception of CKE, which must remain LOW. The refresh addressing and timing is internally generated to reduce power consumption. The SDRAM may remain in SelfRefresh mode for an indefinite period. The SelfRefresh mode is exited by restarting the external clock and then asserting HIGH on CKE (SelfRefresh Exit command).

6.14. SelfRefresh Exit Command

This command is used to exit from the SelfRefresh mode. Once this command is registered, NOP or Device Deselect commands must be issued for tXSR(min.) because time is required for the completion of any bank currently being internally refreshed. If auto refresh cycles in bursts are performed during normal operation, a burst of 4096 auto refresh cycles should be completed just prior to entering and just after exiting the SelfRefresh mode.

6.15. Clock Suspend Mode Entry / PowerDown Mode Entry Command (CKE = "L")

When the SDRAM is operating the burst cycle, the internal CLK is suspended(masked) from the subsequent cycle by issuing this command (asserting CKE "LOW"). The device operation is held intact while CLK is suspended. On the other hand, when all banks are in the idle state, this command performs entry into the PowerDown mode. All input and output buffers (except the CKE buffer) are turned off in the PowerDown mode. The device may not remain in the Clock Suspend or PowerDown state longer than the refresh period (64ms) since the command does not perform any refresh operations.

6.16. Clock Suspend Mode Exit / PowerDown Mode Exit Command (CKE= "H")

When the internal CLK has been suspended, the operation of the internal CLK is reinitiated from the subsequent cycle by providing this command (asserting CKE "HIGH", the command should be NOP or deselect). When the device is in the PowerDown mode, the device exits this mode and all disabled buffers are turned on to the active state. tPDE(min.) is required when the device exits from the PowerDown mode. Any subsequent commands can be issued after one clock cycle from the end of this command.

6.17. Data Write / Output Enable, Data Mask / Output Disable Command (DQM = "L", "H")

During a write cycle, the DQM signal functions as a Data Mask and can control every word of the input data. During a read cycle, the DQM functions as the controller of output buffers. DQM is also used for device selection, byte selection and bus control in a memory system.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Rating

Symbol	Item	Rating	Unit	Note
VIN, VOUT	Input, Output Voltage	-1.0 ~ 4.6	V	1
VDD, VDDQ	Power Supply Voltage	-.0 ~ 4.6	V	1
TA	Ambient Temperature	0 ~ 70	°C	1
TSTG	Storage Temperature	-55 ~ 125	°C	1
TSOLDER	Soldering Temperature (10 second)	260	°C	1
PD	Power Dissipation	1	W	1
IOUT	Short Circuit Output Current	50	mA	1

7.2. Recommended D.C. Operating Conditions (TA = - 0~70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
VDD	Power Supply Voltage	3.0	3.3	3.6	V	2
VDDQ	Power Supply Voltage(for I/O Buffer)	3.0	3.3	3.6	V	2
VIH	LVTTL Input High Voltage	2.0	—	VDDQ+0.3	V	2
VIL	LVTTL Input Low Voltage	- 0.3	—	0.8	V	2

7.3. Capacitance (VDD = 3.3V, f = 1MHz, TA = 25℃)

Symbol	Parameter	Min.	Max.	Unit
CI	Input Capacitance	2	5	pF
CI/O	Input/Output Capacitance	4	6.5	pF

7.4. Recommended D.C. Operating Conditions (VDD = 3.3V ± 0.3V, TA = 0~70℃)

Description/Test condition	Symbol	Max.	Unit	Note
Operating Current tRC ≥ tRC(min), Outputs Open One bank active	IDD1	85	mA	3
Precharge Standby Current in non-power down mode tCK = 15ns, CS# ≥ VIH(min), CKE ≥ V_{IH} Input signals are changed every 2clks	IDD2N	25		
Precharge Standby Current in non-power down mode tCK = ∞, CLK ≤ V_{IL}(max), CKE ≥ V_{IH}	IDD2NS	15		
Precharge Standby Current in power down mode tCK = 15ns, CKE ≤ VIL(max)	IDD2P	2		
Precharge Standby Current in power down mode tCK = ∞, CKE ≤ VIL(max)	IDD2PS	2		
Active Standby Current in non-power down mode tCK = 15ns, CKE ≥ VIH(min), CS# ≥ VIH(min) Input signals are changed every 2clks	IDD3N	30		
Active Standby Current in non-power down mode CKE ≥ VIH(min), CLK ≤ VIL(max), tCK = ∞	IDD3NS	25		
Operating Current (Burst mode) tCK =tCK(min), Outputs Open, Multi-bank interleave	IDD4	100		3, 4

Description/Test condition	Symbol	Max.	Unit	Note
Refresh Current tRC ≥ tRC(min)	IDD5	130		3
Self Refresh Current CKE ≤ 0.2V ; for other inputs VIH ≥VDD - 0.2V, VIL ≤ 0.2V	IDD6	2		

Parameter	Description	Min.	Max.	Unit	Note
IIL	Input Leakage Current (0V ≤ VIN ≤ VDD, All other pins not under test = 0V)	- 10	10	μA	
IOL	Output Leakage Current Output disable, 0V ≤ VOUT ≤ VDDQ)	- 10	10	μA	
VOH	LVTTL Output "H" Level Voltage (IOUT = -2mA)	2.4	—	V	
VOL	LVTTL Output "L" Level Voltage (IOUT = 2mA)	—	0.4	V	

7.5. Electrical Characteristics and Recommended A.C. Operating Conditions (VDD = 3.3V±0.3V, T_A = 0~70℃) (Note: 5, 6, 7, 8)

Symbol	A.C. Parameter		Min.	Max.	Unit	Note
tRC	Row cycle time (same bank)		60	-	ns	
tRCD	RAS# to CAS# delay (same bank)		18	-		
tRP	Precharge to refresh/row activate command (same bank)		18	-		
tRRD	Row activate to row activate delay (different banks)		12	-		
tRAS	Row activate to precharge time (same bank)		42	-		
tWR	Write recovery time		2	-	tCK	
tCCD	CAS# to CAS# Delay time		1	-		
tCK	Clock cycle time	CL* = 2	10	-	ns	9
		CL* = 3	6	-		
tCH	Clock high time		2.5	-		10
tCL	Clock low time		2.5	-		10
tAC	Access time from CLK (positive edge)	CL* = 2	-	6		10
		CL* = 3	-	5		
tOH	Data output hold time		2	-		9
tLZ	Data output low impedance		1	-		
tHZ	Data output high impedance		-	5		8
tIS	Data/Address/Control Input set-up time		1.5	-		10
tIH	Data/Address/Control Input hold time		1	-		10
tPDE	Power Down Exit set-up time		tIS+tCK	-		
tMRD	Mode Register Set Command Cycle Time		2	-	tCK	
tREFI	Refresh Interval Time		-	15.6	μs	
tXSR	Exit Self-Refresh to Read Command		tRC+tIS	-	ns	

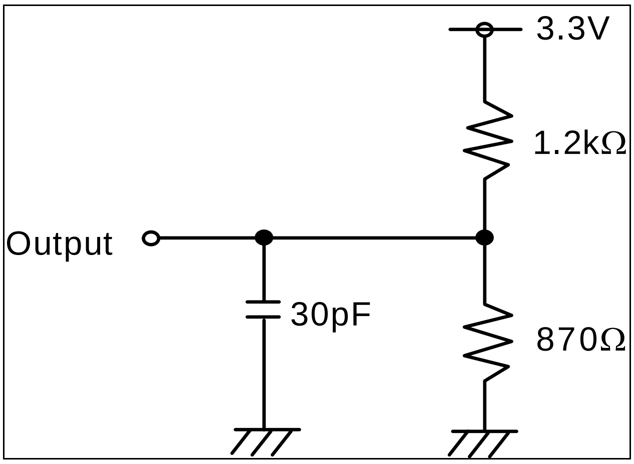
＊ CL is CAS# Latency.

Note:

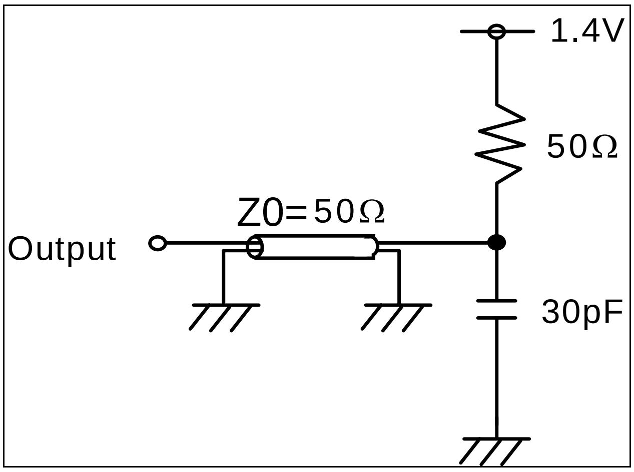
1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to VSS. VIH(Max) = 4.6V for pulse width ≦3ns. VIL(Min) = -1.5V for pulse width ≦ 3ns.
3. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of tCK and tRC. Input signals are changed one time during every 2 tCK.
4. These parameters depend on the output loading. Specified values are obtained with the output open.
5. Power-up sequence is described in Note 11.
6. A.C. Test Conditions

LVTTL Interface

Reference Level of Output Signals	1.4V / 1.4V
Output Load	Reference to the Under Output Load (B)
Input Signal Levels	2.4V / 0.4V
Transition Time (Rise and Fall) of Input Signals	1ns
Reference Level of Input Signals	1.4V



LVTTL D.C. Test Load (A)

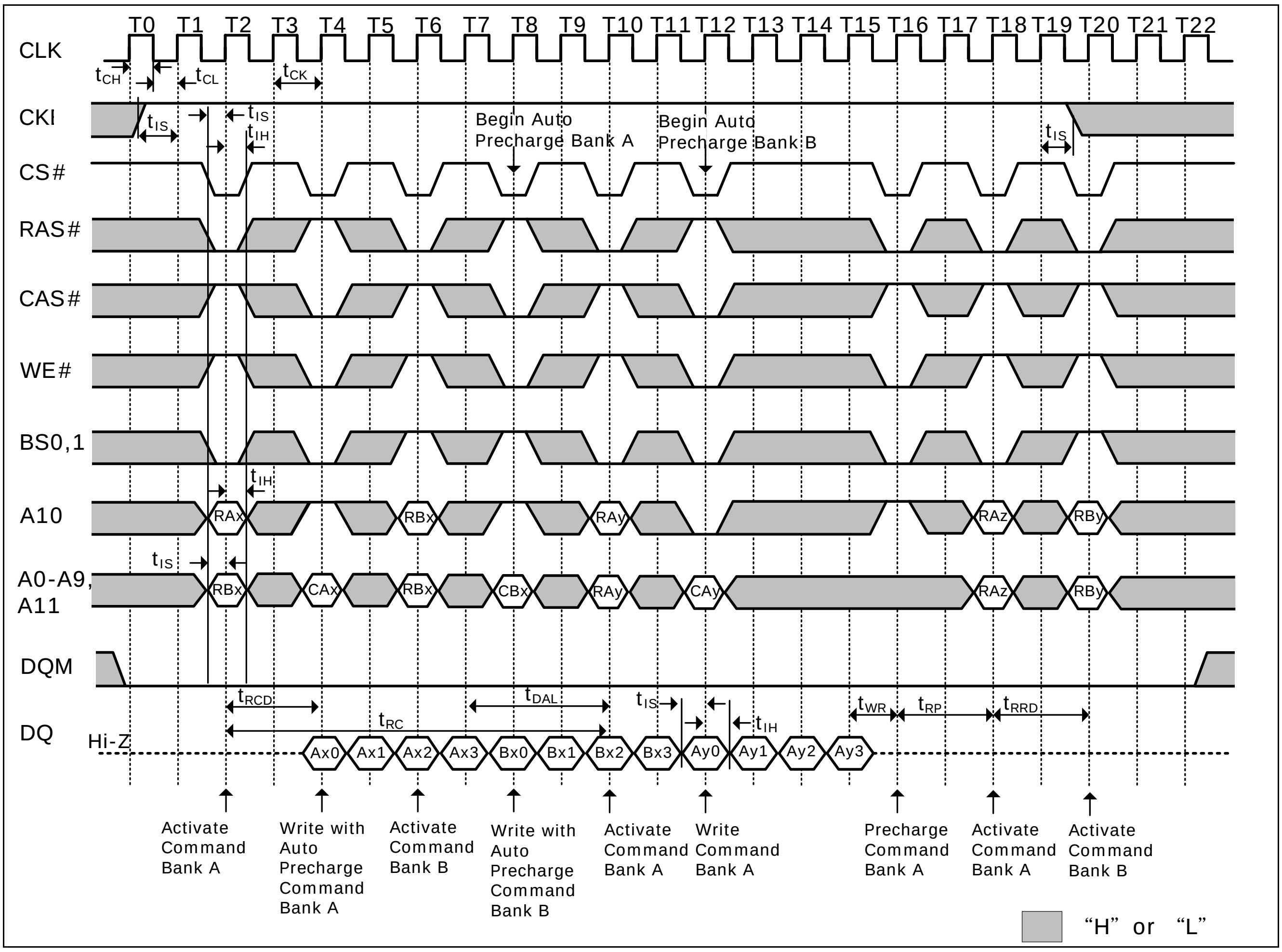


LVTTL A.C. Test Load (B)

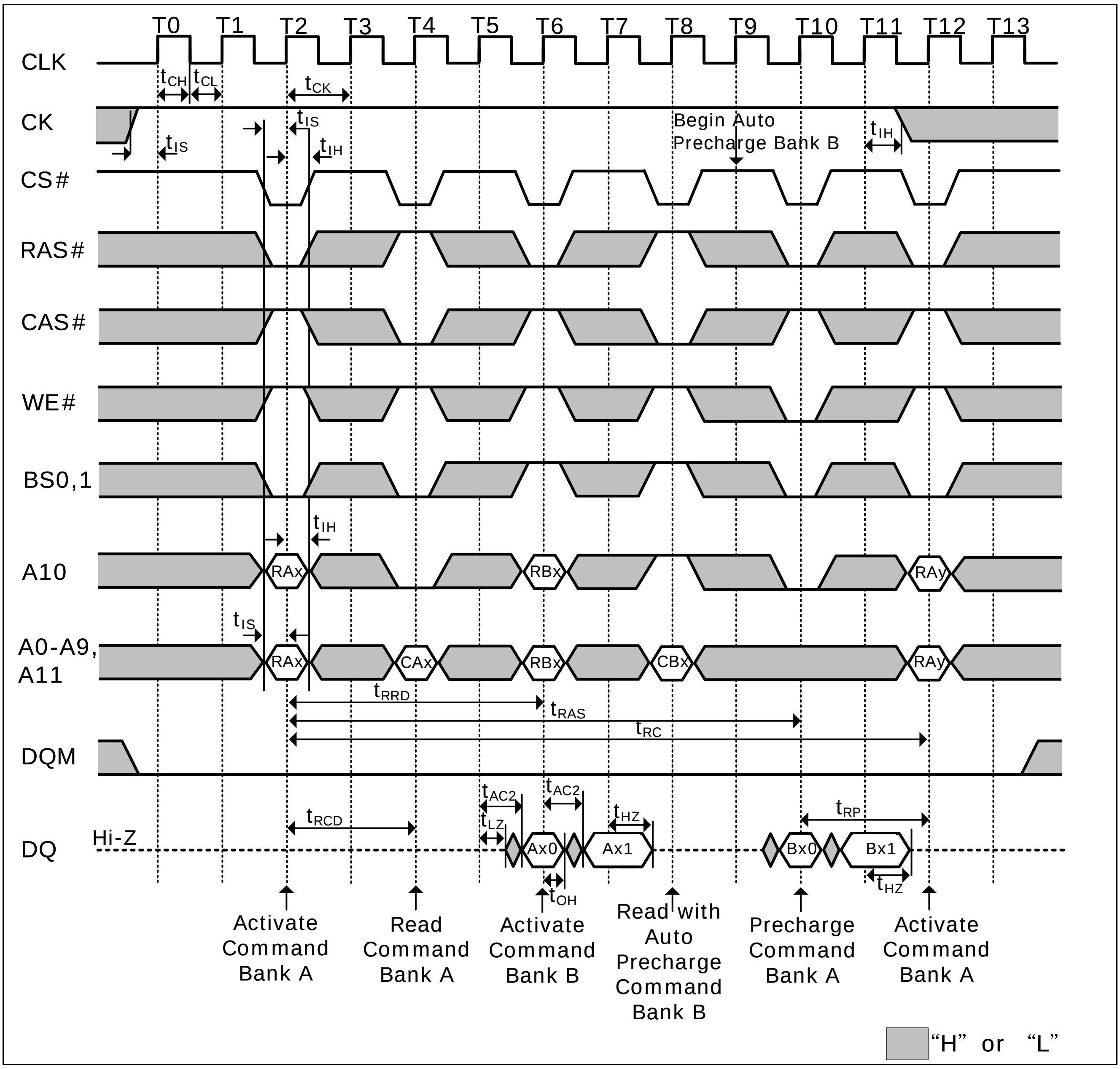
7. Transition times are measured between VIH and VIL. Transition(rise and fall) of input signals are in a fixed slope (1 ns).
8. tHZ defines the time in which the outputs achieve the open circuit condition and are not at reference levels.
9. If clock rising time is longer than 1 ns, (tR / 2 -0.5) ns should be added to the parameter.
10. Assumed input rise and fall time tT (tR & tF) = 1 ns
    If tR or tF is longer than 1 ns, transient time compensation should be considered, i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.
11. Power up Sequence
    Power up must be performed in the following sequence.
    (1) Power must be applied to VDD and VDDQ(simultaneously) when CKE= “L”, DQM= “H” and all input signals are held "NOP" state .
    (2) Start clock and maintain stable condition for minimum 200 µs, then bring CKE= “H” and, it is recommended that DQM is held "HIGH" (VDD levels) to ensure DQ output is in high impedance.
    (3) All banks must be precharged.
    (4) Mode Register Set command must be asserted to initialize the Mode register.
    (5) A minimum of 2 Auto-Refresh dummy cycles must be required to stabilize the internal circuitry of the device.

8. TIMING WAVEFORMS

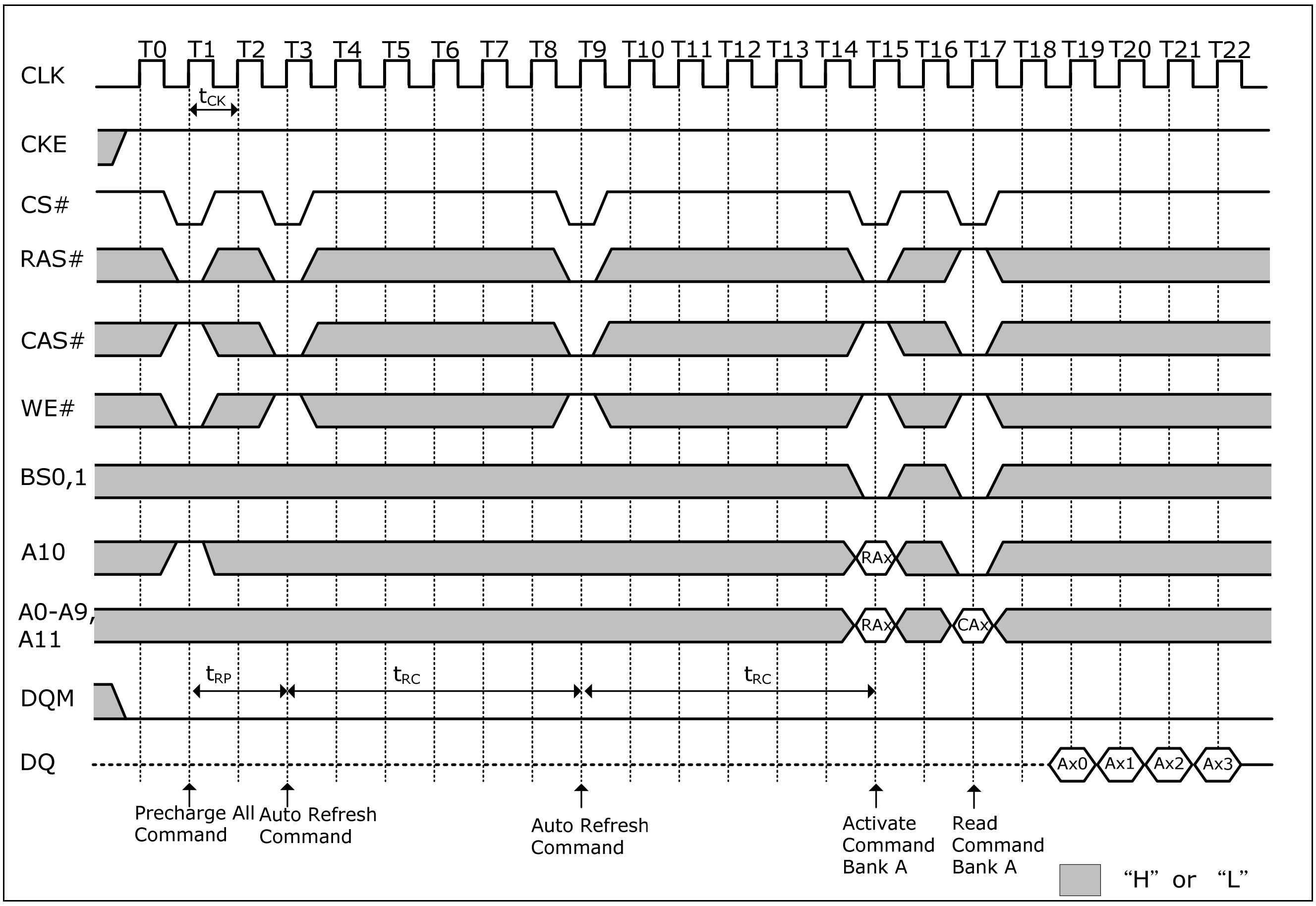
8.1. AC Parameters for Write Timing (Burst Length=4)



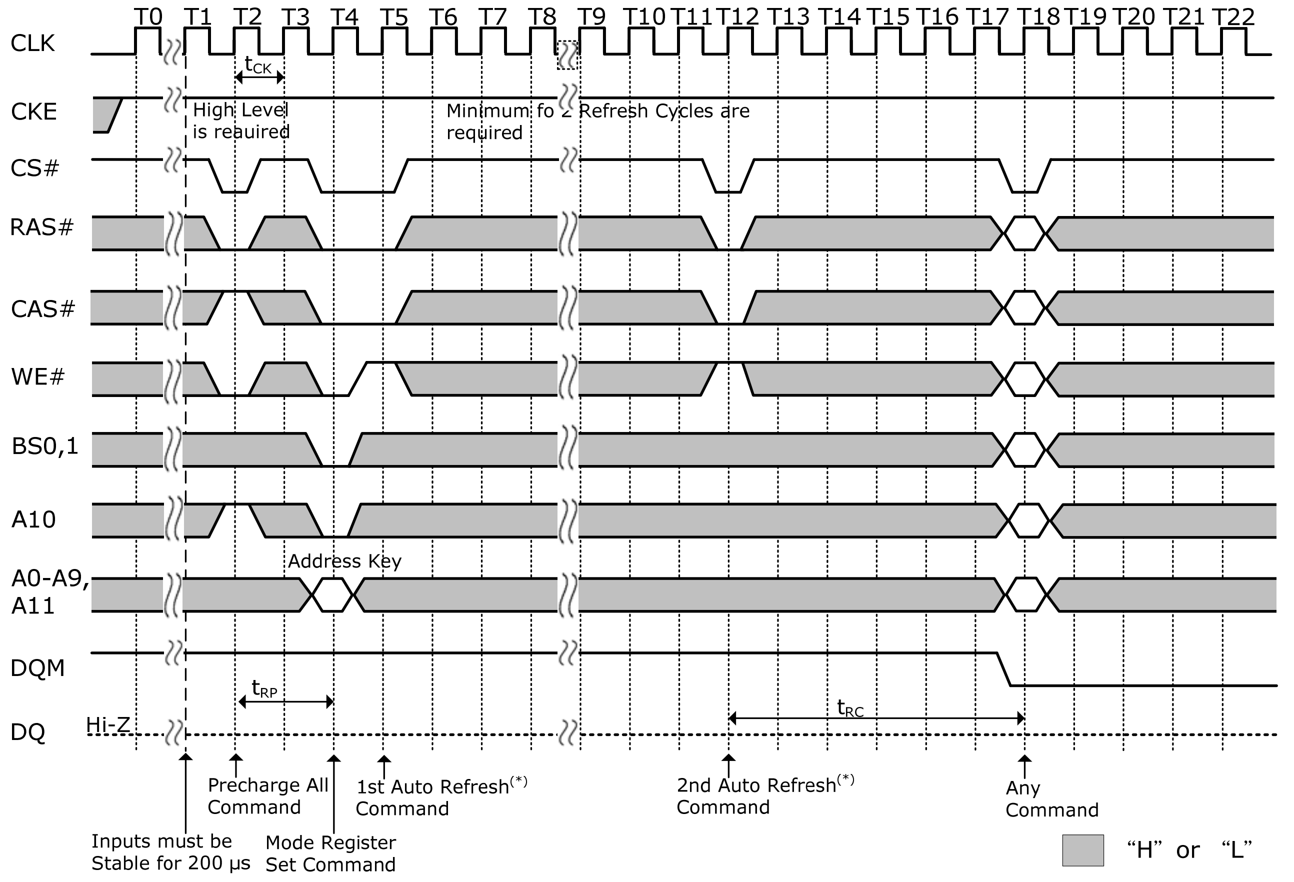
8.2. AC Parameters for Read Timing (Burst Length=2, CAS# Latency=2)



8.3. Auto Refresh (CBR) (Burst Length=4, CAS# Latency=2)

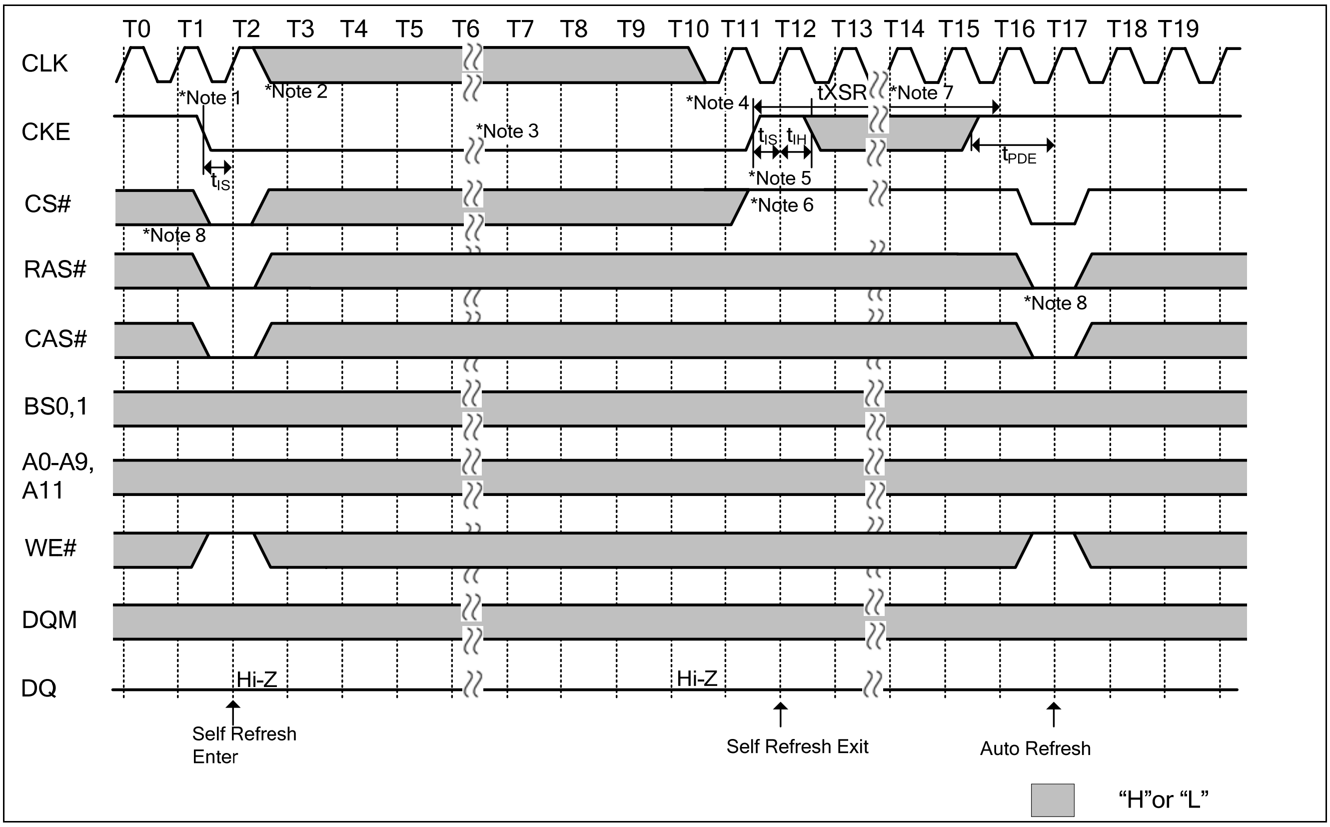


8.4. Power on Sequence and Auto Refresh (CBR)



Note(*):The Auto Refresh command can be issue before or after Mode Register Set command

8.5. Self Refresh Entry & Exit Cycle

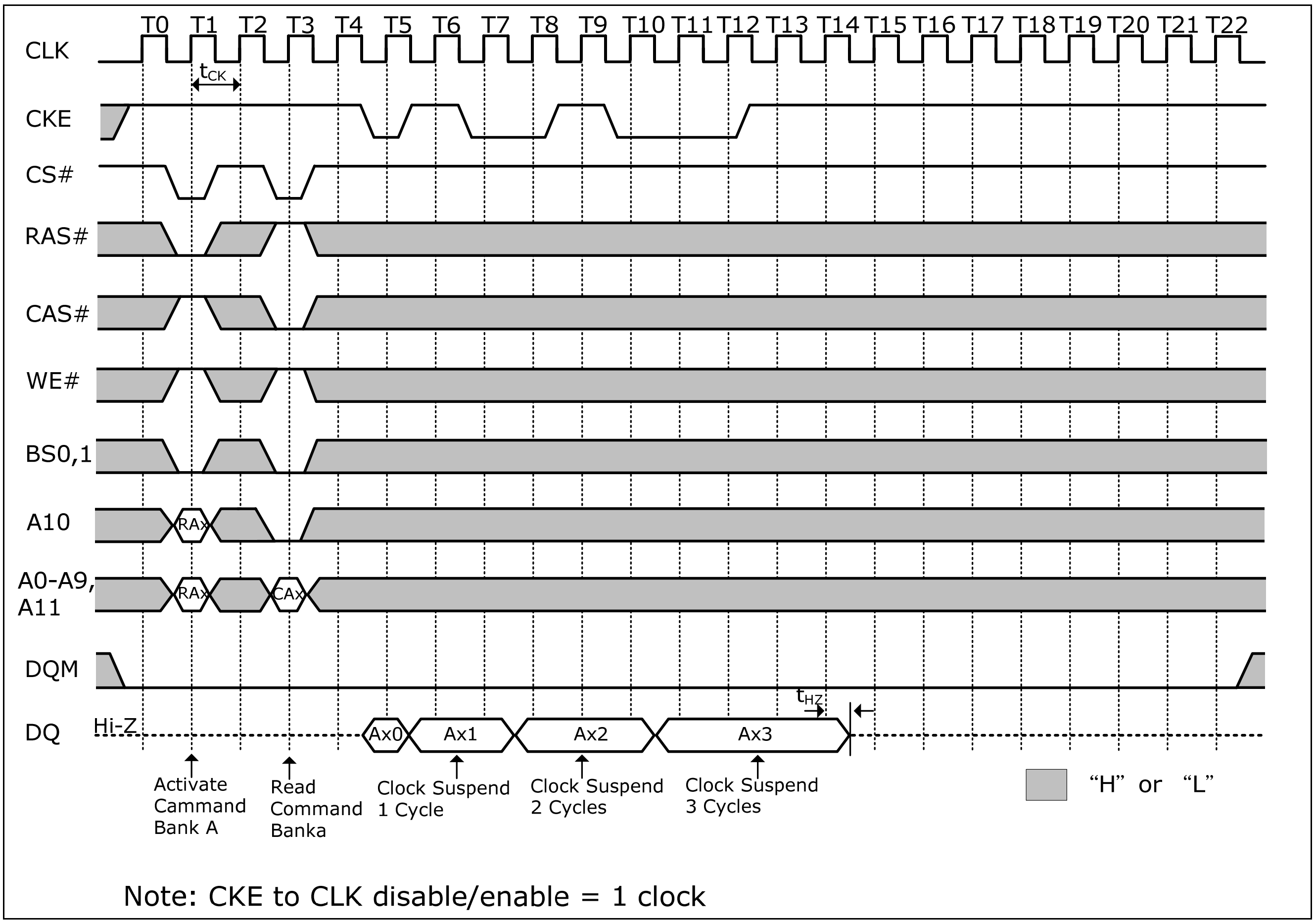


Note: To Enter SelfRefresh Mode

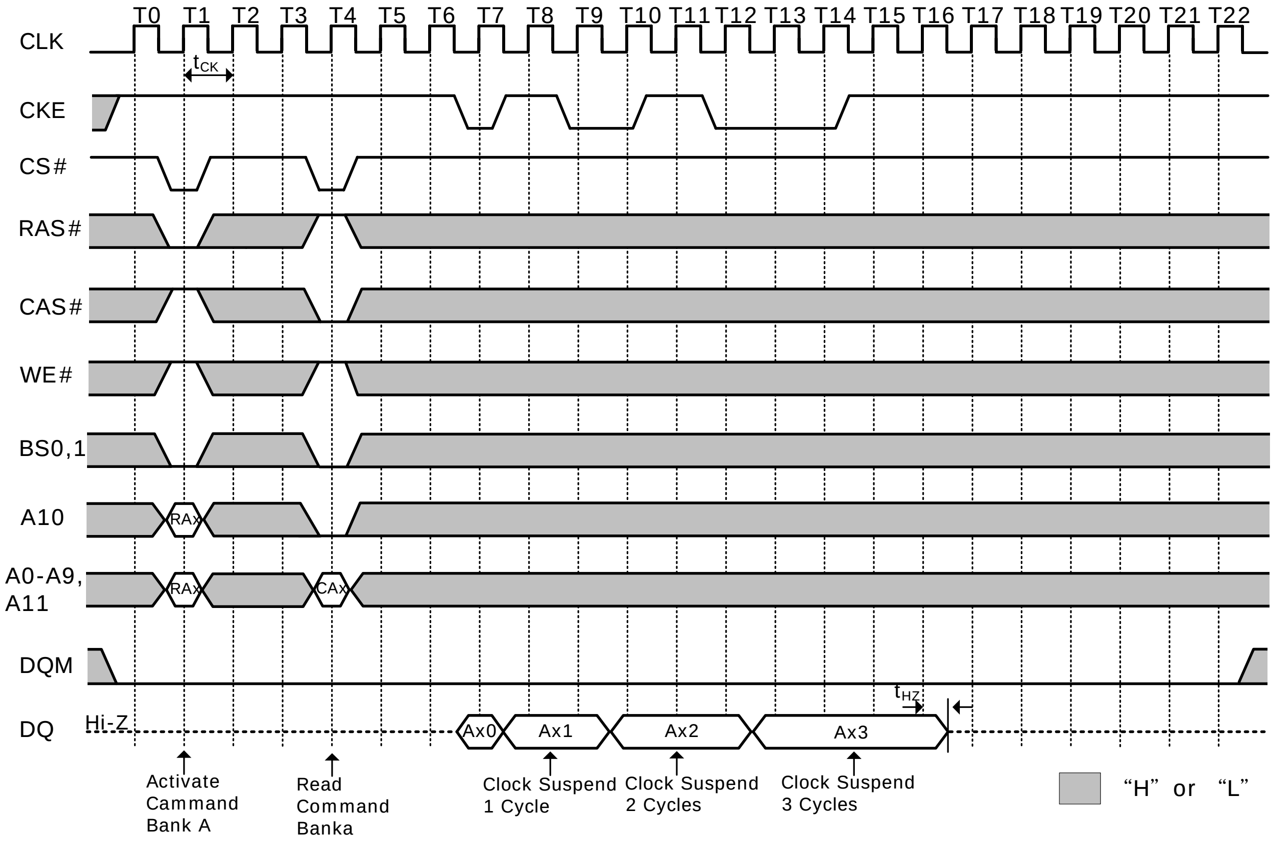
1. CS#, RAS# & CAS# with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in SelfRefresh mode as long as CKE stays "low".
4. Once the device enters SelfRefresh mode, minimum tRAS is required before exit from SelfRefresh. **To Exit SelfRefresh Mode**
5. System clock restart and be stable before returning CKE high.
6. Enable CKE and CKE should be set high for valid setup time and hold time.
7. CS# starts from high.
8. Minimum tXSR is required after CKE going high to complete SelfRefresh exit.
9. 4096 cycles of burst AutoRefresh is required before SelfRefresh entry and after SelfRefresh exit if the system uses burst refresh.

8.6. Clock Suspension During Burst Read (Using CKE)

8.6.1. Burst Length=4, CAS# Latency=2



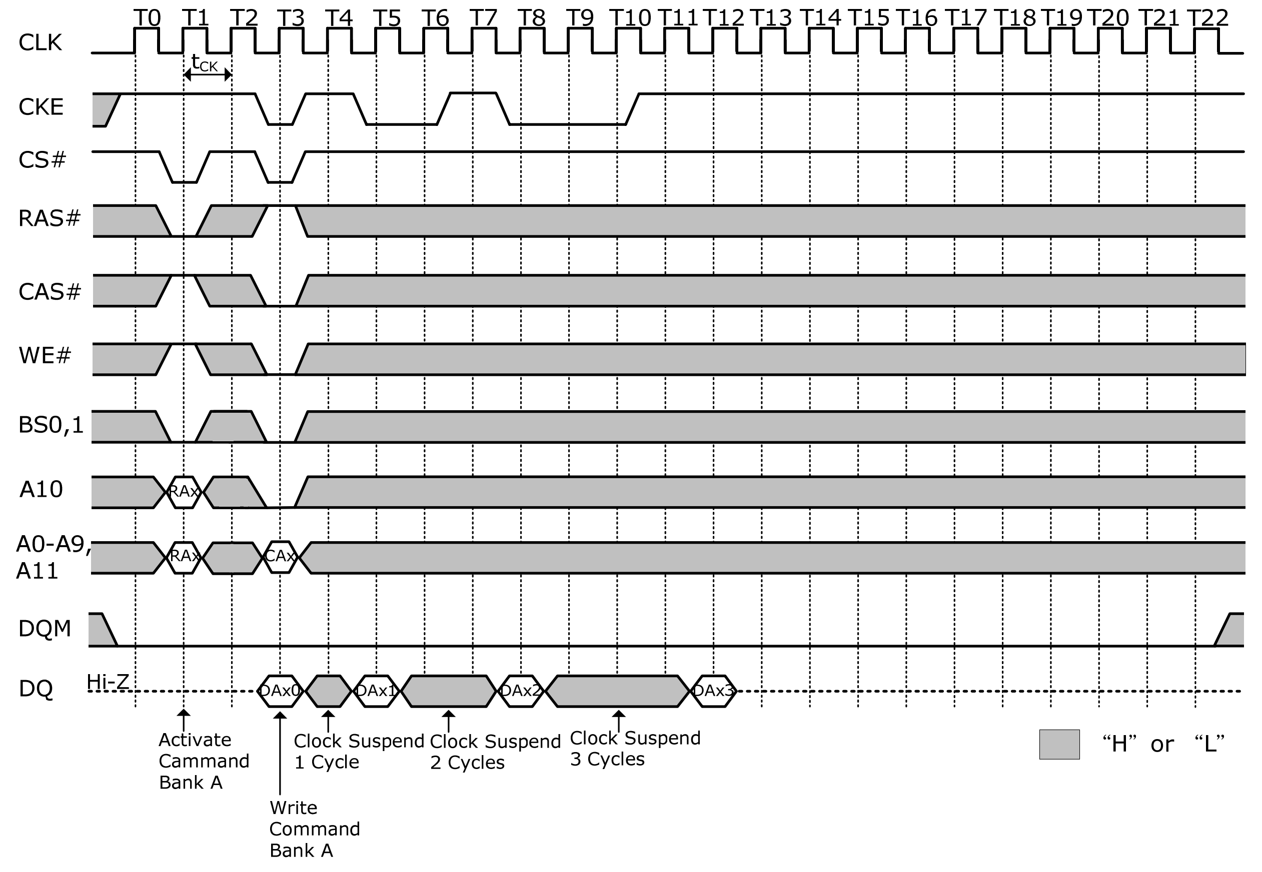
8.6.2. Burst Length=4, CAS# Latency=3



Note: CKE to CLK disable/enable = 1 clock

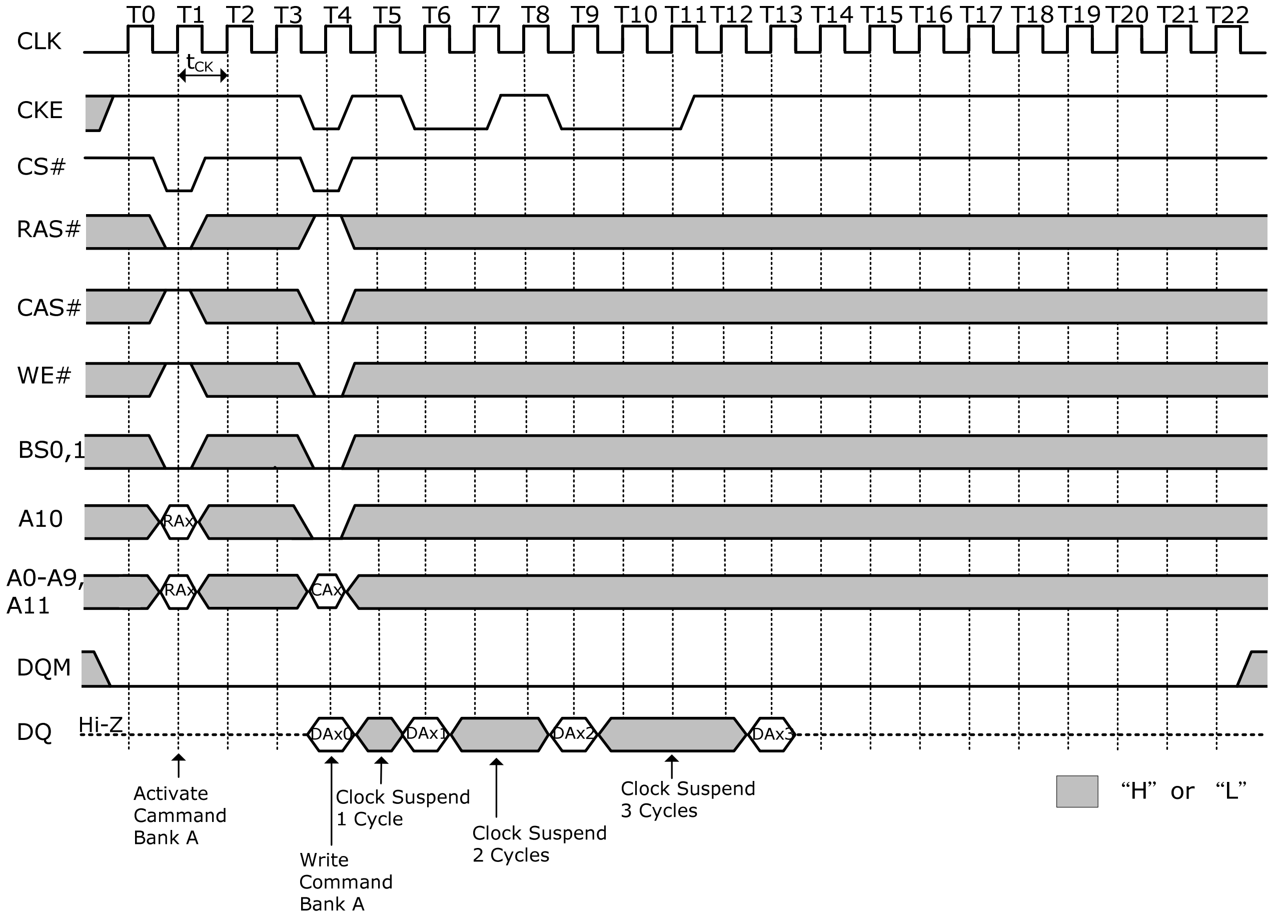
8.7. Clock Suspension During Burst Write (Using CKE)

8.7.1. Burst Length=4, CAS# Latency=2



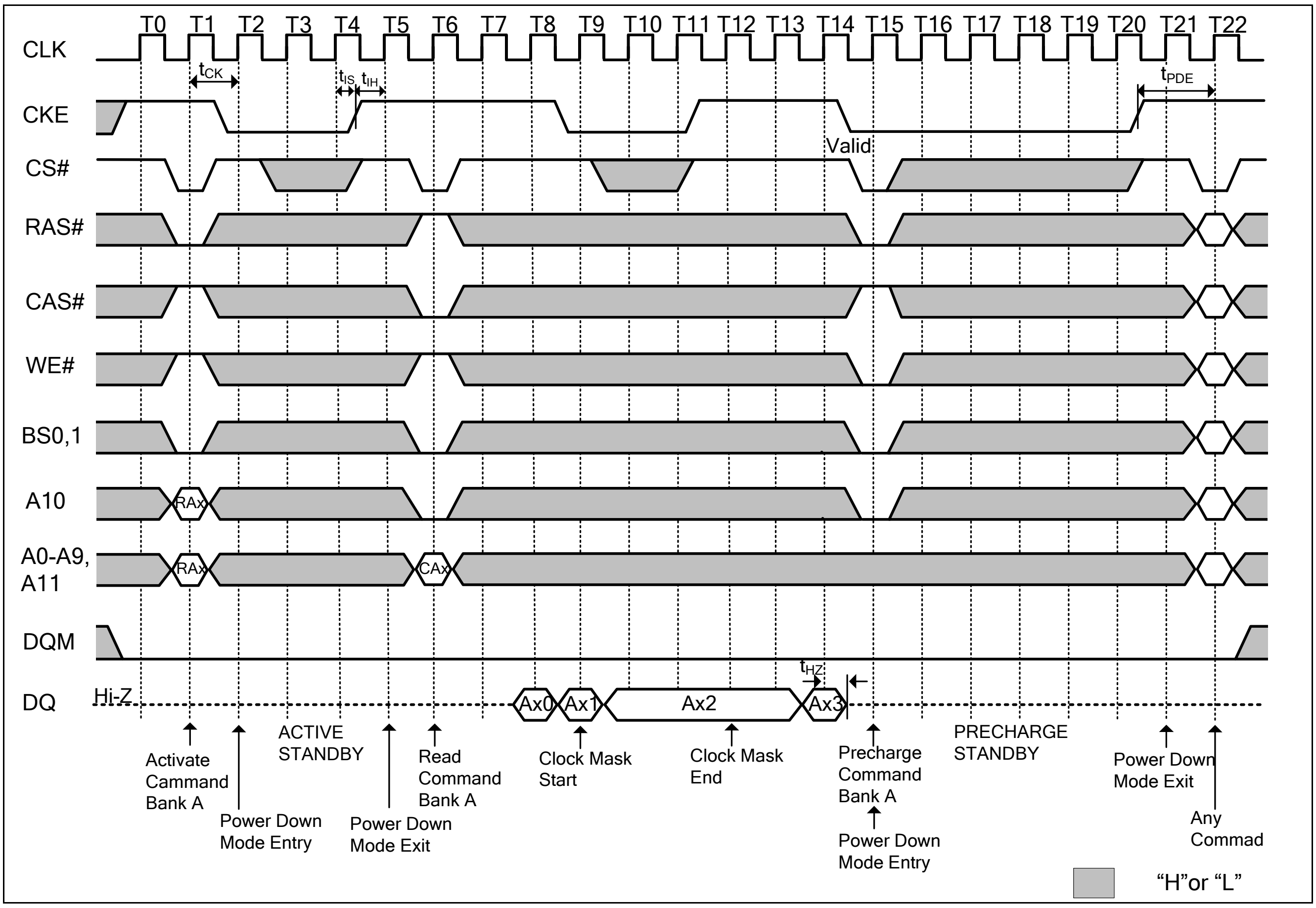
Note: CKE to CLK disable/enable = 1 clock

8.7.2. Burst Length=4, CAS# Latency=3



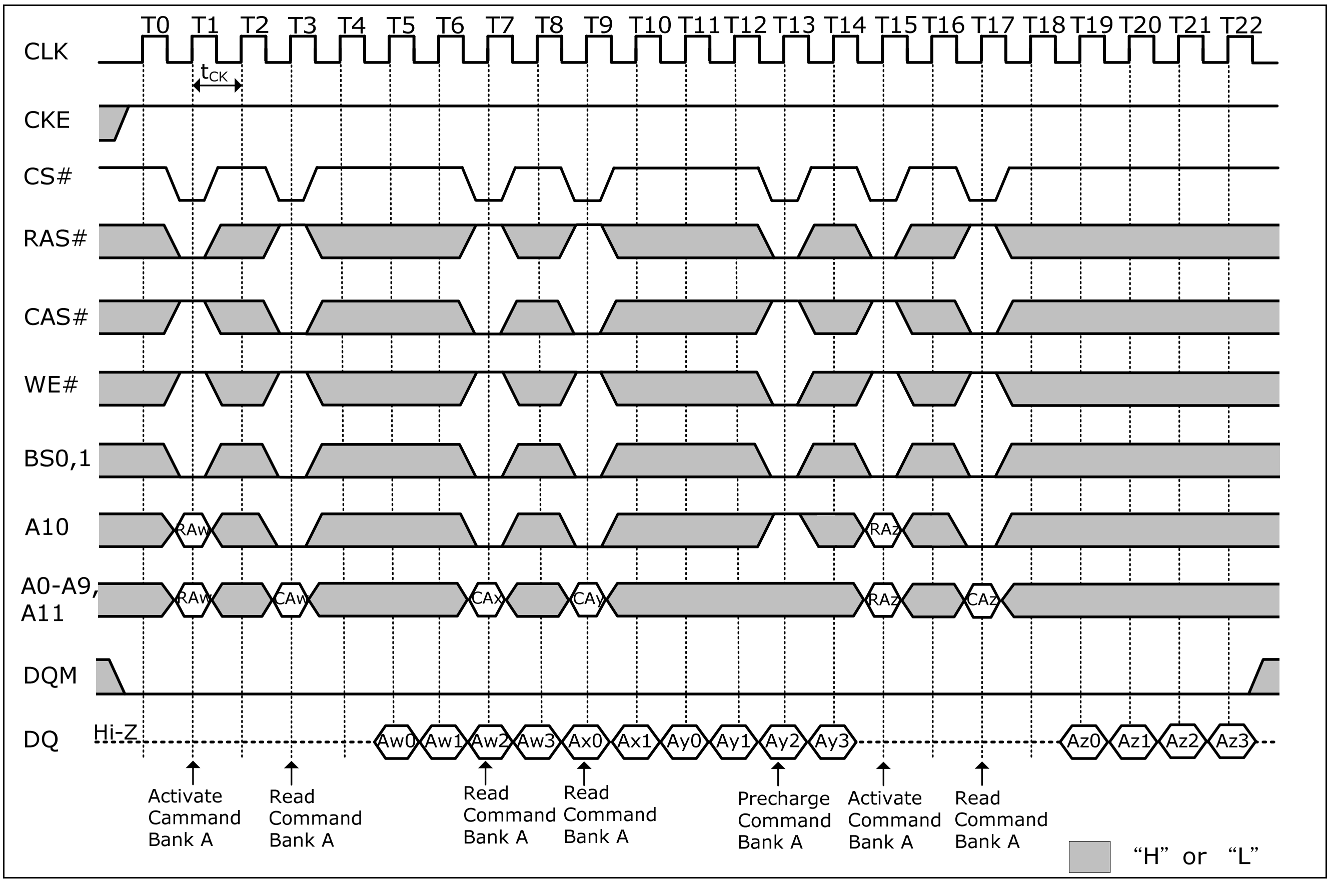
Note: CKE to CLK disable/enable = 1 clock

8.8. Power Down Mode and Clock Mask (Burst Length=4, CAS# Latency=2)

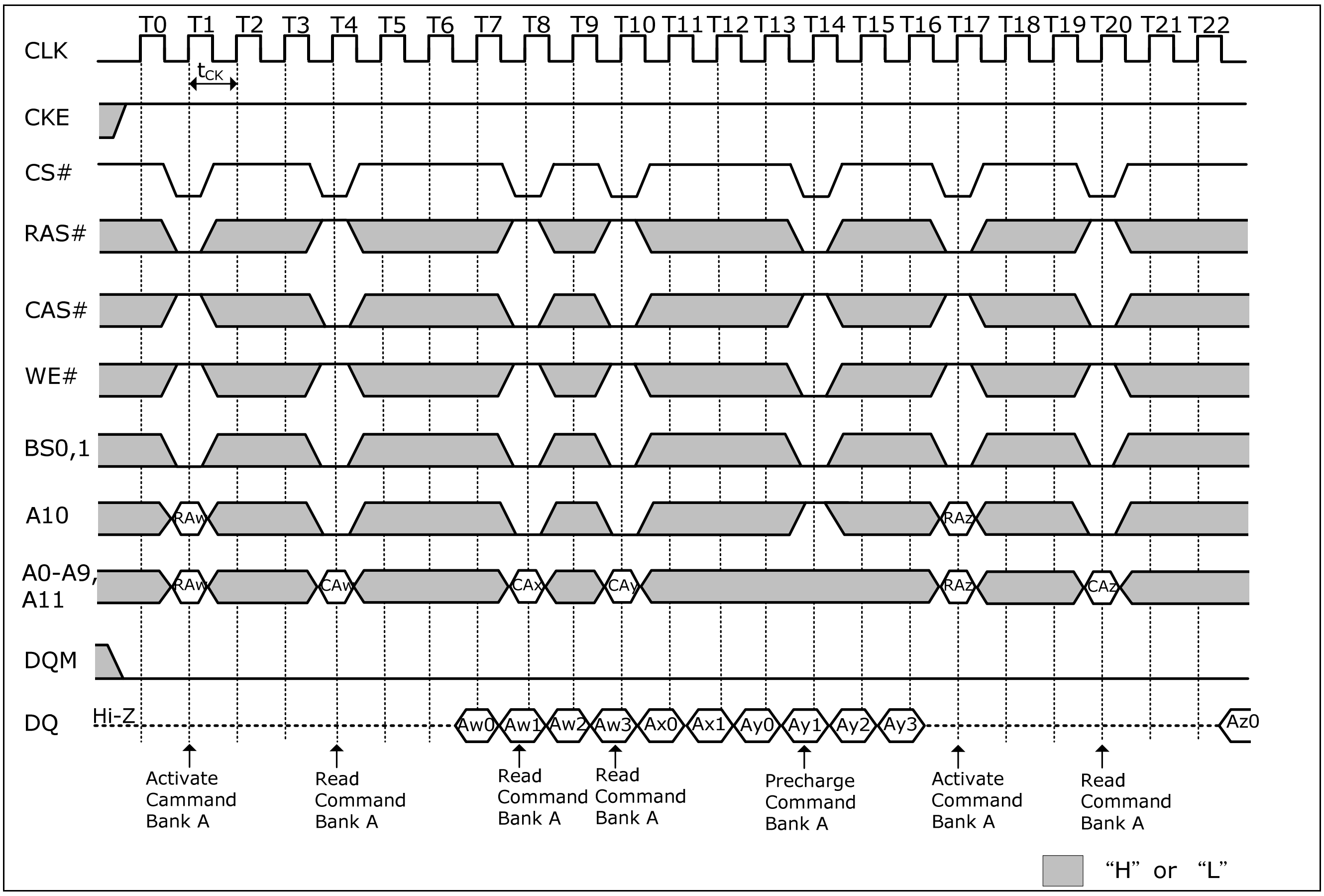


8.9. Random Column Read (Page within same Bank)

8.9.1. Burst Length=4, CAS# Latency=2

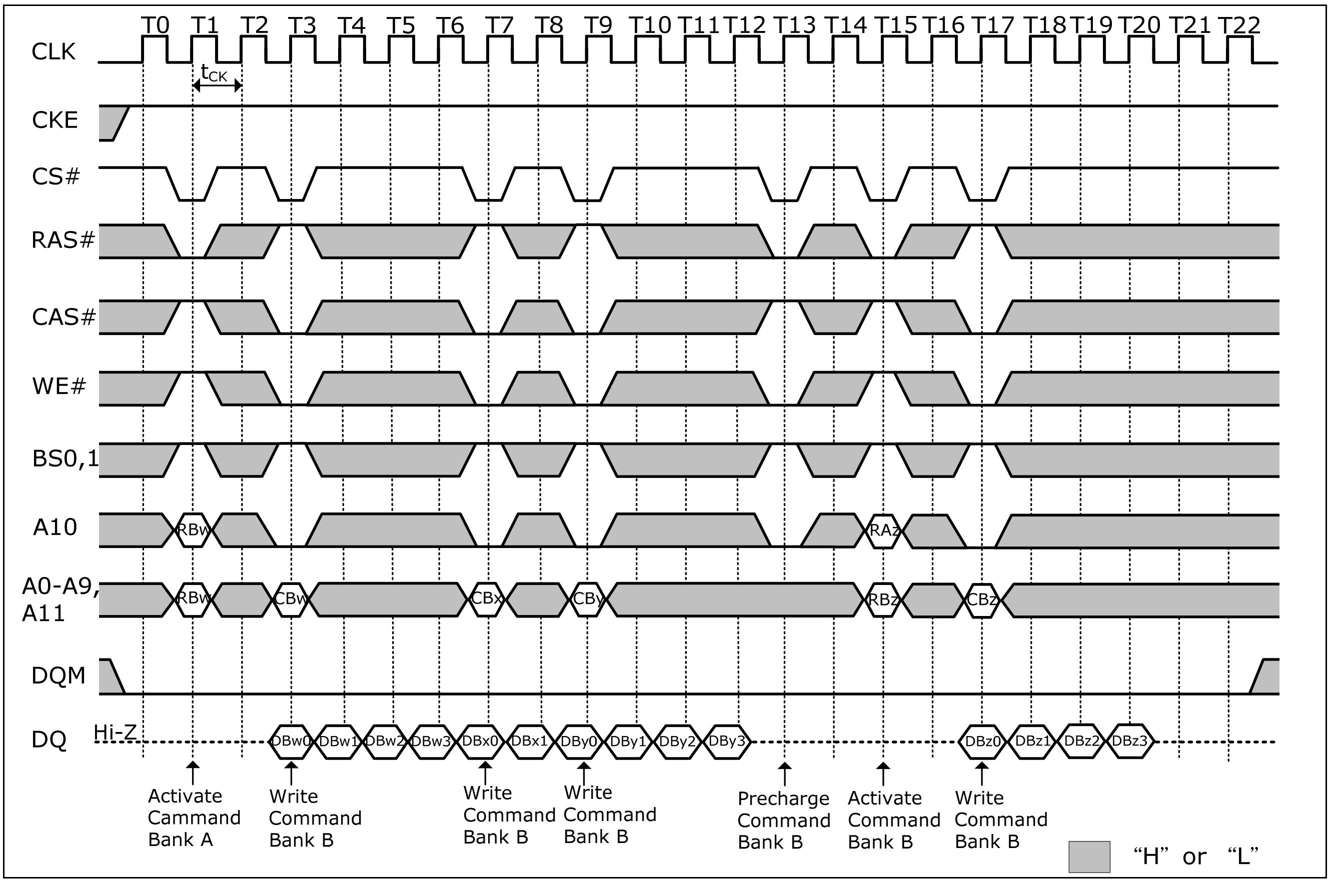


8.9.2. Burst Length=4, CAS# Latency=3

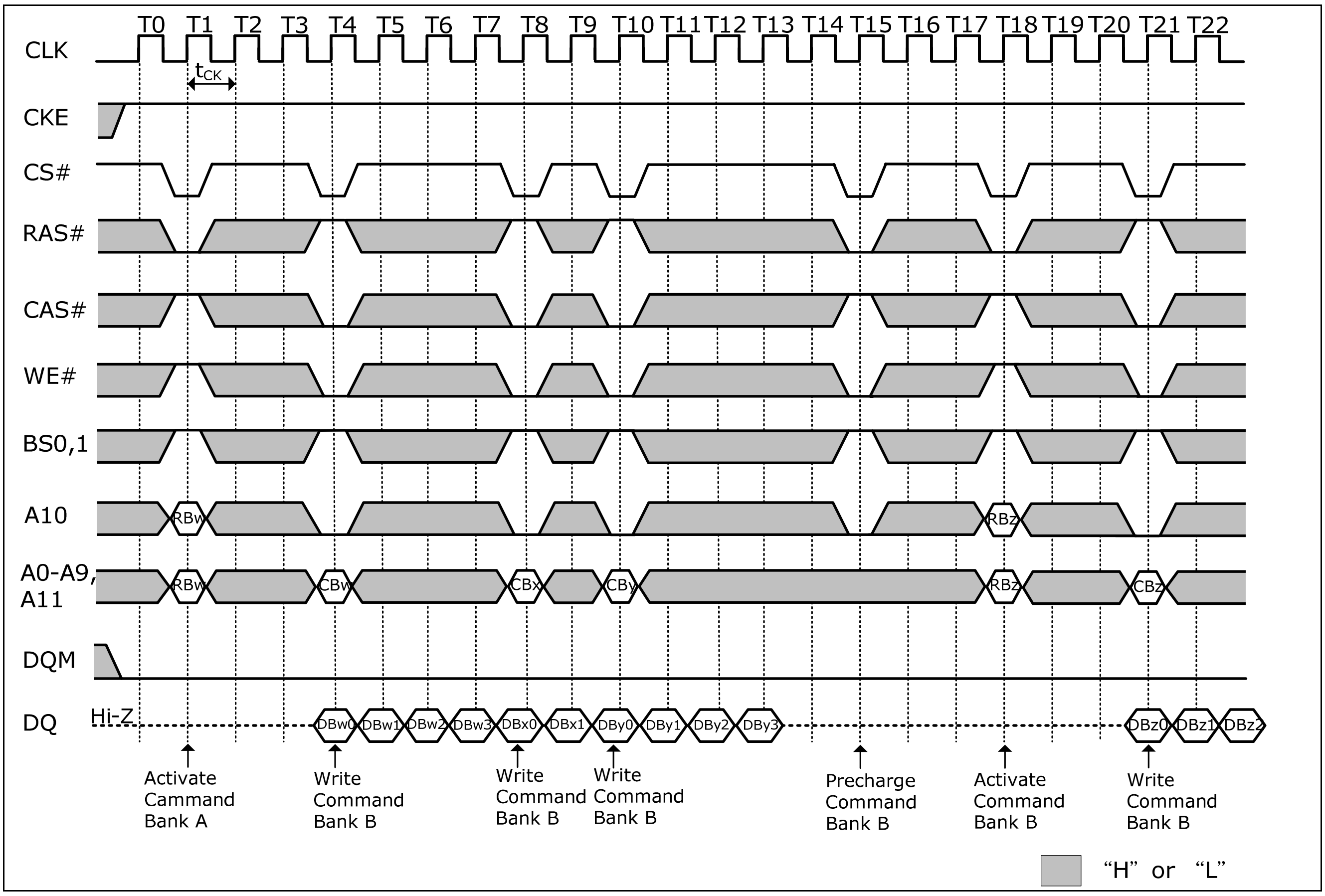


8.10. Random Column Write (Page within same Bank)

8.10.1. Burst Length=4, CAS# Latency=2

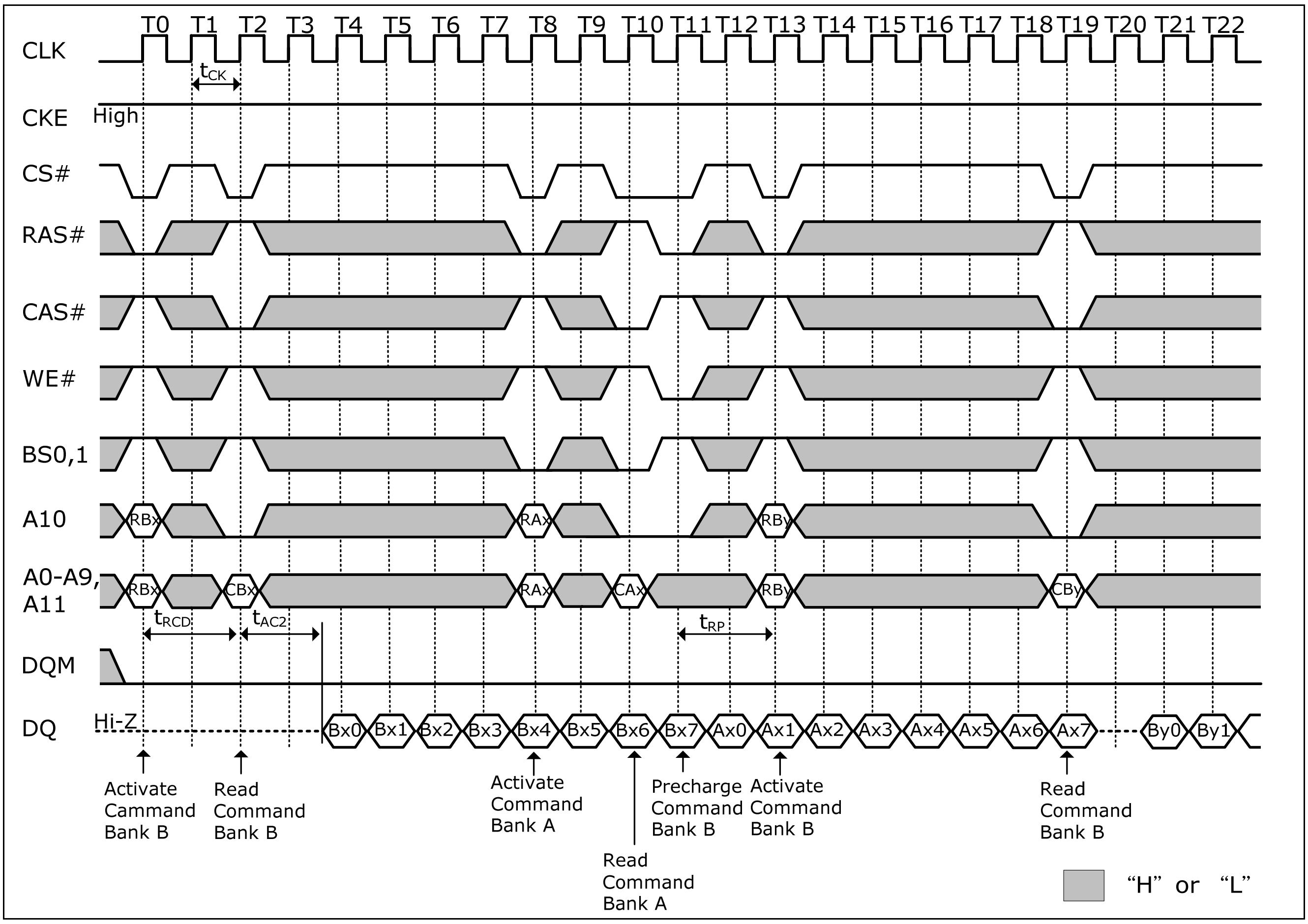


8.10.2. Burst Length=4, CAS# Latency=3

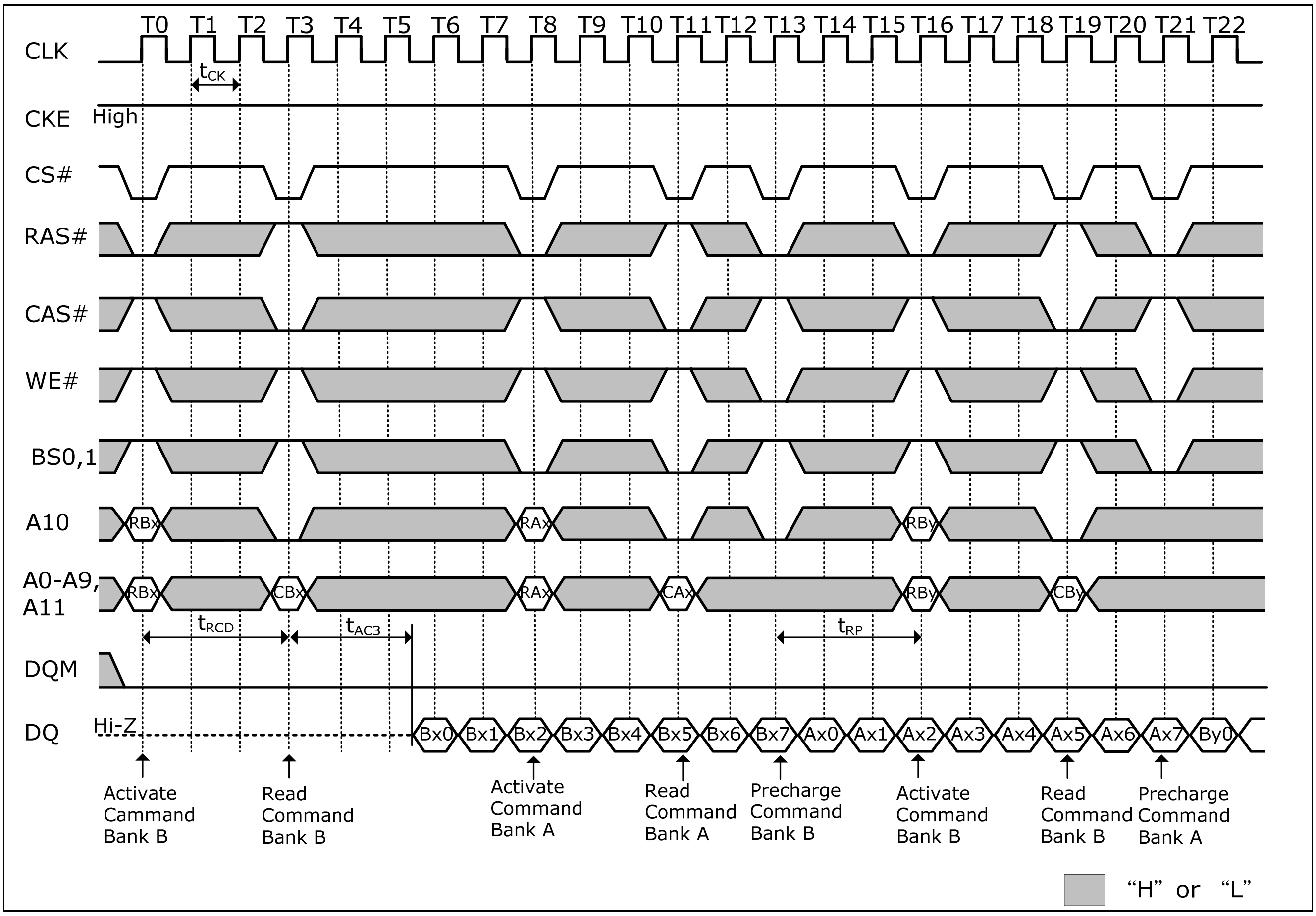


8.11. Random Row Read (Interleaving Banks)

8.11.1. Burst Length=8, CAS# Latency=2

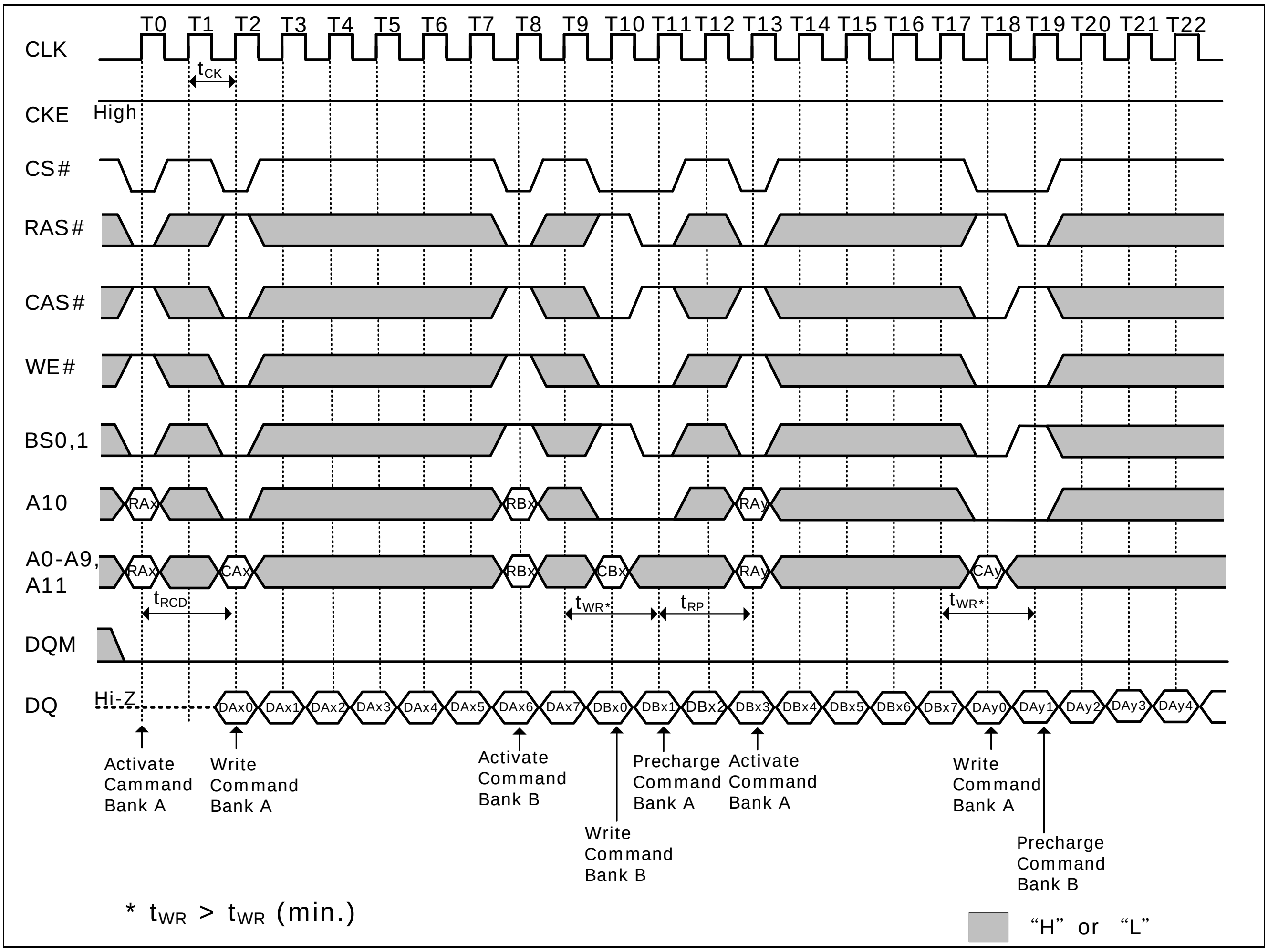


8.11.2. Burst Length=8, CAS# Latency=3

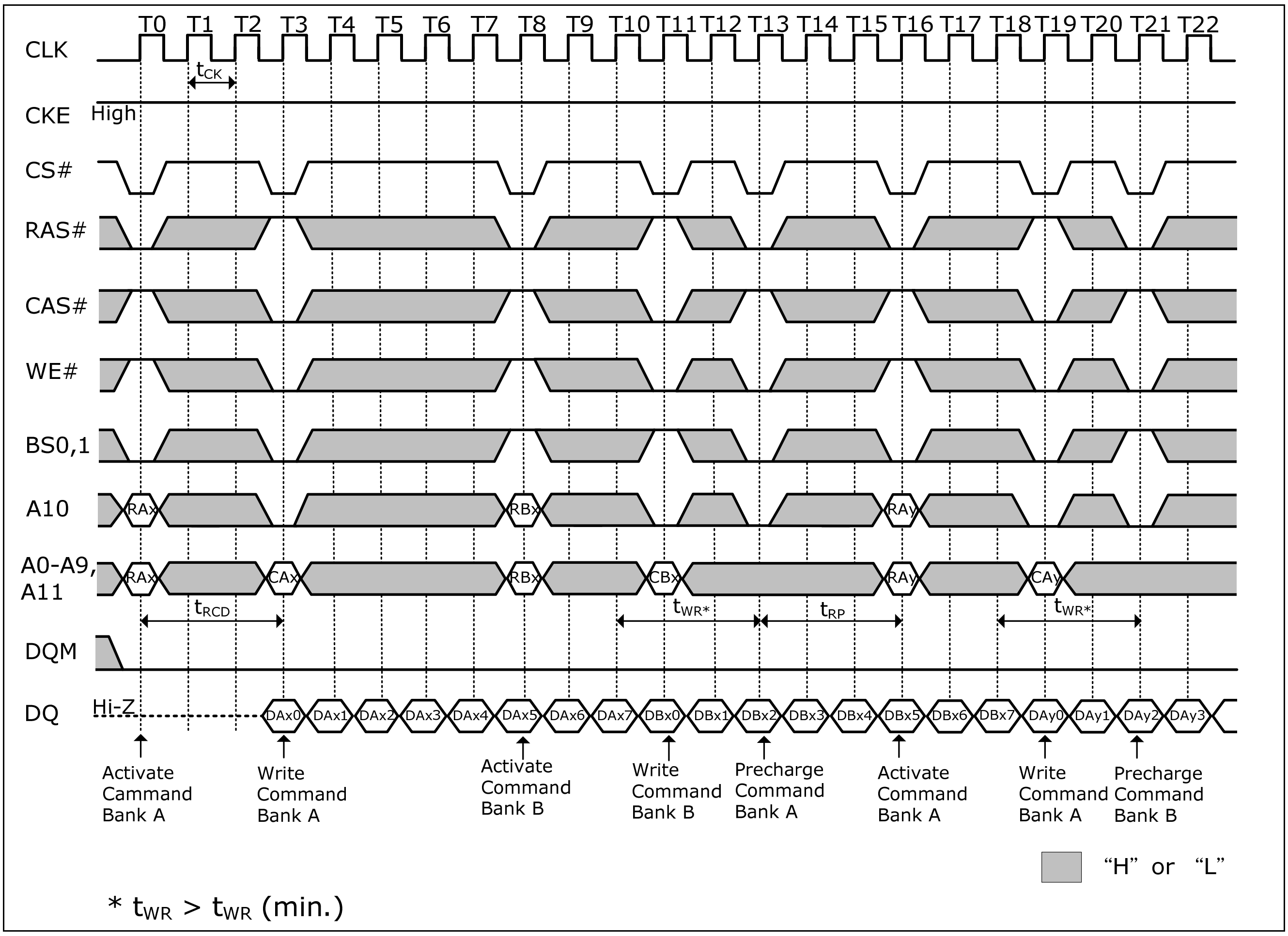


8.12. Random Row Write (Interleaving Banks)

8.12.1. Burst Length=8, CAS# Latency=2

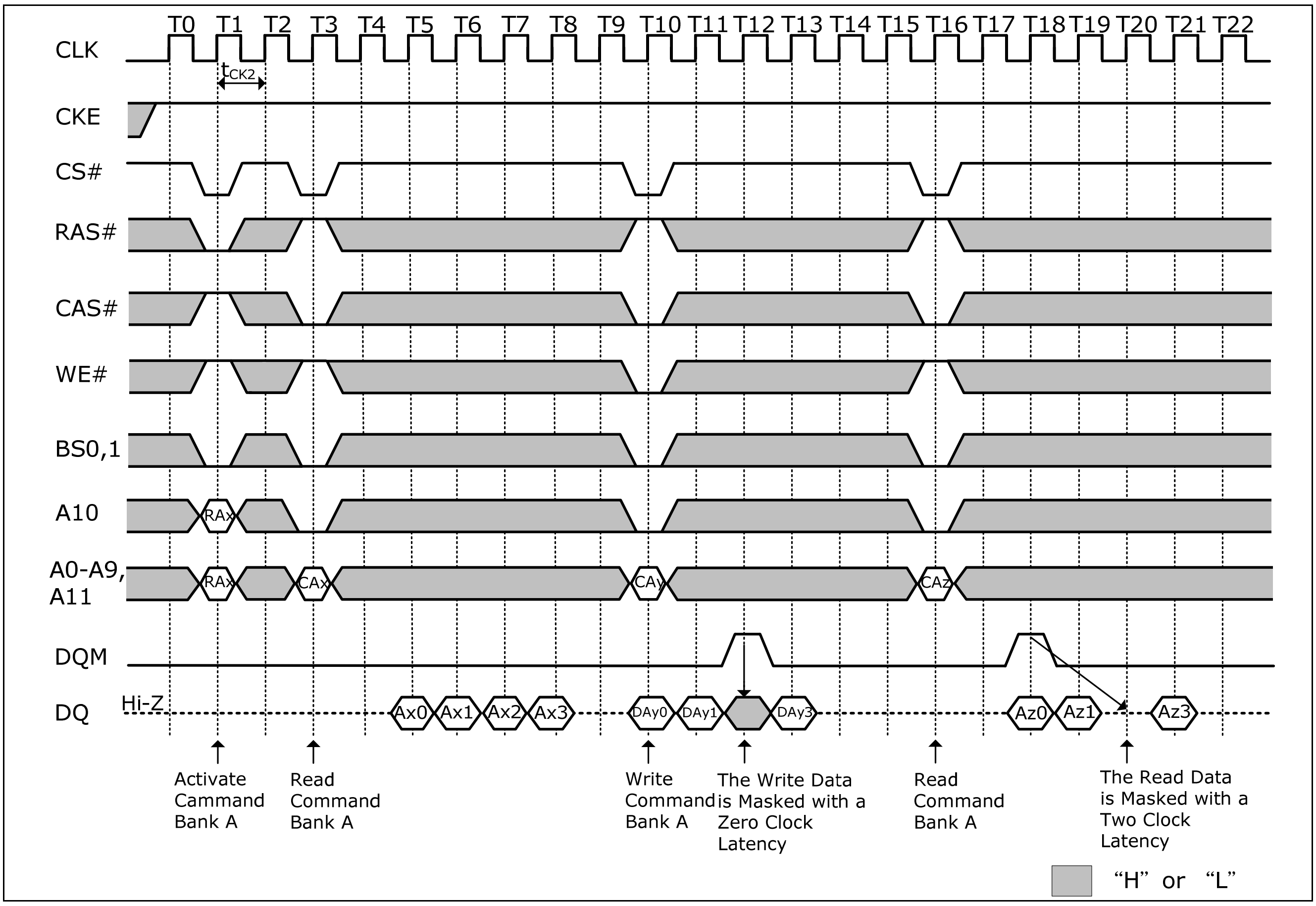


8.12.2. Burst Length=8, CAS# Latency=3

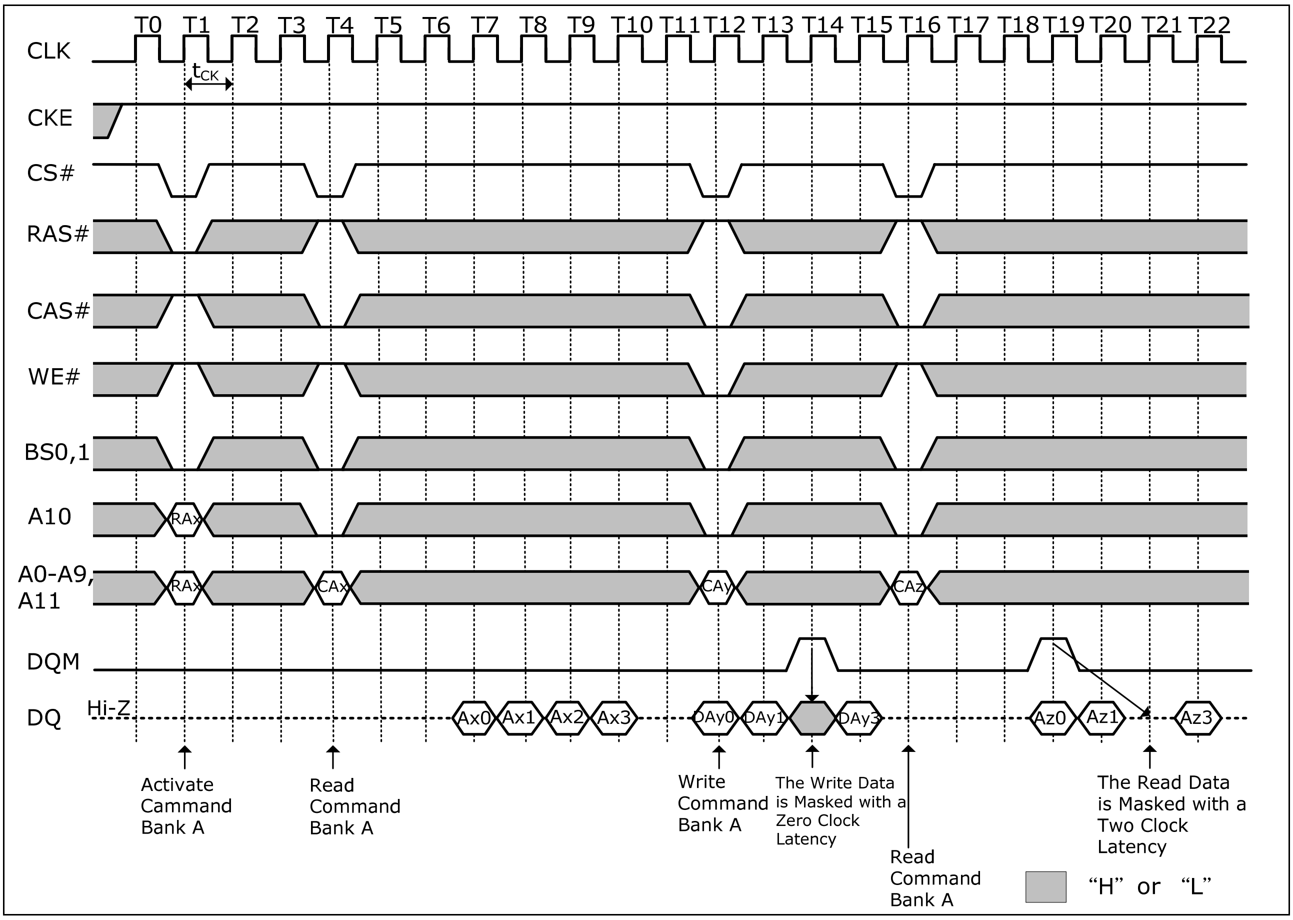


8.13. Read and Write Cycle

8.13.1. Burst Length=4, CAS# Latency=2

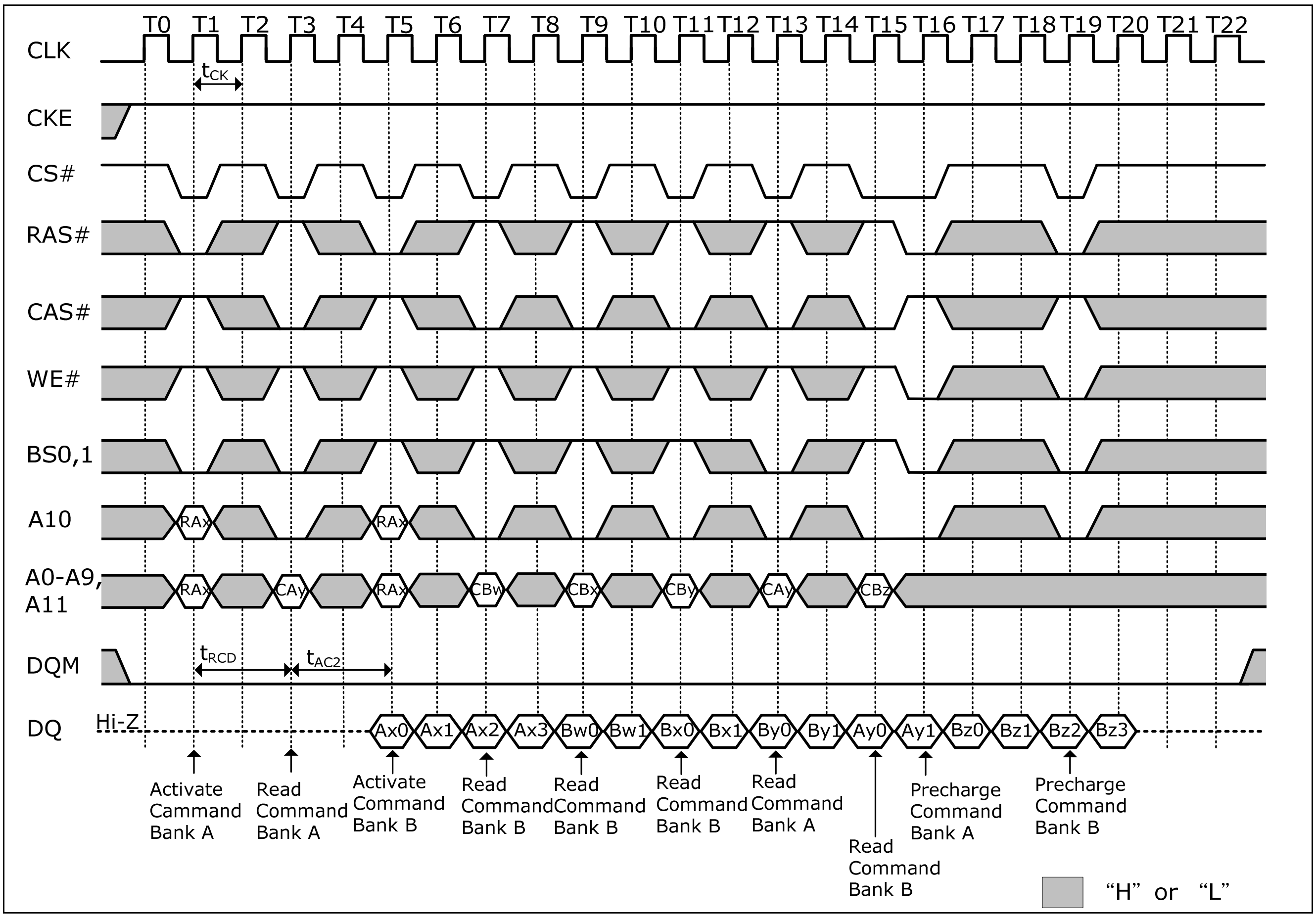


8.13.2. Burst Length=4, CAS# Latency=3

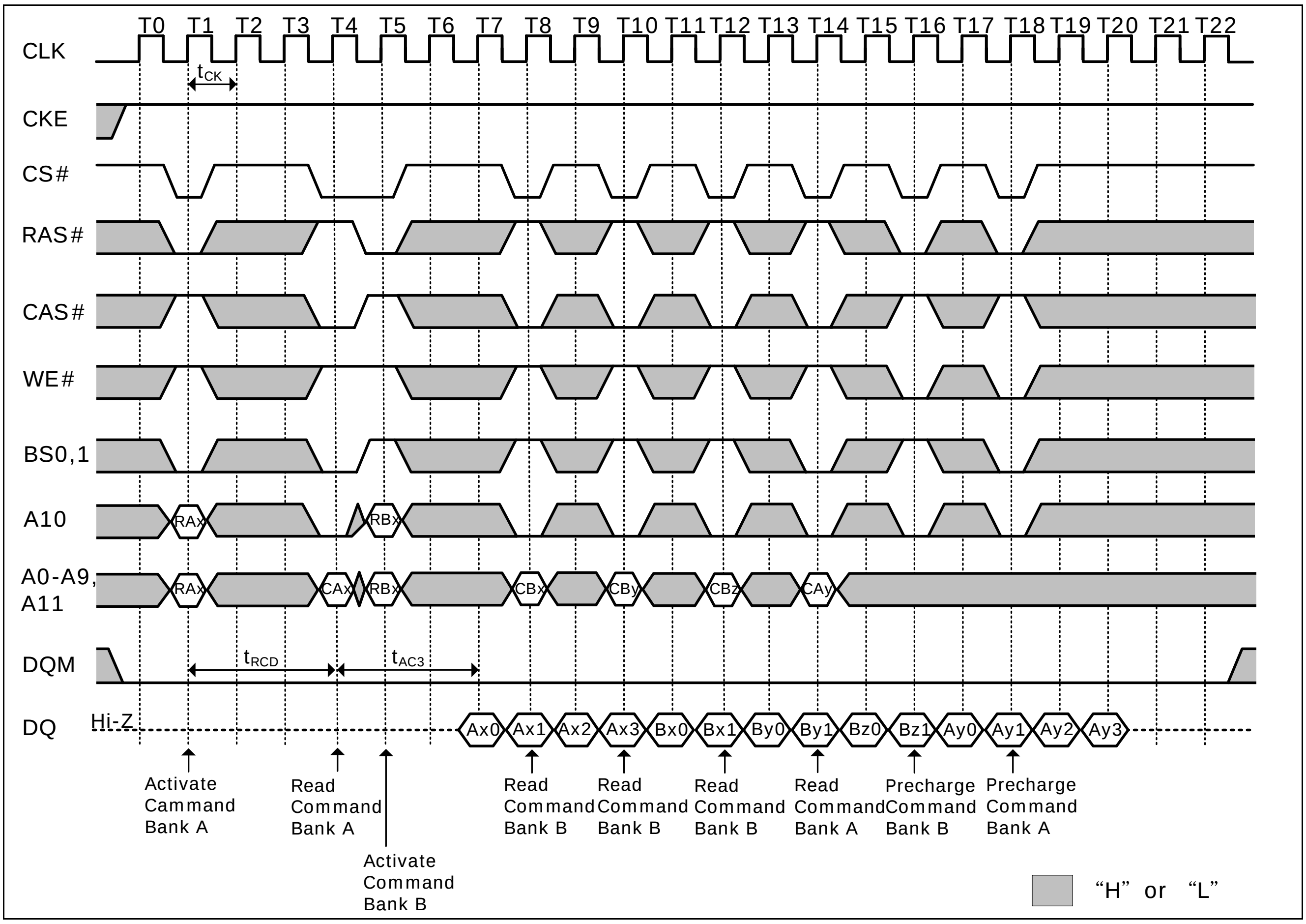


8.14. Interleaving Column Read Cycle

8.14.1. Burst Length=4, CAS# Latency=2

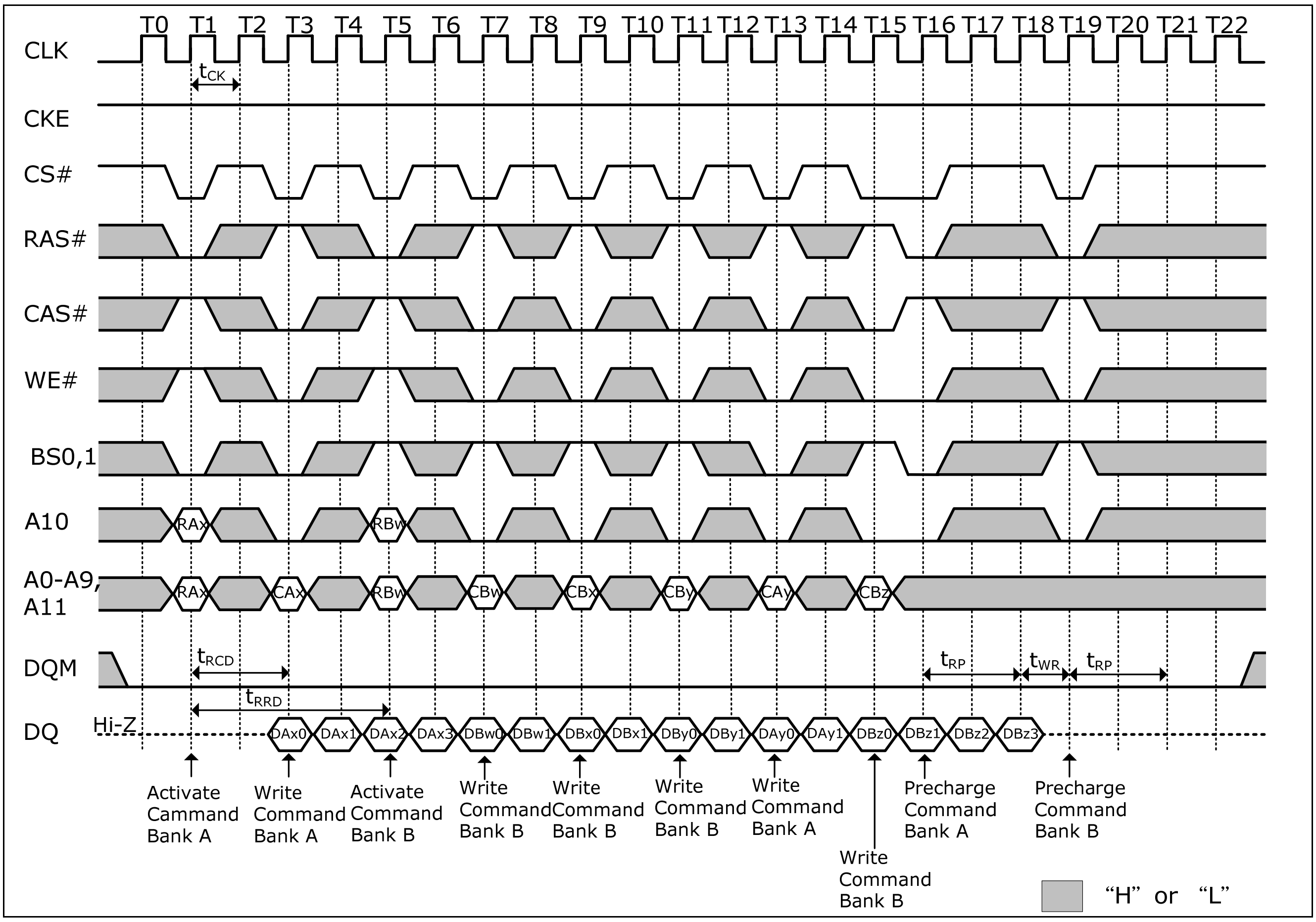


8.14.2. Burst Length=4, CAS# Latency=3

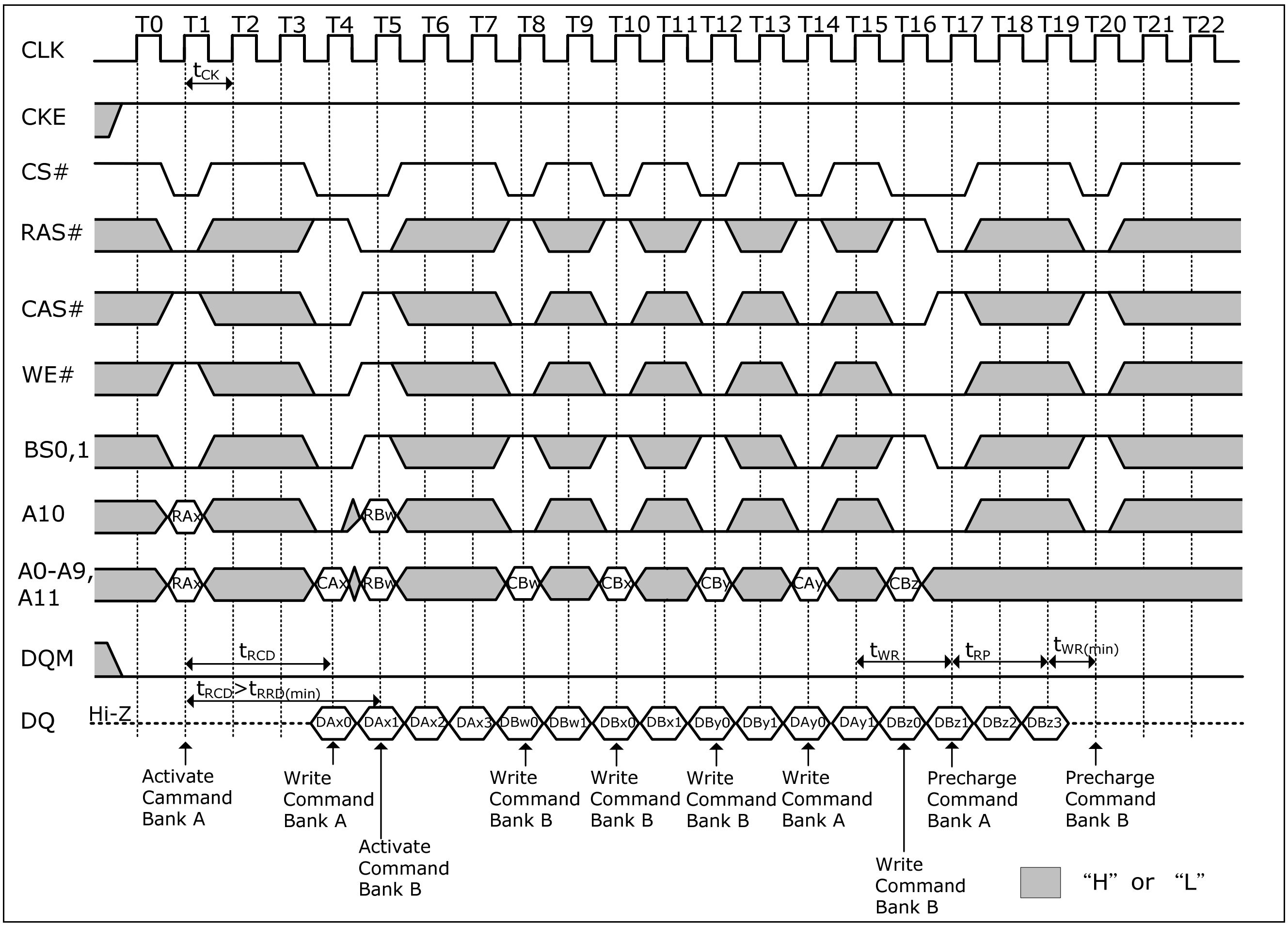


8.15. Interleaved Column Write Cycle

8.15.1. Burst Length=4, CAS# Latency=2

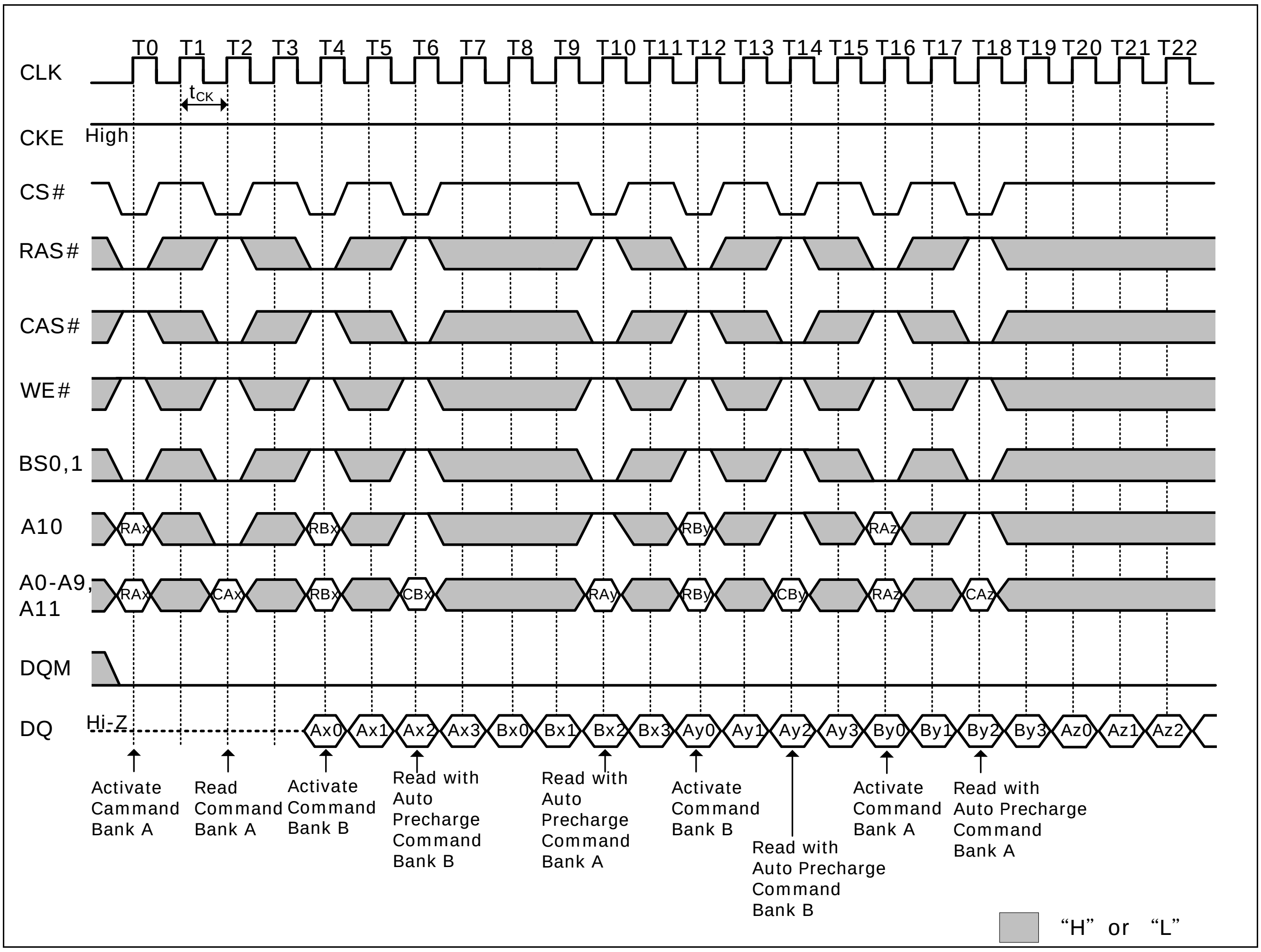


8.15.2. Burst Length=4, CAS# Latency=3

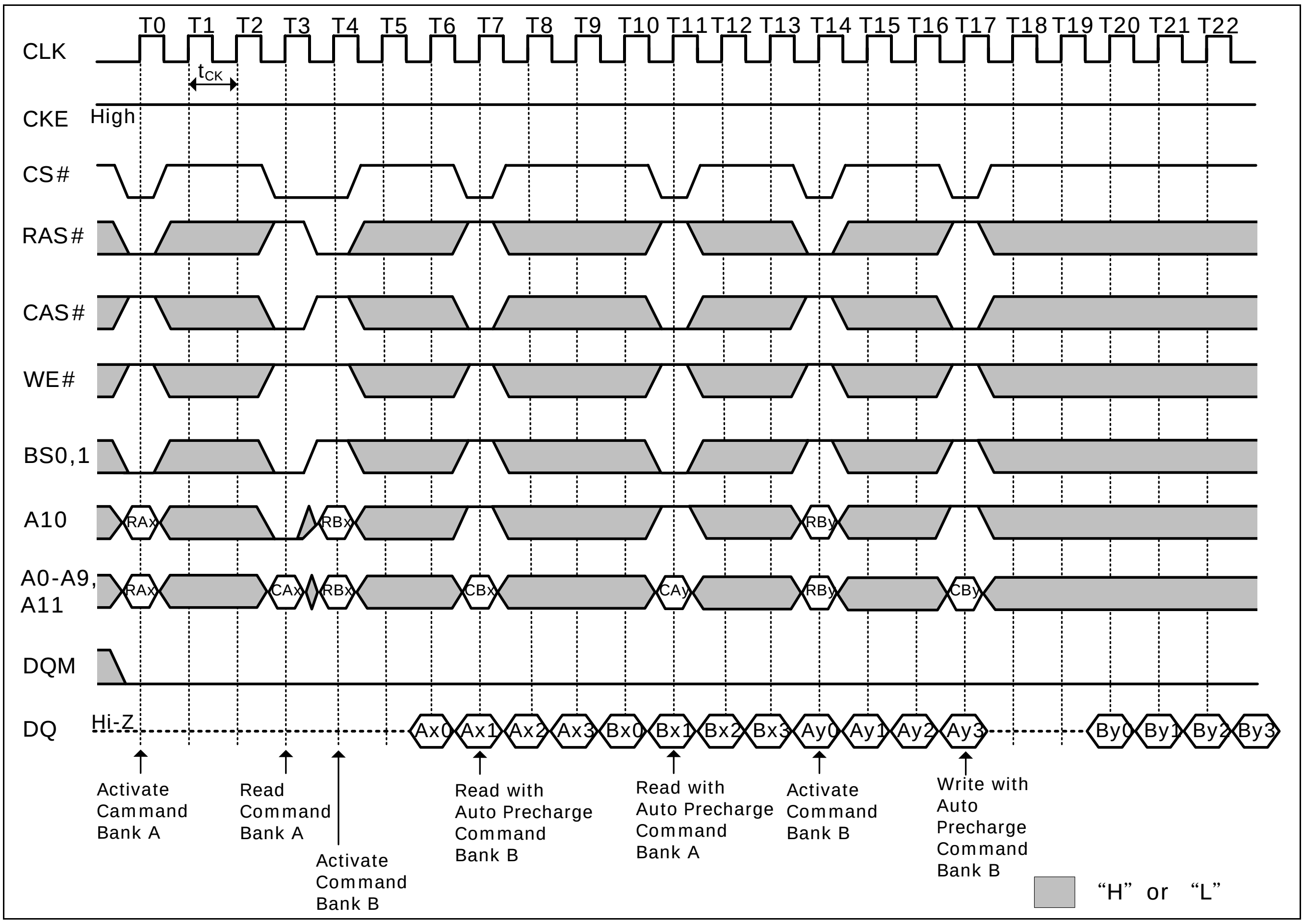


8.16. Auto Precharge after Read Burst

8.16.1. Burst Length=4, CAS# Latency=2

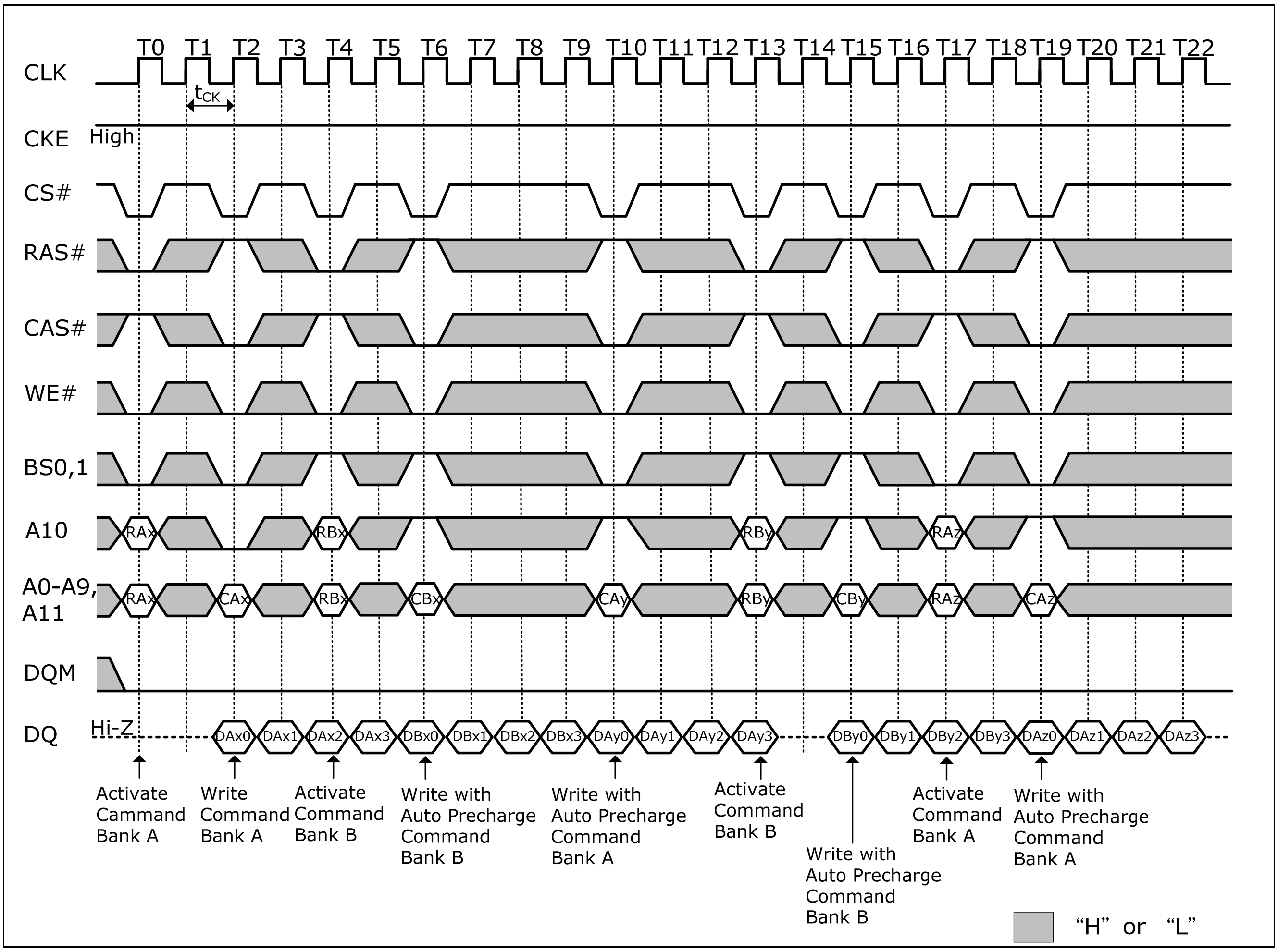


8.16.2. Burst Length=4, CAS# Latency=3

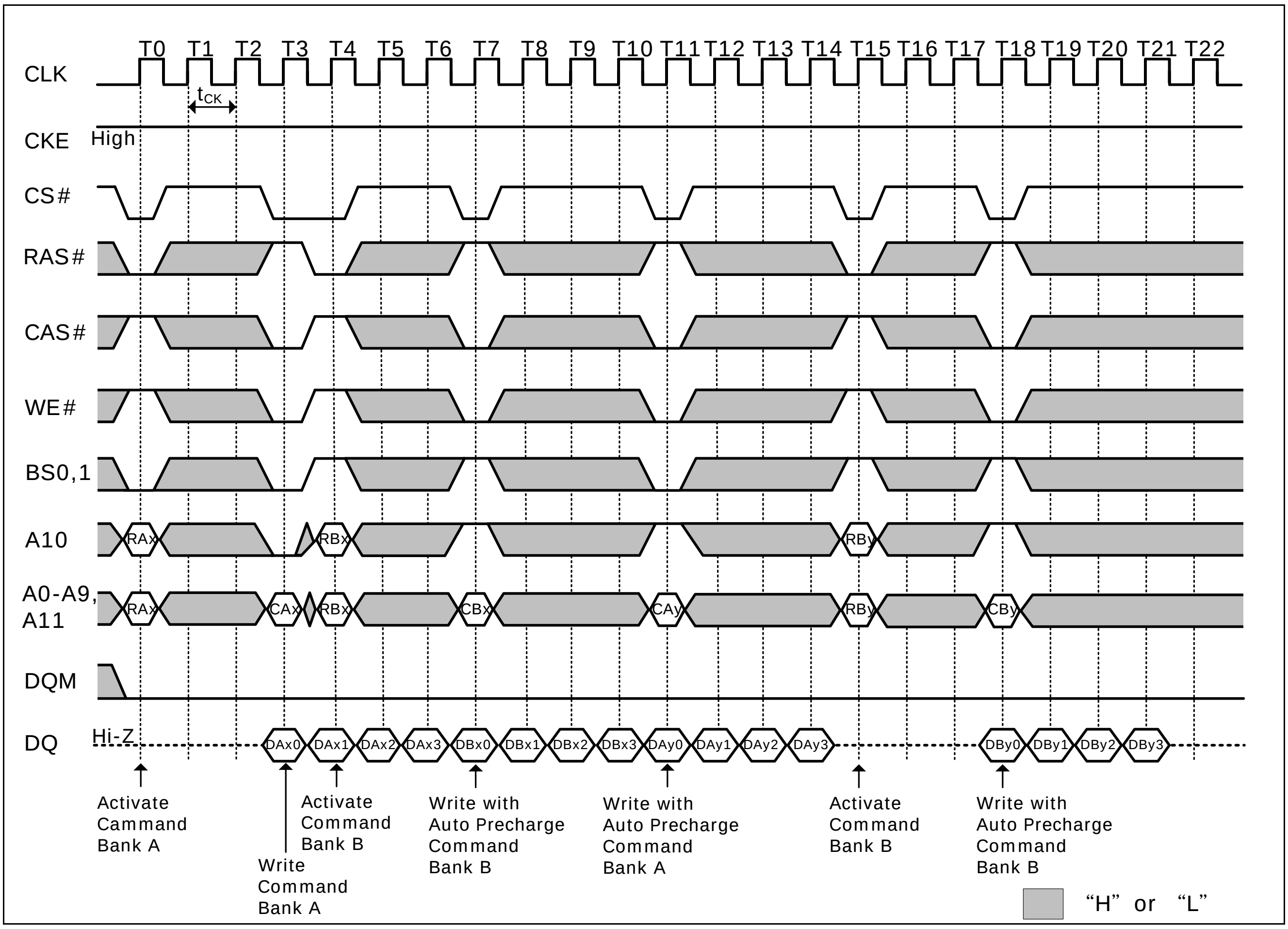


8.17. Auto Precharge after Write Burst

8.17.1. Burst Length=4, CAS# Latency=2

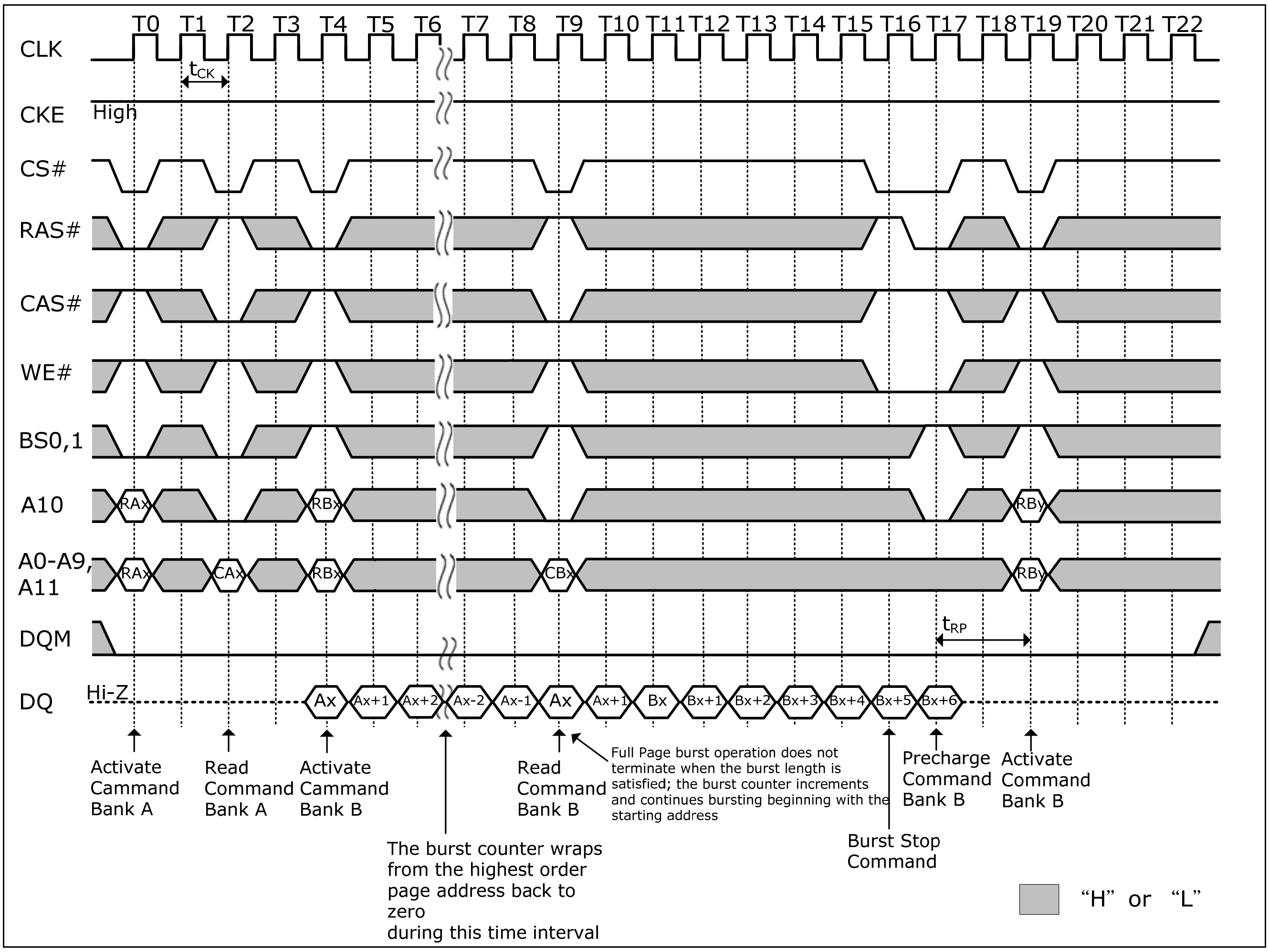


8.17.2. Burst Length=4, CAS# Latency=3



8.18. Full Page Read Cycle

8.18.1. Burst Length=Full Page, CAS# Latency=2



Activate Cammand Bank A

Read Command Bank A

Activate Cammand Bank B

The burst counter wraps from the highest order page address back to zero during this time interval

Read Command Bank B

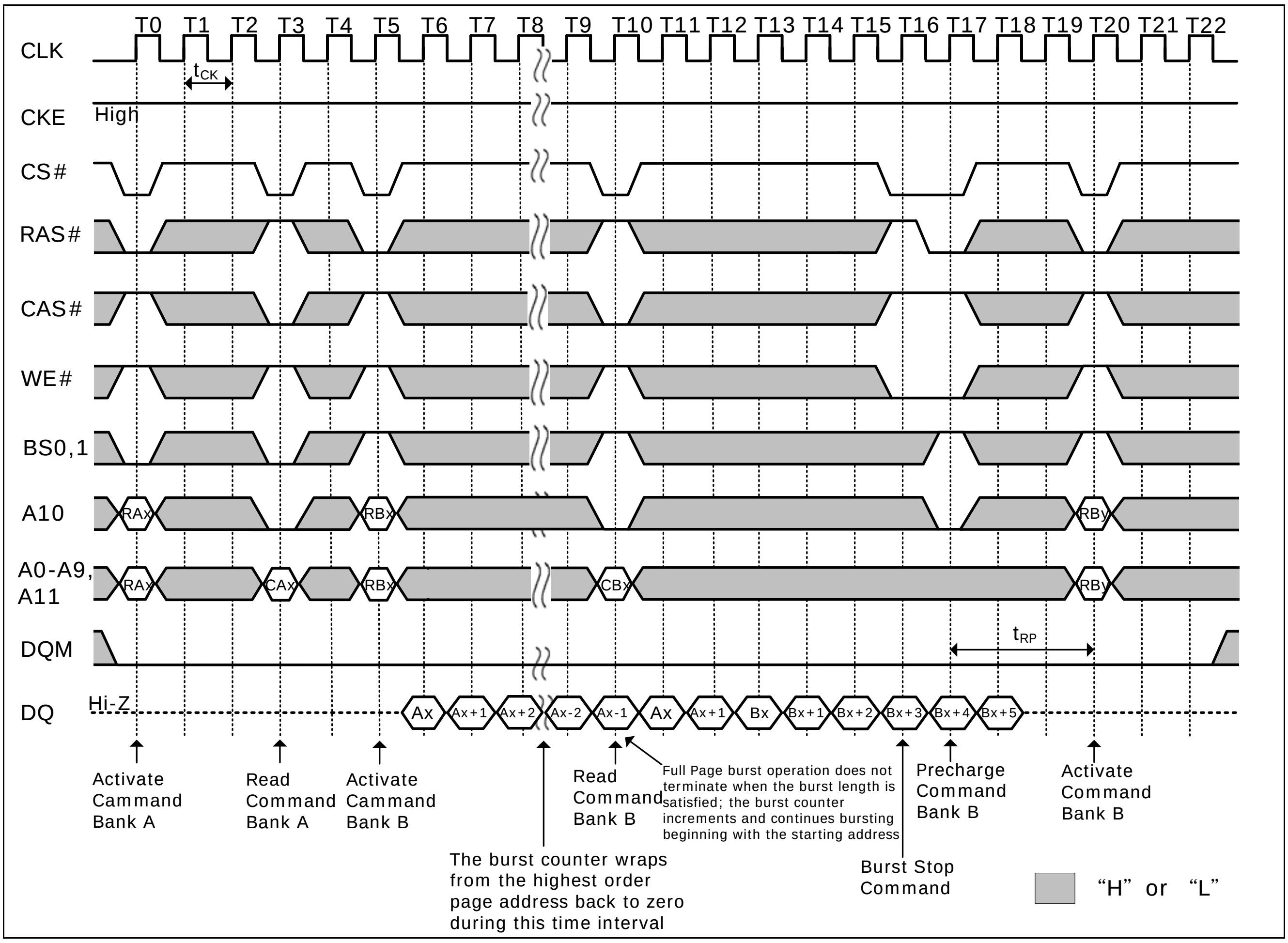
Full Page burst operation does not terminate when the burst length is satisfied; the burst counter increments and continues bursting beginning with the starting address

Burst Stop Command

Precharge Command Bank B

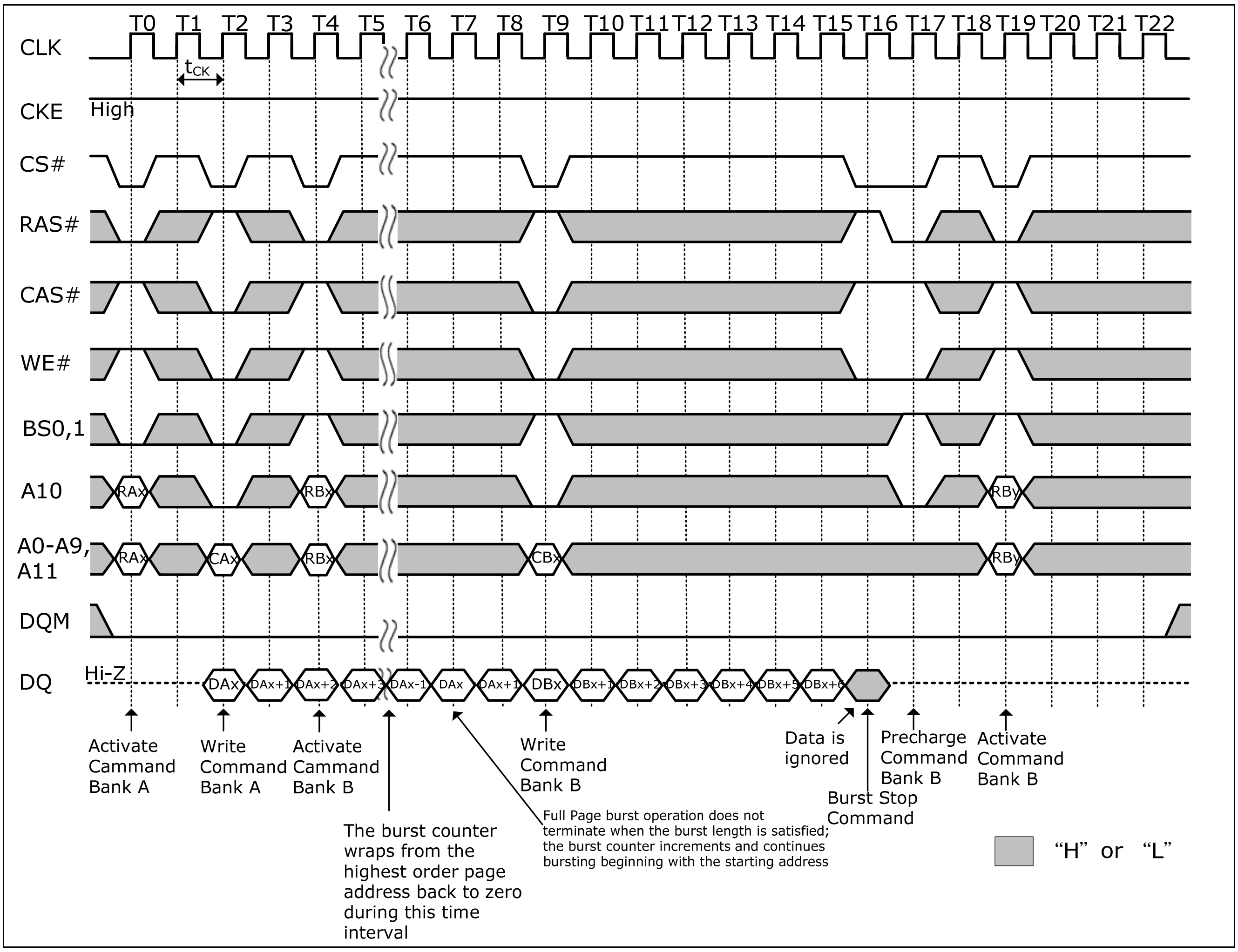
Activate Command Bank B

8.18.2. Burst Length=Full Page, CAS# Latency=3



8.19. Full Page Write Cycle

8.19.1. Burst Length=Full Page, CAS# Latency=2



Activate Cammand Bank A

Write Command Bank A

Activate Cammand Bank B

The burst counter wraps from the highest order page address back to zero during this time interval

Write Command Bank B

Full Page burst operation does not terminate when the burst length is satisfied; the burst counter increments and continues bursting beginning with the starting address

Data is ignored

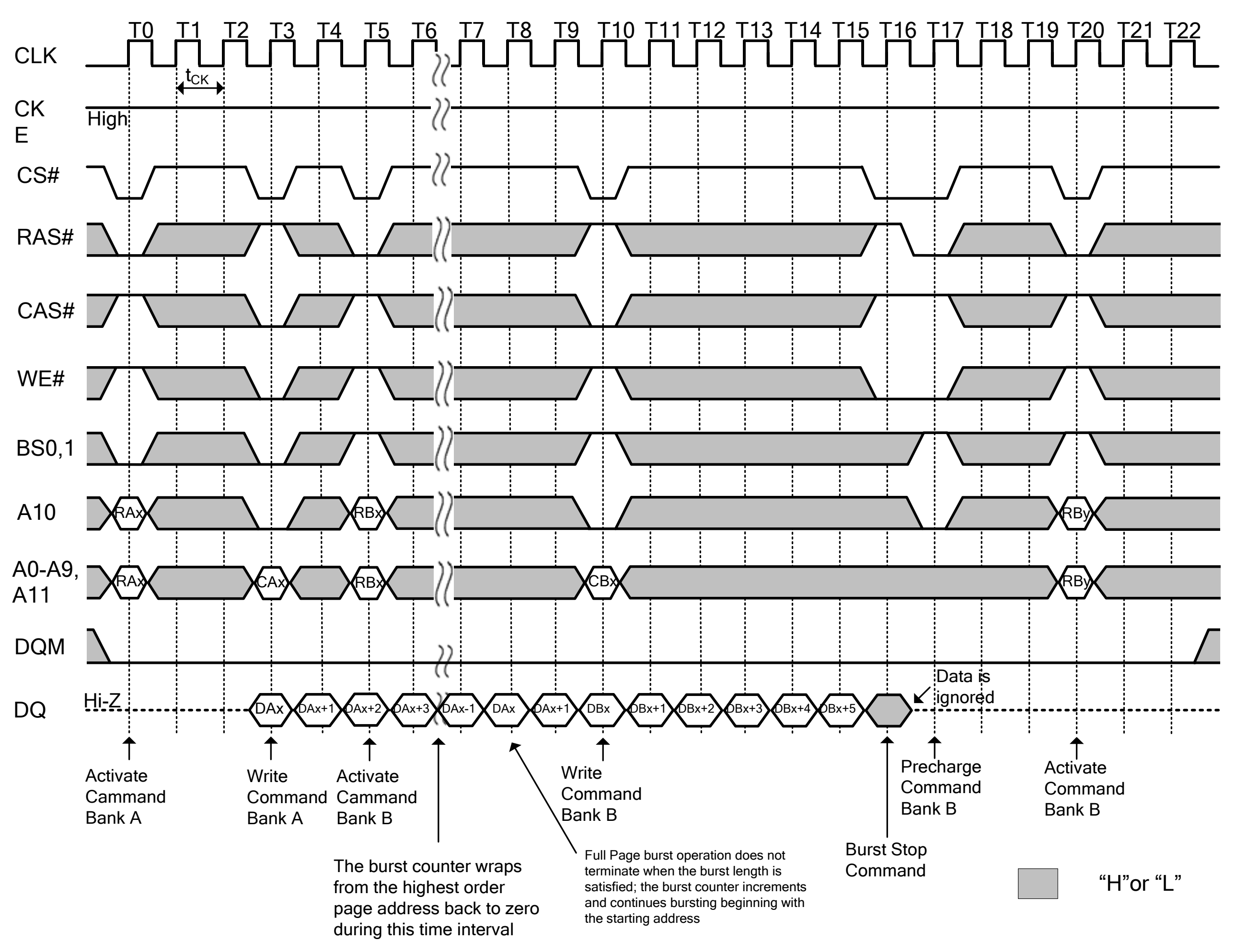
Burst Stop Command

Precharge Command Bank B

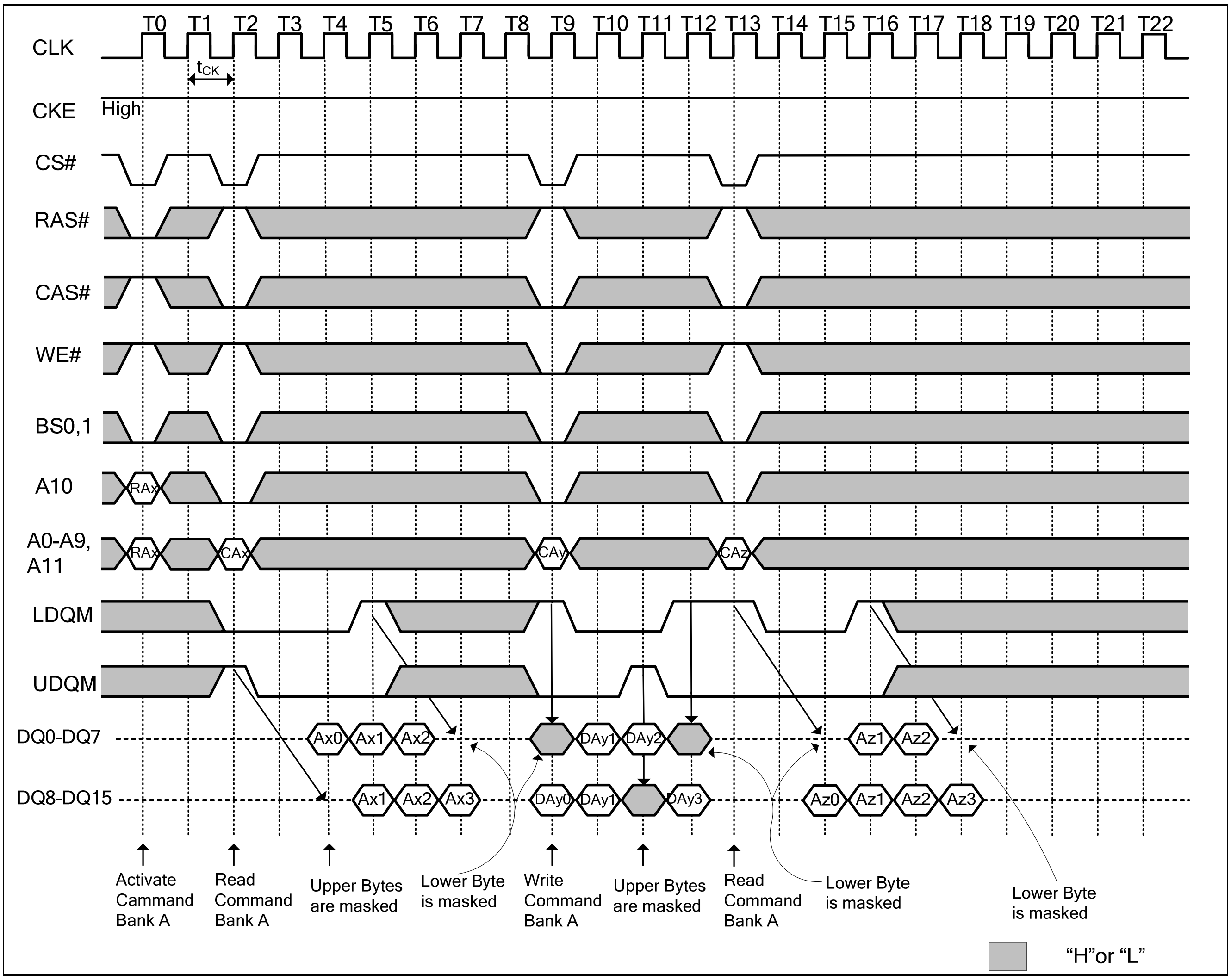
Activate Command Bank B

▨ “H” or “L”

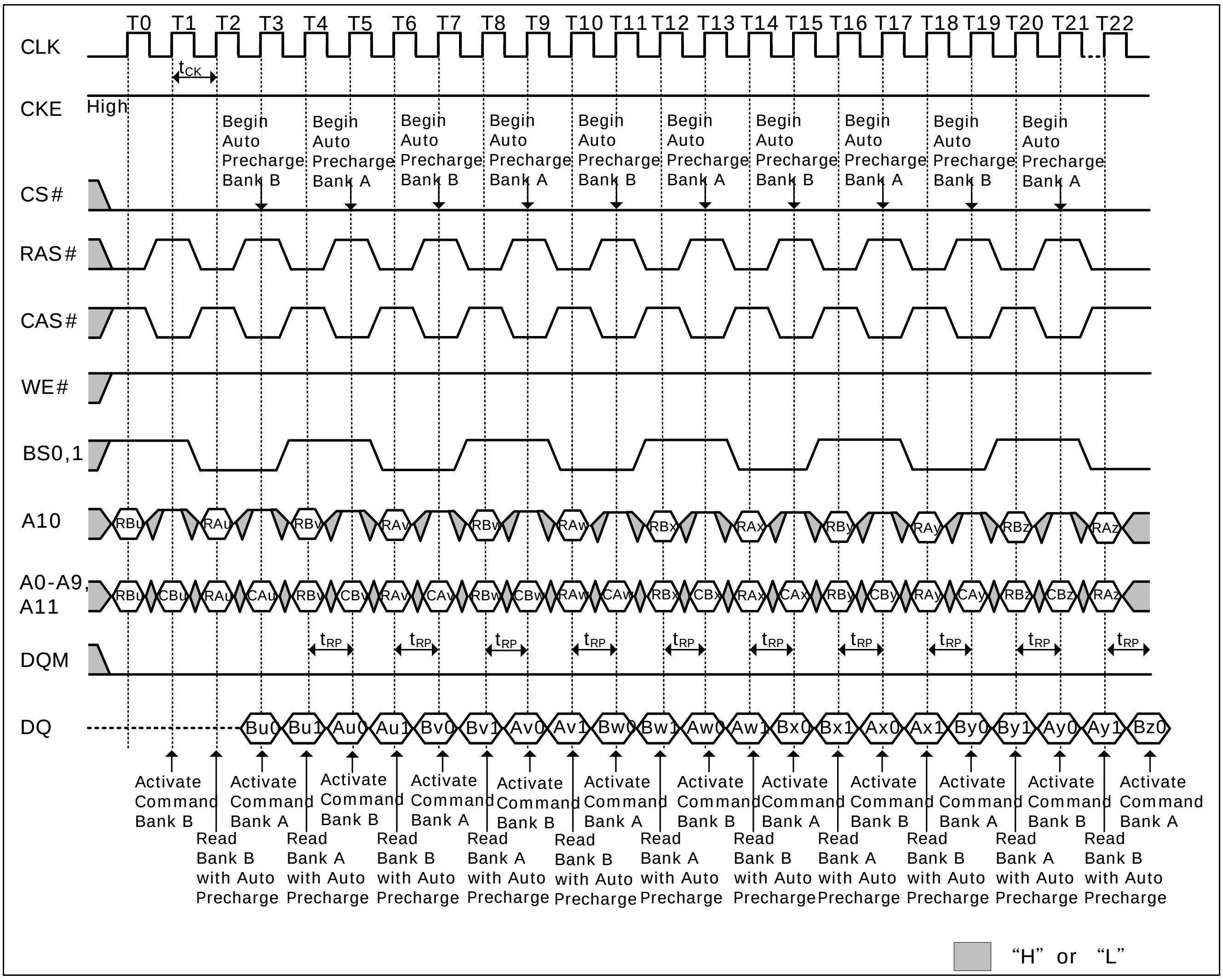
8.19.2. Burst Length=Full Page, CAS# Latency=3



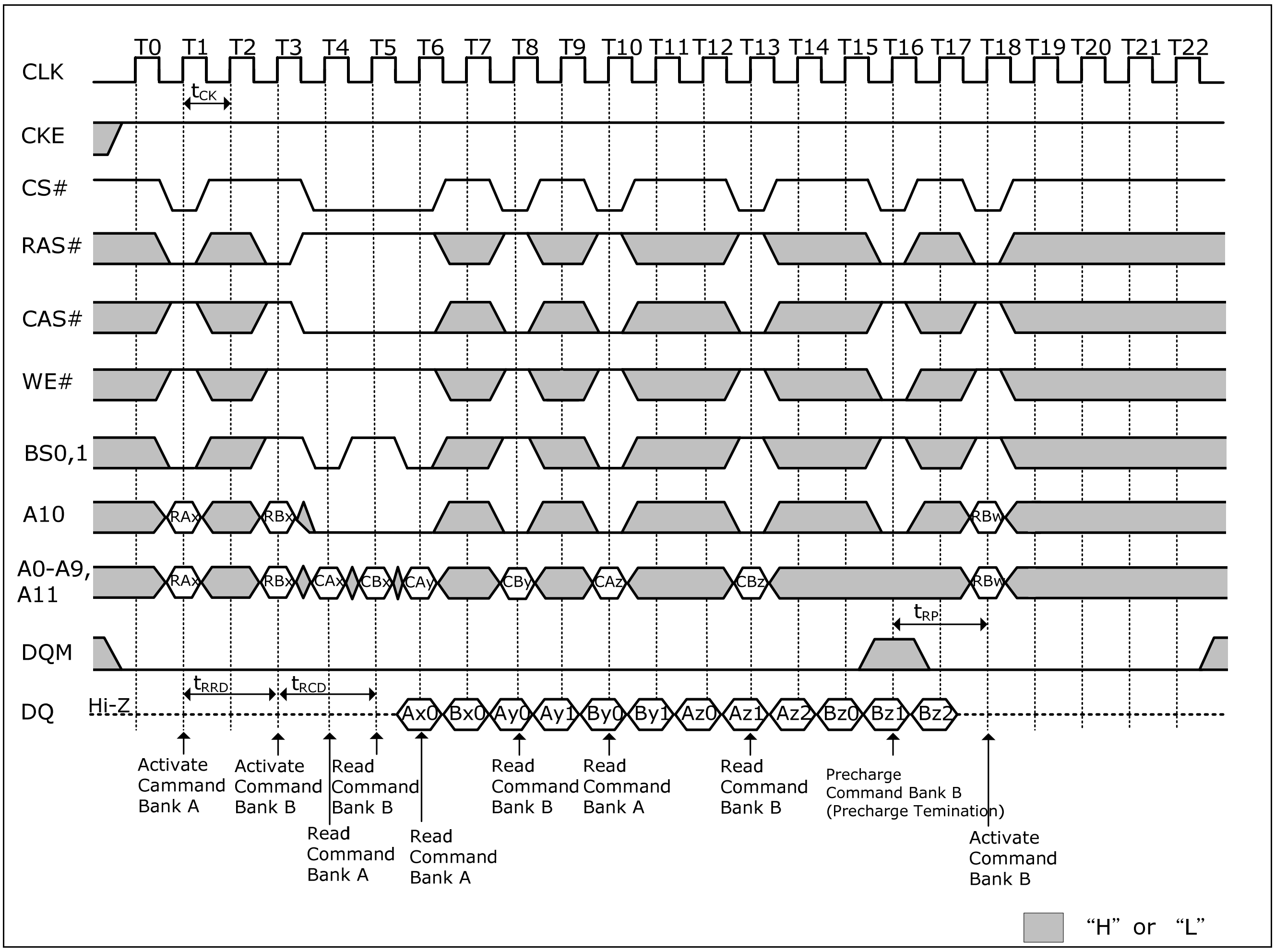
8.20. Byte Write Operation (Burst Length=4)



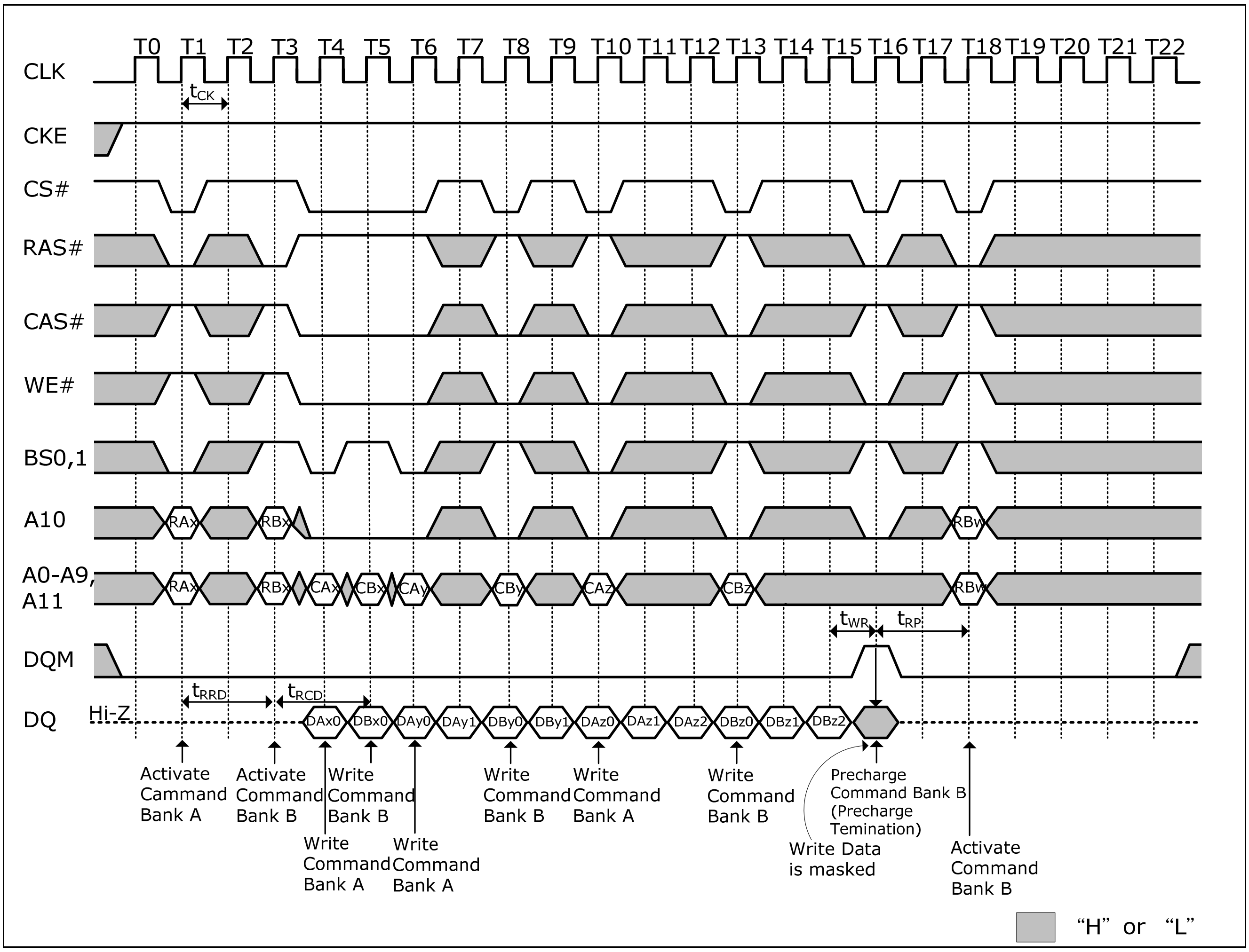
8.21. Random Row Read (Interleaving Banks)(Burst Length=2, CAS# Latency=2)



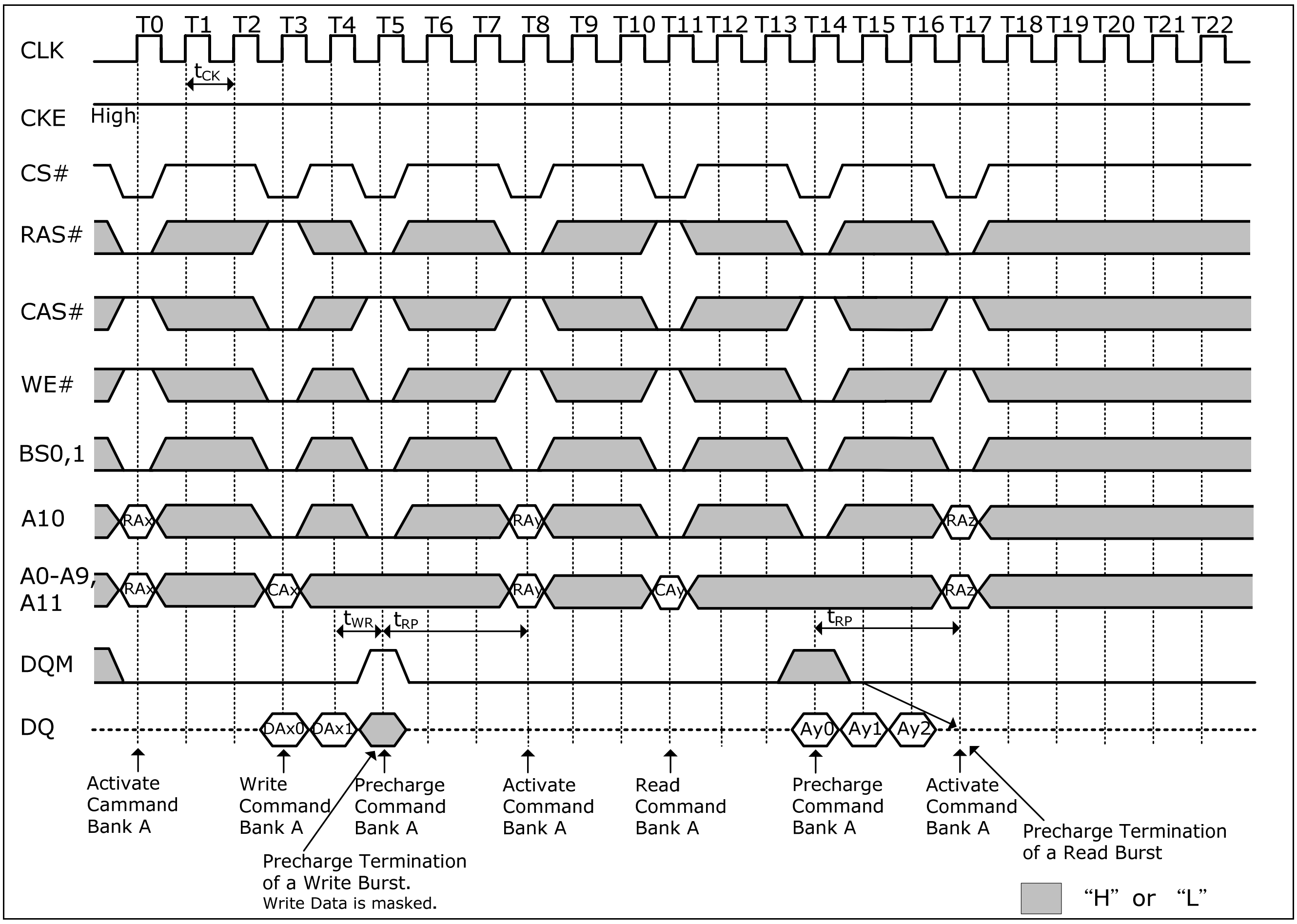
8.22. Full Page Random Column Read (Burst Length=Full Page, CAS# Latency=2)



8.23. Full Page Random Column Write (Burst Length=Full Page, CAS# Latency=2)



8.24. Precharge Termination of a Burst(Burst Length=4, 8 or Full Page, CAS# Latency=3)



9. PACKAGE/ORDERING INFORMATION

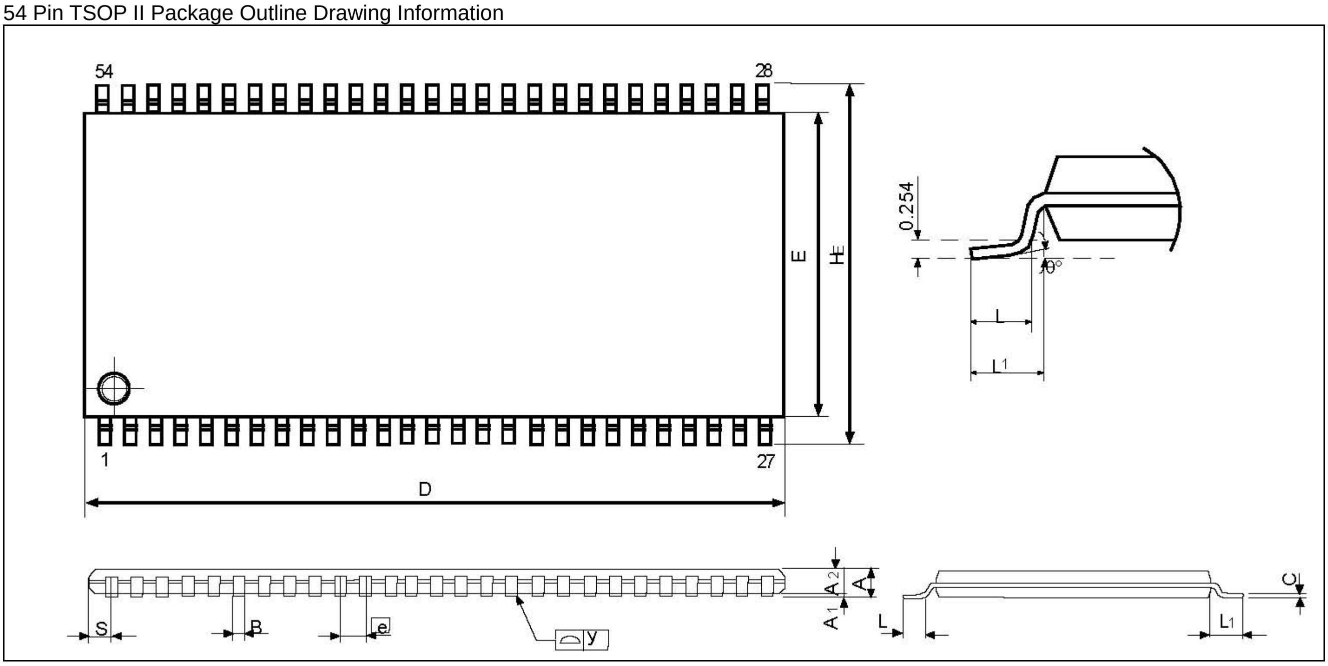
9.1. Ordering Information

Product Number	Package Type
GPR323816A - QA09x	Halogen Free Package

Note1: Package form number (x = 1 - 9, serial number).

9.2. Package Information

54 Pin TSOP II Package Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	---	---	0.047	---	---	1.2
A1	0.002	---	0.008	0.05	---	0.2
A2	0.035	0.039	0.043	0.9	1.0	1.1
B	0.01	0.014	0.018	0.25	0.35	0.45
C	0.004	0.006	0.008	0.12	0.165	0.21
D	0.87	0.875	0.88	22.09	22.22	22.35
E	0.395	0.400	0.405	10.03	10.16	10.29
e	---	0.031	---	---	0.8	---
HE	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.02	0.024	0.4	0.5	0.6
L1		0.032	---	---	0.84	---
S	---	0.028	---	---	0.71	---
y	---	---	0.004	---	---	0.1
θ	0°	---	8°	0°	---	8°

Notes:

1. Dimension D&E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Dimension S includes end flash.
4. Controlling dimension : mm

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
OCT. 08, 2008	1.0	Original	57