LANGUAGE REPEATER

1. GENERAL DESCRIPTION

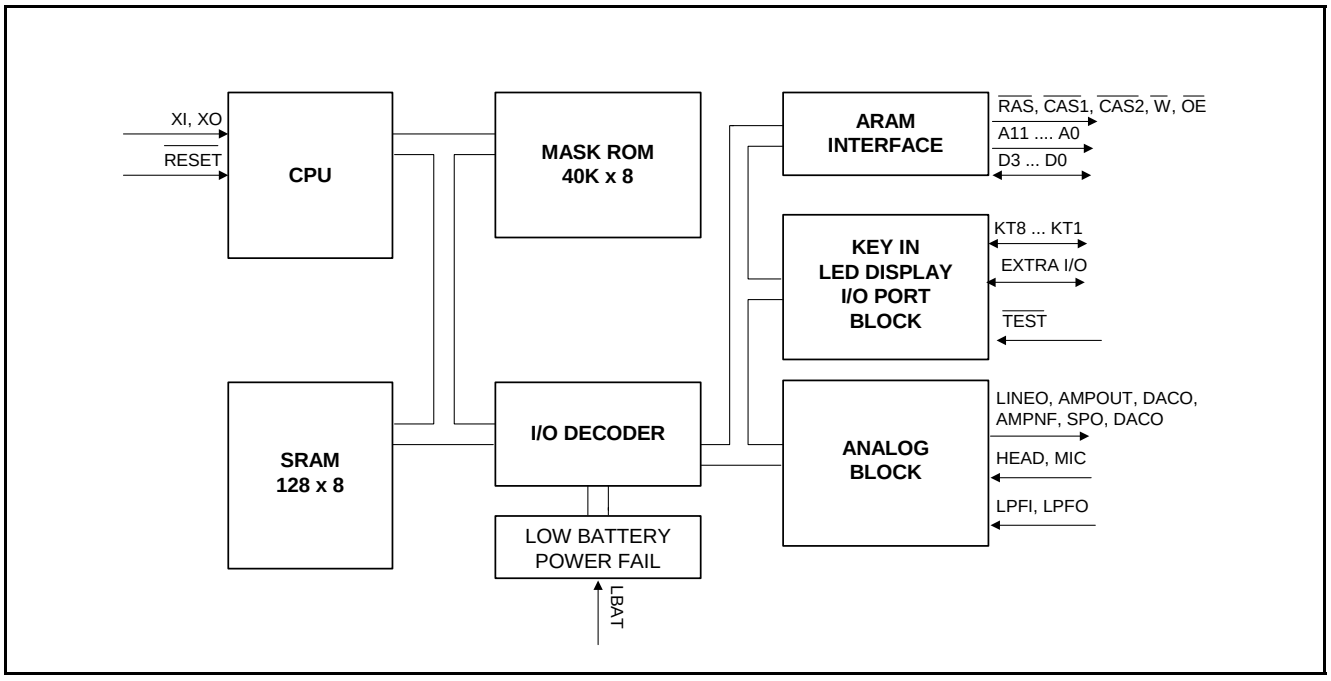
The GPRT5507A integrates an 8-bit CPU, speech generator, segment LED driver, analog switches, programmable attenuator and a gain amplifier into one chip. The GPRT5507A includes a 40K-byte ROM, 128-byte working SRAM, 4 edge-mode interrupts and a fixed time based generator (F_{CPU}/1024)*. This chip which incorporated with 1 or 2 pieces of 4M X 4 ARAM, can be applied to the versatile audio field, such as a language repeater.

*F_{CPU}: CPU clock

2. FEATURES

- 8-bit microprocessor
- Provide 40K x 8 ROM area for program and audio data
- 128 x 8 working SRAM
- Embedded LPF, ADC, DAC for analog processing
- Provide controlled DRAM interfaces
- 4 Interrupt sources
- Built in watch dog timer
- ROSC. or Crystal OSC. selections
- Provide low battery detector
- Provide power down mode

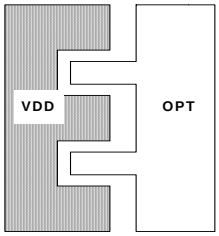
3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
XI	44	I	Crystal OSC Input or ROSC tuning resistor, connected to AVDD
XO	45	O	Crystal OSC Output
OPT	46	I	OSC type selector. '0' or open for X'TAL, '1' for ROSC
$\overline{\text{RESET}}$	59	I	System reset, active low
KT8 - 1	67 - 60	I/O	LED segment driver, Open Drain NMOS output, and Key input (8- 1), TTL and CMOS compatible Input.
A2 - 0 A8 - 3 A11 - 9	71 - 69 84 - 79 3 - 1	O	ARAM Address A11 - 0
D3 - 0	7 - 4	I/O	ARAM Data D3 - 0
$\overline{\text{W}}$	16	O	ARAM Write Enable
$\overline{\text{OE}}$	17	O	ARAM Output Enable
$\overline{\text{RAS}}$	18	O	ARAM ROW Address Strobe
$\overline{\text{CAS1}}$	19	O	ARAM1 Column Address Strobe
$\overline{\text{CAS2}}$	20	O	ARAM2 Column Address Strobe
DACO	23	O	DAC Output
LPFI	24	I	Low Pass Filter Input
LPFO	25	O	Low Pass Filter Output
LBAT	26	I	Low Battery detector Input
AMPOUT	27	O	Gain Amplifier Output
SPO	37	O	Signal Output, goes to speaker amplifier
AMPNF	38	I	Gain Amplifier Input
VREF	39	O	Voltage Reference Output
MIC	40	I	Input signal, comes from microphone
HEAD	41	I	Input signal, comes from magnetic head of tape
$\overline{\text{TEST}}$	42	I	IC test pin, Active Low
EXIO1	58	I/O	Extra I/O port 1
EXIO2	49	I/O	Extra I/O port 2
EXIO3	48	I/O	Extra I/O port 3
EXIO4	47	I/O	Extra I/O port 4
VDD	68	P	Logic power
VSS	21, 43	G	Logic ground
AVDD	22	P	Analog power
AVSS	28	G	Analog ground

* OPT is the selection pin for ROSC or X'TAL. When ROSC is selected, OPT is connected to VDD and if X'TAL is selected, OPT is floating or connected to GND. The PCB layout that looks like in the right figure is proper. This will make it easier for OSC type change.



5. FUNCTIONAL DESCRIPTIONS

The GPRT5507A is a CMOS; low cost, audio processor that can operate with a supply rang from 4.0V to 5.5V. The GPRT5507A has mainly an 8-bit CPU, 128B SRAM, 40KB ROM, several I/O ports and an analog processor. The address map of memory and I/O ports please refer to the programming guide. The analog processor is described in detail in next section.

5.1. Clock Source Selection

There are two options for clock sources. When OPT pin is open or connected to VSS, the crystal oscillator is selected. If the OPT pin connects to VDD, the less accurate R-oscillator is selected. The clock frequency of ROSC depends on the resistor connected between XI and AVDD. The recommended value is 30K Ohms for 3.58MHz and 16K Ohms for 6 MHz respectively.

5.2. Linear Block Description

There are four major parts in the linear block including signal switches, gain amplifier, DAC converter and low pass filter. In recording mode, signal switches select desired inputs and turn on sample and hold circuits. Gain amplifier amplifies the selected signal, and provides flexible gain–adjustment by external resisters and capacitors. A/D converter, which uses SAR algorithm based on CPU converts the amplified signal to digital signal, than store those digital data into ARAM. In playing back mode, D/A converter converts digital signals, which comes from ARAM to analog signal. Following that DAC, low-pass filter with external resistors and capacitors is used to smooth the DAC output waveform.

Note: Heretofore, the above are just hardware descriptions. Please refer to user programming guides for the detail information.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	-10 ^{0}C to +60 ^{0}C
Storage Temperature	T_{STO}	-50 ^{0}C to +150 ^{0}C

Note: Stresses beyond those given in the Absolute Maximum Ratings table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

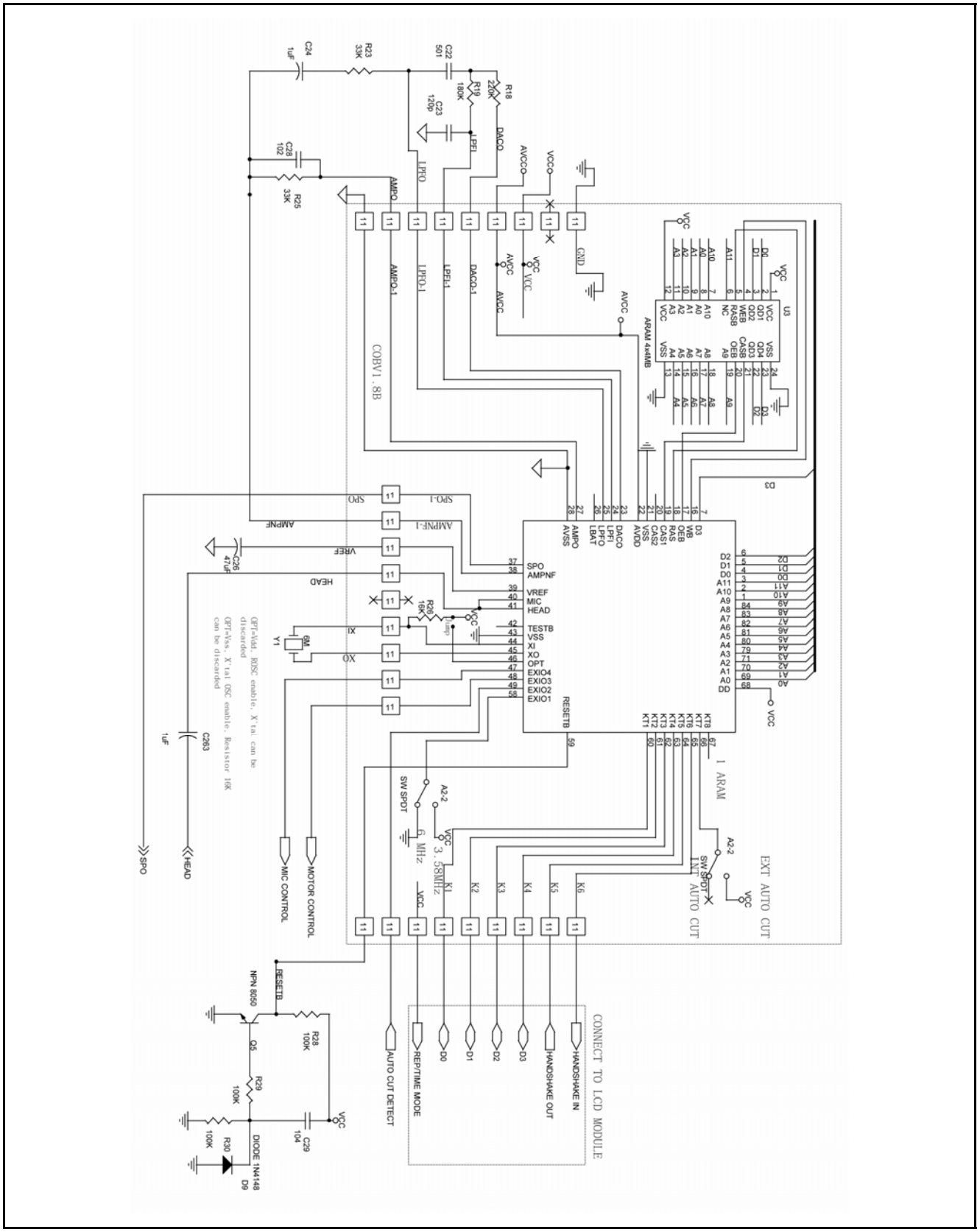
6.2. DC Characteristics (VDD = 5.0V; T_{AMB} = 25℃, CPU clock = 3.58MHz)

Characteristics	Symbol	Limit			Unit	Test Conditions
		Min.	Typ.	Max.		
Input Voltage *1	V_{IL}	-	-	0.4	V	-
	V_{IH}	2.4	-	-		
Input Voltage *2	V_{IL}	-	-	0.8	V	-
	V_{IH}	4.0	-	-		
Output Voltage *3	V_{OL}	-	-	0.8	V	I_{OUT} = 8mA
Output Voltage *4	V_{OL}	-	-	0.4	V	I_{OUT} = 0.1mA
	V_{OH}	4.0	-	-		I_{OUT} = -0.1mA
Operating Voltage	VDD	4.5	5.0	5.5	V	-
DAC full scale voltage	V_{FS}	-	1.5	-	V	Peak to peak value
Operating Current	I_{OP}	-	15	-	mA	Chip goes into recording mode
Standby Current	I_{STABY}	-	4.0	-	mA	Chip goes into backup mode

Note*1: KT8 - 1, TTL and CMOS compatible input
Note*2: Other Logic Pins, CMOS input
Note*3: KT8 - 1, Open NMOS drain output
Note*4: Other Logic Pins, CMOS output

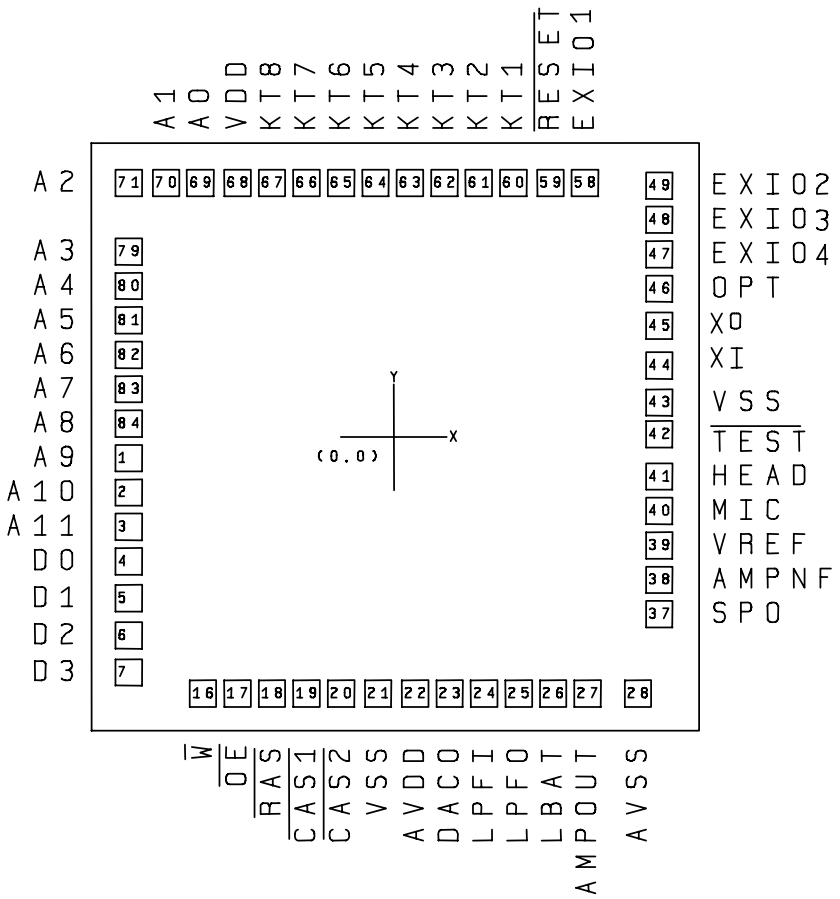
7. APPLICATION CIRCUIT

7.1. LCD Language Repeater Application Circuit



8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

8.2. Ordering Information

Product Number	Package Type
GPRT5507A-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

8.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	A9	-1000	-76	44	XI	993	274
2	A10	-1000	-206	45	XO	993	417
3	A11	-1000	-336	46	OPT	993	558
4	D0	-1000	-468	47	EXIO4	993	688
5	D1	-1000	-608	48	EXIO3	993	818
6	D2	-1000	-748	49	EXIO2	993	948
7	D3	-1000	-888	58	EXIO1	720	962
16	$\overline{W}$	-726	-965	59	$\overline{RESET}$	585	962
17	$\overline{OE}$	-596	-965	60	KT1	450	962
18	$\overline{RAS}$	-466	-965	61	KT2	320	962
19	$\overline{CAS1}$	-336	-965	62	KT3	190	962
20	$\overline{CAS2}$	-206	-965	63	KT4	60	962
21	VSS	-63	-965	64	KT5	-70	962
22	AVDD	79	-965	65	KT6	-200	962
23	DACO	209	-965	66	KT7	-330	962
24	LPFI	339	-965	67	KT8	-460	962
25	LPFO	469	-965	68	VDD	-595	962
26	LBAT	599	-965	69	A0	-730	962
27	AMPOUT	729	-965	70	A1	-865	962
28	AVSS	916	-965	71	A2	-1000	962
37	SPO	993	-673	79	A3	-1000	704
38	AMPNF	993	-543	80	A4	-1000	574
39	VREF	993	-413	81	A5	-1000	444
40	MIC	993	-283	82	A6	-1000	314
41	HEAD	993	-153	83	A7	-1000	184
42	$\overline{TEST}$	993	7	84	A8	-1000	54
43	VSS	993	132				

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
MAR. 04, 2005	1.1	Remove chip size.	6
MAY. 24, 2004	1.0	First Edition Note: The GPRT5507A data sheet v1.0 is a continued version of SPT5507A data sheet v1.1.	9