DATA SHEET

GPT1000A

General Touch Sensor Controller

APR. 30, 2012

Version 1.1

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GENERAL TOUCH SENSOR CONTROLLER

1. GENERAL DESCRIPTION

The GPT1000A, a general purpose touch sensor controller, equips an 8-bit CMOS microprocessor, 8K-byte embedded flash, and 256-byte working SRAM. It allows the control of 24 IOs configurable as capacitive sensing buttons or GPIOs. Moreover, three PWMs are built-in to support hardware LED control with hold and dimming function. The PWM can output to IOB or IOC individually to produce fancy LED effect with simple program. To communicate with host devices, the GPT1000A equips SPI or I2C interfaces. The GPT1000A operates at a wide voltage range of 2.6V – 5.5V. The maximum CPU frequency runs up to 8MHz. Sleep mode and halt mode are also provided to optimize system performance and power consumption. The In-Circuit Emulation (ICE) function is built-in with on-chip re-programmable non-volatile memory.

2. FEATURES

- 8-bit microprocessor with ICE function
  - Embedded flash 8K bytes
  - SRAM 256 bytes
- Clock
  - Built-in 8MHz ROSC
  - Built-in 30KHz ROSC for time-base function
  - /1, /2, /4, /8, /16, /32 of 8MHz clock output for CPU
- Operating Voltage: 2.6V ~ 5.5V
- Industrial Temperature Range: -40℃ ~ 85℃
- Operation Modes
  - Operating mode, Sleep mode, and Halt mode
- Timer/Counter
  - 8-bit timers with selective clock sources
  - Programmable auto sleep timer
- Power management for system reliability
  - Low-Voltage-Reset function
  - Power-On-Reset function
  - Watchdog reset (derived from 30KHz clock)
- Eight Interrupt / Wakeup sources (INT / WP)
  - Timer overflow
  - Counter
  - IOA[7:0], IOB[7:0], IOC[7:0] key-changed
  - Serial interface interrupt
  - Sensor counter interrupt
  - External interrupt
- Up to 24 I/Os
  - IOA[7:0]:programmable as GPIO/Wakeup-able IO/external INT
  - IOB[7:0]:programmable as GPIO/Wakeup-able IO/PWM output
  - IOC[7:0]:programmable as GPIO/Wakeup-able IO/PWM output
- Capacitive sensors
  - Supports max. 24 capacitive sensor I/Os of individual keys.
  - Built-in auto sleep/wakeup function to minimize power consumption during sensing operation.
- Three PWMs with programmable hold-time and fade-out time for LED drive
- SPI slave interface supports different polarity and phase modes
- I2C slave interface

Note:

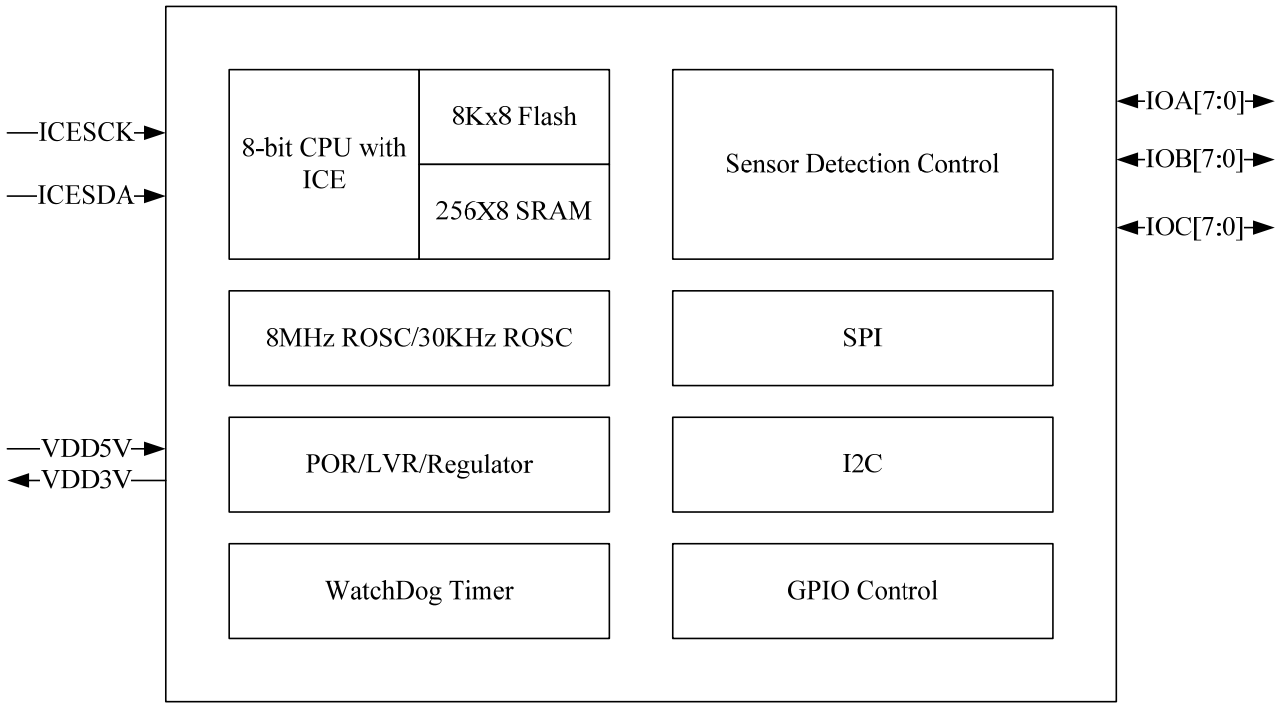
(1)The frequency deviation for built-in 8MHz ROSC is +-10% at room temperature.

(2)The frequency deviation for built-in 30KHz ROSC is +-15% at room temperature.

3. APPLICATION FIELD

- Home appliance, MP3 capacitive touch pad controller, toy, general touch application, or general purpose controller.

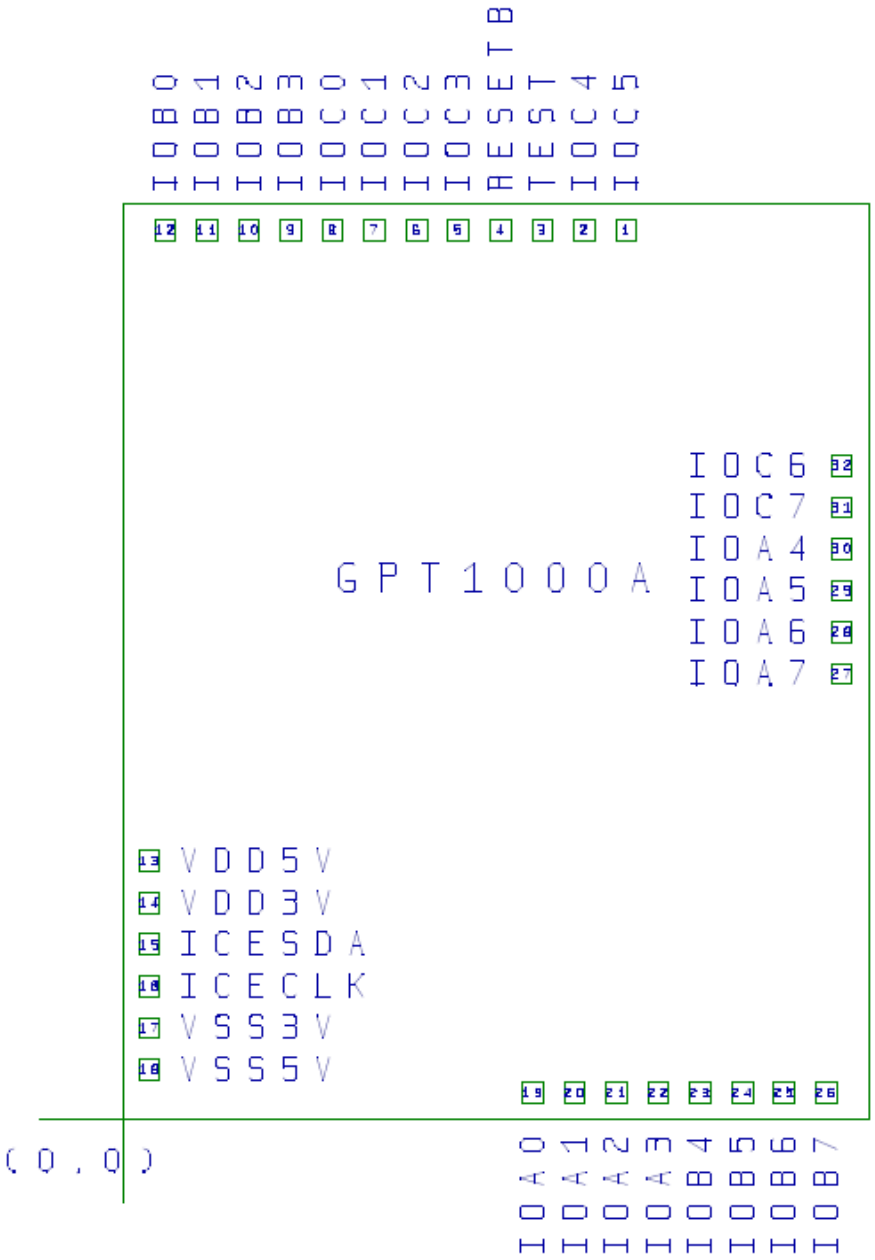
4. BLOCK DIAGRAM



5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Package No.					Type	Description
		QFN32	LQFP32	SSOP20 (HG082)	SSOP20 (HG083)	SOP16		
IOA[7:0]	27-30, 22-19	26-29, 21-18	26-29, 21-18	13-16, 12-9	1-2, 16-13	11-14, 7-10	I/O	8-bit I/O port, each pin can be set as an input or output individually. Input mode: Each one of IOA [7:0] is a CMOS input with programmable internal pull-low resistors. Output mode: CMOS output. All pins are capable of wakeup and external interrupt function is available on IOA2 or IOA4. IOA can be programmed as special function IO for I^2C(IOA[1:0]) or SPI(IOA[3:0]) interface, or sensor IO inputs.
IOB[7:0]	26-23, 9-12	25-22, 8-11	25-22, 8-11	-	20-17, 5-8	1-3, 16	I/O	8-bit I/O port, every two pins can be set as an input or output individually. Input mode: Every two pins can be programmed as CMOS input pin with internal pull-low resistors. Output mode: Every two pins can be programmed as CMOS output or open-drain output. IOB can be programmed as PWM output or sensor IO inputs.
IOC[7:0]	31-32, 1-2, 5-8	30-32, 1, 4-7	30-32, 1, 4-7	17-20	16-13	-	I/O	8-bit I/O port, every two pins can be set as an input or output individually. Input mode: Every two pins can be programmed as CMOS input pin with internal pull-low resistors. Output mode: Every two pins can be programmed as CMOS output or open-drain output. IOC can be programmed as PWM output or sensor IO inputs.
RESETB	4	3	3	2	4	15	I	System reset input. It is LOW-active and with internal pull-high resistor. All of the internal registers are reset to the default state when this pin is set to Low level.
TEST	3	2	2	1	3	-	I	IC Test pin: It is HIGH-active and with internal pull-low resistor. User must leave this pin opened to work in normal mode.
ICECLK	16	15	15	6	-	-	I	ICE clock signal. Should be connected to ground if not in development mode.
ICESDA	15	14	14	5	-	-	I/O	ICE data signal. Should be kept floating if not in development mode
VDD5V	13	12	12	3	9	4	I	IO and regulator power input.
VSS5V	18	17	17	8	12	6	I	IO and regulator ground input.
VDD3V	14	13	13	4	10	5	O	Regulator output for core logic circuit power.
VSS3V	17	16	16	7	11	6	I	Ground input pin for core logic circuit.

5.1. PAD Assignment



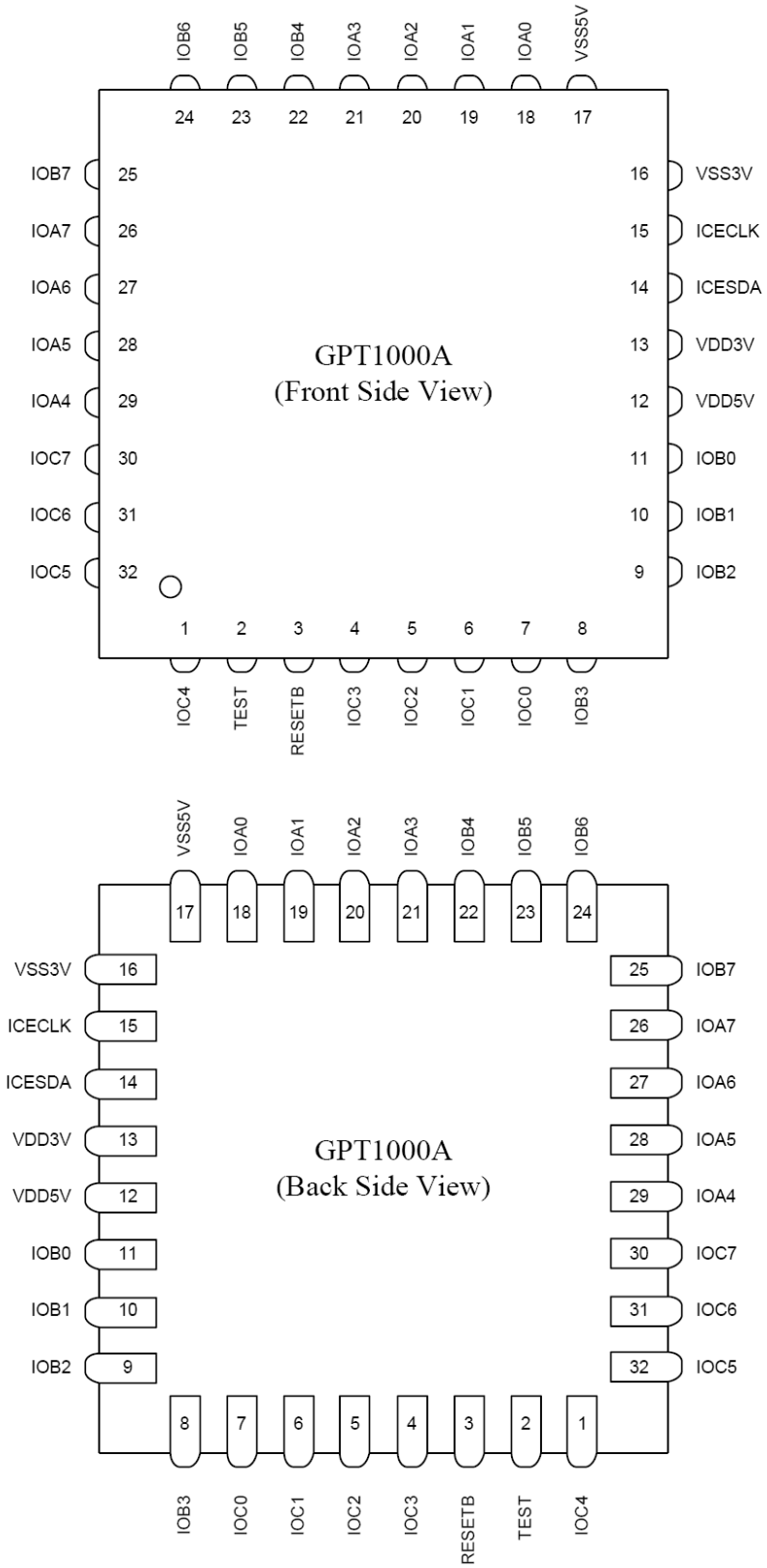
This IC substrate should be connected to VSS or kept floating.

Note1: To ensure IC functions properly, bond all VDD and VSS pins.

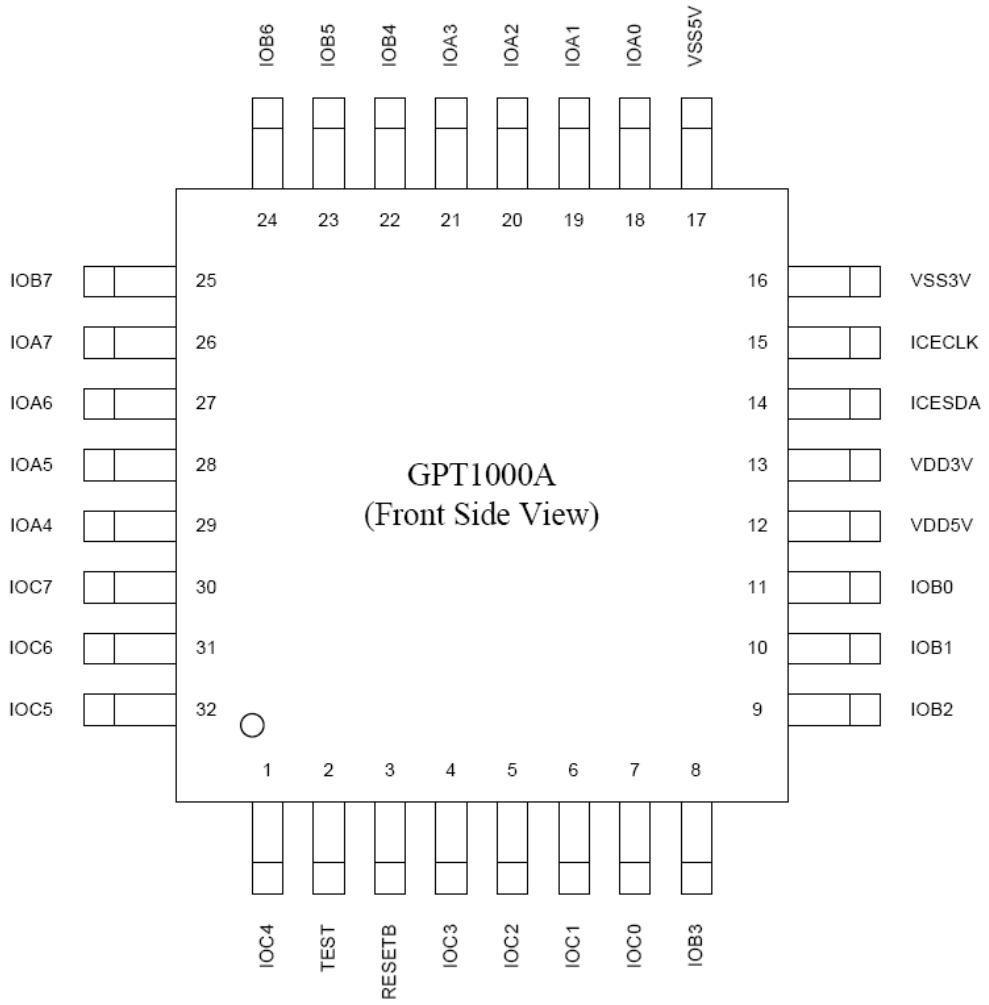
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

5.2. Package PIN Assignment

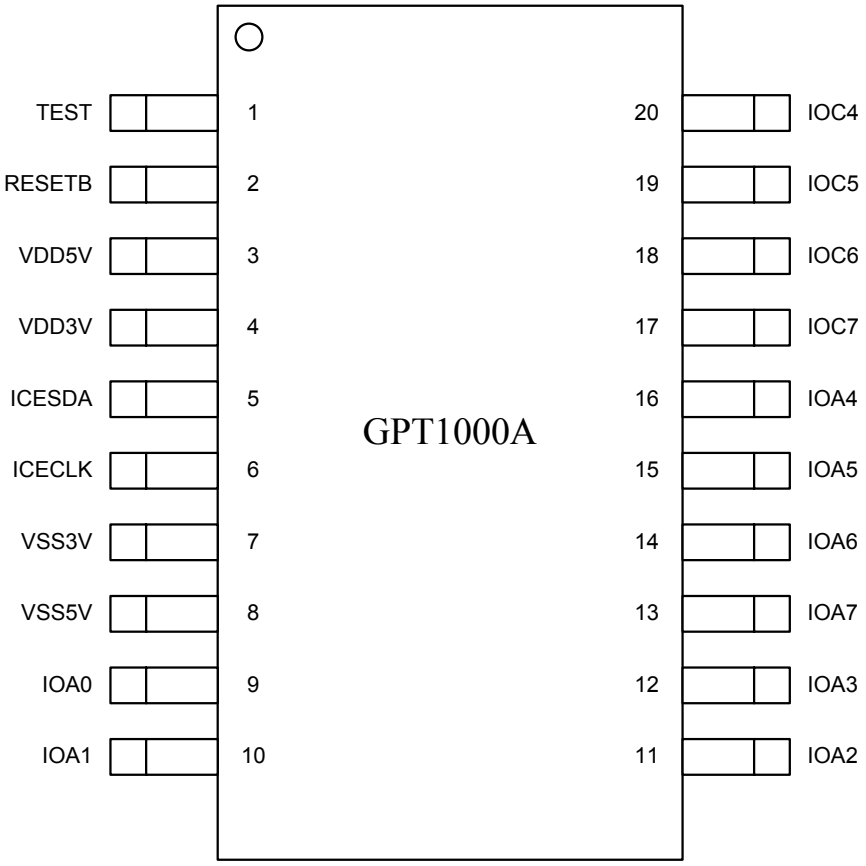
5.2.1. QFN32



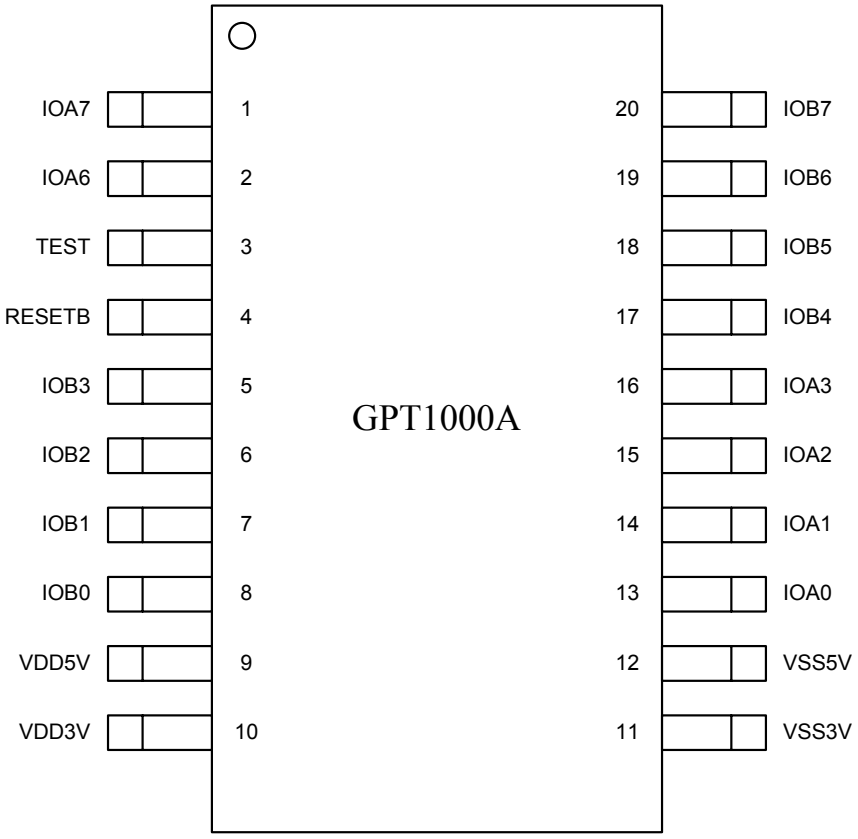
5.2.2. LQFP32


IOB6
IOB5
IOB4
IOA3
IOA2
IOA1
IOA0
VSS5V
24
23
22
21
20
19
18
17
IOB7
25
IOA7
26
IOA6
27
IOA5
28
IOA4
29
IOC7
30
IOC6
31
IOC5
32
16
VSS3V
15
ICECLK
14
ICESDA
13
VDD3V
12
VDD5V
11
IOB0
10
IOB1
9
IOB2
GPT1000A
(Front Side View)
1
2
3
4
5
6
7
8
IOC4
TEST
RESETB
IOC3
IOC2
IOC1
IOC0
IOB3

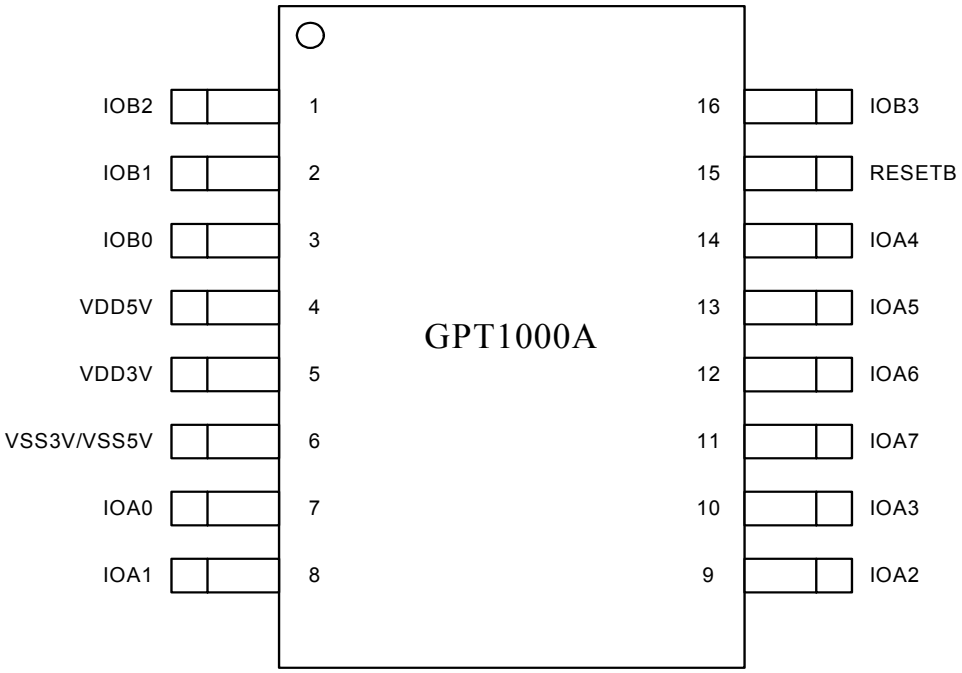
5.2.3. SSOP20(HG082)



5.2.4. SSOP20(HG083)



5.2.5. SOP16


IOB2
1
IOB1
2
IOB0
3
VDD5V
4
VDD3V
5
VSS3V/VSS5V
6
IOA0
7
IOA1
8
GPT1000A
16
IOB3
15
RESETB
14
IOA4
13
IOA5
12
IOA6
11
IOA7
10
IOA3
9
IOA2

6. FUNCTIONAL DESCRIPTIONS

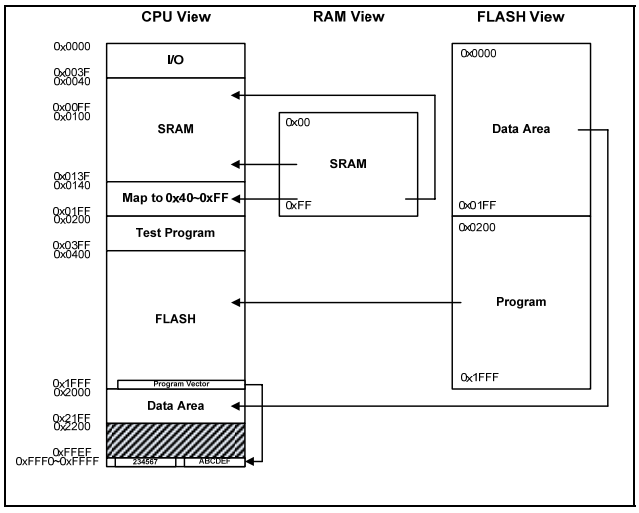
6.1. CPU

The microprocessor in GPT1000A is a high performance 8-bit processor equipped with Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). Up to 8.0MHz CPU speed is able to achieve the best performance.

6.2. Memory

The GPT1000A contains internal SRAM and flash, where the SRAM size is 256-byte and the flash size is 8K-byte. The SRAM starts from address $0040 to $01FF where the area $0140 to $01FF is double mapped as shown in following figure. The built-in flash area is from 0x200 to 0x21FF. The on-chip programmability makes GPT1000A more flexible and easy to develop an application.

6.2.1. Memory mapping

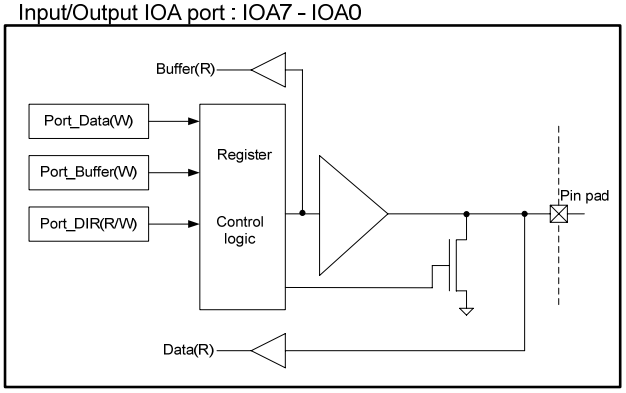


6.3. I/O Port

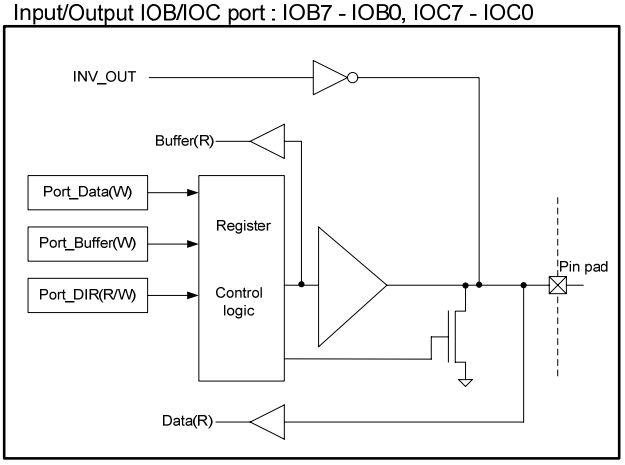
There are 24 IOs (IOA7-0, IOB7-0 and IOC7-0) in GPT1000A. IOA is bit-controlled and IOB and IOC are controlled by registers every two bits. They can be programmed as input (pure input or pull-low) or output buffer. When programmed as output buffers, IOA, IOB and IOC can be selected as either buffer outputs or open-drain outputs. In addition to ordinary I/O function, IOA is also shared with some special functions such as SPI or I^2C interface, external interrupt inputs, timer external clock inputs or IR transmitter outputs. Both IOB and IOC can be high-sink PWM outputs to directly drive LEDs with hold and dimming hardware control.

6.3.1. I/O Configuration

Input/Output IOA port : IOA7 - IOA0



Input/Output IOB/IOC port : IOB7 - IOB0, IOC7 - IOC0



Please refer to the *GPT1000A programming guide -- I/O Configuration* for more information.

All I/Os are set as input mode without pull-low after RESET.

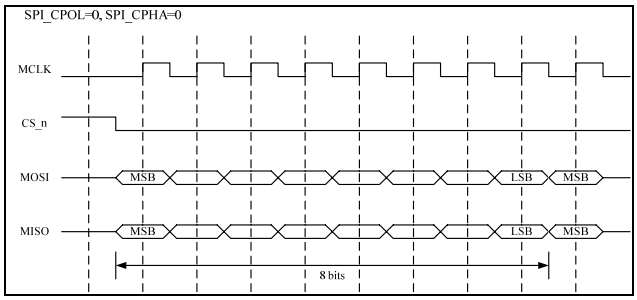
6.4. PWM

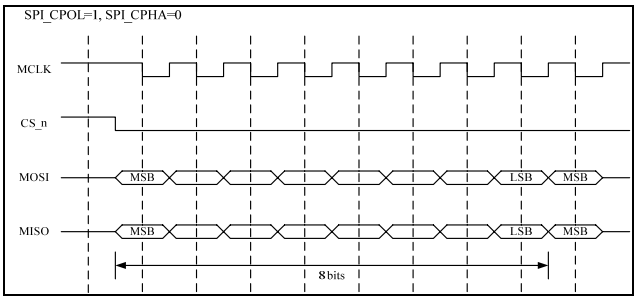
In GPT1000A, three PWMs are built-in. And with IO's high sink ability, external LEDs can be directly driven. Moreover, the hardware hold and dimming control is supported to ease the use for users.

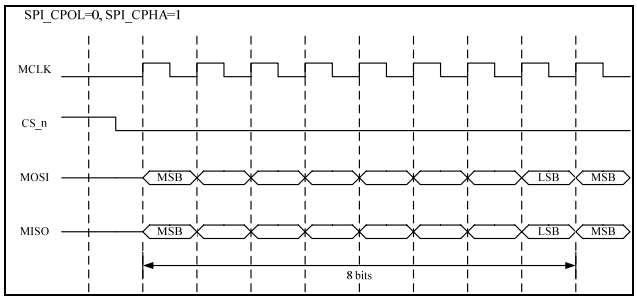
6.5. Serial Interfaces

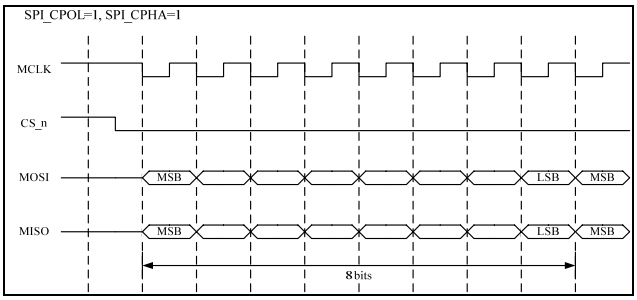
6.5.1. Serial Interface (SPI Interface)

A Serial Peripheral Interface (SPI) is supported in GPT1000A. There are four control signals in SPI including CS_n, SCLK (SCK), MOSI (SDI), and MISO (SDO). They are shared with IOA3-IOA0. Four types of operating mode can be selected through registers. They are supported as follows:









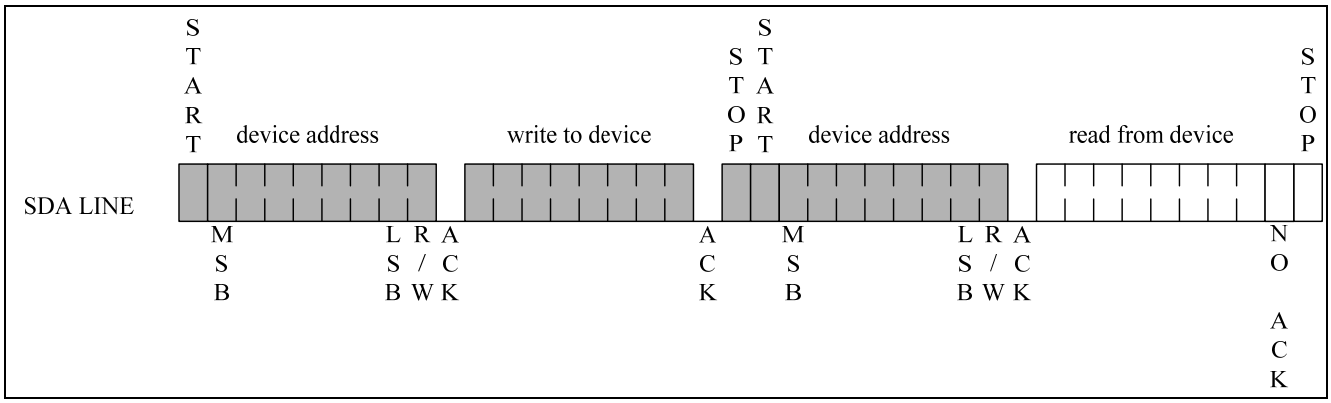
6.5.2. Serial Interface (I^2C Interface)

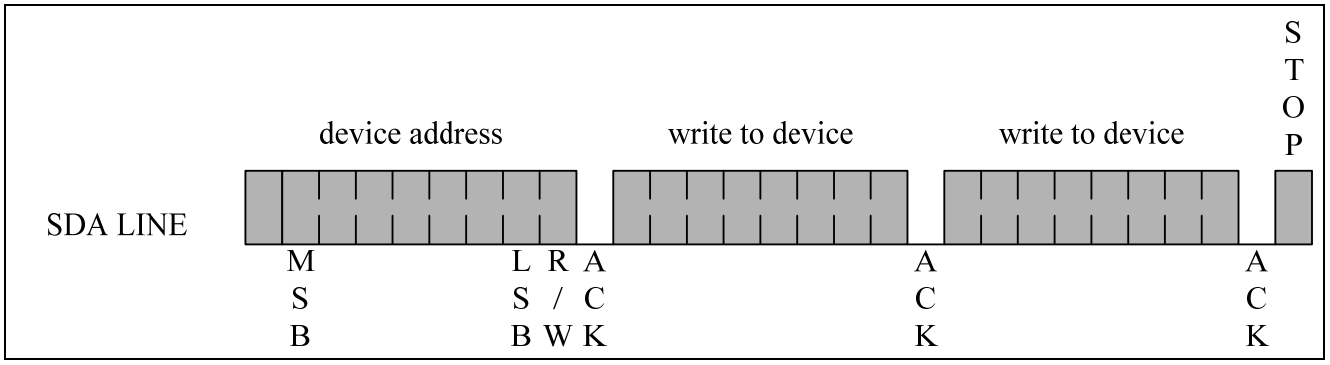
A Serial Inter-IC bus Interface (I^2C) is also supported in GPT1000A. Only two wires, SCK and SDA, are needed to implement the protocol, and they are shared with IOA1-IOA0.

Whenever a byte of data is received or transmitted, an IRQ is generated to notify CPU for next operation.

= master writes to slave.

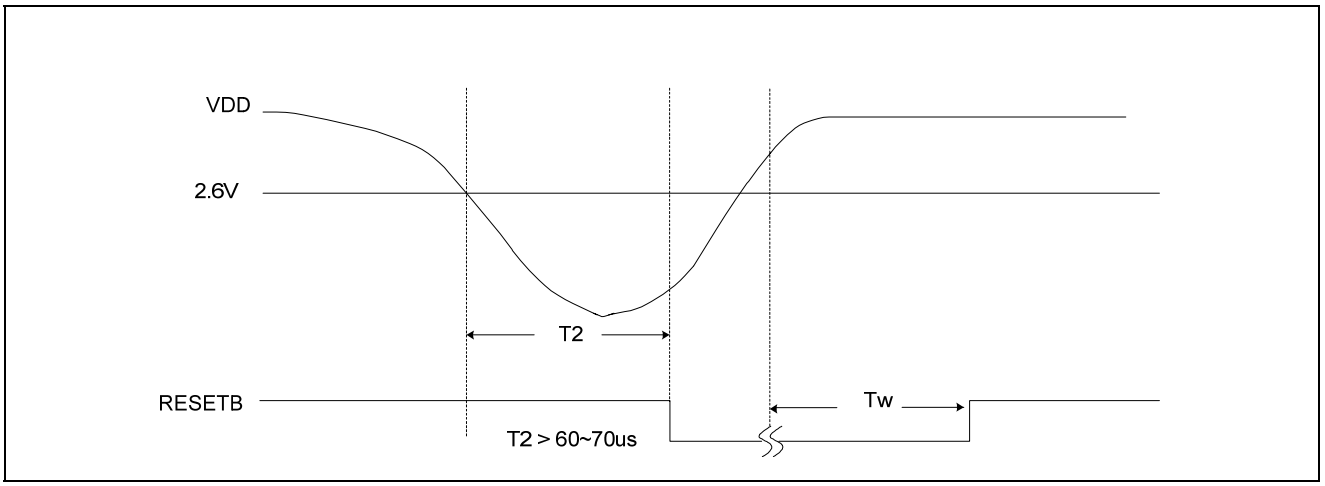
= slave writes to master





6.6. Low Voltage Reset

The GPT1000A has a Low Voltage Reset (LVR) function. In general, the CPU becomes unstable and malfunctioned when the power voltage drops below specific operating voltage. With the unique design of Low Voltage Reset in GPT1000A, it is able to reset all functions to the initial operation (stable) state if the VDD power-supply voltage drops below 2.6V.



(The LVR function is the same as Power ON Reset or External Reset.)

6.7. Timer/Counter

The GPT1000A has a built-in 8-bit timer/counter. It is a up-count and reloadable counter. When the counter rolls from $FF to $00, the carry (overflow) signal will reload user's preset value into timer automatically and up-count again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. User can read the counter value while it is running without influencing the timer/counter or reset it. Moreover, the counter overflow signal becomes a toggle output to IOA4 or IOA5 to support the application such as IR carrier frequency generating.

There is also a built-in timer for automatically sleep/wake-up system inside GPT1000A. The sleep timer can be programmed from 0.9765ms to 62.5ms to fit performance and power needs.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMR	8-bit Timer	8MHz, 2MHz, 500KHz, 250KHz, 125KHz, external clock input from IOA5 or IOA3

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 5.5V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	-40℃ to +85℃
Storage Temperature	T_{STO}	-50℃ to +150℃

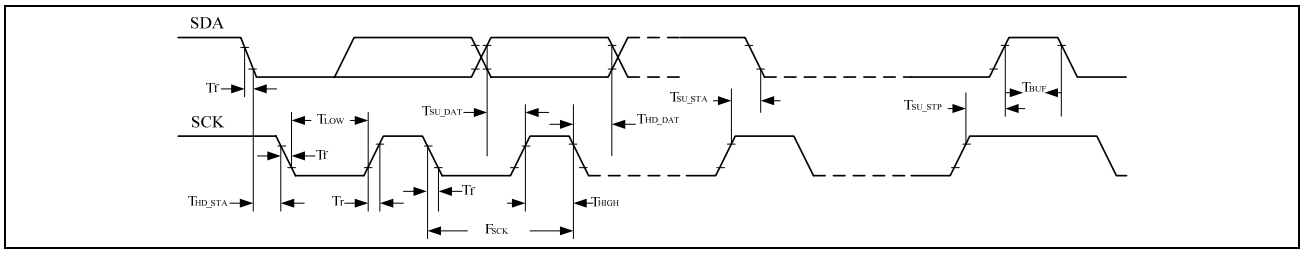
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD5V = 3.3V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage 1	VDD5V	2.6	-	5.5	V	For regulator input and IO power
Operating Voltage 2	VDD3V	2.5	3.3	-	V	Regulator output for core power
CPU Operating Speed	F_{CPU}	0.25	-	8	MHz	VDD3V=2.5 ~ 3.3V
Operating Current	I_{OP1}	-	5	6	mA	VDD3V=3.3V, F_{CPU}=8MHz
Halt Mode Current	I_{HALT}	-	50	100	μA	CPU sleep and wakeup every 256ms, VDD3V=3.3V
Standby Current	I_{STB}	-	-	2	μA	VDD3V=3.3V, all off
Input High Level	V_{IH}	0.7*VDD5V	-	-	V	VDD5V=3.3V
Input Low Level	V_{IL}	-	-	0.3*VDD5V	V	VDD5V=3.3V
IO Output High Current	I_{OH}	-5	-	-	mA	V_{OH} =2.31V, VDD5V=3.3V
IO Output Sink Current	I_{OL}	15	-	-	mA	V_{OL} =0.99V, VDD5V=3.3V
Pull Low Resistor	R_{LOW}	-	200	-	KΩ	VDD5V=3.3V

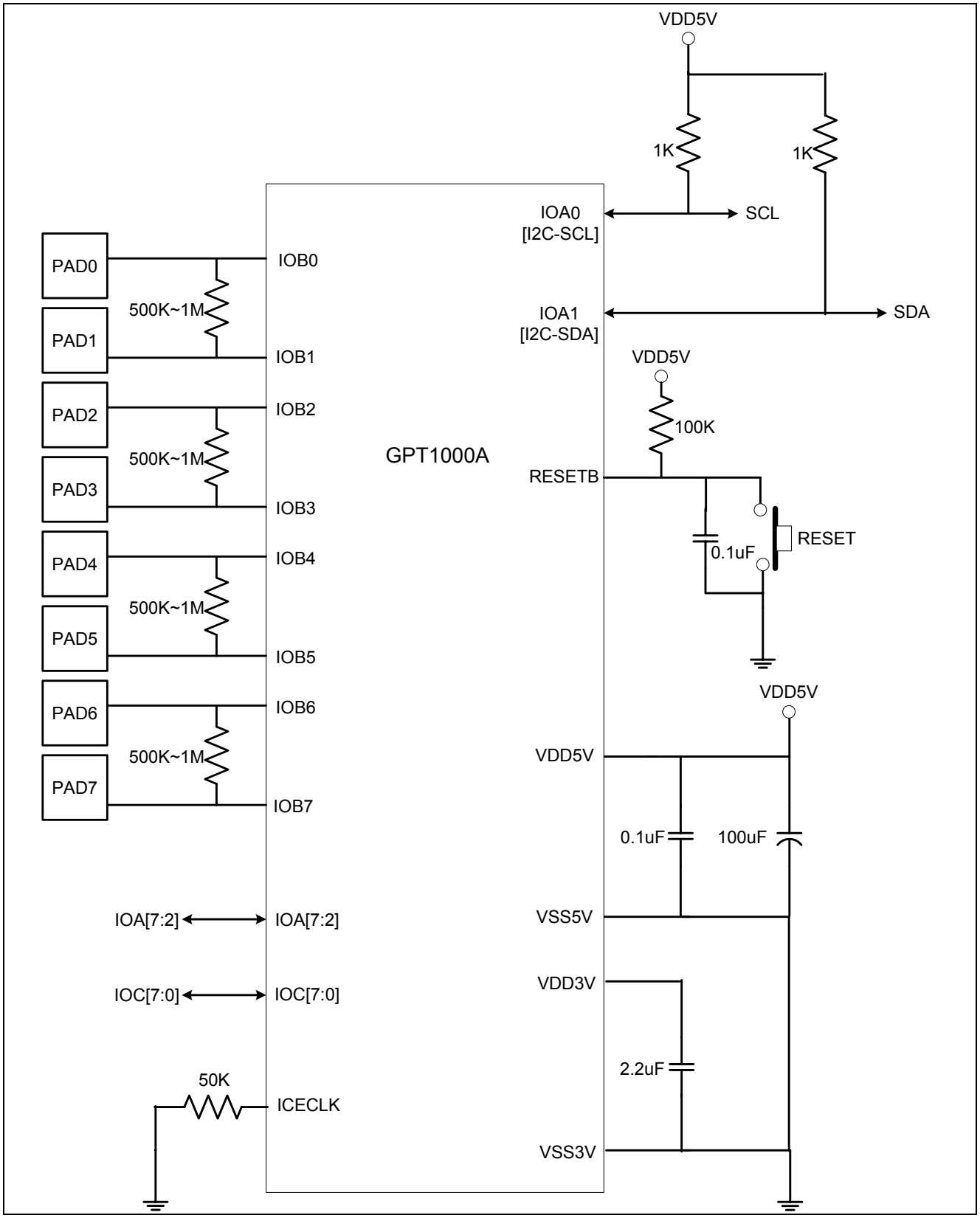
7.3. AC Characteristics

Parameter	Min	Max	Unit	Description
F_{SCK}	-	400	KHz	SCK clock frequency
T_{HD_STA}	0.6	-	us	Hold time for START condition
T_{SU_STA}	0.6	-	us	Setup time for START condition
T_{SU_STP}	0.6	-	us	Setup time for STOP condition
T_f	-	0.3	us	Data/Clock rise time
T_r	-	0.3	us	Data/Clock fall time
T_{LOW}	1.3	-	us	Low period of SCK clock
T_{HIGH}	0.6	-	us	High period of SCK clock
T_{SU_DAT}	100	-	ns	Data setup time
T_{HD_DAT}	300	-	ns	Data hold time
T_{BUF}	1.3	-	us	Data free time between START and STOP condition


SDA
SCK
Tf
TLOW
TSU_DAT
THD_DAT
TSU_STA
TSU_STP
TBUF
THD_STA
Tr
Tf
Tr
THIGH
FSCK

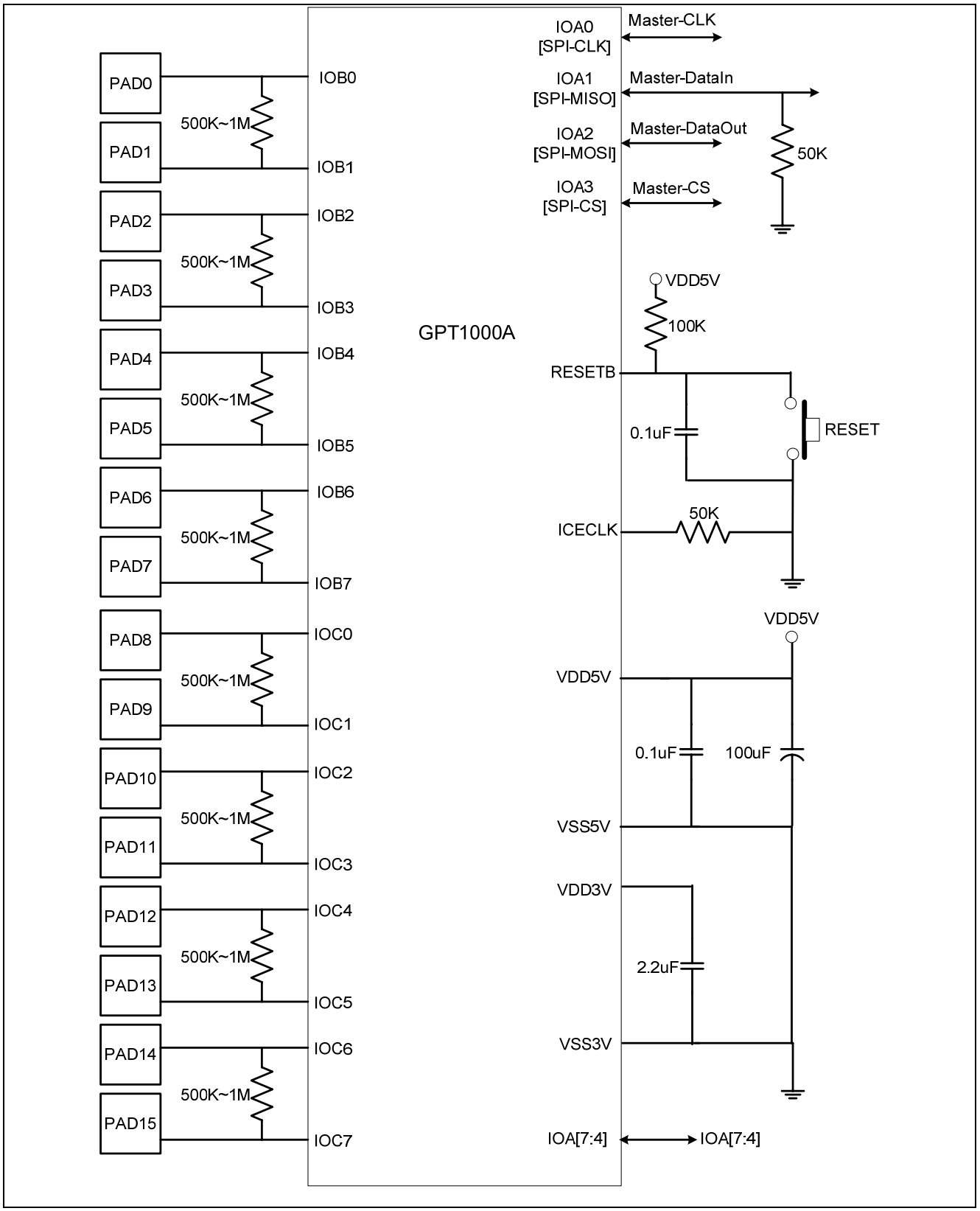
8. APPLICATION CIRCUIT

8.1. Connected to Host through I²C



Note: ICECLK should be connected VSS when not in development mode.

8.2. Connected to Host through SPI



Note1: ICECLK should be connected VSS when not in development mode.

Note2: In SPI application, IOA1 should be connected VSS via 50K resistor.

9. PACKAGE / PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPT1000A - NnnV - C	Chip form
GPT1000A - NnnV - QV04x	Halogen Free Package - QFN 32 (5x5x0.75mm)
GPT1000A - NnnV - QL21x	Halogen Free Package - LQFP 32 (7x7x1.4mm)
GPT1000A - NnnV - HG08x	Green Package - SSOP 20 (150mil)
GPT1000A - NnnV - HS03x	Green Package - SOP 16 (150mil)

Note1: Code number is assigned for customer.

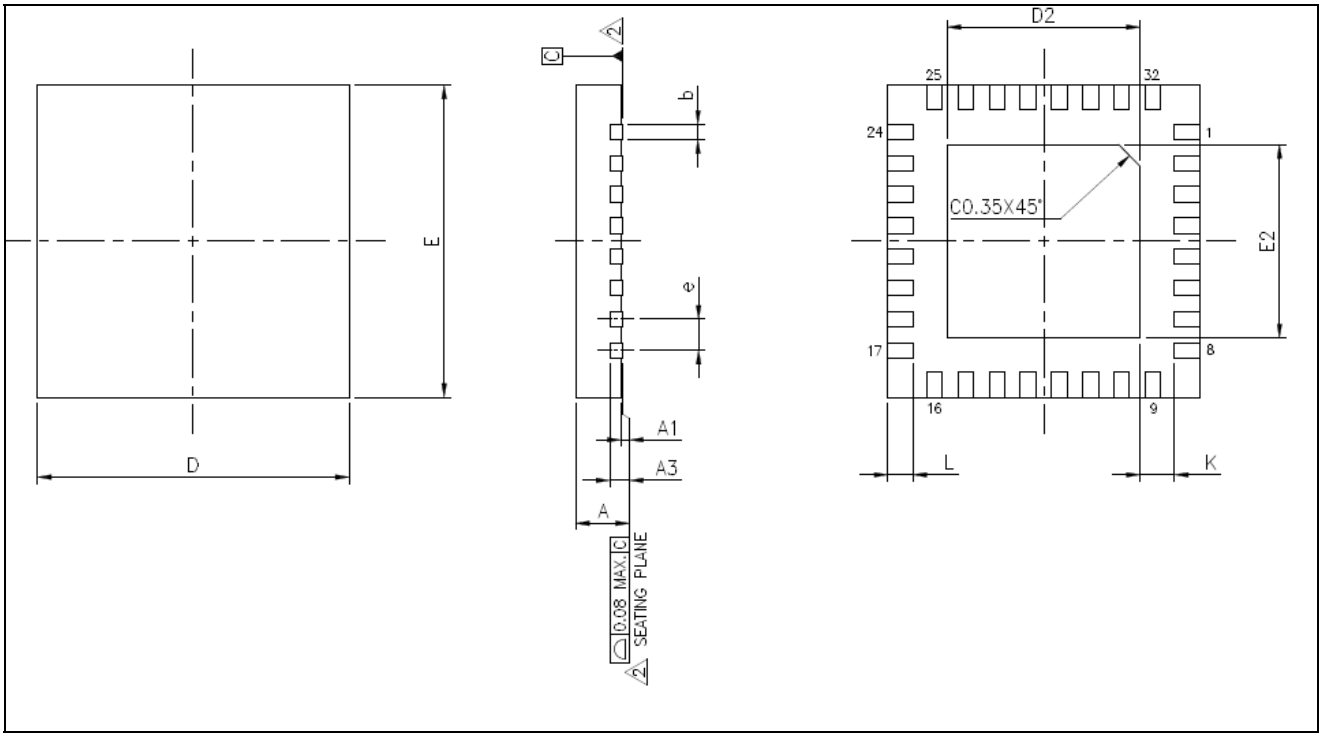
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 0 - 9, serial number).

Note4: There are two types in SSOP20, difference pin assignment in each package. Pin assignment and product number please checks with page9 and page10.

9.2. Package Information

9.2.1. QFN32



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e		0.50 BSC.	
L	0.35	0.40	0.45
K	0.20	—	—

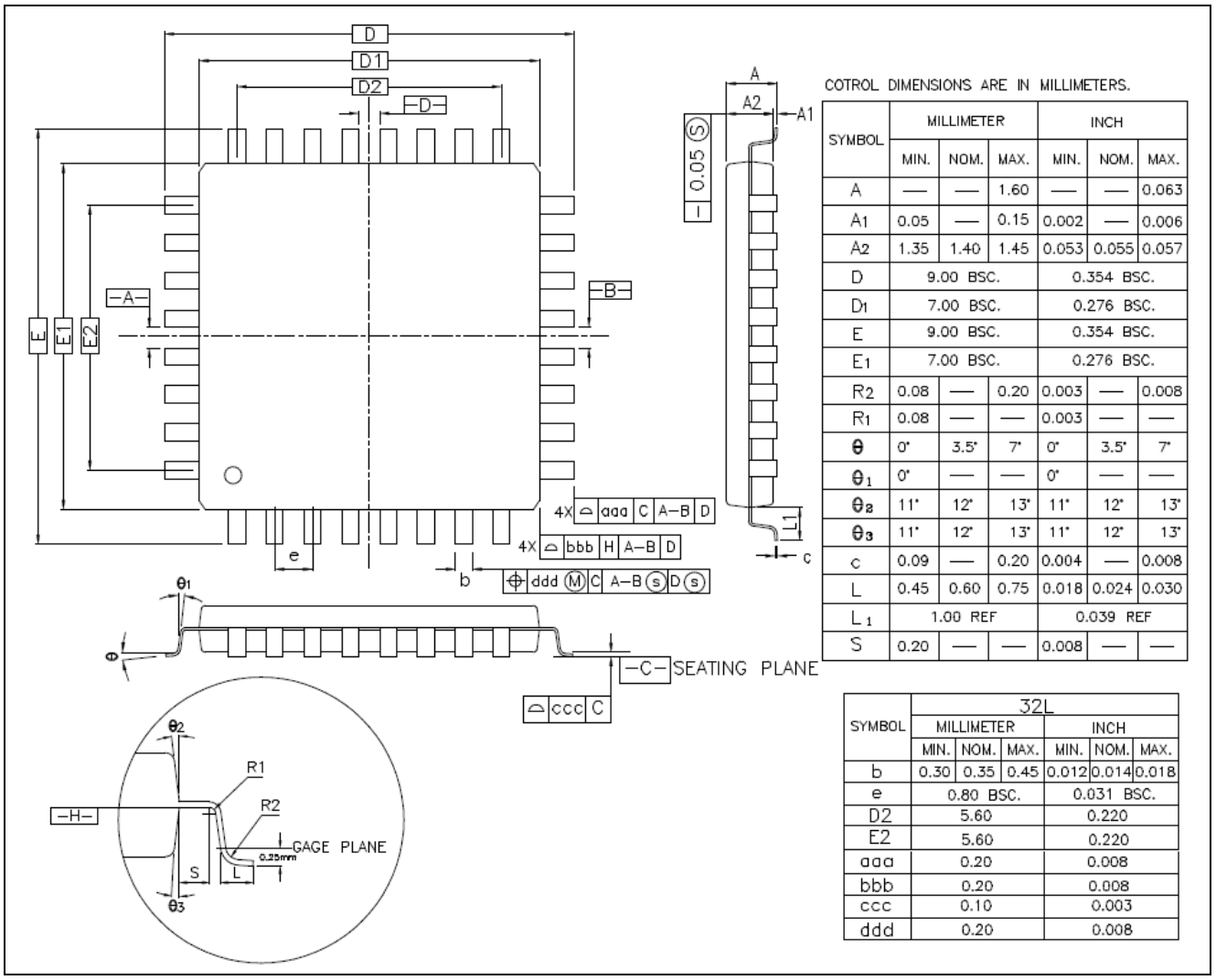
UNIT : mm

	D2			E2		
EXPOSED PAD	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
2.7X2.7	2.60	2.70	2.80	2.60	2.70	2.80
3.2X3.2	3.10	3.20	3.30	3.10	3.20	3.30

UNIT : mm

NOTES :
1. JEDEC OUTLINE : N/A.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. THE MINIMUM "K" VALUE OF 0.20mm APPLIES.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

9.2.2. LQFP32

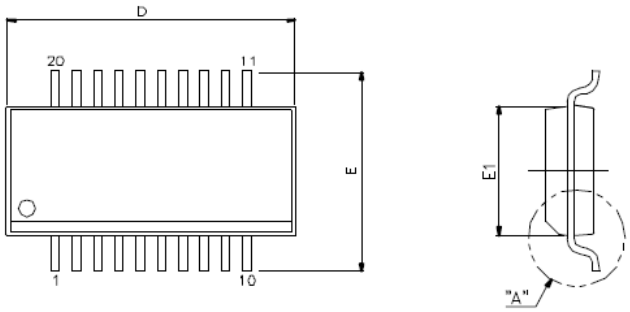


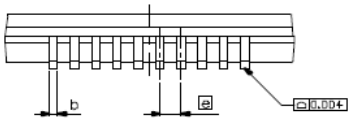
COTROL DIMENSIONS ARE IN MILLIMETERS.

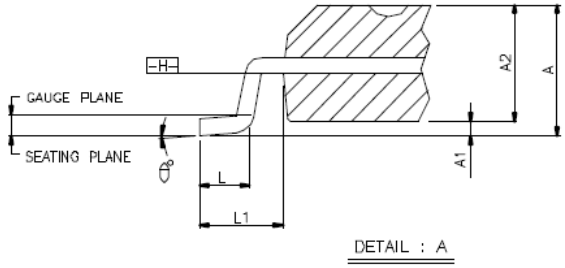
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	32L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.30	0.35	0.45	0.012	0.014	0.018
e	0.80 BSC.			0.031 BSC.		
D2	5.60			0.220		
E2	5.60			0.220		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.10			0.003		
ddd	0.20			0.008		

9.2.3. SSOP20







DETAIL : A

SYMBOLS	MIN.	NOM.	MAX.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	–	–	0.059
b	0.008	–	0.012
C	0.007	–	0.010
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
e	0.025 BASIC		
L	0.016	0.025	0.050
L1	0.041 BASIC		
θ°	0°	–	8°

UNIT : INCH

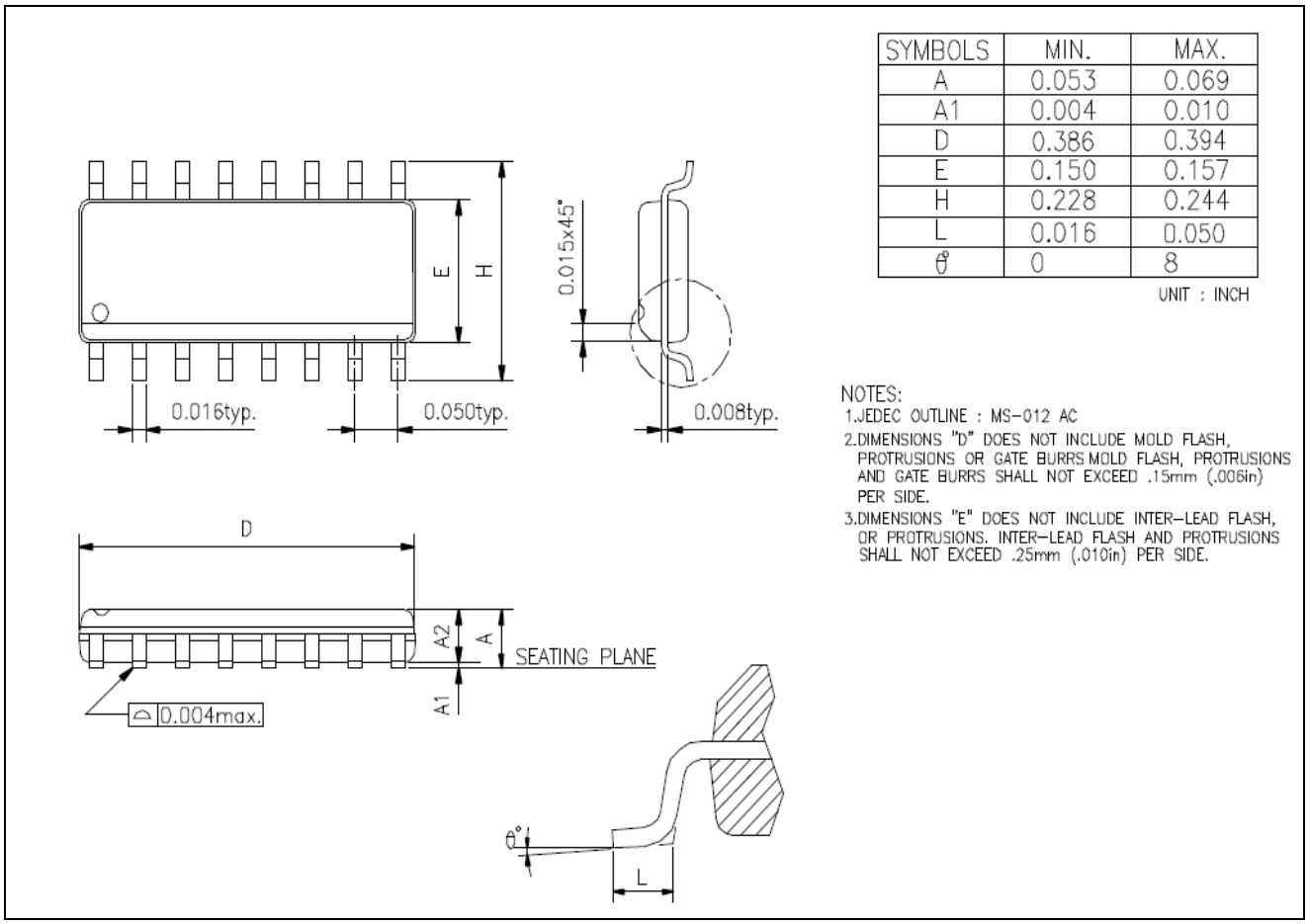
NOTES:

1 JEDEC OUTLINE : MO-137 AD

2 DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006" PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.010" PER SIDE.

3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.004" TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.002" AT LEAST

9.2.4. SOP16



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-012 AC
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
APR. 30, 2012	1.1	1. Remove TSSOP16 package information. 2. Add SSOP20 product number.	 9-10
AUG. 26, 2011	1.0	Modify 8. APPLICATION CIRCUITS.	18, 19
APR. 18, 2011	0.6	1. Modify “Signal Description”. 2. Modify 32K ROSC as 30K ROSC. 3. Add TSSOP16 package information. 4. Modify “Application Circuit”.	6 4~5 6,13,20,25 18~19
NOV. 04, 2010	0.5	1. Modify SOP16 package information. 2. Add I^2C AC characteristics	 5,11,14
APR. 19, 2010	0.4	1. Add SSOP20(2) and SOP16 package information.	10~11, 18,22
JAN. 07, 2010	0.3	1. Add LQFP32 and SSOP20 package information. 2. Modify DC characteristics of I_{OH}/I_{OL} measurement condition.	8~9, 16, 18~19 13
OCT. 27, 2009	0.2	Remove SOP32 package information.	8, 14
SEP. 29, 2009	0.1	Original	19