



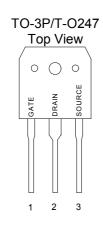
GENERAL DESCRIPTION

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced MOSFET is designed to withstand high energy in avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional and safety margin against unexpected voltage transients.

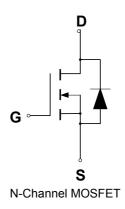
FEATURES

- ◆ Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- ◆ I_{DSS} and V_{DS}(on) Specified at Elevated Temperature
- ◆ Isolated Mounting Hole Reduces Mounting Hardware

PIN CONFIGURATION



SYMBOL



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain to Current — Continuous	I _D	23.5	Α
- Pulsed	I _{DM}	70.5	
Gate-to-Source Voltage — Continue	V_{GS}	±30	٧
Total Power Dissipation – TO3P		255	W
– TO247		225	W/°C
Derate above 25℃ – TO3P		2.1	
– TO247		2	
Operating and Storage Temperature Range		-55 to 150	$^{\circ}\!\mathbb{C}$
Single Pulse Drain-to-Source Avalanche Energy $-T_J = 25^{\circ}$ C		2420	
$(V_{DD} = 100V, V_{GS} = 10V, I_{L} = 22A, L = 10mH, R_{G} = 25\Omega)$			mJ
Thermal Resistance — Junction to Case -TO3P		0.48	°C/W
 Junction to Case -TO247 		0.6	
 Junction to Ambient -TO3P, TO247 	θ_{JA}	40	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds		260	$^{\circ}\!\mathbb{C}$
ESD SENSITIVITY — HBM, C=100pF, R=1.5kΩ		2000	V





ORDERING INFORMATION

Part Number	Package
GPT24N50GN3P*	TO-3P
GPT24N50GN247*	TO-247

^{*}Note: G : Suffix for PB Free Product

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_J = 25^{\circ}C$.

				GPT24N50		
Characteristic		Symbol	Min	Тур	Max	Units
Drain-Source Breakdown Voltage		500			V	
$(V_{GS} = 0 \text{ V}, I_D = 250 \ \mu \text{ A})$	$V_{(BR)DSS}$	500			V	
Drain-Source Leakage Current		lasa			1	uA
$(V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V})$		I _{DSS}			l	uA
Gate-Source Leakage Current-Forward	d	I _{GSSF}			100	nA
$(V_{gsf} = 30 \text{ V}, V_{DS} = 0 \text{ V})$	IGSSF			100	IIA	
Gate-Source Leakage Current-Reverse		l			100	nA
$(V_{gsr} = 30 \text{ V}, V_{DS} = 0 \text{ V})$	I _{GSSR}			100	IIA	
Gate Threshold Voltage		$V_{GS(th)}$	3		5	V
$(V_{DS} = V_{GS}, I_{D} = 250 \ \mu A)$		V GS(th)	3			
Static Drain-Source On-Resistance (Vo	R _{DS(on)}			0.19	Ω	
Forward Transconductance (V _{DS} = 50 V	/, I _D = 12A) *	g FS		25		S
Input Capacitance	$(V_{DS} = 25 \text{ V}. V_{GS} = 0 \text{ V}.$	C_{iss}		3992.1		pF
Output Capacitance	$(v_{DS} - 23 \text{ v}, v_{GS} - 0 \text{ v},$ f = 1.0 MHz)	C _{oss}		418.9		pF
Reverse Transfer Capacitance	1 = 1.0 (VII 12)	C_{rss}		20.89		pF
Turn-On Delay Time		t _{d(on)}		40.4		ns
Rise Time	$(V_{DD} = 250 \text{ V}, I_D = 24 \text{ A},$	t _r		82		ns
Turn-Off Delay Time	$R_G = 25\Omega)$ *	$t_{d(off)}$		130		ns
Fall Time		t _f		76.8		ns
Total Gate Charge	0/ 400 \/ 1 04 4	Q_g		85.6		nC
Gate-Source Charge	$(V_{DS} = 400 \text{ V}, I_D = 24 \text{ A},$	Q_{gs}		18.8		nC
Gate-Drain Charge	V _{GS} = 10 V)*	Q_{gd}		32.2		nC
	SOURCE-DRAIN DIODE CHA	ARACTERISTICS		•	•	
Forward On-Voltage(1)	(1	V_{SD}			1.5	V
Forward Turn-On Time	$(I_S = 24 \text{ A},$	t _{on}		**		ns
Reverse Recovery Time d _{IS} /d _t = 100A/µs)		t _{rr}		510		ns

^{*} Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%

^{**} Negligible, Dominated by circuit inductance





TYPICAL ELECTRICAL CHARACTERISTICS

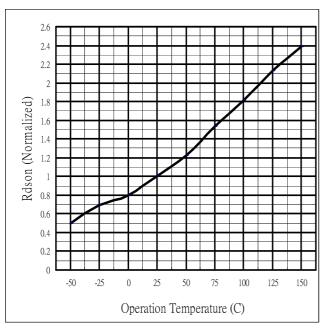


Fig 1. On-Resistance Variation with vs. Temperature

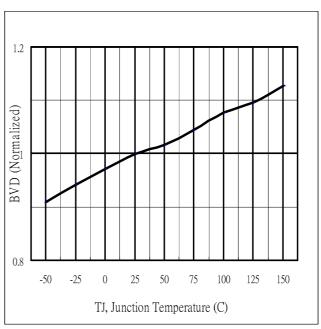


Fig.2 Breakdown Voltage Variation vs. Temperature

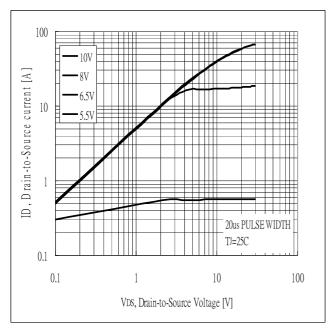


Fig 3. Typical Output Characteristics

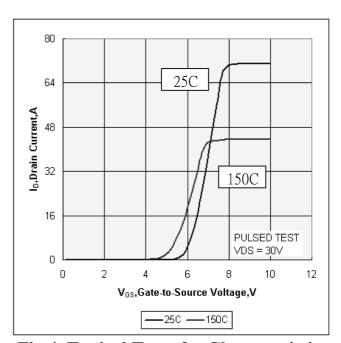


Fig 4. Typical Transfer Characteristics







Power Field Effect Transistor

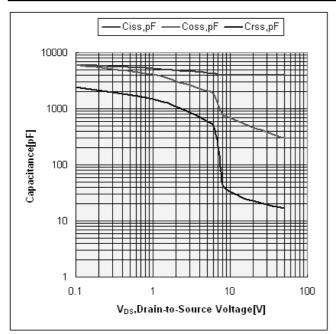


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

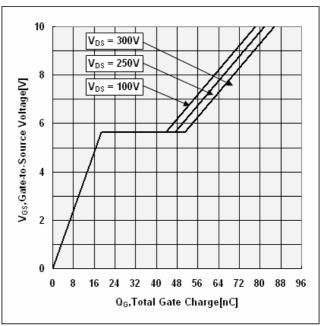
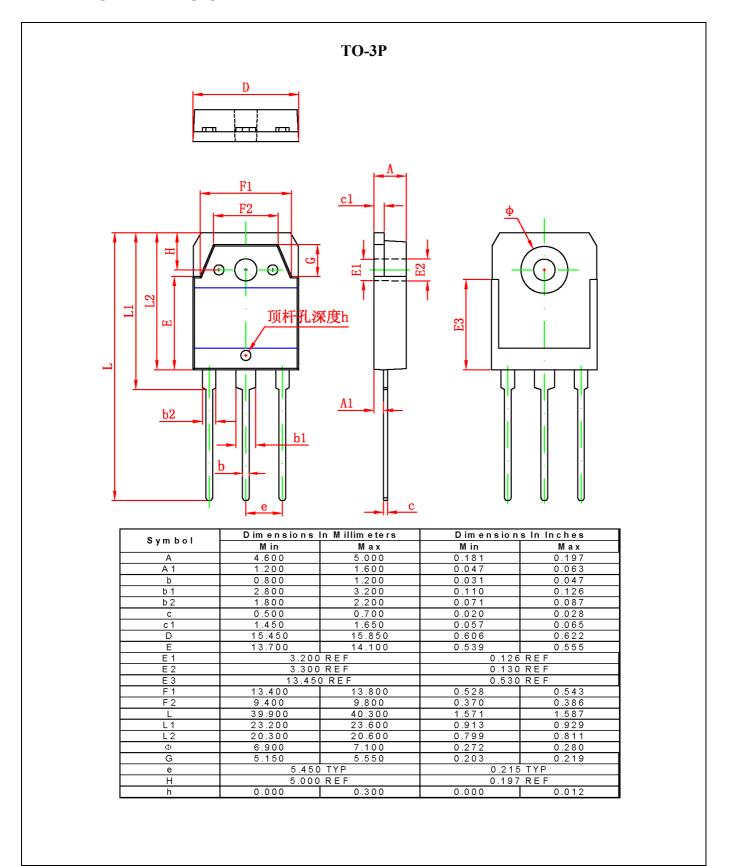


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage



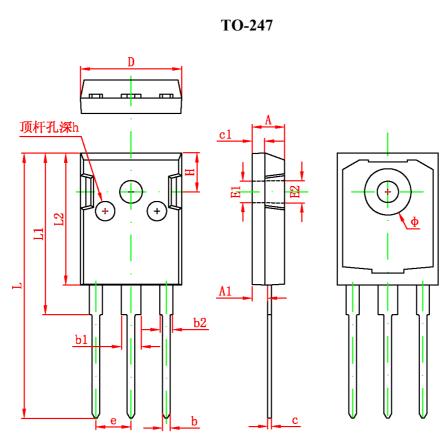


PACKAGE DIMENSION









Creshol	Dimensions In Millimeters		Dimensions In Inches		
Symbol	Min	Max	Min	Max	
Α	4.850	5.150	0.191	0.200	
A1	2.200	2.600	0.087	0.102	
b	1.000	1.400	0.039	0.055	
b1	2.800	3.200	0.110	0.126	
b2	1.800	2.200	0.071	0.087	
С	0.500	0.700	0.020	0.028	
c1	1.900	2.100	0.075	0.083	
D	15.450	15.750	0.608	0.620	
E1	3.500 REF		0.138 REF		
E2	3.600 REF		0.142 REF		
L	40.900	41.300	1.610	1.626	
L1	24.800	25.100	0.976	0.988	
L2	20.300	20.600	0.799	0.811	
Ф	7.100	7.300	0.280	0.287	
е	5.450 TYP		0.215 TYP		
Н	5.980 REF		0.235 REF		
h	0.000	0.300	0.000	0.012	





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