DATA SHEET

GPUSB101A

USB Bridge Controller

Sep 24, 2014

Version 1.4

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USB BRIDGE CONTROLLER

1. GENERAL DESCRIPTION

The GPUSB101A carries an 8-bit processor, 16K bytes OTP ROM, 256 bytes working SRAM, six 64 bytes buffer SRAM, 2 set 12-bit timers, and 20 general I/Os. The general I/Os can be programmed as parallel bus or SPI.

There are three main functions for the bridge IC.

- USB to parallel bus
- USB to SPI
- Parallel bus to SPI

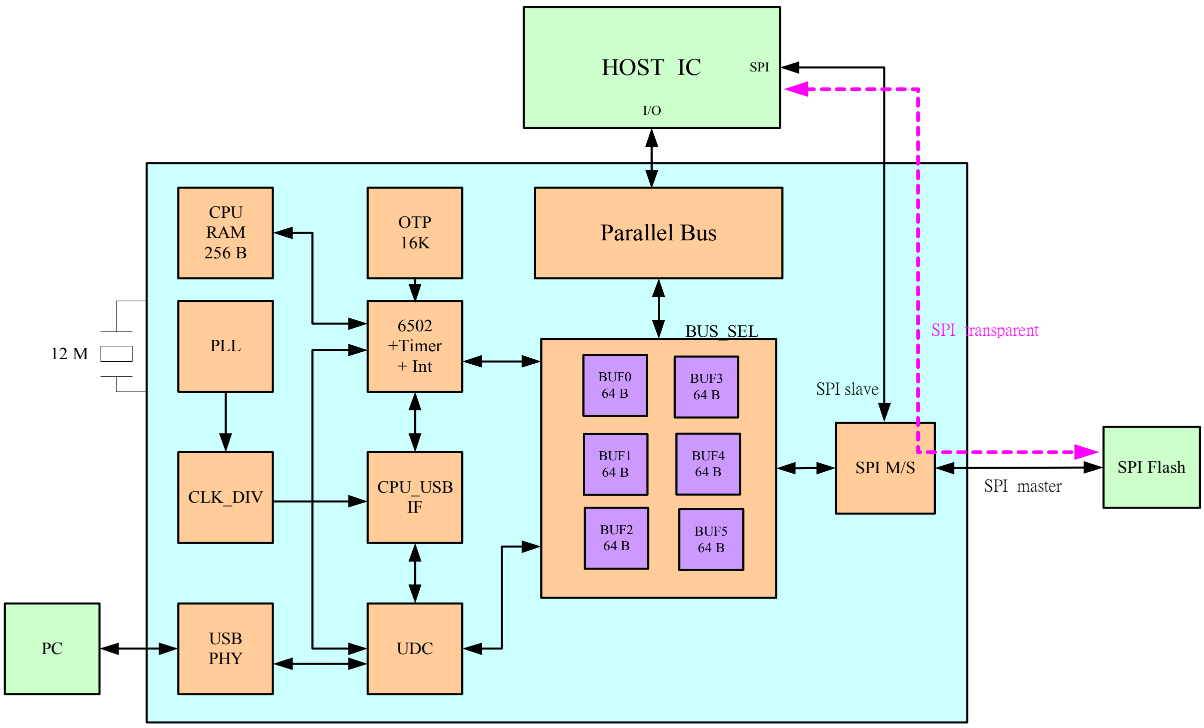
2. APPLICATION FIELD

- USB Bulk transfer for download
- USB Isochronous IN transfer for MIC in (needs extra ADC)
- USB Isochronous OUT transfer for speaker out(needs extra DAC)
- USB Interrupt IN transfer for small data communication

3. FEATURES

- Working Voltage: 2.4V - 3.6V (without USB)
  3.0V - 3.6V (with USB)
- IOA, IOB Working Voltage: 2.4V - 5.5V
- IOC Working Voltage: 2.4V - 3.6V
- CPU Speed: 0.09375MHz - 12MHz
- ROM Size: 16 K bytes OTP ROM
- RAM Size: 256 bytes working SRAM
  Six 64 bytes buffer SRAM
- Two 12-bit timers/counters
- On-chip Voltage Regulator: 3.3 V output
- USB Specification 2.0 compliant; full-speed (12 Mbps)
- USB supports Bulk IN, Bulk OUT, Interrupt IN, Isochronous IN and Isochronous OUT transfer mode
- 20 GPIO port (Parallel bus and SPI share with GPIO)
- Supports parallel bus 4 bit mode (5 pin for control and 4 pin for data)
- Supports parallel bus 8 bit mode (5 pin for control and 8 pin for data)
- Supports SPI master mode
- Supports SPI slave mode
- Supports SPI transparent mode (Host IC can control SPI slave device through bridge IC)

4. BLOCK DIAGRAM

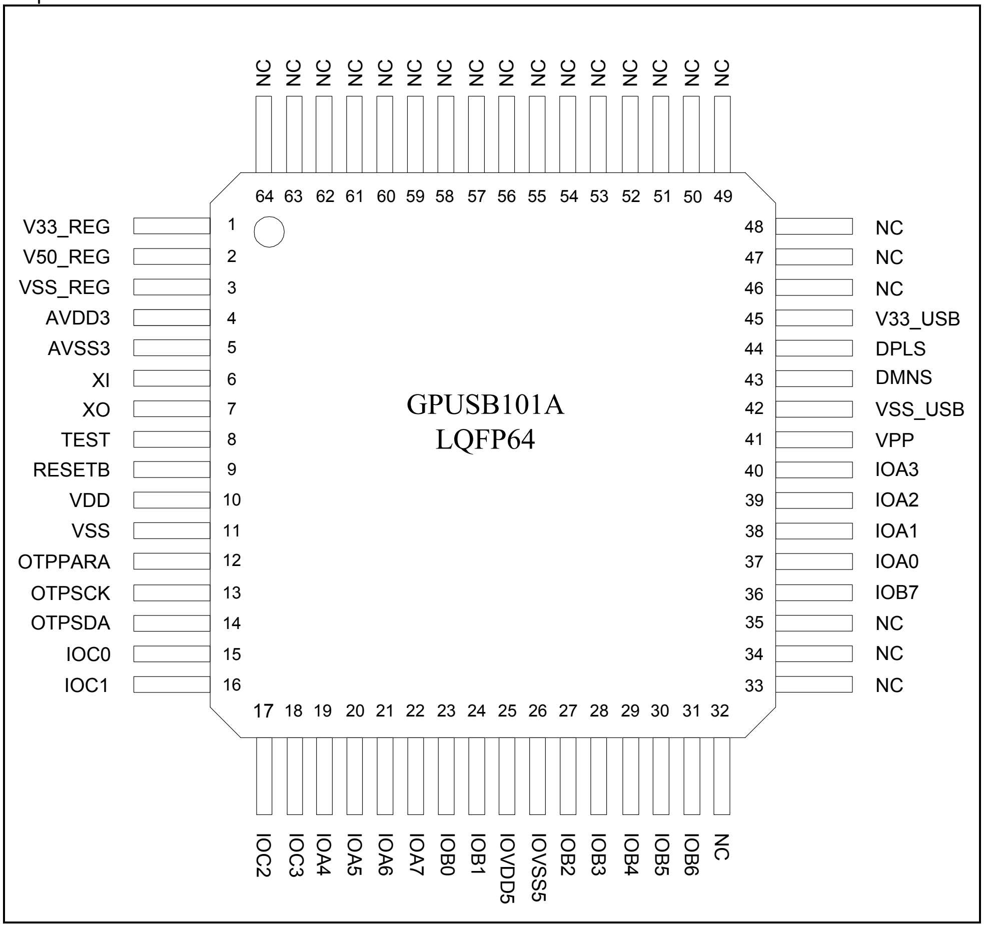


5. SIGNAL DESCRIPTIONS

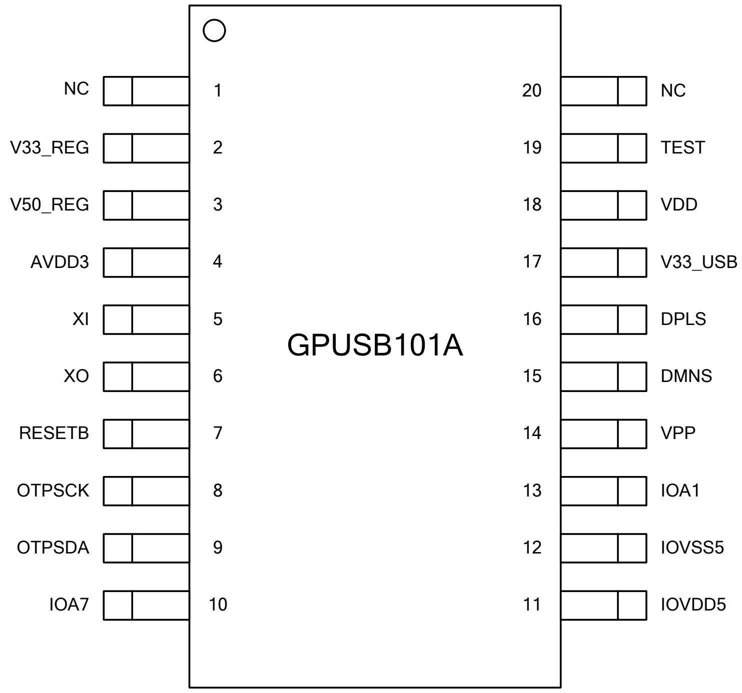
Pad Name	PIN NO.	LQFP64 PIN NO.	Type	Description
XI	6	6	I	Oscillator crystal input
XO	7	7	O	Oscillator crystal output
V50_REG	2	2	P	Regulator power 5V input
VSS_REG	3	3	G	Regulator power ground input
V33_REG	1	1	P	Regulator power 3.3V output
RESETB	9	9	I	System reset pin (active low)
TEST	8	8	I	TEST Mode selection pin, high is test mode and low is normal mode (Pad internal pull low)
VDD	10	10	P	Positive power supply for core and IOC (2.4V~3.6V)
VSS	11	11	G	Ground reference for core
AVDD3	4	4	P	Positive power supply for analog circuit
AVSS3	5	5	G	Ground reference for analog circuit
V33_USB	41	45	P	USB power 3.3V input
VSS_USB	38	42	G	USB power ground input
DPLS	40	44	I/O	USB DPLS
DMNS	39	43	I/O	USB DMNS
IOA[7:0]	22-19, 36-33	22-19, 40-37	I/O	bi-directional I/O ports, power source from IOVDD5(2.4V~5.5V)
IOB[7:0]	32-27, 24-23	36,31-27, 24-23,	I/O	bi-directional I/O ports, power source from IOVDD5(2.4V~5.5V)
IOC[3:0]	18-15	18-15	I/O	bi-directional I/O ports, power source from VDD(2.4V~3.6V)
OTPSCK	13	13	I	OTP writer clock input (Pad internal pull low)
OTPSDA	14	14	I/O	OTP writer data input/output (Pad internal pull low)
IOVDD5	25	25	P	IOA and IOB power source input (2.4V~5.5V)
IOVSS5	26	26	G	IOA and IOB power source ground input
OTPPARA	12	12	I	OTP test pin (Pad internal pull low)
VPP	37	41	P	OTP high voltage power supply for programming
Total: 41 Pads				

5.1. PIN Map

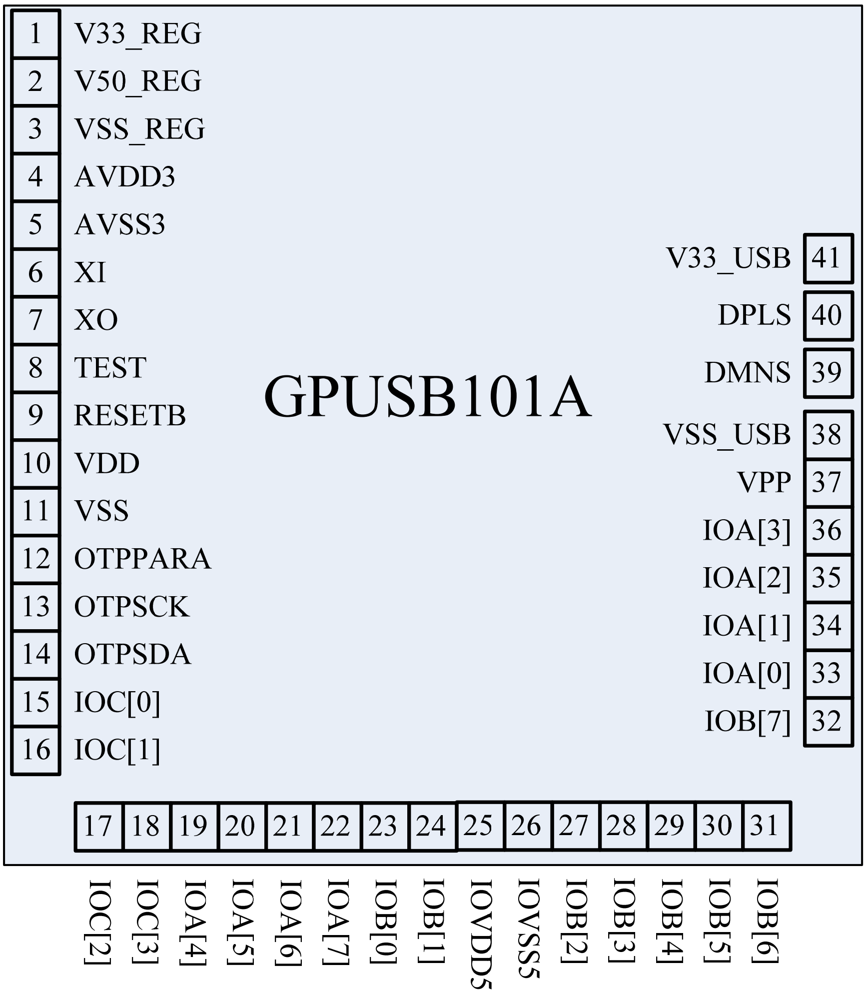
LQFP 64 Package Top View



SSOP 20 Package Top View



5.2. PAD Assignment



6. FUNCTIONAL DESCRIPTIONS

6.1. Power Saving Mode

The GPUSB101A features a power saving mode(or called standby mode) for low power application. To enter standby mode, the desired key wakeup port(IOA[7:0]) must be configured to input first. And read the P_IOA_Data to latch the IOA state before entering the standby mode.

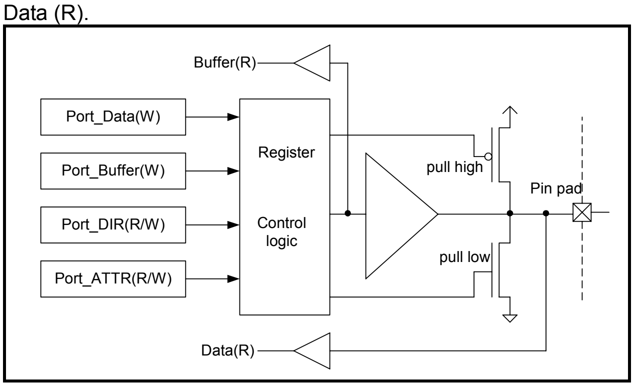
6.2. PLL (Phase Lock Loop)

The purpose of PLL is to provide stable output frequency which reference a base frequency (from crystal). The PLL output frequency is 48MHz. It is used for USB device core.

6.3. I/O

Three I/O ports are built in GPUSB101A - PortA, PortB and PortC, total has 20 bit-programmable I/Os. The PortA is a general purpose I/O with programmable wakeup capability, i.e. IOA [7:0] is the key wakeup port. To activate key wakeup function, latch data on P_IOA_Data and enable the key wakeup function. Wakeup is triggered when the PortA state is different from at the time latched. Furthermore, the I/O ports can be operated at 5V level(only PortA and PortB), higher than the CPU core which is a 3.3V level system.

Suppose system operating voltage is running at 3.3V, then IOVDD5 (power for I/O) operates from 3.3V to 5.5V. In such condition, the I/O pad is capable of operating from 0V through IOVDD5. The following diagram is an I/O schematic. Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer (R) and Data (R).



In addition to a general purpose I/O port function, PortA/B/C also shares some special functions. A summary of PortA/B/C special functions is listed as follows:

Port A

Port A	IOA[7]	IOA[6]	IOA[5]	IOA[4]	IOA[3]	IOA[2]	IOA[1]	IOA[0]
Wakeup	V	V	V	V	V	V	V	V
Parallel	-	-	-	para_int	para_wrb	para_rdb	para_csb	para_cdb

Port B

Port B	IOB[7]	IOB [6]	IOB[5]	IOB [4]	IOB [3]	IOB [2]	IOB [1]	IOB [0]
Parallel	para_data[7]	para_data[6]	para_data[5]	para_data[4]	para_data[3]	para_data[2]	para_data[1]	para_data[0]
SPI slave	spi_rxd	spi_txd	spi_clk	spi_csb	-	-	-	-

Port C

Port C	IOC [3]	IOC [2]	IOC [1]	IOC [0]
SPI master	spi_rxd	spi_txd	spi_clk	spi_csb

6.4. Parallel Bus

There is a parallel bus slave side on GPUSB101A. The host IC as a parallel bus master role. Host IC can use GPIO toggle to implement signals like section 6.4.3. According to host IC GPIOs number. The customer can select 8 bit mode (5 control pin and 8 data pin) or 4 bit mode (5 control pin and 4 data pin). Besides Para_int is input pin, others control pin are output pin. If the GPUSB101A has request to host IC. GPUSB101A may issues Parallel_int pin then host IC must polling the status register and knows what request from GPUSB101A.

6.4.1 The description of parallel bus I/O

Pad name	Type	IO	Description
Para_cdb	I	IOA[0]	Parallel bus for command or data transfer (high is command and low is data)
Para_csb	I	IOA[1]	Parallel bus chip enable (active low)
Para_rdb	I	IOA[2]	Parallel bus write enable (active low)
Para_wrb	I	IOA[3]	Parallel bus read enable (active low)
Para_int	O	IOA[4]	Parallel bus interrupt out
Para_data[7:0]	I/O	IOB[7:0]	Parallel bus bi-directional data

6.4.2 The function of parallel bus

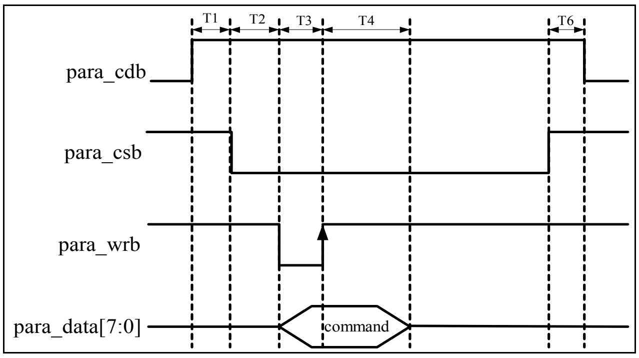
Para_cdb	Para_wrb	Para_rdb	Description
1	0	1	Write command register
1	1	0	Read status register
0	0	1	Write data
0	1	0	Read data

Note1: command register is read only bridge IC.
Note2: status register is read only for host IC.

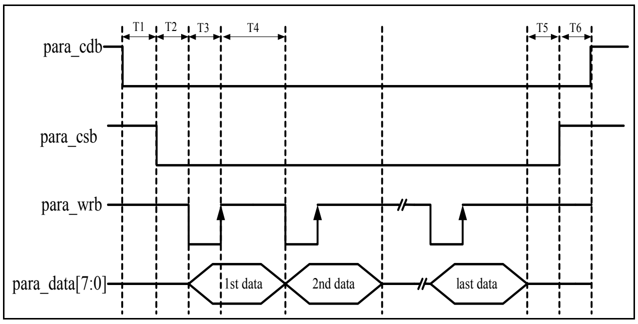
6.4.3 Timing diagram

8 bit mode

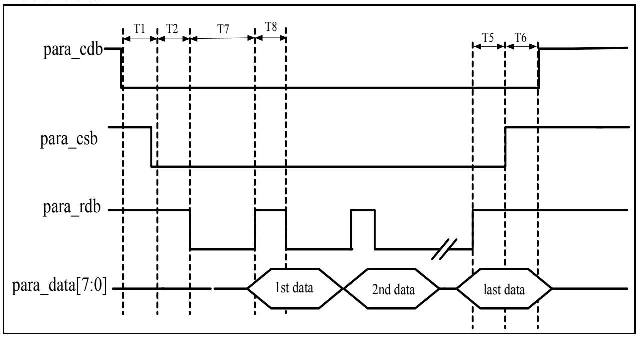
Write command



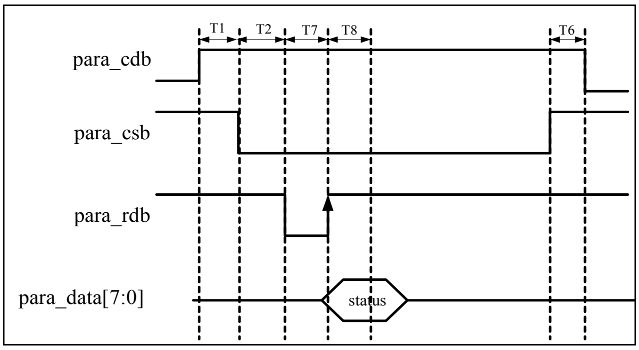
Write data



Read data



Read status



6.4.4 Timing constrain

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
cdb to csb delay time	T1	100	-	-	ns
csb to wrb(rdb) delay time	T2	100	-	-	ns
wrb to data setup time	T3	100	-	-	ns
wrb to data hold time	T4	200	-	-	ns
wrd to csb delay time	T5	100	-	-	ns
csb to cdb delay time	T6	100	-	-	ns
Data out stable time	T7	300	-	-	ns
Latch data hold time	T8	0	-	-	ns

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Min.	Max.	Unit
IOA , IOB PAD Supply Voltage	IOVDD5	-0.3	5.5	V
IOC PAD Supply Voltage	VDD	-0.3	3.6	V
Analog Supply Voltage	AVDD3	-0.3	3.6	V
Core Supply Voltage	VDD	-0.3	3.6	V
ESD Protection(HBM)	V_{ESD}	2K	-	V
Operating Temperature Range	T_A	0	+60	℃
Storage Temperature Range	T_{STO}	-50	+150	℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 3.3V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Core Operating Voltage	VDD	2.4	3.3	3.6	V	
IOA, IOB PAD Operating Voltage	IOVDD5	2.4	-	5.5	V	
IOC PAD Operating Voltage	VDD	2.4	3.3	3.6	V	
Analog Operating Voltage	AVDD3	2.4	-	3.6	V	
Operating Current	I_{OP}	-	4.3	6	mA	F_{CPU} = 12MHz @ 3.3V(Typ.), USB OFF
Standby Current	I_{STBY1}	-	3	5	μA	VDD = 3.3V, whole chip with regulator ON
	I_{STBY2}	-	1	3	μA	VDD = 3.3V, whole chip with regulator OFF
Input High Level (IOA,IOB)	V_{IH1}	0.7Vdd	-	-	V	
Input Low Level (IOA,IOB)	V_{IL1}	-	-	0.3Vdd	V	
Input High Level (IOC)	V_{IH2}	0.7Vdd	-	-	V	
Input Low Level (IOC)	V_{IL2}	-	-	0.3Vdd	V	
Output High Current (IOA,IOB)	I_{OH1}	-2	-	-	mA	V_{OH} = 0.9*IOVDD5, IOVDD5=3.3V
		-4	-	-		V_{OH} = 0.9*IOVDD5, IOVDD5=5V
Output Sink Current (IOA,IOB)	I_{OL1}	3	-	-	mA	V_{OL} = 0.1*IOVDD5, IOVDD5=3.3V
		6	-	-		V_{OL} = 0.1*IOVDD5, IOVDD5=5V
Output High Current (IOC)	I_{OH2}	-2	-	-	mA	V_{OH} = 0.9*VDD, VDD=3.3V
Output Sink Current (IOC)	I_{OL2}	3	-	-	mA	V_{OL} = 0.1*VDD, VDD=3.3V
Pull-up Resistor (IOA,IOB)	R_{PU1}	-	170	-	KΩ	Vin = GND, IOVDD5=3.3V
		-	95	-		Vin = GND, IOVDD5=5V
Pull-down Resistor (IOA,IOB)	R_{PD1}	-	160	-	KΩ	Vin = IOVDD5, IOVDD5=3.3V
		-	95	-		Vin = IOVDD5, IOVDD5=5V
Pull-up Resistor(IOC)	R_{PU2}	-	110	-	KΩ	Vin = GND, VDD=3.3V
Pull-down Resistor(IOC)	R_{PD2}	-	130	-	KΩ	Vin = VDD, VDD=3.3V

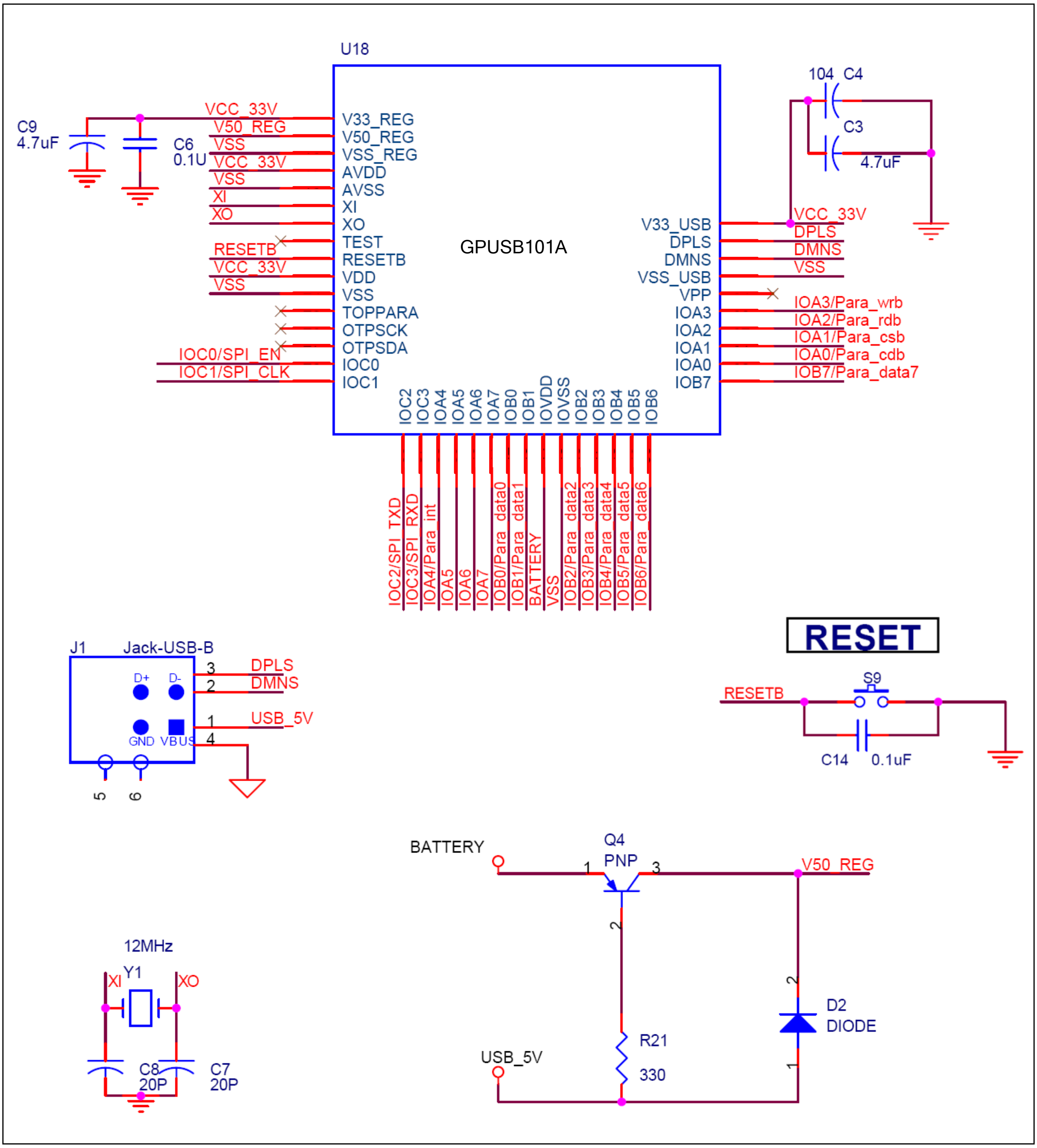
7.3. Regulator Characteristics

Characteristics	Symbol	Unit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage	V50_REG	2.4	-	5.5	V	
Maximum Current Output	IREGO	-	-	60	mA	V50_REG>=3.3V, V_{DROP}<0.2V

Characteristics	Symbol	Unit			Unit	Test Condition
		Min.	Typ.	Max.		
Output Voltage	V33_REG	3.0	3.3	3.6	V	Note1
Drop Voltage	V_{DROP}	-	-	200	mV	V50_REG=3.3V, IREGO=60mA
Standby Current	IREGS	-	-	2	uA	

Note1: When input voltage below 3.3V will limit the output of the regulator to V50_REG- V_{DROP}.

8. APPLICATION CIRCUITS



9. PACKAGE/ORDERING INFORMATION

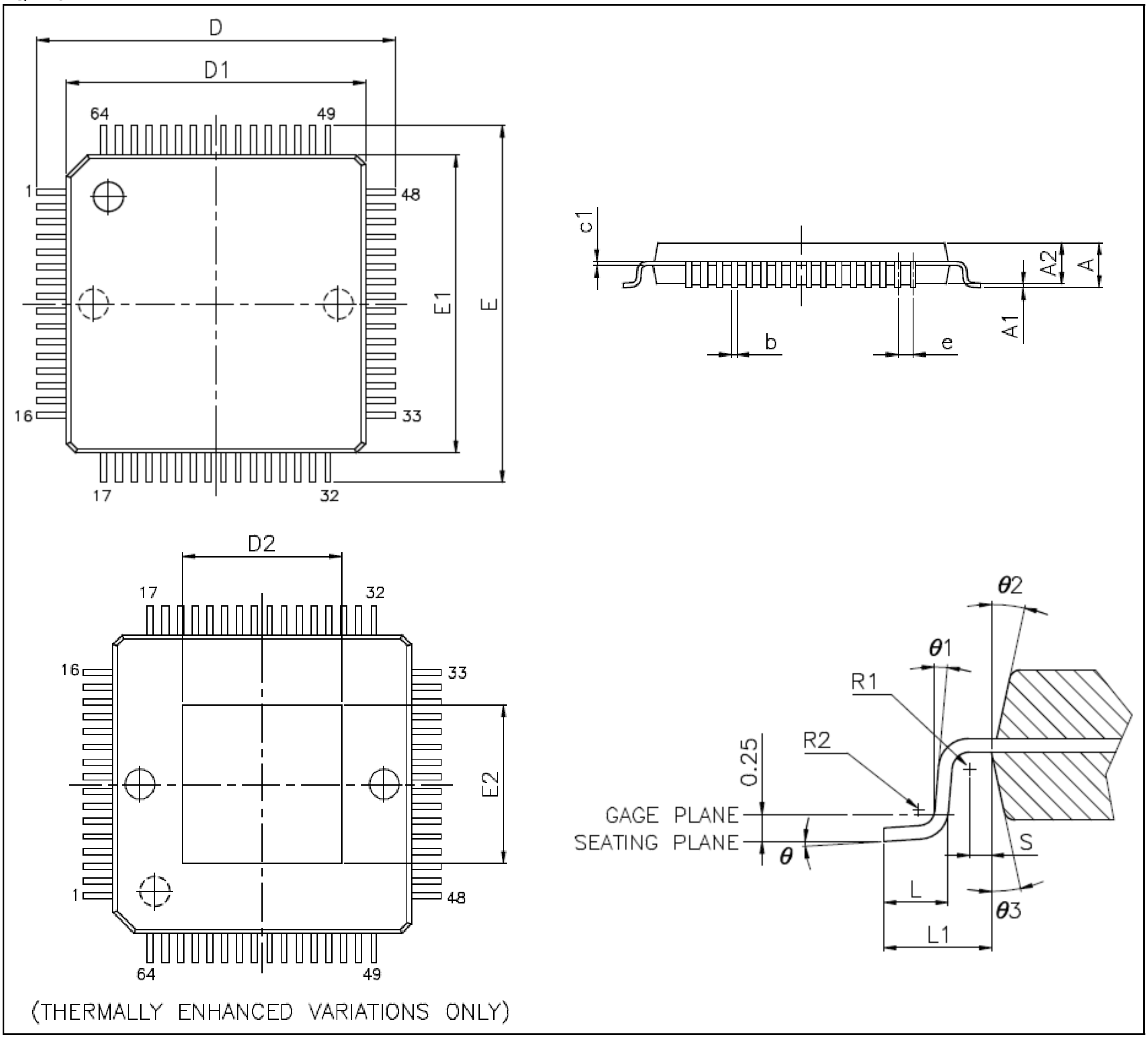
9.1. Ordering Information

Product Number	Package Type
GPUSB101A-NnnV-C	Chip form
GPUSB101A-NnnV-QL02x	Halogen Free 64 pin LQFP Package
GPUSB101A-NnnV-HG02x	Green Package - SSOP 20 (209mil)

Note1: Code number is assigned for customer.
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).
Note3: Package form number (x = 1 - 9, serial number).

9.2. Package Information

LQFP 64



Symbols	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15

Symbols	Min.	Nom.	Max.
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	-	0.16
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
S		0.20 REF	
θ		3.5° REF	
θ1		5.0° REF	
θ2		12° REF	
θ3		12° REF	
R1		0.16 REF	
R2		0.15 REF	

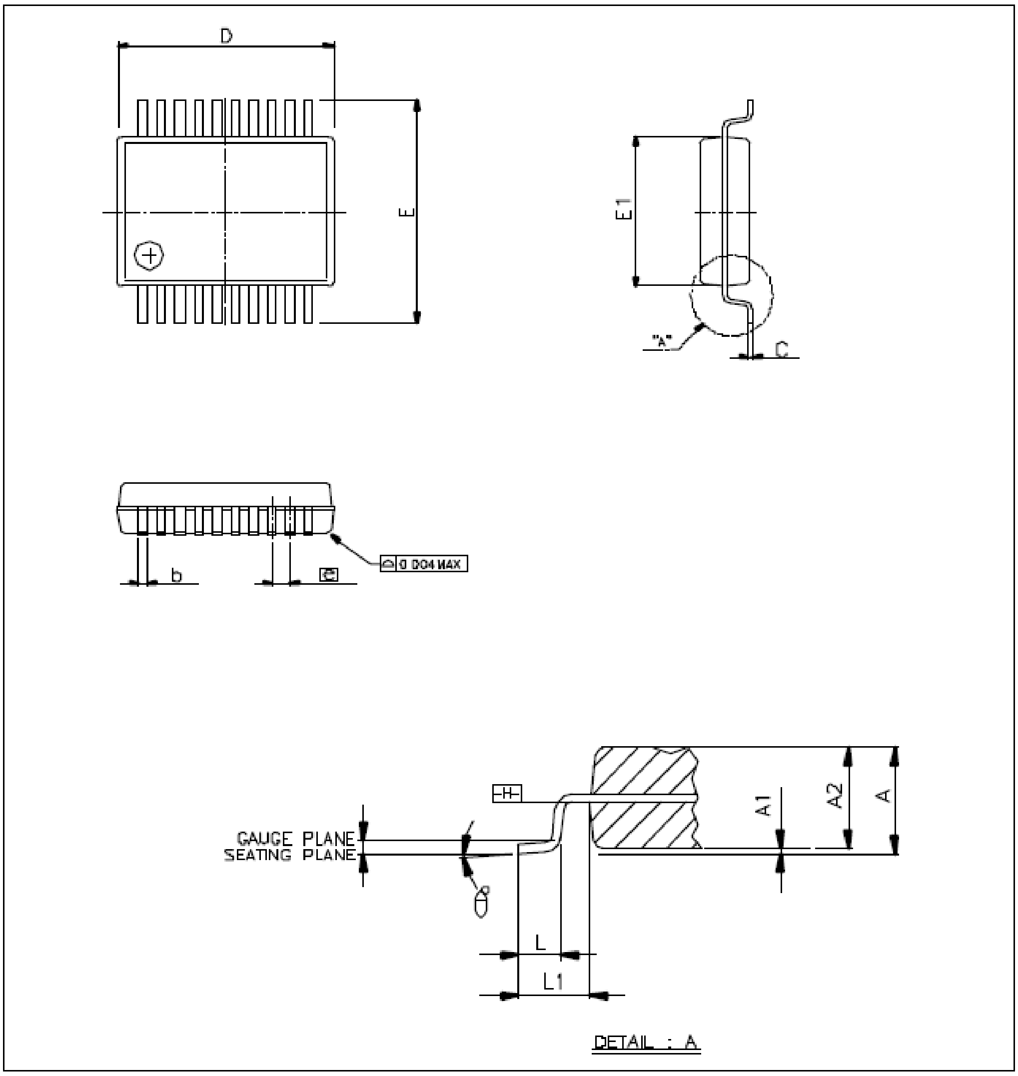
Thermally enhanced dimension(shown in mm)

Pad Size	E2		D2	
	Min.	Max.	Min.	Max.
210x21E	4.27	5.33	4.27	5.33
260x26E	5.28	6.60	5.28	6.60

Notes:

1. JEDEC Outline:
   MS-026 BCD
   MS-026 BCD-HD(Thermally Enhanced Variations Only)
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.

SSOP 20



Symbol	Millimeter		
	Min.	Nom.	Max.
A	--	--	2.0
A1	0.05	--	--
A2	1.65	1.75	1.85
b	0.22	--	0.38
c	0.09	--	0.21
D	6.90	7.20	7.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	0.65 BSC		
L	0.55	0.75	0.95
L1	1.25 REF		
R1	0.09	--	--
θ°	0°	4°	8°

10. GPUSB101A USER'S GUIDE

10.1. Introduction

10.1.1. Features

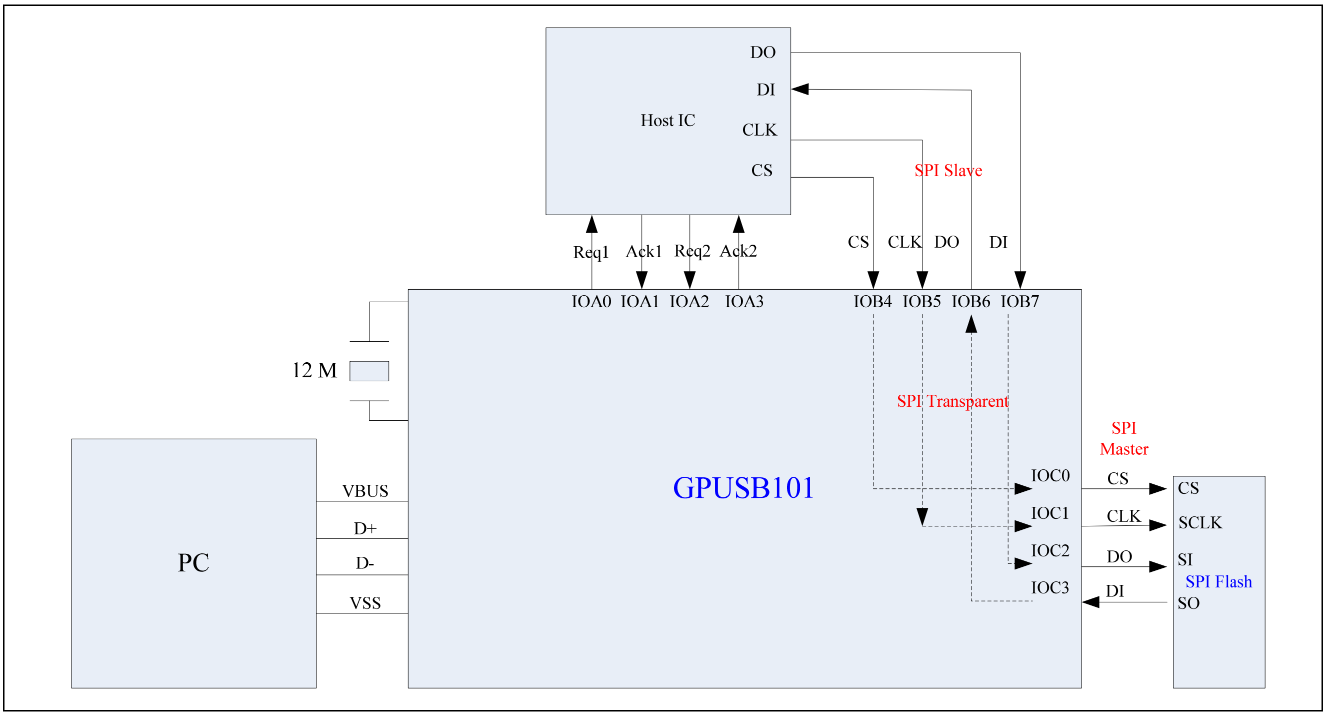
GPUSB101A is a bridge IC which provides the interface between PC and a host controller through USB1.1 Vender Command. When PC detects that GPUSB101A is plugged in, PC will indicate that a new USB device is inserted on device manager, and the PC application can access that new USB device via Generalplus USB driver. In GPUSB101A, there are 4 interfaces to interface with a host controller, including SPI interface, Parallel Bus 8 bit interface, Parallel Bus 4 bit interface, and Software UART. Moreover, the communication protocol between GPUSB101A and PC follows the USB1.1 specification.

By GPUSB101A, PC is able to write, read and erase SPI Flash as a mass storage device and then the host controller can access SPI Flash either through SPI interface of the host controller or through the interfaces of GPUSB101A. Moreover, the application program on PC also can interact with the host controller to perform some applications such as playing songs, driving LEDs or motors through USB vender commands.

Interface	I/O	Function
SPI	8	1. PC Download data to SPI flash 2. PC access HOST IC 3. HOST IC access SPI flash
Parallel 8 bit	13	1. PC Download data to SPI flash 2. PC access HOST IC 3. HOST IC access SPI flash
Parallel 4 bit	9	1. PC Download data to SPI flash 2. PC access HOST IC 3. HOST IC access SPI flash
S/W UART	2	1. PC access HOST IC

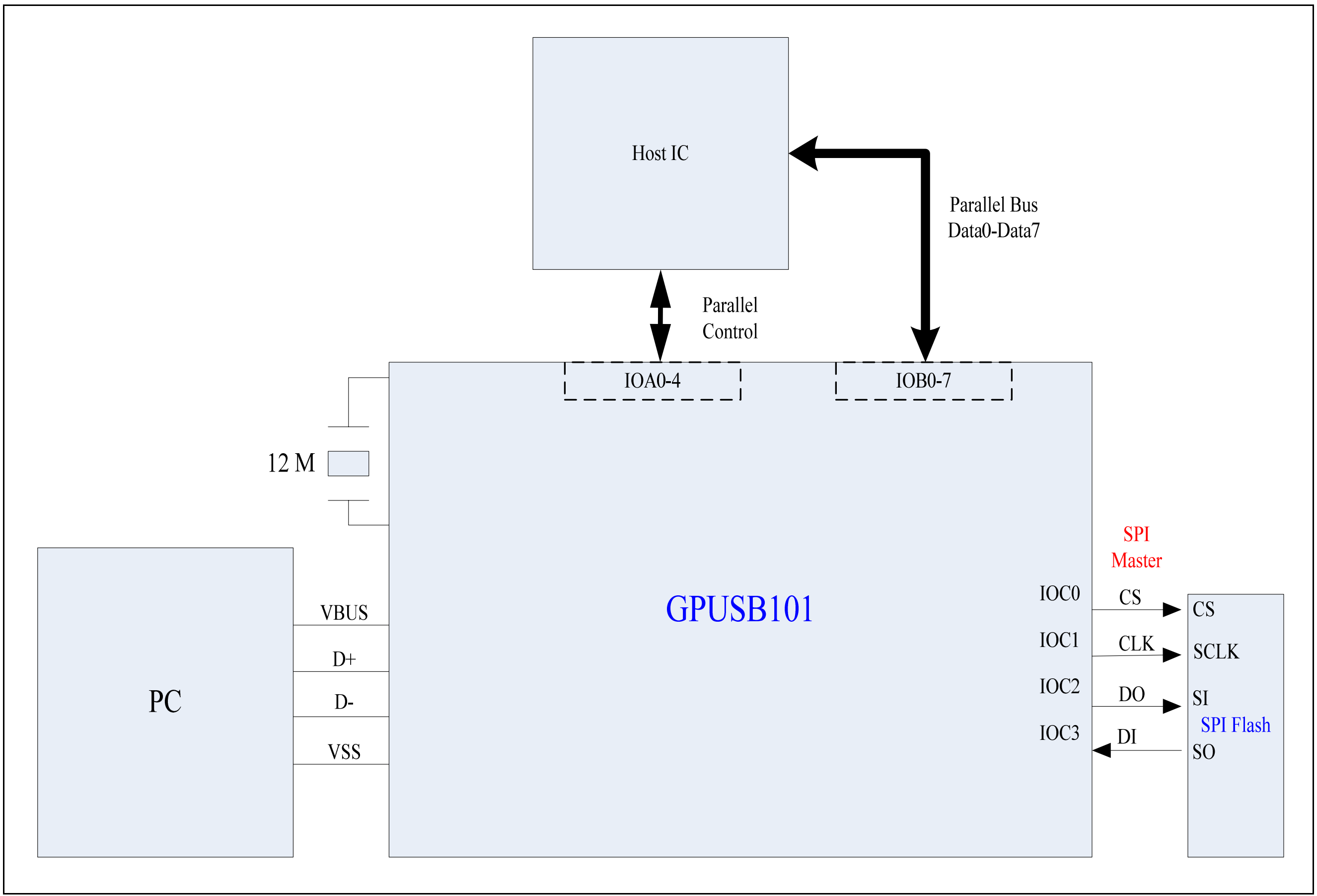
10.2. System Function Diagram

10.2.1. SPI interface: 4 GPIO + 4 SPI



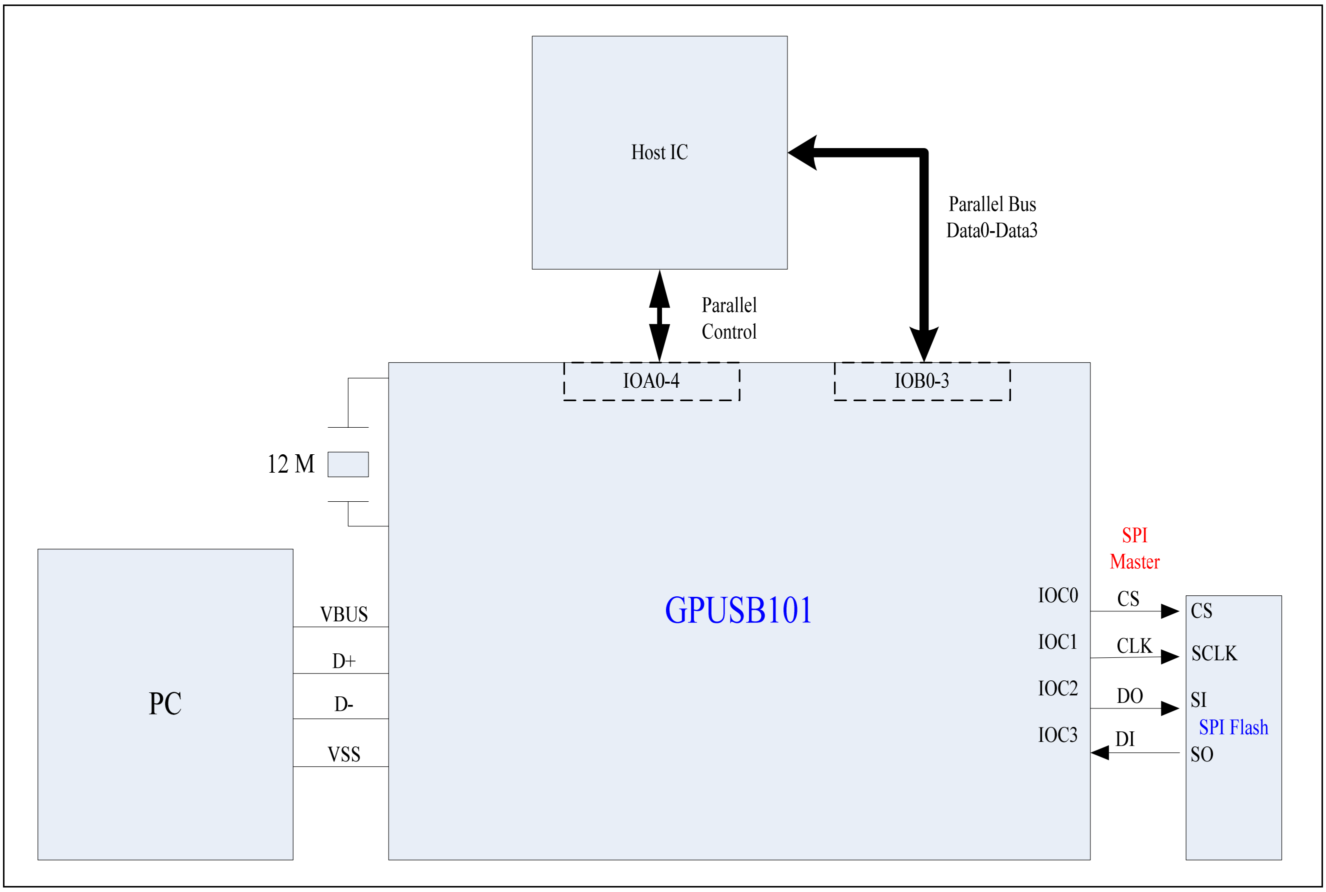
Application	Path	Class	Transfer	Note
Download	PC → GPUSB101A → SPI Master mode → SPI flash	Mass storage	Bulk	Vendor command
PC link Host IC	PC → GPUSB101A → SPI Slave mode → Host IC	Mass storage	Bulk	Vendor command
Host IC access flash	Host IC → SPI/Transparent mode → SPI flash	Mass storage	Bulk	Vendor command

10.2.2. Parallel Bus 8 bit interface: 5 GPIO control pin + 8 GPIO data pin



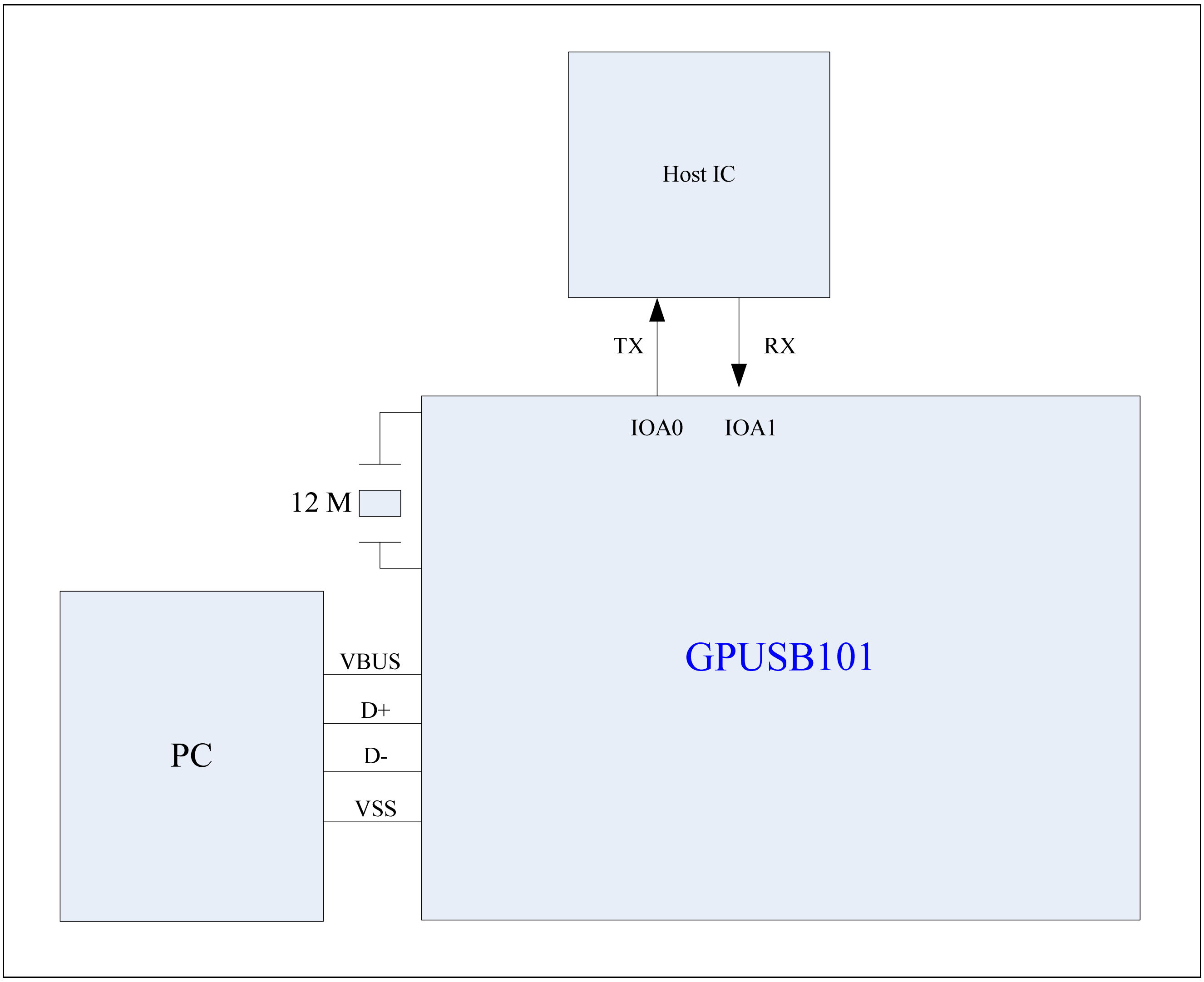
Application	Path	Class	Transfer	Note
Download	PC → GPUSB101A → SPI Master mode → SPI flash	Mass storage	Bulk	Vendor command
PC link Host IC	PC → GPUSB101A → Parallel bus 8 bit → Host IC	Mass storage	Bulk	Vendor command
Host IC access flash	GPIC → Parallel bus 8 bit → GPUSB101A → SPI Master mode → SPI flash	Mass storage	Bulk	Vendor command

10.2.3. Parallel Bus 4 bit interface: 5 GPIO control pin + 4 GPIO data pin



Application	Path	Class	Transfer	Note
Download	PC → GPUSB101A → SPI Master mode → SPI flash	Mass storage	Bulk	Vendor command
PC link Host IC	PC → GPUSB101A → Parallel bus 4 bit → Host IC	Mass storage	Bulk	Vendor command
Host IC access flash	GPIC → Parallel bus 4 bit → GPUSB101A → SPI Master mode → SPI flash	Mass storage	Bulk	Vendor command

10.2.4. Software UART: 2 GPIO pin



Application	Path	Class	Transfer	Note
PC link Host IC	PC → GPUSB101A → I/O(S/W UART) → Host IC	Mass storage	Bulk	Vendor command

10.3. USB Bulk Only Command Protocol

GPUSB101A must receive USB vendor command from USB Host (PC). The command format is following USB mass storage device class command.

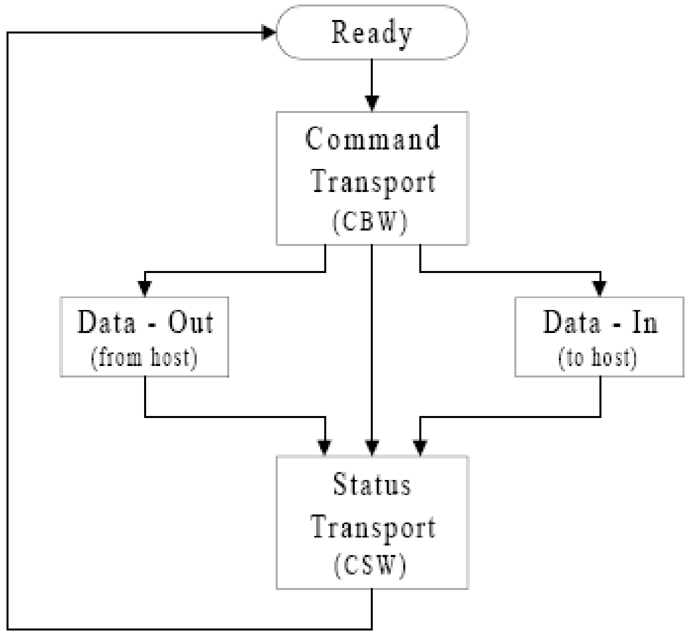


Figure 1 - Command/Data/Status Flow

Figure 1 - Command/Data/Status Flow shows the flow for Command Transport, Data-In, Data-Out and Status Transport. The following sections define Command and Status Transport.

10.3.1. Command Block Wrapper (CBW)

The CBW shall start on a packet boundary and shall end as a short packet with exactly 31 (1Fh) bytes transferred. Fields appear aligned to byte offsets equal to a multiple of their byte size. All subsequent data and the CSW shall start at a new packet boundary. All CBW transfers shall be ordered with the LSB (byte 0) first (little endian). Refer to the USB Specification Terms and Abbreviations for clarification.

bit / Byte	7	6	5	4	3	2	1	0
0-3	*dCBWSignature*							
4-7	*dCBWTag*							
8-11 (08h-0Bh)	*dCBWDataTransferLength*							
12 (0Ch)	*bmCBWFlags*							
13 (0Dh)	Reserved (0)				*bCBWLUN*			
14 (0Eh)	Reserved (0)			*bCBWCBLength*				
15-30 (0Fh-1Eh)	*CBWCB*							

TABLE 7.3.1. Command Block Wrapper

dCBWSignature:

Signature that helps identify this data packet as a CBW. The signature field shall contain the value 43425355h (little endian), indicating a CBW.

dCBWTag:

A Command Block Tag sent by the host. The device shall echo the contents of this field back to the host in the dCSWTag field of the associated CSW. The dCSWTag positively associates a CSW with the corresponding CBW.

dCBWDataTransferLength:

The number of bytes of data that the host expects to transfer on the Bulk-In or Bulk-Out endpoint (as indicated by the Direction bit) during the execution of this command. If this field is zero, the device and the host shall transfer no data between the CBW and the associated CSW, and the device shall ignore the value of the Direction bit in bmCBWFlags.

bmCBWFlags:

The bits of this field are defined as follows:
Bit 7 Direction - the device shall ignore this bit if the dCBWDataTransferLength field is zero, otherwise:
0 = Data-Out from host to the device,
1 = Data-In from the device to the host.
Bit 6 Obsolete. The host shall set this bit to zero.
Bits 5...0 Reserved - the host shall set these bits to zero.

bCBWLUN:

The device Logical Unit Number (LUN) to which the command block is being sent. For devices that support multiple LUNs, the host shall place into this field the LUN to which this command block is addressed. Otherwise, the host shall set this field to zero.

bCBWCBLength:

The valid length of the CBWCB in bytes. This defines the valid length of the command block. The only legal values are 1 through 16 (01h through 10h). All other values are reserved.

CBWCB:

The command block to be executed by the device. The device shall interpret the first bCBWCBLength bytes in this field as a command block as defined by the command set identified by bInterfaceSubClass. If the command set supported by the device uses command blocks of fewer than 16 (10h) bytes in length, the significant bytes shall be transferred first, beginning with the byte at offset 15 (Fh). The device shall ignore the content of the CBWCB field past the byte at offset (15 + bCBWCBLength - 1).

10.3.2. Command Status Wrapper (CSW)

The CSW shall start on a packet boundary and shall end as a short packet with exactly 13 (0Dh) bytes transferred. Fields appear aligned to byte offsets equal to a multiple of their byte size. All CSW transfers shall be ordered with the LSB (byte 0) first (little endian). Refer to the USB Specification Terms and Abbreviations for clarification.

bit / Byte	7	6	5	4	3	2	1	0
0-3	*dCSWSignature*							
4-7	*dCSWTag*							
8-11 (8-Bh)	*dCSWDataResidue*							
12 (Ch)	*bCSWStatus*							

TABLE 7.3.2. Command Status Wrapper

dCSWSignature:

Signature that helps identify this data packet as a CSW. The signature field shall contain the value 53425355h (little endian), indicating CSW.

dCSWTag:

The device shall set this field to the value received in the dCBWTag of the associated CBW.

dCSWDataResidue:

For Data-Out the device shall report in the dCSWDataResidue the difference between the amounts of data expected as stated in the dCBWDataTransferLength, and the actual amount of data processed by the device. For Data-In the device shall report in the dCSWDataResidue the difference between the amount of data expected as stated in the dCBWDataTransferLength and the actual amount of relevant data sent by the device. The dCSWDataResidue shall not exceed the value sent in the dCBWDataTransferLength.

bCSWStatus:

bCSWStatus indicates the success or failure of the command. The device shall set this byte to zero if the command completed successfully. A non-zero value shall indicate a failure during command execution according to the following table:

Value	Description
00h	Command Passed ("good status")
01h	Command Failed
02h	Phase Error
03h and 04h	Reserved (Obsolete)
05h to FFh	Reserved

10.4. Vender Command

PC <-> GPUSB

Command Block Wrapper 15th byte-30th byte

Byte Bit	7	6	5	4	3	2	1	0
0	Operation Code							
1								
2	(MSB) Reserved							
3								
4								
5								
6								
7	(MSB) Transfer Length							
8								
9								
10								
11								

Command	OP Code	Description
Get IC Version	F0 10	Generalplus verify
SPI Flash Read	FD 28	SPI Flash physical read
SPI Flash Write	FD 2A	SPI Flash physical write
SPI Flash Sector Erase	FD 20	SPI Flash sector erase, erase size = 64K Bytes
SPI Flash Chip Erase	FD FF	SPI Flash sector erase, erase size = 4M Bytes
Set Vender ID	FF F0	Generalplus verify
Reserved write	Ex xx.	PC write data to Host IC
Reserved read	Dx xx	PC read data from Host IC

10.4.1. Get IC version

Command Block Wrapper 15th byte-30th byte

Byte Bit	7	6	5	4	3	2	1	0
0	**F0 10**							
1								
2	(MSB) **Reserved**							
3								
4								
5								
6								
7	(MSB) **Reserved**							
8								
9								
10								
11								

Operation Code	Function	Comment
0xF010	Set vendor ID	*CBW Byte 15: 0xF0 *CBW Byte 16: 0x10 *CBW Byte 29-30: GP Tag
		*IN 11 Bytes for IC Version information

10.4.2. SPI Flash Read

Command Block Wrapper 15th byte-30th byte

Byte Bit	7	6	5	4	3	2	1	0
0	**FD 28**							
1								
2	(MSB) **LBA (Logical Block Address)**							
3								
4								
5								
6	06							
7	(MSB) **Transfer Length (scoters)**							
8								
9								
10								
11								

1 scoters = 512 bytes

Operation Code	Function	Comment
0XFD28	SPI flash Physical Read	*CBW Byte 15: 0XFD *CBW Byte 16: 0x28 *CBW Byte 17: High word High byte Address *CBW Byte 18: High word Low byte Address *CBW Byte 19: Low word High byte Address *CBW Byte 20: Low word Low byte Address *CBW Byte 21: 0x06. it mean SPI Nor Flash *CBW Byte 22: High Operation Data Length *CBW Byte 23: Low Operation Data Length *CBW Byte 29-30: GP Tag

10.4.3. SPI Flash Write

Command Block Wrapper 15th byte-30th byte

Byte Bit	7	6	5	4	3	2	1	0
0	**FD 2A**							
1								
2	(MSB) **LBA (Logical Block Address)**							
3								
4								
5								
6	06							
7	(MSB) **Transfer Length (sectors)**							
8								
9								
10								
11								

1 sectors = 512 bytes

Operation Code	Function	Comment
0XFD2A	SPI flash Physical Write	*CBW Byte 15: 0xFD *CBW Byte 16: 0x2A *CBW Byte 17: High word High byte Address *CBW Byte 18: High word Low byte Address *CBW Byte 19: Low word High byte Address *CBW Byte 20: Low word Low byte Address *CBW Byte 21: 0x06 .it mean SPI NorFlash *CBW Byte 22: High Operation Data Length *CBW Byte 23: Low Operation Data Length *CBW Byte 29-30: GP Tag

10.4.4. SPI Flash Sector Erase

Command Block Wrapper 15th byte-30th byte

Byte Bit	7	6	5	4	3	2	1	0
0	**FD 20**							
1								
2	(MSB) **LBA (Logical Block Address)**							
3								
4								
5								
6	06							
7	(MSB) **Transfer Length (sectors)**							
8								
9								
10								
11								

1 sectors = 512 bytes

Operation Code	Function	Comment
0XFD20	SPI flash Physical scoter erase, erase size = 64K Bytes(GPR25L320A)	*CBW Byte 15: 0xFD *CBW Byte 16: 0x20 *CBW Byte 17: High word High byte Address *CBW Byte 18: High word Low byte Address *CBW Byte 19: Low word High byte Address *CBW Byte 20: Low word Low byte Address *CBW Byte 21: 0x06 .it mean SPI Nor Flash *CBW Byte 22: High Operation Data Length *CBW Byte 23: Low Operation Data Length *CBW Byte 29-30: GP Tag

10.4.5. SPI Flash Chip Erase

Command Block Wrapper 15th byte-30th byte

Byte Bit	7	6	5	4	3	2	1	0
0	**FD FF**							
1								
2	(MSB) **LBA (Logical Block Address)**							
3								
4								
5								
6	06							
7	(MSB) **Transfer Length (sectors)**							
8								
9								
10								
11								

1 sectors = 512 bytes

Operation Code	Function	Comment
0XFDFF	SPI flash Physical scoter erase, erase size = 4MBytes(GPR25L320A)	*CBW Byte 15: 0xFD *CBW Byte 16: 0xFF *CBW Byte 17: High word High byte Address *CBW Byte 18: High word Low byte Address *CBW Byte 19: Low word High byte Address *CBW Byte 20: Low word Low byte Address *CBW Byte 21: 0x06 .it mean SPI Nor Flash *CBW Byte 22: High Operation Data Length *CBW Byte 23: Low Operation Data Length *CBW Byte 29-30: GP Tag

10.4.6. Set Vender ID

Command Block Wrapper 15th byte-30th byte

Byte Bit	7	6	5	4	3	2	1	0
0	**FF F0**							
1								
2	(MSB) **Reserved**							
3								
4								
5								
6								
7	(MSB) **Transfer Length (bytes)**							
8								
9								
10								
11								

Operation Code	Function	Comment
0xFFF0	Set vendor ID	*CBW Byte 15: 0xFF *CBW Byte 16: 0xF0 *CBW Byte 29-30: GP Tag
		*IN 10 Bytes for IC Version information

This command can make sure Generalplus device.

10.4.7. Reserved write

Command Block Wrapper 15th byte-30th byte

Byte Bit	7	6	5	4	3	2	1	0
0	EX XX							
1								
2	(MSB) Reserved							
3								
4								
5								
6								
7	(MSB) Reserved							
8								
9								
10								
11								

Operation Code	Function	Comment
0xEX XX	Reserved write	*CBW Byte 15: 0xEX *CBW Byte 16: 0xXX *CBW Byte 29-30: GP Tag

Example:

1. Application: PC + GPUSB101A + GPF8
2. PC issue customer command 0xE000 to GPF8
3. *CBW Byte 15 = 0xE0 & *CBW Byte 16 = 0x00,
4. GPUSB101A will transfer two bytes data 0xE0, 0x00 to GPF8, and then continue transfer N bytes data to GPF8. N = CBW Byte 8-11 **dCBWDataTransferLength:**

10.4.8. Reserved Read

Command Block Wrapper 15th byte-30th byte

Byte Bit	7	6	5	4	3	2	1	0
0	DX XX							
1								
2	(MSB) Reserved							
3								
4								
5								
6								
7	(MSB) Reserved							
8								
9								
10								
11								

Operation Code	Function	Comment
0xDX XX	Reserved read	*CBW Byte 15 :0xDX *CBW Byte 16 :0xXX *CBW Byte 29-30: GP Tag

Example:

1. Application: PC + GPUSB101A + GPF8
2. PC issue to read GPF8 status
3. *CBW Byte 15 = 0xD0 & *CBW Byte 16 = 0x00,
4. GPUSB101A will transfer two bytes data 0xD0, 0x00 to GPF8, and then continue transfer N bytes data from GPF8. N = CBW Byte 8-11 **dCBWDataTransferLength**:

10.5. GPUSB Interface Protocol Command List

GPUSB -> Host IC

Command	OP Code	Description
USB Plug in	C0 00	USB plug in issue
PC suspend	C0 01	USB Plug out or PC suspend issue
PC resume	C0 02	PC resume issue
Vender command Write	EX XX	Customer define
Vender command Read	DX XX	Customer define

Example Vender command Write

1. E0 00: KEY 1 (PC issue PLAY)
2. E0 01: KEY 2 (PC issue NEXT)
3. E0 02: KEY 3 (PC issue PREVIOUS)

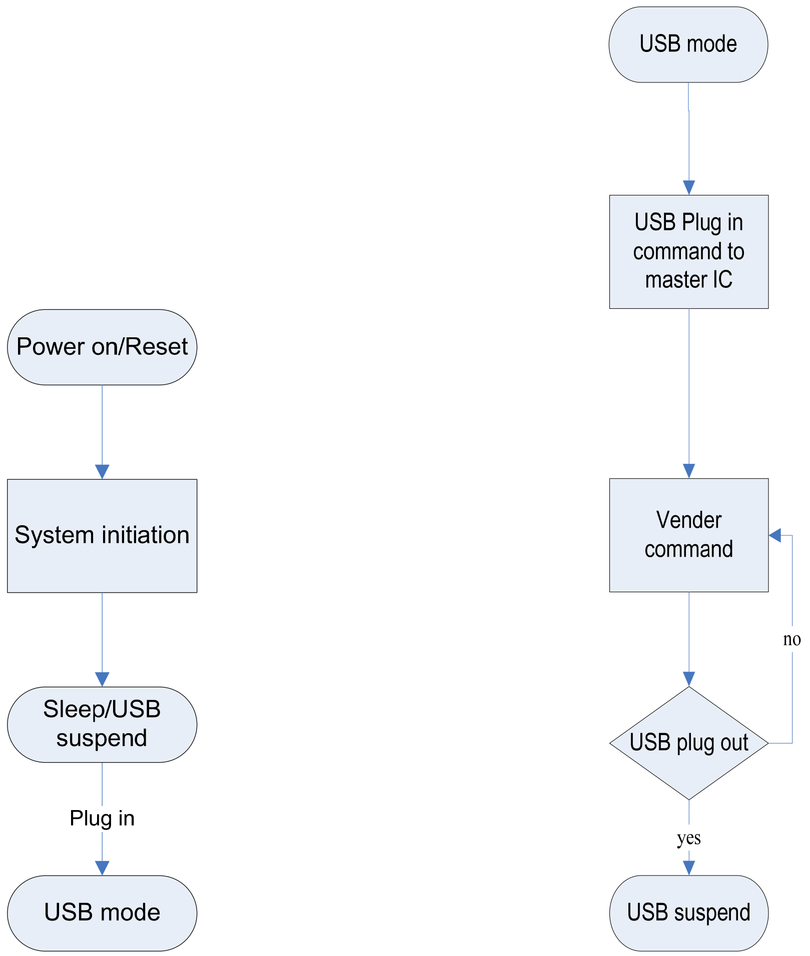
Example Vender command Read

1. D0 00: status1 (PC read Host IC I/O status)
2. D0 01: status2 (PC read Host IC Program status)

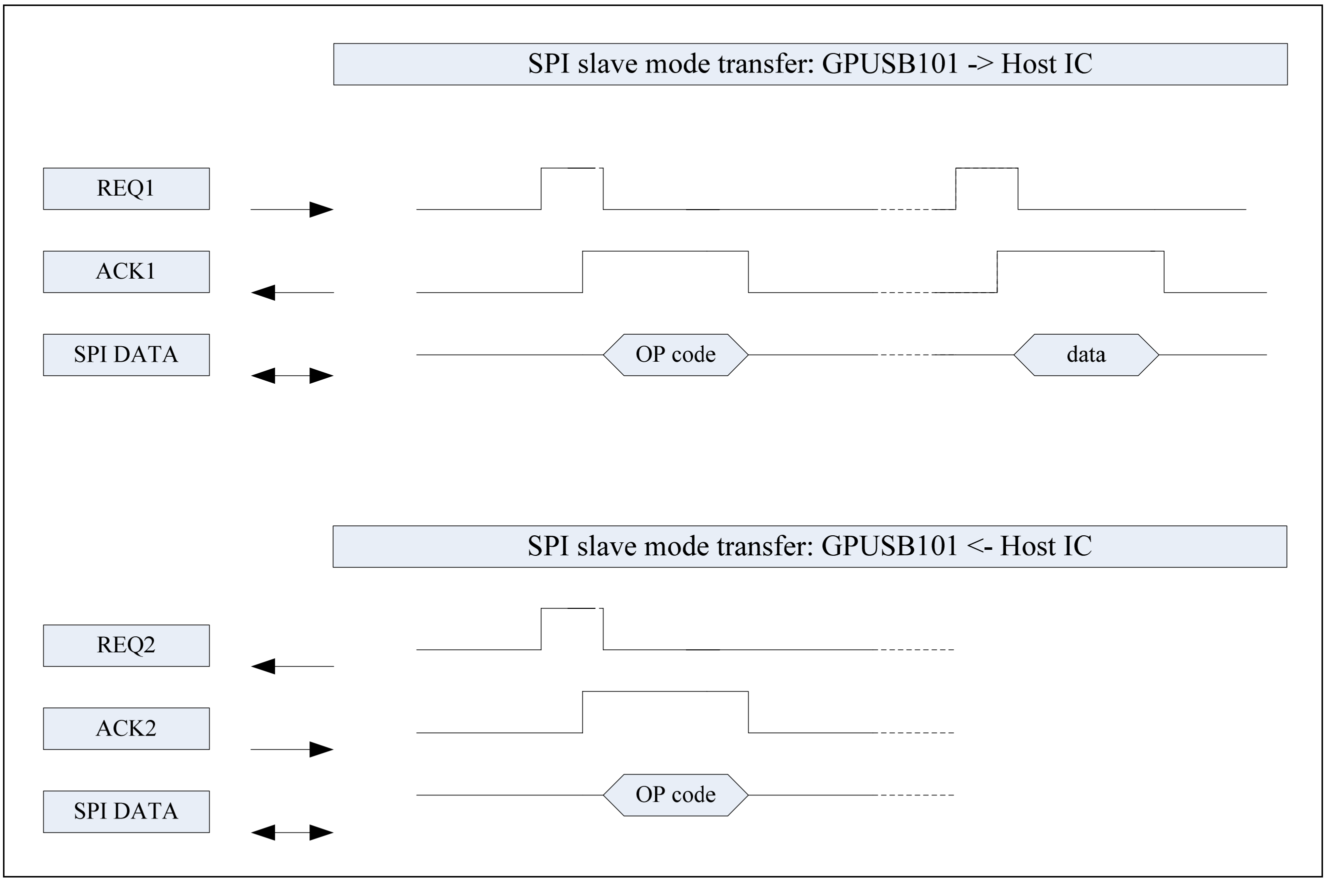
Host IC -> GPUSB

Command	OP Code	Description
SPI transparent mode	B0 01	Host IC issue GPUSB101A SPI transparent mode

10.6. GPUSB Program Flow



10.6.1. SPI interface protocol



Example

1. If GPUSB101A command Host IC to do something, op code = E0 01, Data = 12H, 34H, 56H, 78H
2. GPUSB101A command REQ1 = Hi, and wait Ack1 = Hi (when Host IC receive REQ1 = Hi, Host IC must stop access SPI Flash data, and command ACK1 = Hi)
3. When Ack1 = Hi, GPUSB101A will issue SPI Slave mode and command REQ1 = Low
4. Then Host IC can start SPI TX protocol, and latch two bytes OP CODE = E0 01, command ACK1 = low
5. GPUSB101A continue command REQ1 = Hi, wait Ack1 = Hi
6. Host IC command ACK1 = Hi, GPUSB101A command REQ1 = Low
7. Then Host IC can start SPI TX protocol, and latch four bytes data =12H, 34H, 56H, 78H, command ACK1 = low
8. OP code must be two bytes, data transfer max = 64bytes/frame

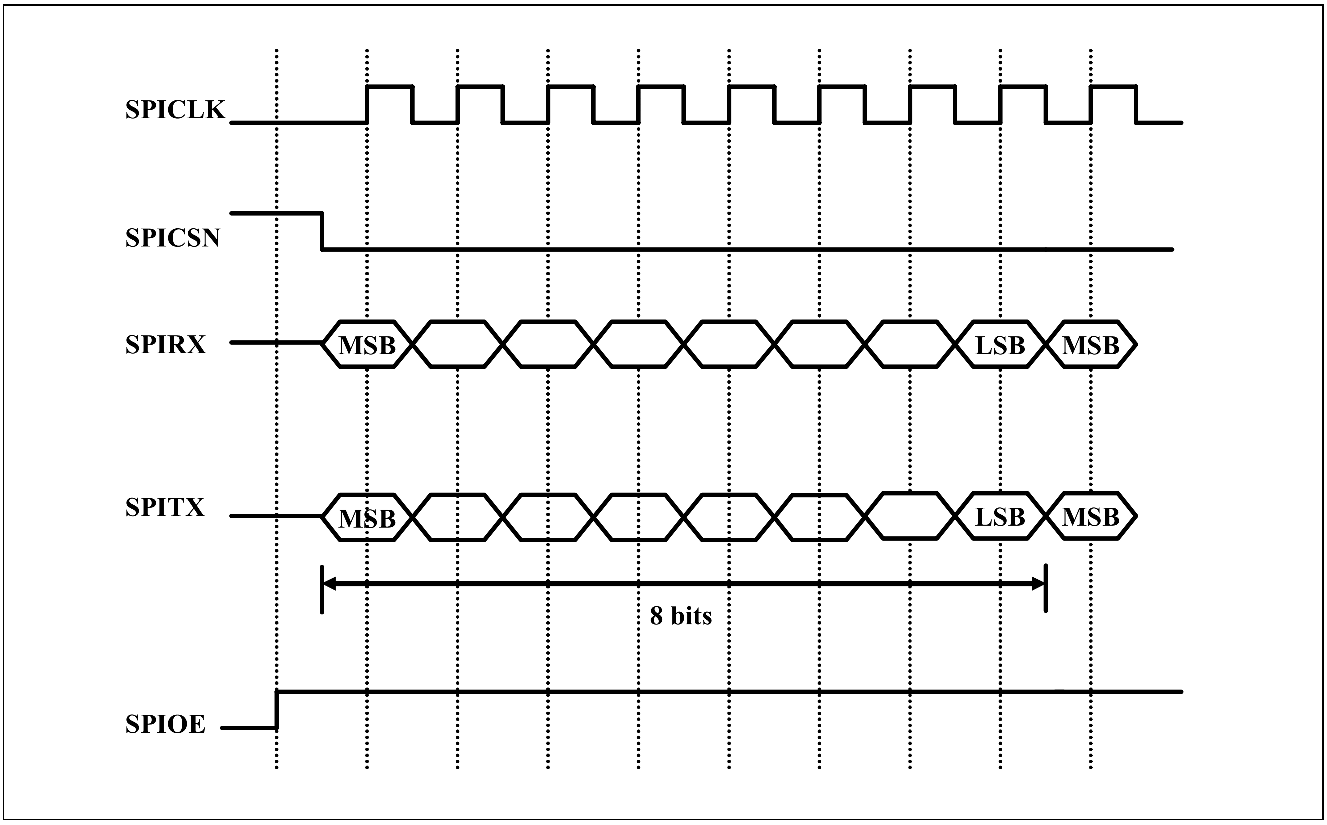
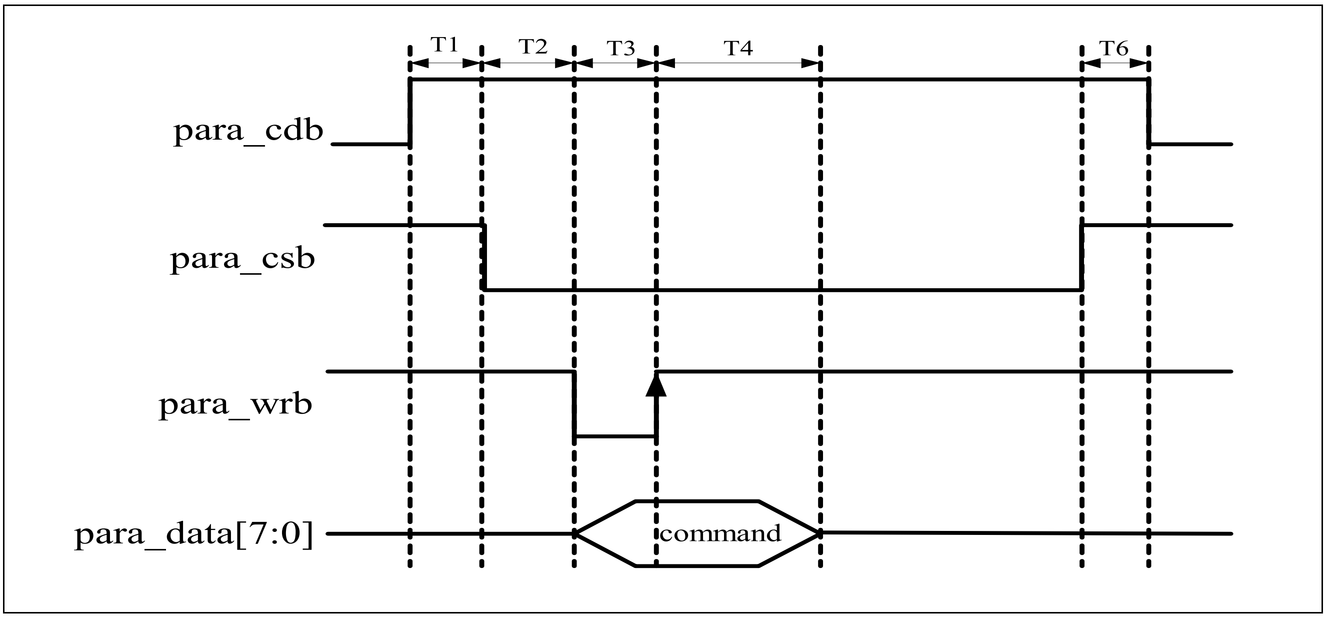


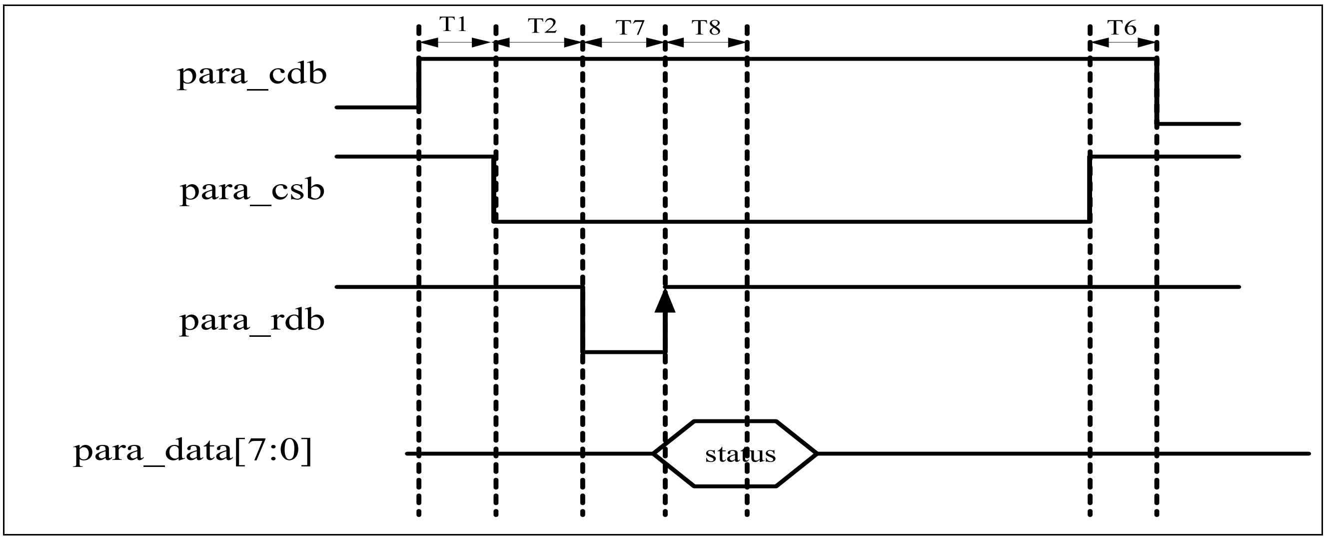
Fig1. Master Mode, SPO = 0, SPH = 0

10.6.2. Parallel bus 8 bit mode

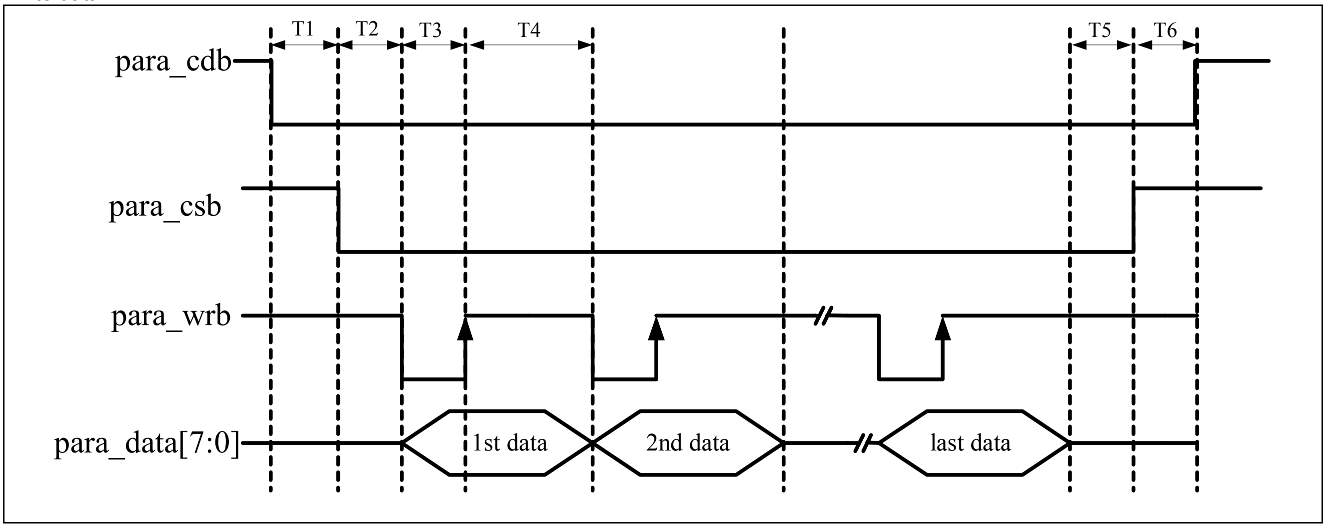
Write command:



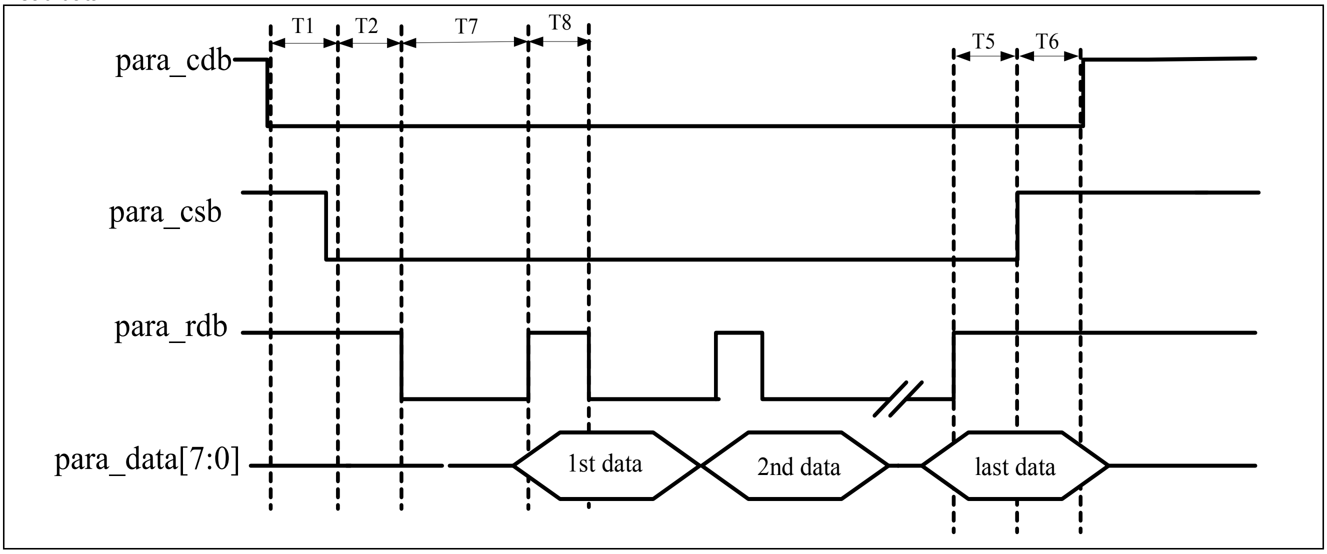
Read status:



Write data:

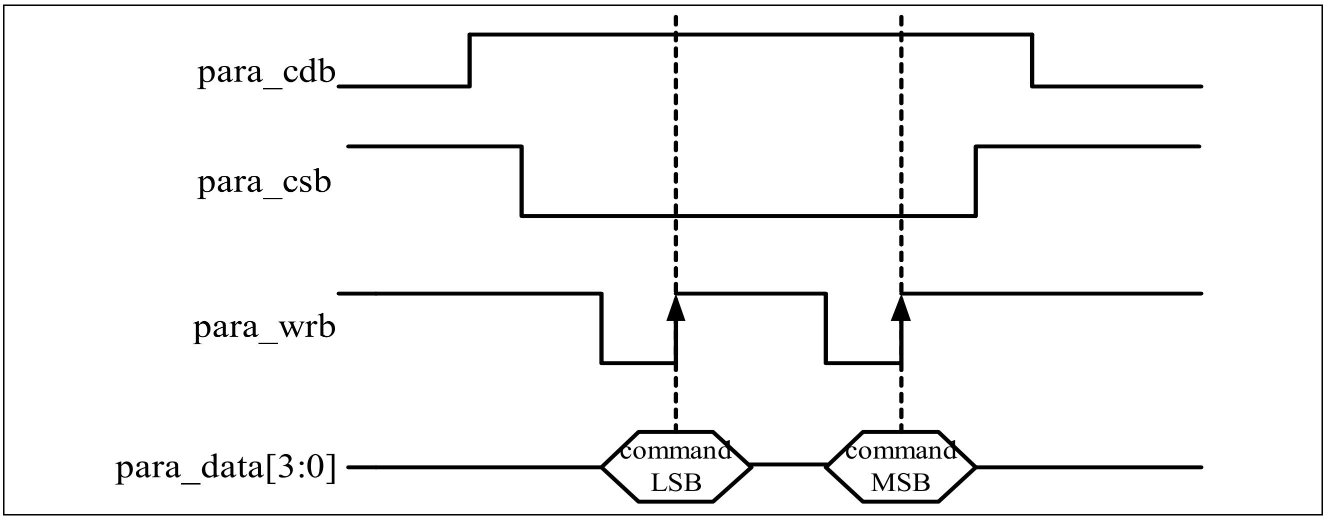


Read data:

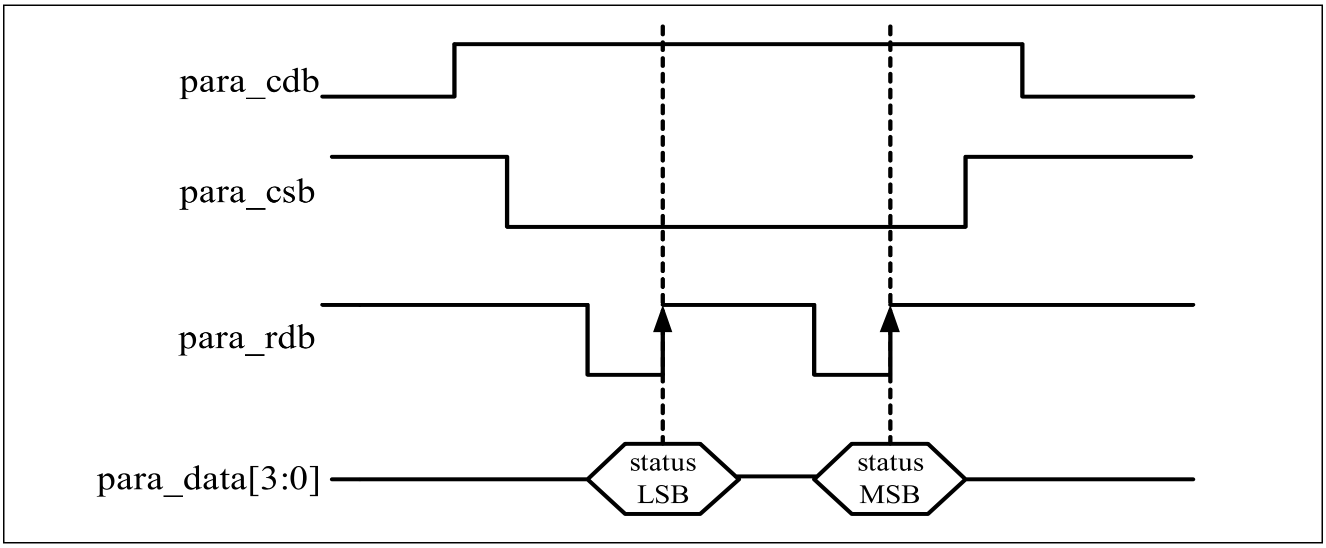


10.6.3. Parallel bus 4 bit mode

Write command:

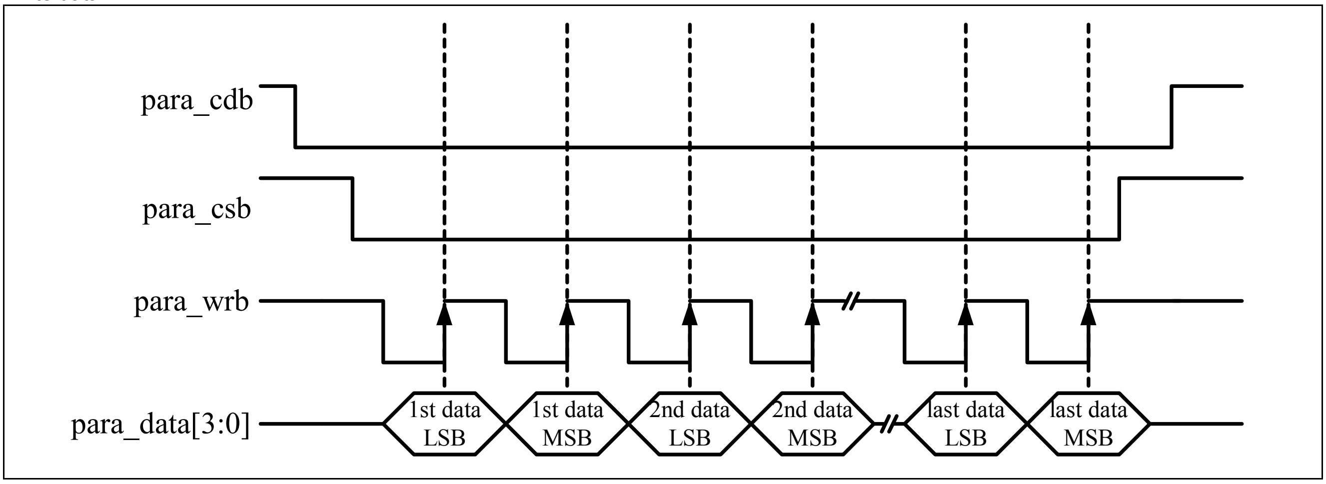


Read status:

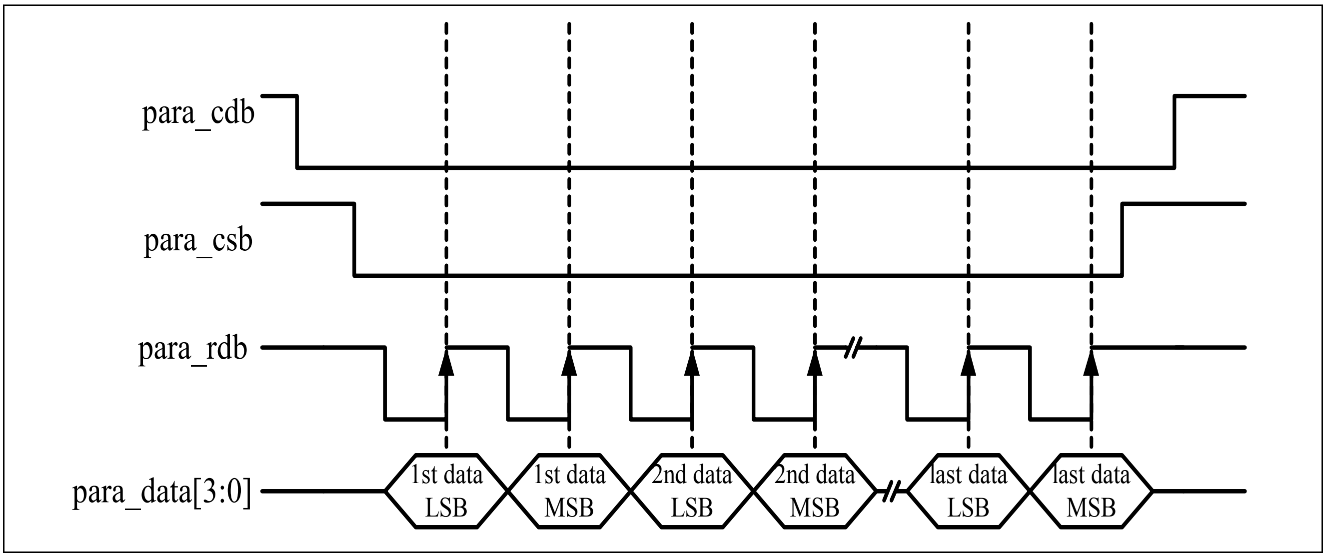


Note: After Para_rdb falling edge, para_data is output until para_csb rising edge.

Write data:



Read data:



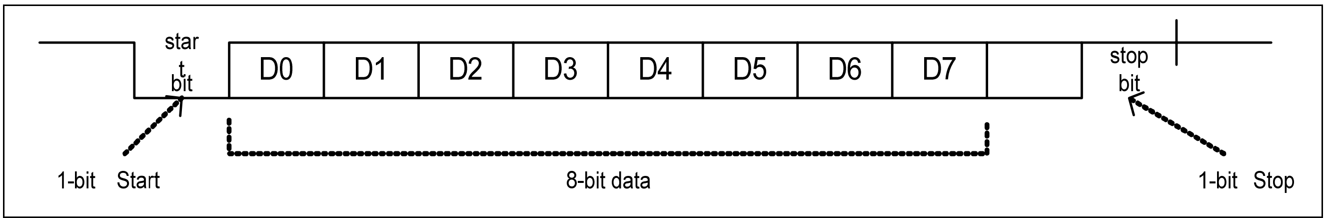
Timing constrain

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
cdb to csb delay time	T1	100	-	-	ns
csb to wrb(rdb) delay time	T2	100	-	-	ns
wrb to data setup time	T3	100	-	-	ns
wrb to data hold time	T4	200	-	-	ns
wrd to csb delay time	T5	100	-	-	ns
csb to cdb delay time	T6	100	-	-	ns
Data out stable time	T7	300	-	-	ns
Latch data hold time	T8	0	-	-	ns

Note: The 4 bit mode time constrain is the same as 8 bit mode.

10.6.4. S/W UART mode

UART Data Frame Format



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12. REVISION HISTORY

Date	Revision #	Description	Page
SEP 24, 2014	1.4	1. Modify section 5.2 Pin Map. 2. Modify section 9.1 Ordering Information. 3. Modify section 9.2 Package Information.	7 15 16
MAY 13, 2011	1.3	Modify 6.4.2 The function of parallel bus.	9
MAR. 18, 2010	1.2	Modify 10.1.1 Features.	15
JUN. 13, 2008	1.1	1. Add pin description of VDD power range. 2. Add section 5.2 Pin Map. 3. Modify section 7.2 DC Characteristics of I_{OH}, I_{OL}, R_{PU} & R_{PD}. 4. Add section 7.3 Regulator Characteristics. 5. Modify section 9.1 Ordering Information. 6. Add section 9.2 Package Information.	5 6 10 11 13 13
JAN. 30, 2008	1.0	1. Modify section 5. SIGNAL DESCRIPTIONS. 2. Modify section 5.1 PAD Assignment.	5 6
OCT. 23, 2007	0.1	Original	33