DATA SHEET

![Generalplus logo]

GPY0029B

Linear Regulator

JAN. 19, 2010

Version 1.4

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LINEAR REGULATOR

1. GENERAL DESCRIPTION

The GPY0029B is a voltage regulator IC with ultra-low quiescent current and low voltage detection by CMOS process.   It operates to +7.0V input range and delivers up to 150mA.

2. APPLICATION

- Battery-powered equipment
- Hand-held communication equipment
- Audio/Video system
- Toys

3. FEATURES

- Low Quiescent Current (Typ. 3µA @ V_{OUT} = 3.0V/3.3V, V_{IN} = 5.0V)
- High Current Driving Capability
  (Typ. 150mA @ V_{OUT} = 3.0V/3.3V, V_{IN} = 5.0V)
- Over Current Limitation (Typ. 300mA @ V_{OUT} = 3.0V/3.3V, V_{IN} = 5.0V)
- Small Dropout Voltage (Typ. 40mV @ V_{OUT} = 3.0V/3.3V, I_{OUT} = 1.0mA)
- Low Temperature-Drift Coefficient of Output Voltage
  (Typ. ±50ppm/^{0}C)
- Excellent Line Regulation (Typ. 0.15%/V)
- High Accuracy Output Voltage (±3%)
- RESET output pin for low V_{IN} and low V_{OUT} detection
- Only One 10µF Capacitor Required (ESR Range : 0.5 ~ 5 Ω)
- Three pin Types of Package or Dice Form

4. BLOCK DIAGRAM

GPY0029B
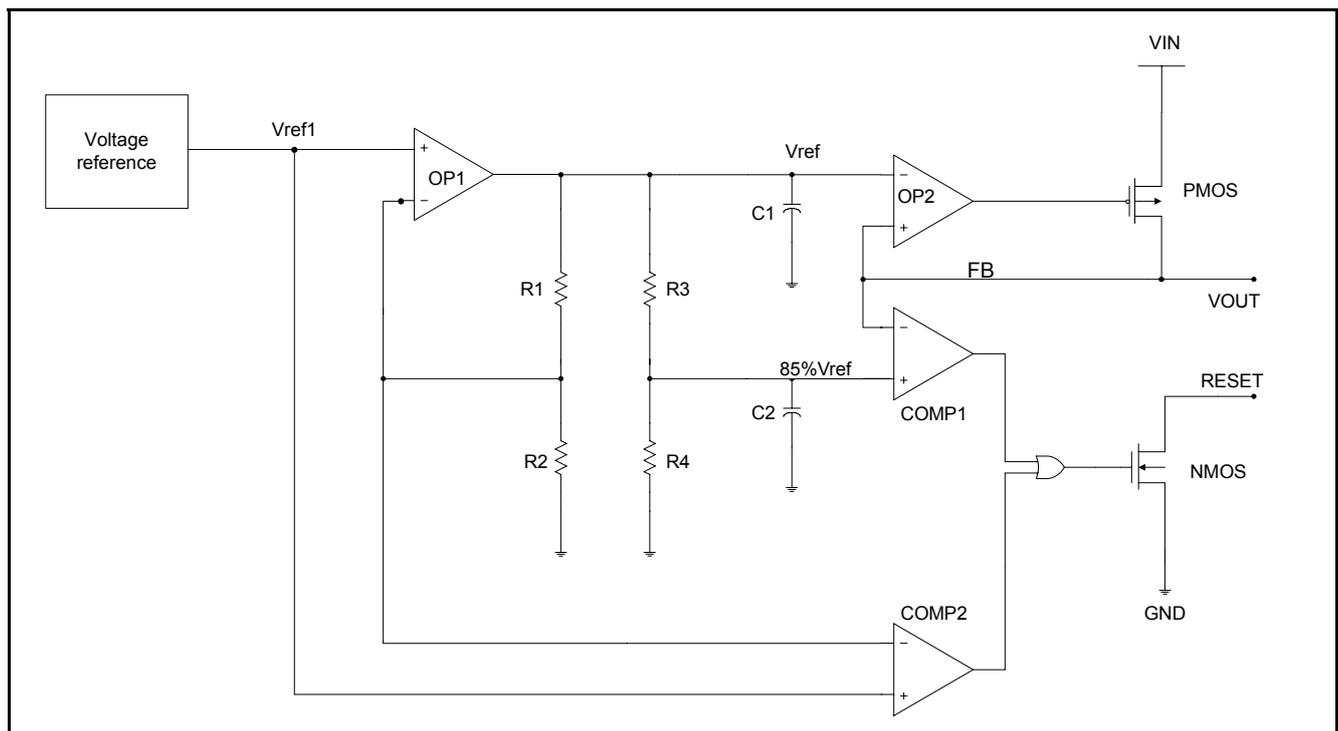
5. SIGNAL DESCRIPTIONS

5.1. 4 PIN Only For Chip On Board (COB)

Mnemonic	PIN No.	PAD No.	Type	Description
RESET	1	5	O	Open Drain Reset Output, Low Reset
GND	2	4	G	Chip Ground
VOUT	3	2	O	Output Regulated Voltage
VIN	4	1	I	Input Voltage
FB	3	3	I	Regulator Feedback Input. FB pad must be bonded to VOUT pin

5.2. 3 PIN (SOT-89)

Mnemonic	PIN No.	Type	Description
GND	1	G	Chip Ground
VIN	2	I	Input Voltage
VOUT	3	O	Output Regulated Voltage

5.3. PIN Configuration
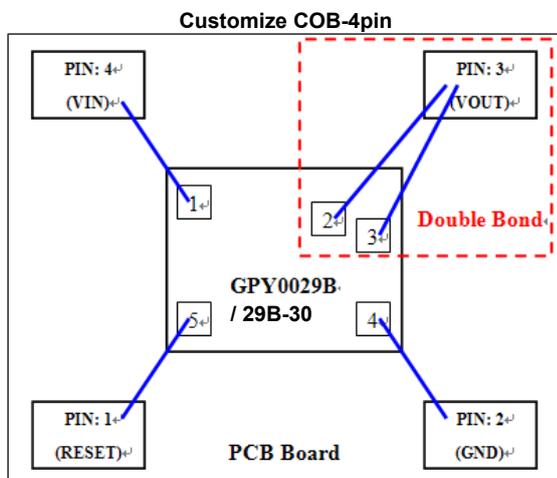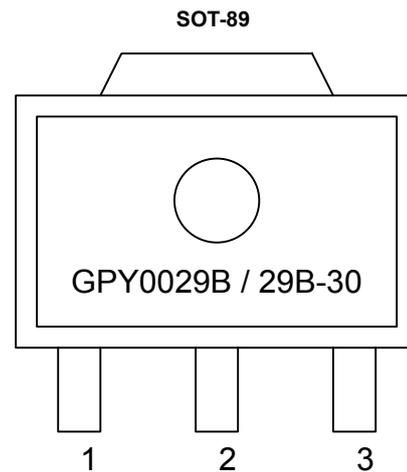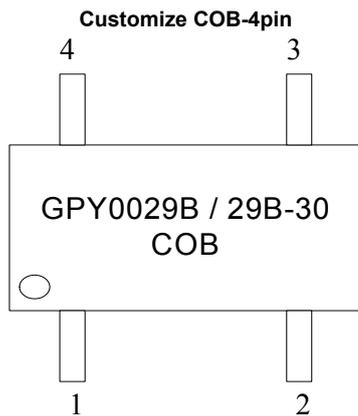
5.4. PAD Assignment and Locations

```
┌──────────────────────────────────────────┐
│ ┌─┐                              ┌─┐       │
│ │1│                              │2│       │
│ └─┘                              └─┘  ┌─┐  │
│ VIN                              VOUT │3│  │
│                                       └─┘  │
│                                        FB  │
│                                            │
│                                            │
│ RESET                               GND    │
│ ┌─┐                                 ┌─┐    │
│ │5│                                 │4│    │
│ └─┘                                 └─┘    │
└──────────────────────────────────────────┘
( 0 , 0 )
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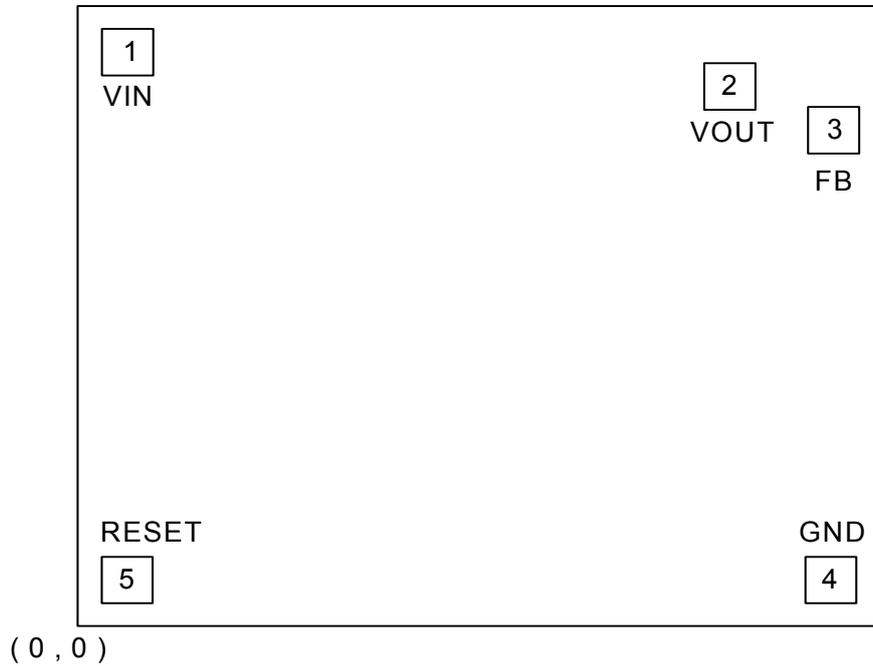
This IC substrate should be connected to VSS

Note1: To ensure IC functions properly, please bond all of VDD and VSS pins.
Note2: FB pad must be bonded to VOUT pin in COB or SOT89 package.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristic	Symbol	Rating	Unit
Input Voltage	V_{IN}	+7.0V	V
Output Voltage	V_{OUT}	$-0.3 \sim (V_{IN} + 0.3)$	V
Operating Temperature	T_{OPT}	0 - 70	℃
Storage Temperature	T_{STG}	-40 - 125	℃
Power Consumption (#)	P_{WATT}	500	mW

Note1: Stresses beyond those given in the "Absolute Maximum Ratings" table may cause operational errors or damage to the device. For normal operational conditions, see Electrical Characteristic.

Note2: (#) applied to SOT-89 package.

Note3: For bonding-wire current density & package power dissipation issues, we highly recommend that the power consumption should not exceed "Absolute Maximum Ratings"; it may cause device damage or affect device reliability.

6.2. DC Characteristic

(V_{IN} = 5.0V, V_{OUT} (target) = 3.0V / 3.3V, C_{IN} = C_{OUT} = 10μF, Typical values are at T_{OPT} = 25ºC)

Item		Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Input Voltage	GPY0029B		V_{IN}	3.0	-	7.0	V
	GPY0029B-30			2.7	-	7.0	V
Output Voltage	GPY0029B	10μA≦ I_{OUT} ≦150mA	V_{OUT}	3.2	3.3	3.4	V
	GPY0029B-30			2.91	3.0	3.09	V
Output Current		V_{IN} = 3.6V	I_{OUT}	150	-	-	mA
Current Limit			I_{LIM}	200	300	-	mA
Load Regulation		V_{IN} = 5.0V, 1mA ≦ I_{OUT} ≦ 150mA	$\triangle V_{OUT}$	-	40	60	mV
Line Regulation		I_{OUT} = 1mA, V_{OUT} + 0.5V ≦ V_{IN} ≦ 7.0V	$\dfrac{\Delta Vout}{\Delta Vin \times Vout}$	-	0.15	-	%/V
Dropout Voltage		I_{OUT} = 1mA, Vin = V_{OUT} (normal), V_{DIF} = V_{IN} - V_{OUT} , V_{OUT} = 3.3V	V_{DIF}	-	40	60	mV
Quiescent Current		I_{OUT} = 0	I_{SS}	-	3.0	6.0	μA
Temperature Coefficient		I_{OUT} = 10mA, $0^{O}C \leq T_{OPT} \leq 70^{O}C$, V_{OUT} = 3.3V	$\dfrac{\Delta Vout}{\Delta T}$	-	±50	-	ppm/℃
Reset Function							
RESET Output Low Voltage		RESET Output Sinking 2mA	V_{OL}	-	50	100	mV
Output High Leakage Current		V_{RESET} = 5V	I_{RESET}	-	-	100	nA
Threshold to Output Voltage	GPY0029B	Rising edge, referred to V_{OUT}	V_{THVOUT}	-	2.87	-	V
	GPY0029B-30			-	2.65	-	V
Threshold to Input Voltage	GPY0029B	Falling edge of VIN	V_{THVIN}	-	2.90	-	V
	GPY0029B-30			-	2.65	-	V
Power-ON Reset Delay Time		See Timing Diagram	T_{DPOR}	-	22	-	mS
VIN Reset Delay Time		See Timing Diagram	T_{DLVIN}	-	-	100	mS
V_{OUT} Reset Delay Time		See Timing Diagram	T_{DLVOUT}	1	-	8	mS

Note1: V_{OUT} (normal) @ V_{IN} = 5.0V, I_{OUT} = 1mA, Vout = 3.0V / 3.3V, T_{OPT} = 25 ^{O}C

Note2: Pwatt = (V_{IN} - V_{OUT})* I_{OUT}; SOT-89 package maximum power dissipation is 500mW for GPY0029B.

6.3. Typical Operating Characteristics

6.3.1. Output voltage vs. output current (V_{OUT} = 3.3V)
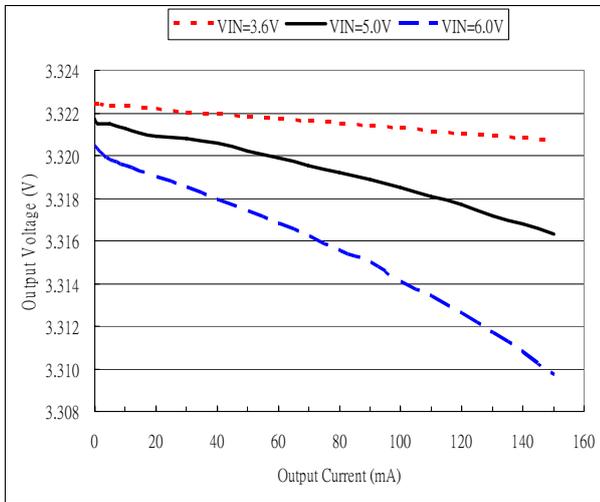

6.3.2. Output voltage vs. input voltage (V_{OUT} = 3.3V)
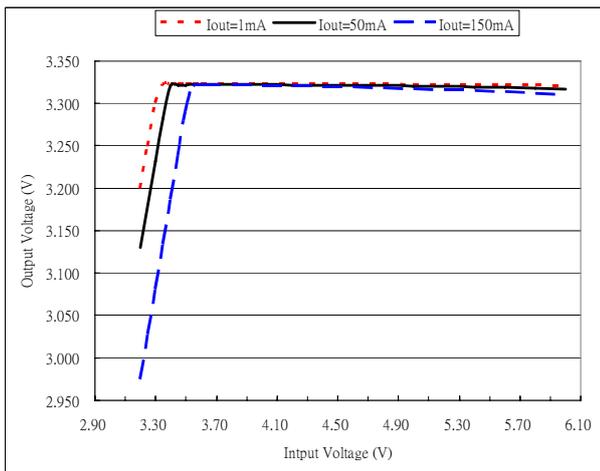
6.3.3. Load transient response; I_{OUT} = 10mA to 150mA

(ΔV_{OUT} = 32mV)

(ΔV_{OUT} = 46mV)

V_{IN} = 5.0V; I_{OUT} =10mA to 150mA & tr=tf=10µs; C_{OUT}=10µF

CH1: 500mV CH2: 50.0mV M 100µs
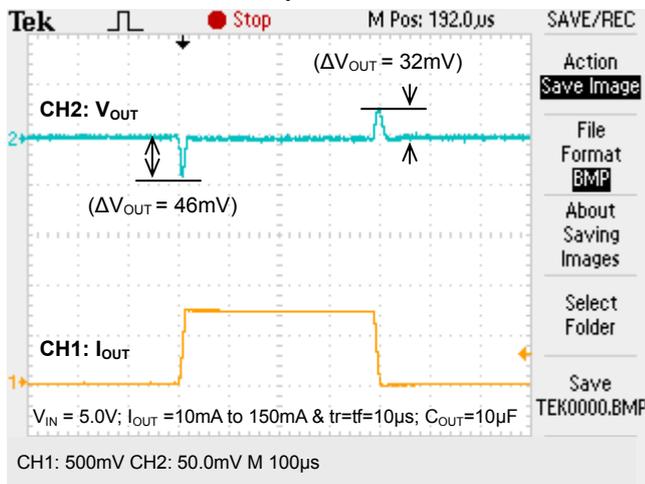
6.3.4. Load transient response; I_{OUT} = 1mA to 50mA

(ΔV_{OUT} = 30mV)

(ΔV_{OUT} = 45mV)

V_{IN} = 5.0V; I_{OUT} =1mA to 50mA & tr=tf=10µs; C_{OUT}=10µF

CH1: 200mV CH2: 50.0mV M 100µs
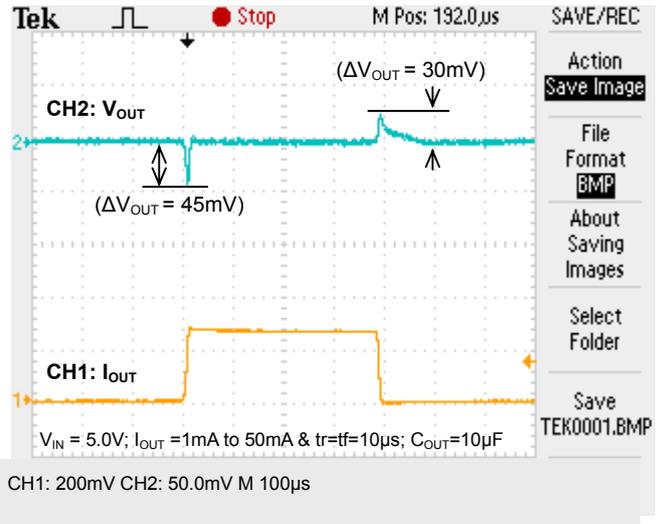
6.3.5. Line transient response; I_{OUT}=150mA(V_{IN}=4 to 5V)

(ΔV_{OUT} = 8mV)

(ΔV_{OUT} = 8mV)

V_{IN} =4.0V to 5.0V & tr=tf=10µs; I_{OUT} =150mA; C_{OUT}=10µF

CH1: 500mV CH2: 20.0mV M 100µs
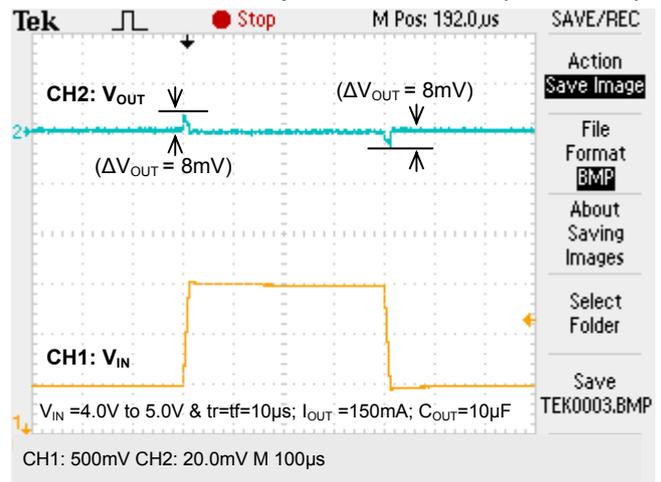
6.3.6. Line transient response; I_{OUT}=10mA (V_{IN}=4 to 5V)

(ΔV_{OUT} = 3mV)

(ΔV_{OUT} = 5mV)

V_{IN} =4.0V to 5.0V & tr=tf=10µs; I_{OUT} =10mA; C_{OUT}=10µF

CH1: 500mV CH2: 20.0mV M 100µs

Version: 1.4
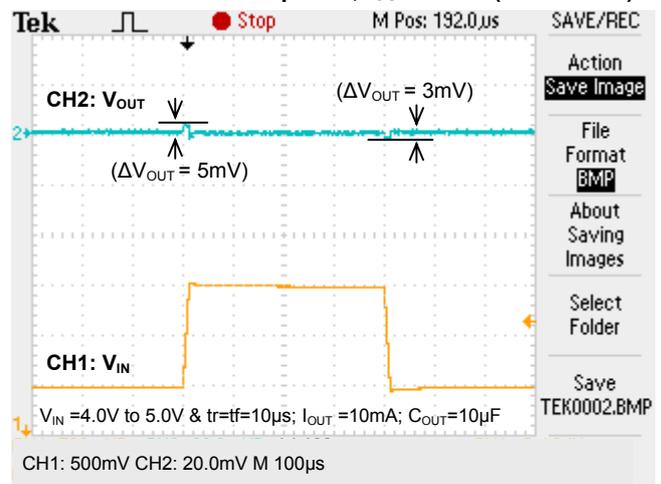
6.4. Application Circuit

6.4.1. PIN (with Reset Function)

VIN

VIN

VIN

10μF

GND

GND

GPY0029B / 29B-30

VOUT / FB

VOUT

RESET

RESET

VOUT

VOUT

100K

10μF
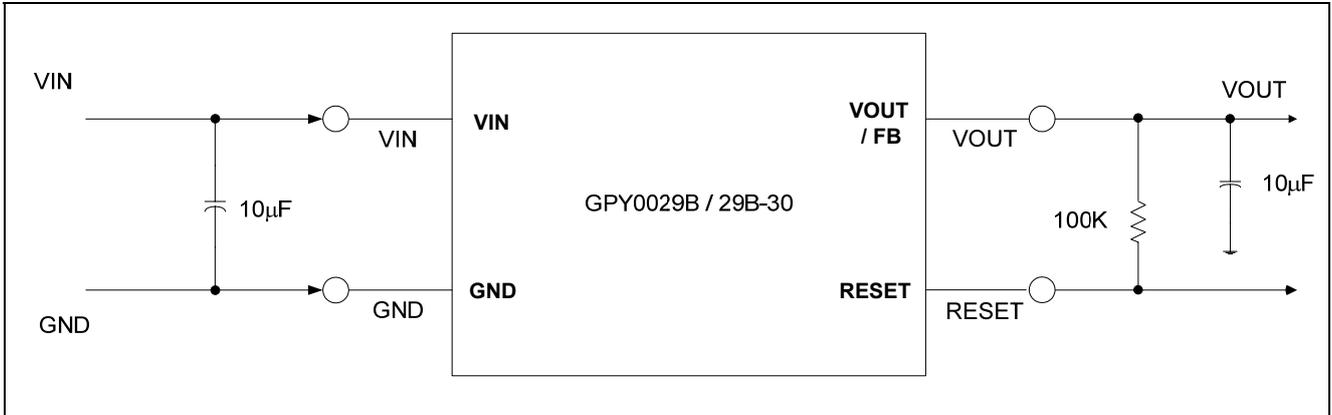
RESET

Note: FB pad must be bonded to VOUT pin in COB.

6.4.2. PIN (no Reset Function)

VIN

VIN

VIN

10μF

GND

GND

GPY0029B / 29B-30

VOUT / FB

VOUT

VOUT

VOUT

10μF
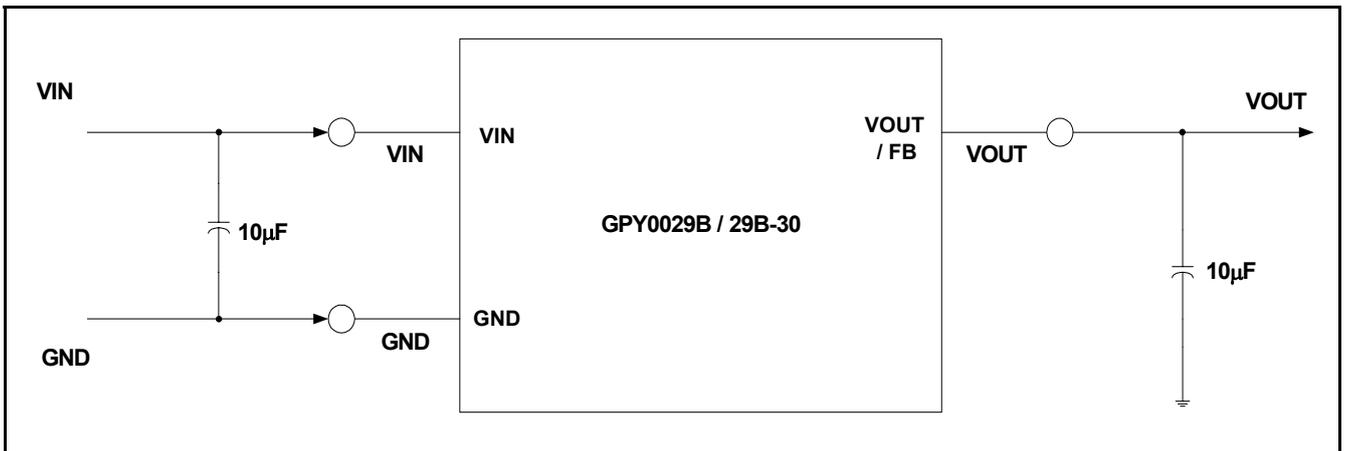
Note: FB pad must be bonded to VOUT pin in COB or SOT89 package.

6.5. Reset Timing Diagram
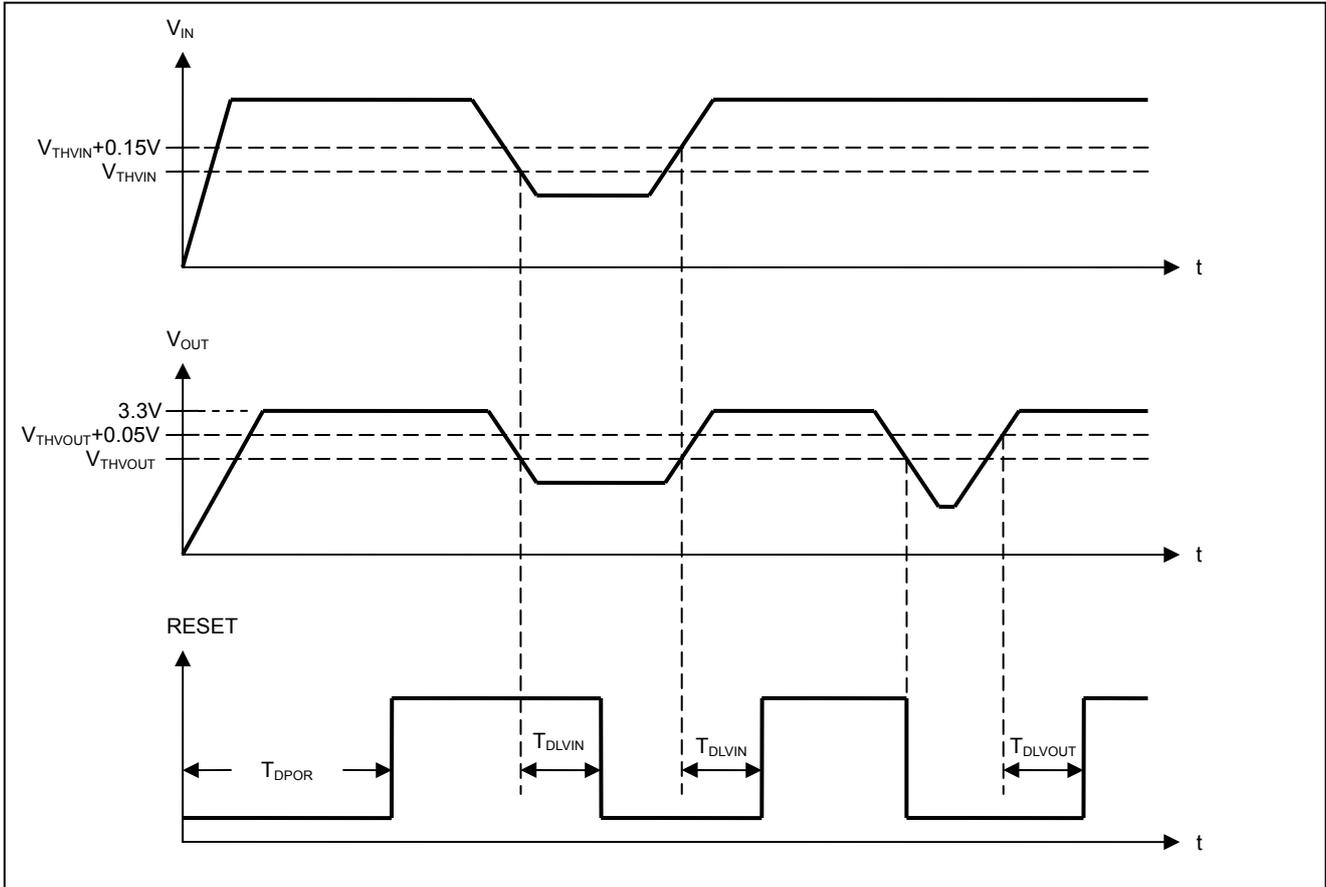
Note: When power on, Low V_{IN} threshold voltage is V_{THVIN}.

7. PACKAGE/PAD LOCATIONS

7.1. Ordering Information

Product Number	Output Voltage (V)	Package Type	Package Marking
GPY0029B - C	3.3	Chip form (V_{OUT} = 3.3V ±3%)	N/A
GPY0029B - 30 - C	3.0	Chip form (V_{OUT} = 3.0V ±3%)	N/A
GPY0029B - HE011	3.3	Package form - SOT89 (V_{OUT} = 3.3V ±3%)	Y0029B
GPY0029B - 30 - HE011	3.0	Package form - SOT89 (V_{OUT} = 3.0V ±3%)	Y29B30
GPY0029B - EE011	3.3	Package form (Tape & reel) - SOT89 (V_{OUT} = 3.3V ±3%)	Y0029B
GPY0029B - 30 - EE011	3.0	Package form (Tape & reel) - SOT89 (V_{OUT} = 3.0V ±3%)	Y29B30

7.2. Package Information

7.2.1. 3 PIN SOT89 package size
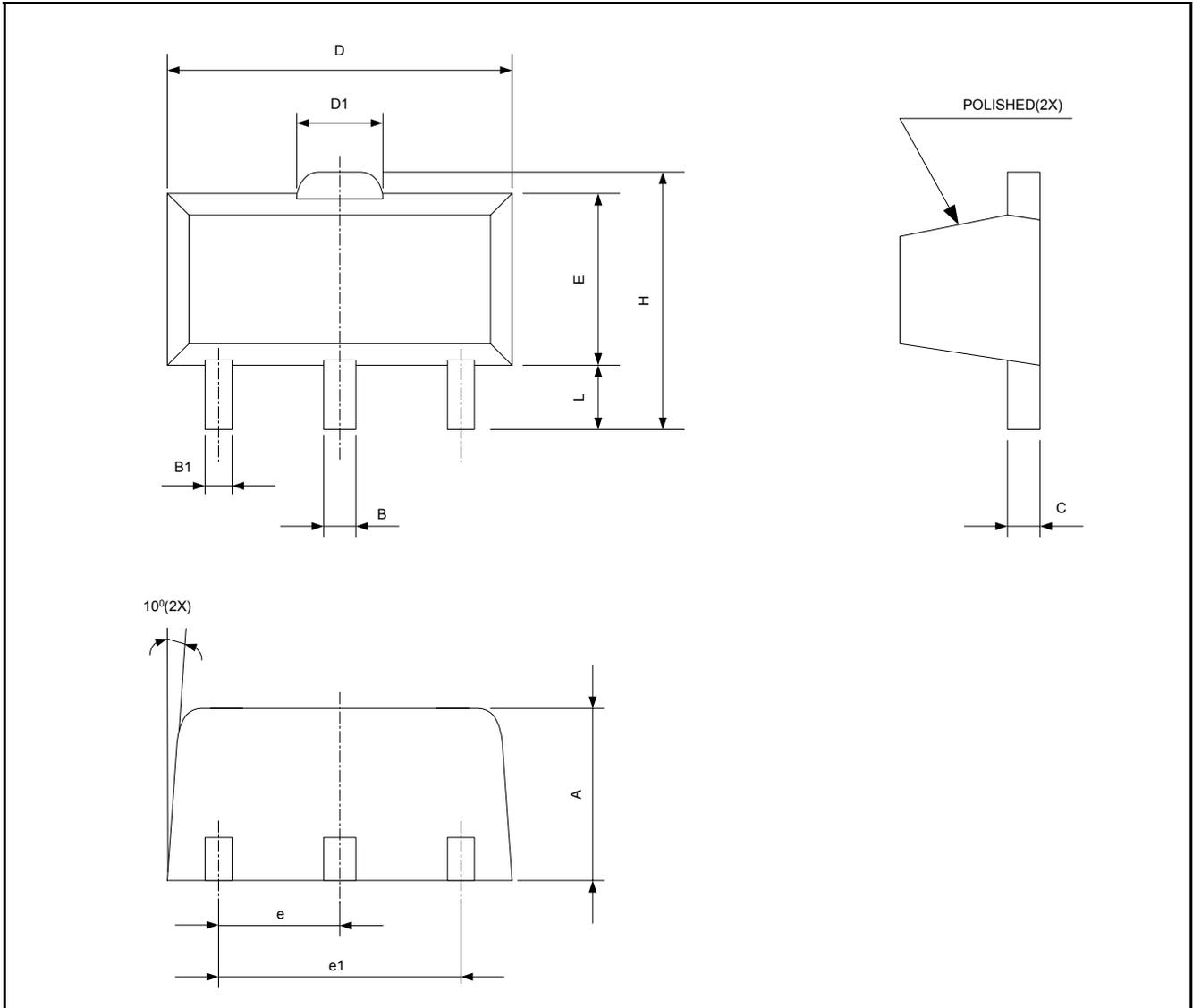
Symbol	Min.	Max.	Unit
A	1.40	1.60	Millimeter
B	0.44	0.56	Millimeter
B1	0.36	0.48	Millimeter
C	0.35	0.44	Millimeter
D	4.40	4.60	Millimeter
D1	1.35	1.83	Millimeter
E	2.29	2.60	Millimeter
H	3.94	4.25	Millimeter
e	1.50 BSC		Millimeter
e1	3.00 BSC		Millimeter
L	0.89	1.2	Millimeter

7.2.2. 4-PIN Chip On Board (COB) bonding diagram

Pin: 4		Pin: 3
(VIN)		(VOUT)

1		2	3

GPY0029B / 29B-30

| 5 | | 4 |

Pin: 1		Pin: 2
(RESET)		(GND)
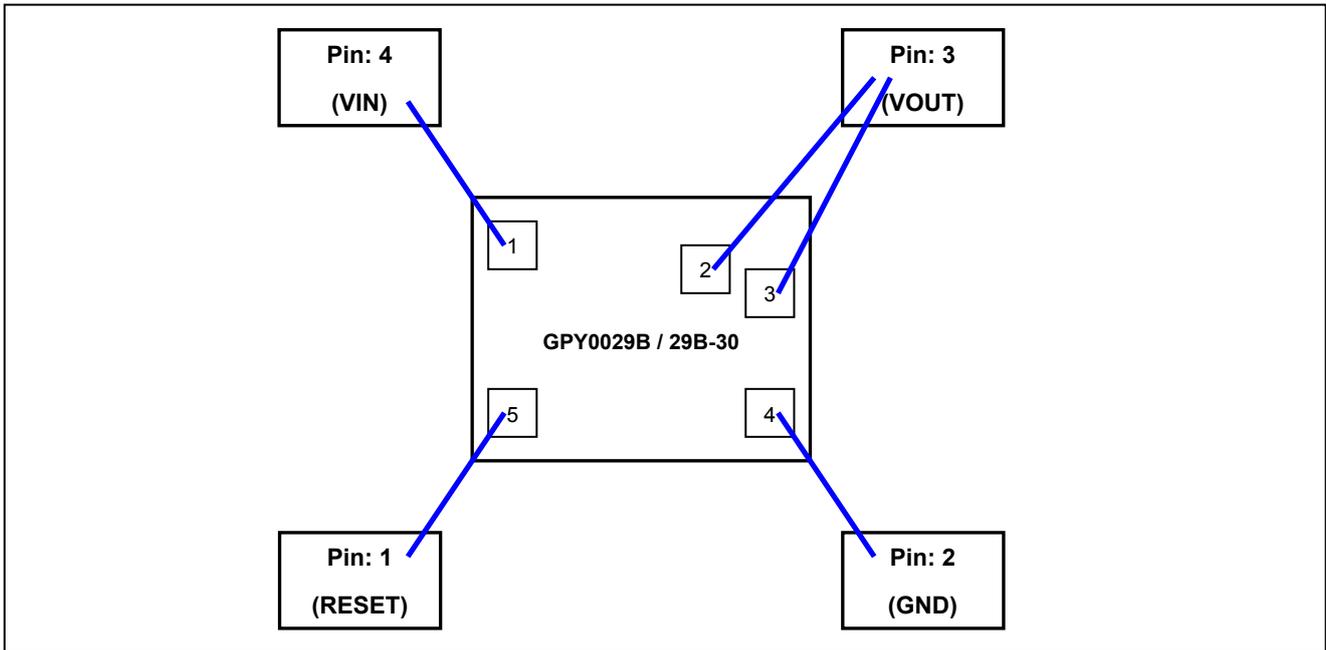
7.3. Storage Condition and Period for Package

Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
SOT	LEVEL 3	220 +5/-0℃	N/A	No

Note1: Please refer to IPC/JEDEC standard J-STD-020A and EIA JEDEC stand JFSD22-A112.
Note2: or refer to the "CAUTION Note" on dry pack bag.

7.4. Recommended SMT Temperature Profile

This "Recommended" temperature profile is a rough guideline for SMT process reference. Most of GENERALPLUS lead-frame base products choose Matte Tin and Sn/Bi for plating recipe. For PPF (Pre-Plated Frame) product with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.

Recommended Reflow Profile for 63/37 Solder Paste or Cu lead frame
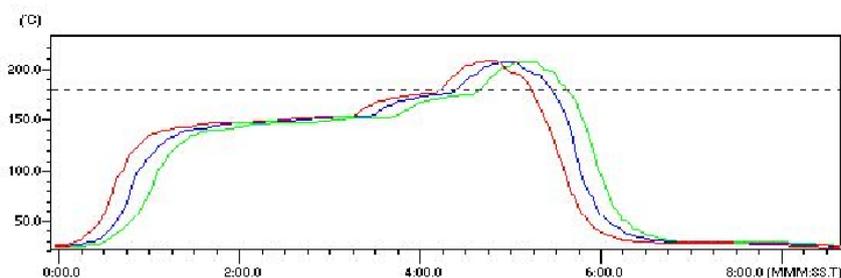
This profile is designed for use with Sn63 or Sn62 and can serve as a general guideline in establishing a reflow profile.

Reflow Profile:
- Heating-up @1~3°C per sec to 140°C
- Preheat @ 140-150°C for 120 ~ 160 sec
- Ramp @ 2~3 °C per sec to peak temperature (220 ~ 225 °C), Temperature over 183°C for 45~ 75 sec
- Cooling down to room temperature @4~2°C per sec to avoid undesired intermatalic compound layer.

Recommended Reflow Profile for Lead-free Solder Paste or PPF lead frame
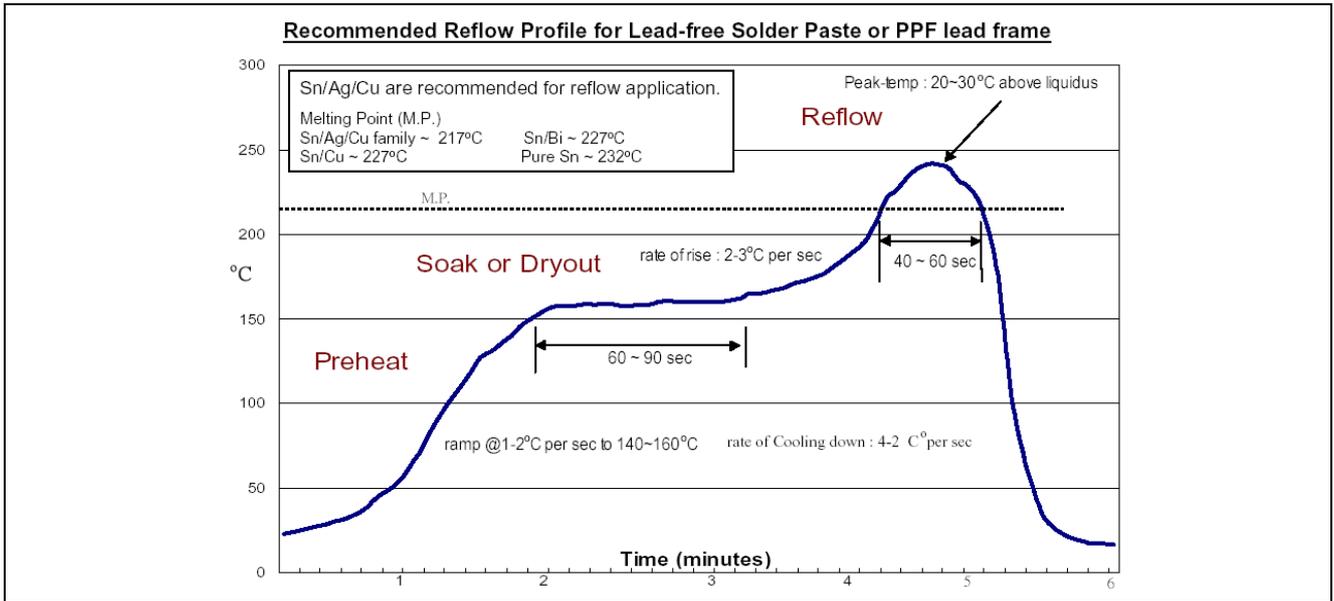
8. HTOL TEST RESULT

Package	Check Point (168hrs; 500hrs; 1000hrs)		
Type	168hrs	500hrs	1000hrs
COB4	77pcs sample are all passed	77pcs sample are all passed	77pcs sample are all passed
SOT89	77pcs sample are all passed	77pcs sample are all passed	77pcs sample are all passed

Note1: Testing Conditions: V_{IN}=5.0V, V_{OUT}=3.3V, I_{OUT}=150mA, Temp=125℃.

Note2: Testing Method: Reference to MIL-STD-883E method 1005.8.

Note3: COB Material: Hysol EO1016.

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10. REVISION HISTORY

Date	Revision #	Description	Page
JAN. 19, 2010	1.4	1. Modify Block Diagram in section 4.	3
		2. Modify Signal Descriptions in section 5.1. and 5.3.	4
		3. Modify Application Circuit in section 6.4.	8
JUN. 29, 2007	1.3	1. Modify Ordering Information in section 7.2.	9
JUN. 20, 2007	1.2	1. Modify the diagram in section 5.3.	4
		2. Add V_{OUT} = 3.0V specification in section 6.2.	5
		3. Modify the diagram in section 6.4.1 and 6.4.2.	7
		4. Modify Order Information in section 7.2.	9
		5. Modify HTOL TEST RESULT in section 8.	12
DEC. 26, 2006	1.1	1. Modify the figure in section 6.3.2.	6
		2. Add "4 PIN Chip On Board (COB) Bonding Diagram" in section 7.3.2.	11
NOV. 15, 2006	1.0	Original	14