



DATA SHEET

GPY0030B

Audio Driver

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Feb. 01, 2008

Version 1.2

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GPY0030B

AUDIO DRIVER

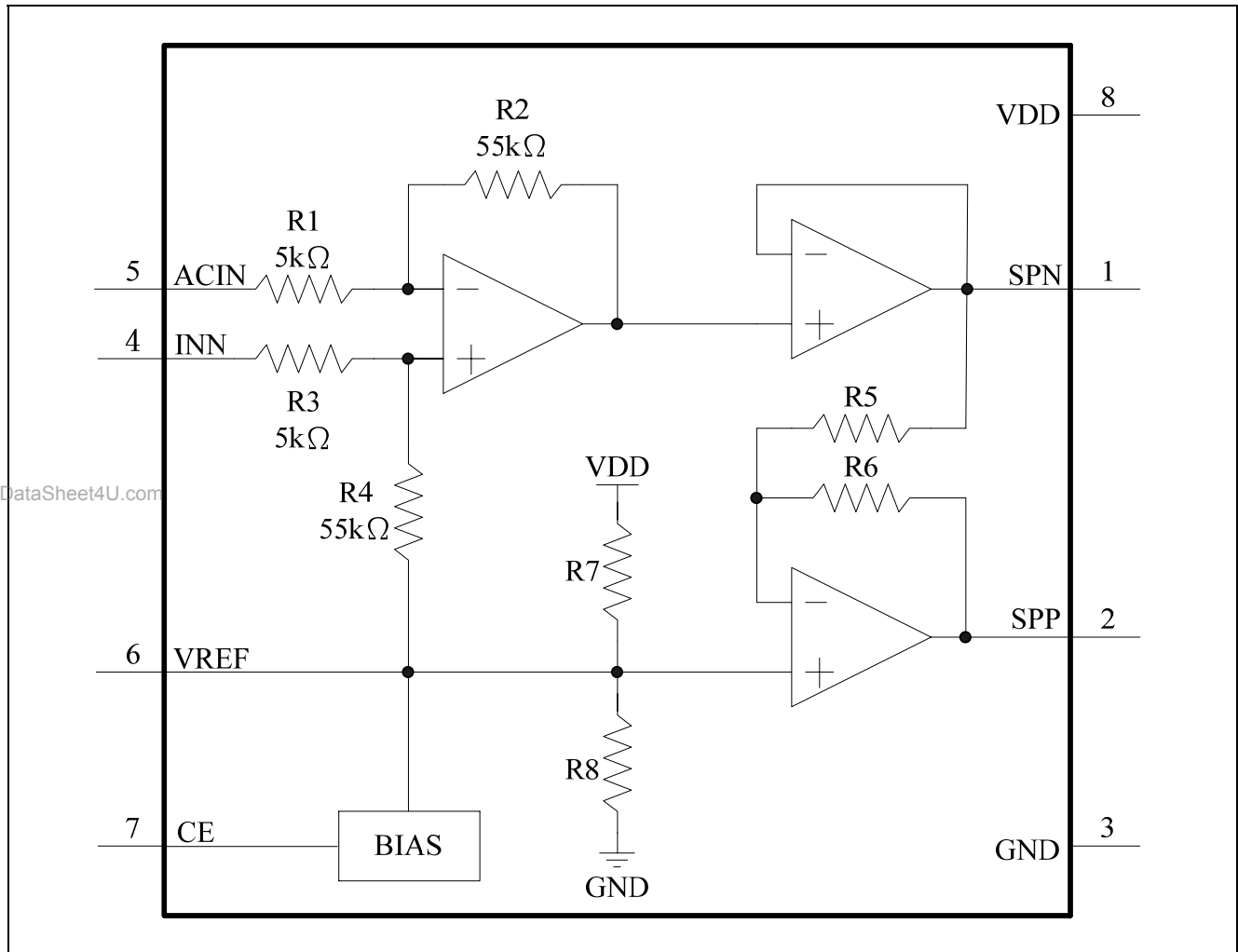
1. GENERAL DESCRIPTION

The GPY0030B is an audio driver whose gain can be adjusted by external resistor (Maximum gain is 20) and embedded the de-pop circuit to minimize the turn-on and turn-off pop noise. Normally, it is applied for GPC series, GPF series, GPL series and other GENERALPLUS products. The GPY0030B is easily to be used in various applications and products.

2. FEATURES

- Wide operation range: 2.4V - 6.8V
- Bridge-Tied Load
- Low distortion: THD+N = 0.15% (Typ.)
(For VDD = 5.0V, R_L = 8.0Ω & P_{out} = 500mW)
- High output power: P_{OUT} = 825mW
(For VDD = 5.0V, THD+N = 1.0%, f = 1.0KHz & R_L = 8.0Ω)
- Low standby current: 1.0μA
- Minimize the turn-on and turn-off pop noise

3. BLOCK DIAGRAM

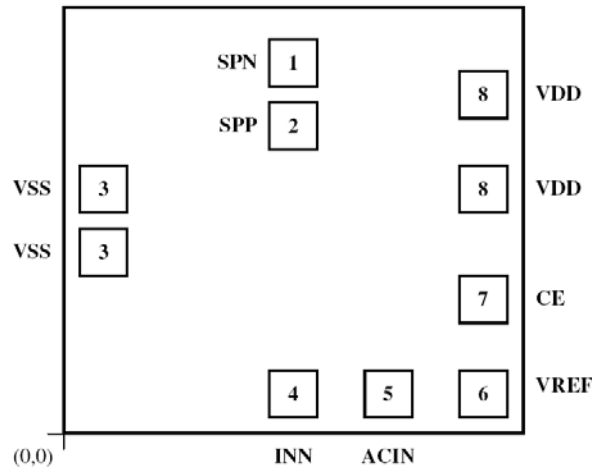


GPY0030B

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description	Electrical Characteristics
SPN	1	O	Audio output negative	-
SPP	2	O	Audio output positive	-
VSS	3	I	Power VSS	-
INN	4	I	Signal input negative	-
ACIN	5	I	Signal input positive	-
VREF	6	O	Reference voltage	VDD/2
CE	7	I	Chip enable	-
VDD	8	I	Power VDD	2.4V - 6.8V

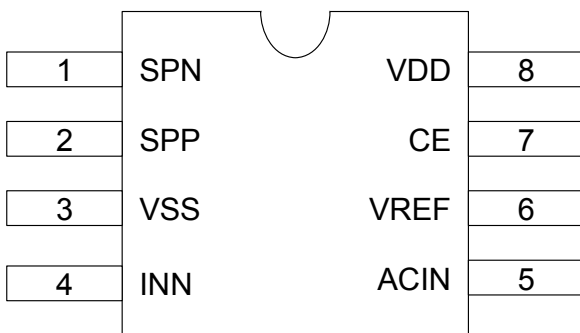
4.1. PAD Assignment



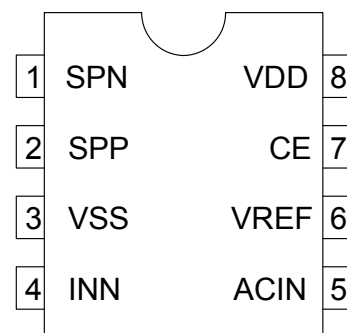
This IC substrate should be connected to VSS

Note: To ensure the IC functions properly, please bond all of VDD and VSS pins.

4.2. Package Pin Assignment



SOP 8



PDIP 8

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to $V_+ + 0.5V$
Operating Temperature	T_A	0°C to +60°C
Storage Temperature	T_{STO}	-50°C to +150°C

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

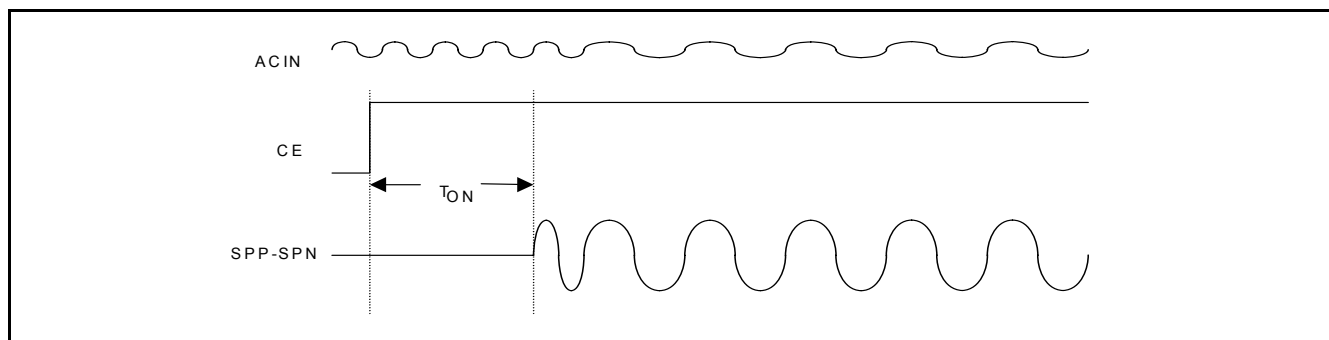
5.2. DC Characteristics ($T_A = 25^\circ\text{C}$)

Item	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Operation Voltage		V_{DD}	2.4	-	6.8	V
Shutdown Current	$CE = V_{SS}$	I_{STBY}	-	0.1	1.0	μA
Operating Current	$V_{DD} = 5.0V, CE = V_{DD}, \text{No Load}$	I_{DD}	-	2.5	-	mA
Reference Voltage	$V_{DD} = 5.0V$	V_{REF}	-	$V_{DD}/2$	-	V
Input Resister(CE)	$CE = V_{DD}$	R_{CE}	-	40	-	k Ω
Input Current(CE)	$CE = 2.3V \text{ at } V_{DD} = 5.0V$	I_{CE}	-	85	-	μA
Total Harmonic Distortion + Noise	$V_{DD} = 5.0V, R_L = 8.0\Omega, P_{OUT} = 500mW$	THD+N	-	0.15	-	%
Output Power	$V_{DD} = 5.0V, \text{THD+N} = 1\%, f = 1.0KHz \text{ \& } R_L = 8.0\Omega$	P_{OUT}	-	825	-	mW
	$V_{DD} = 5.0V, \text{THD+N} = 10\%, f = 1.0KHz \text{ \& } R_L = 8.0\Omega$	P_{OUT}	-	1000	-	mW
Output Offset Voltage	$V_{IN} = 0V$	V_{OS}	-	30	-	mV
Power Rejection Ratio	$f = 1kHz$	PSRR	-	70	-	dB
Enable Time	$V_{DD} = 5.0V, C_{IN} = 1.0\mu F, CVREF = 4.7\mu F$	T_{ON}	-	60	-	ms
	$V_{DD} = 5.0V, C_{IN} = 1.0\mu F, CVREF = 2.2\mu F$		-	45	-	ms
	$V_{DD} = 3.3V, C_{IN} = 1.0\mu F, CVREF = 4.7\mu F$		-	60	-	ms
	$V_{DD} = 3.3V, C_{IN} = 1.0\mu F, CVREF = 2.2\mu F$		-	45	-	ms
Shutdown Time	$V_{DD} = 5.0V, C_{IN} = 1.0\mu F, CVREF = 4.7\mu F$	T_{OFF}	-	80	-	ms
	$V_{DD} = 5.0V, C_{IN} = 1.0\mu F, CVREF = 2.2\mu F$		-	45	-	ms
	$V_{DD} = 3.3V, C_{IN} = 1.0\mu F, CVREF = 4.7\mu F$		-	80	-	ms
	$V_{DD} = 3.3V, C_{IN} = 1.0\mu F, CVREF = 2.2\mu F$		-	45	-	ms

Note1: Output power = $(V_{O(PEAK)})^2/2/R_L$; $V_{O(PEAK)} = (V_{I(PEAK)}) * \text{GAIN}$;

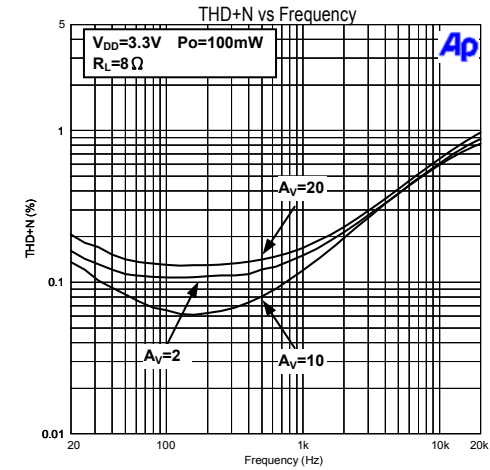
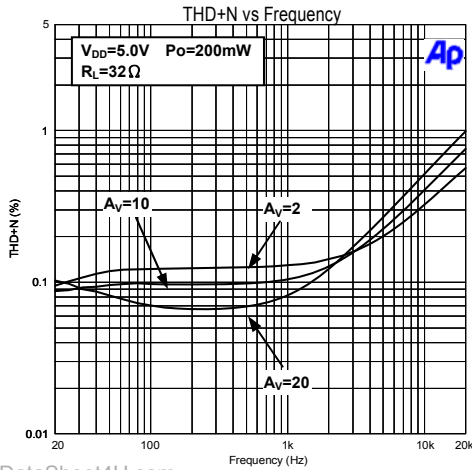
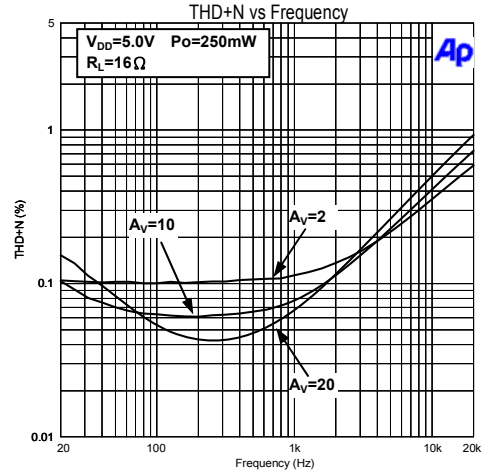
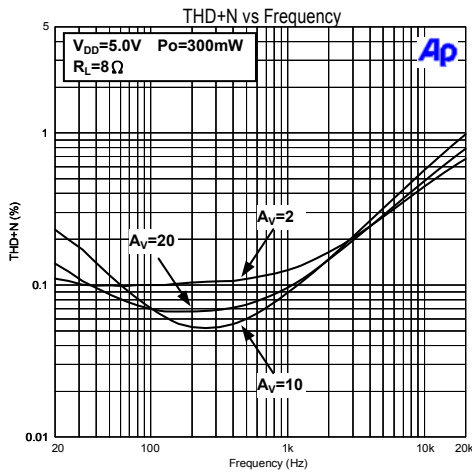
So we can get the input range from output power, output loading and audio driver's gain.

Note2: t_{ON} is the time from CE high (chip enable) to SPP or SPN output.

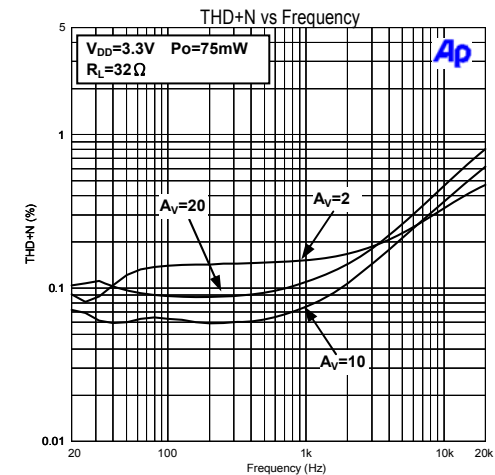
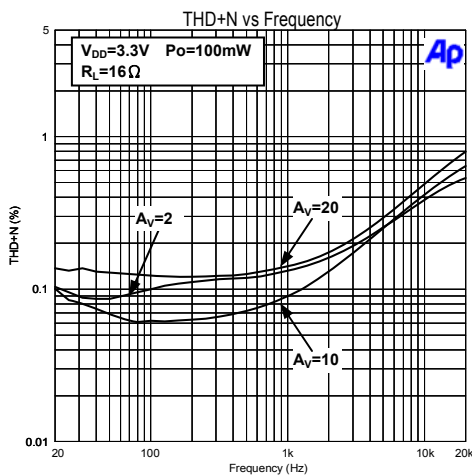


5.3. Typical Performance Characteristics

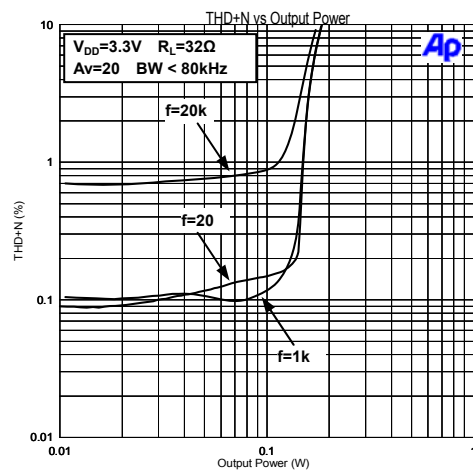
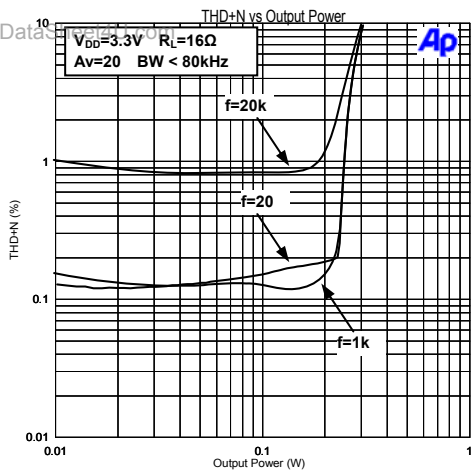
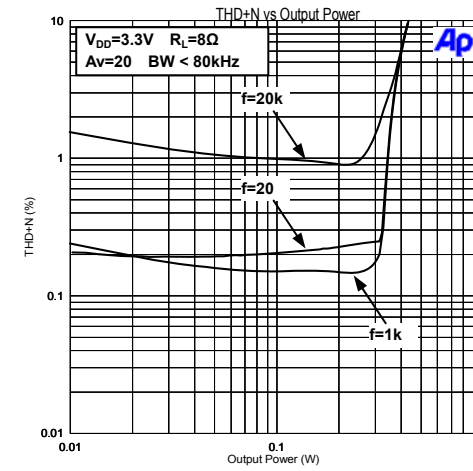
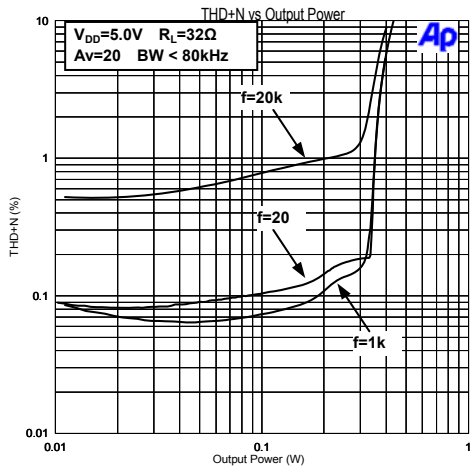
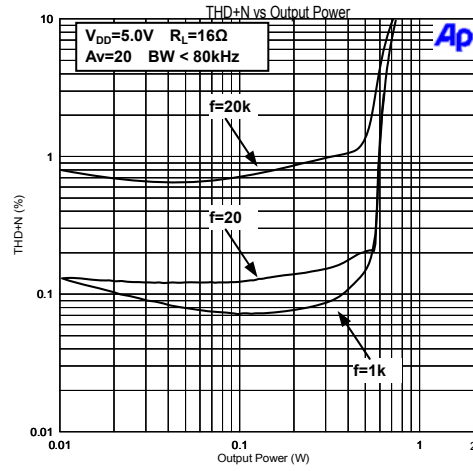
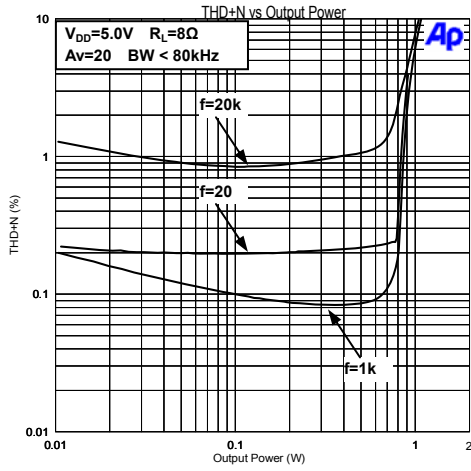
5.3.1. THD+N vs. Frequency



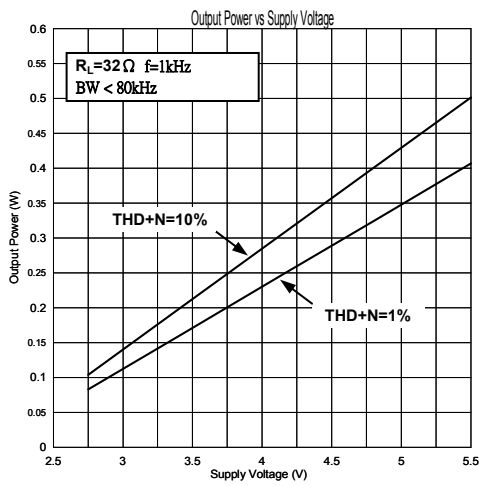
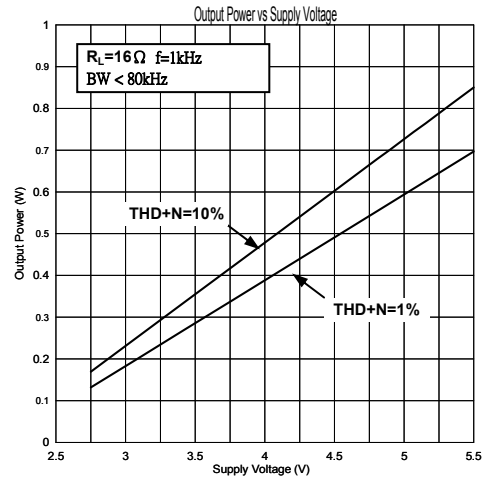
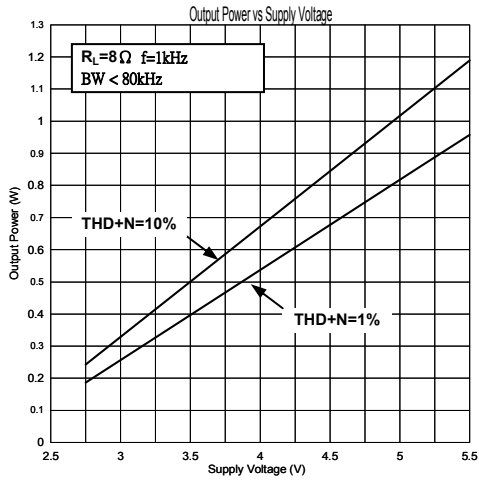
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5.3.2. THD+N vs. Output Power

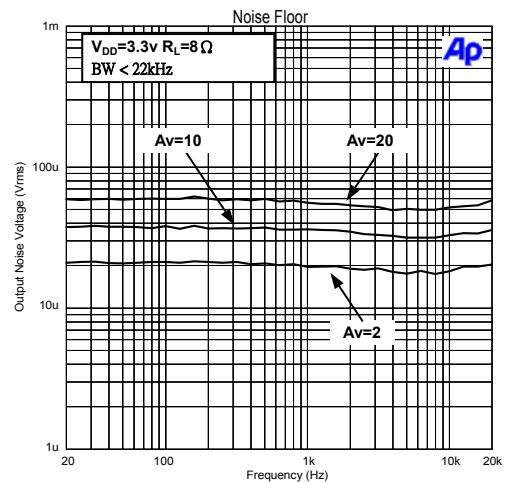
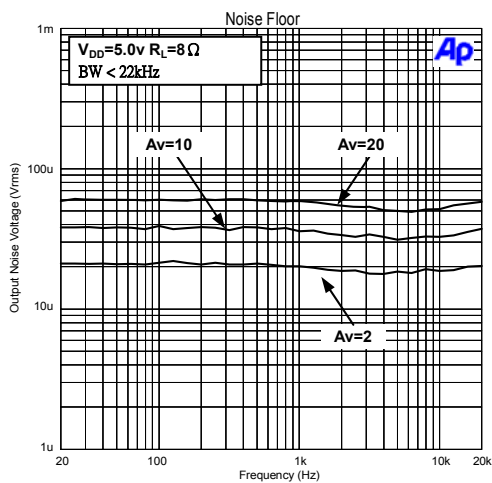


5.3.3. Output Power vs. Supply Voltage



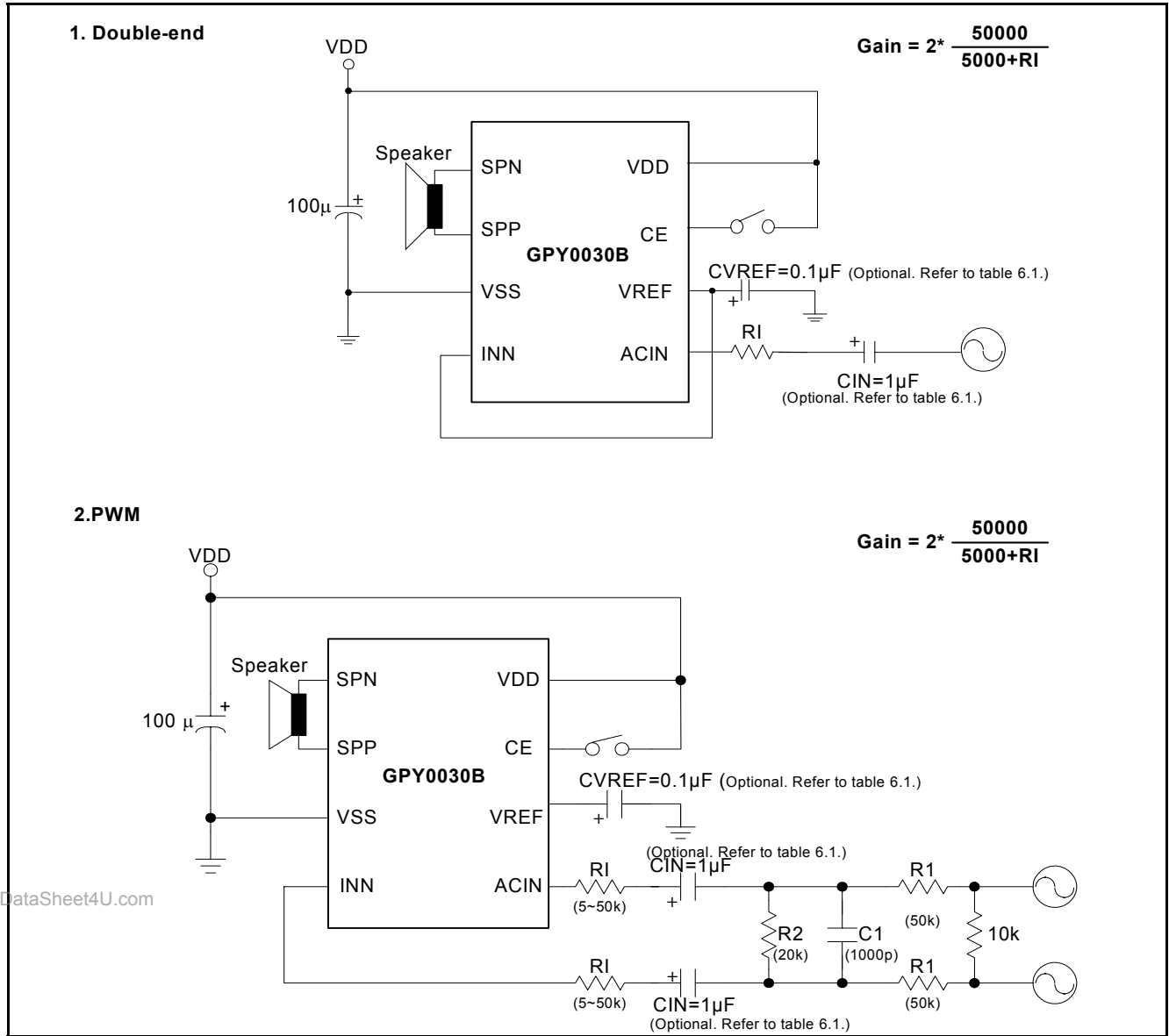
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5.3.4. Noise



GPY0030B

6. APPLICATION CIRCUIT



6.1. De-pop sound comparison between GPY0030A and GPY0030B: (Double-End Application Circuit)

No.	CIN	CVREF	GPY0030A				GPY0030B			
			fc (Hz)*	T _{ON} (ms)	T _{OFF} (ms)	Pop Sound (mV _{p-p})	fc (Hz)*	T _{ON} (ms)	T _{OFF} (ms)	Pop Sound (mV _{p-p})
1	0.1uF	0.1uF	318	15	5	300	318	30	20	81.3
2	0.22uF	0.22uF	145	15	5	362.5	145	30	20	187.5
3	1.0uF	0.1uF	31.8	15	5	812.5	31.8	40	40	162.5
4	1.0uF	2.2uF	-	-	-	-	31.8	45	45	118.8
5	1.0uF	4.7uF	-	-	-	-	31.8	60	80	106.3

Note1: When switching GPY0030A to GPY0030B, customers don't need to change external component and pop sound level is smaller than GPY0030A. Detail differences between GPY0030A and GPY0030B, please refer to DCN.

Note2: Pop sound level measurement condition (RI=0Ω, input tied to ground and 8Ω Speaker).

Note3: If customers need even lower pop sound level(GPY0030B), we recommend to use option 5 capacitor value. Option 3 is GPY0030A data sheet default value.

Note4: High Pass Filter Frequency $f_c=1/(2\pi \cdot R_{IN} \cdot C_{IN})$, $R_{IN}=RI+5K=5K$ (i.e. RI=0Ω). Option 1 will lose some lower frequency response in both GPY0030A & GPY0030B.

GPY0030B

7. PACKAGE/PAD LOCATIONS

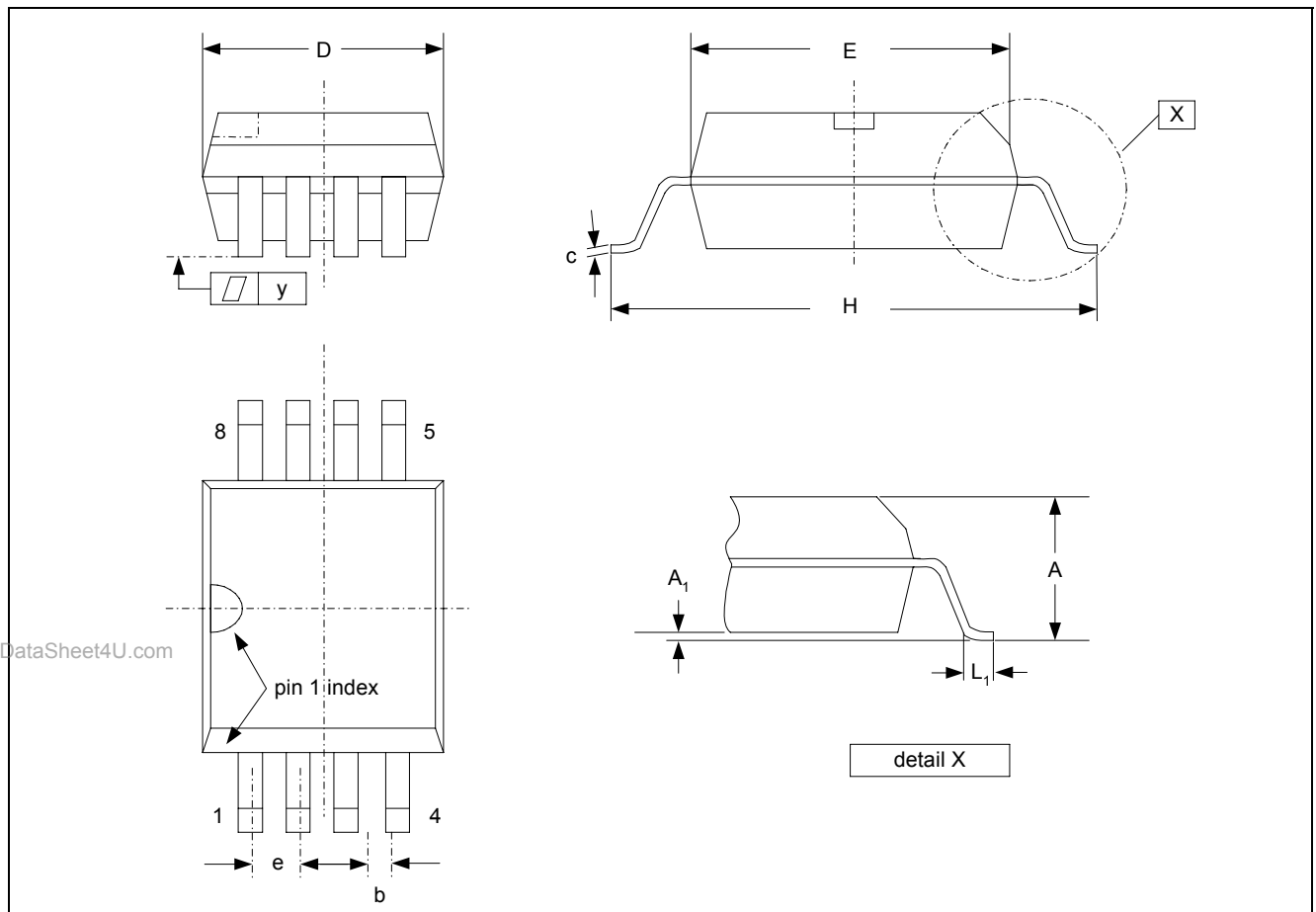
7.1. Ordering Information

Product Number	Package Type
GPY0030B - C	Chip form
GPY0030B - HS01x	Green Package - SOP8 (150mil)
GPY0030B - HD01x	Green Package - PDIP 8 (300mil)

Note: Package form number (x = 1 - 9, serial number).

7.2. Package Information

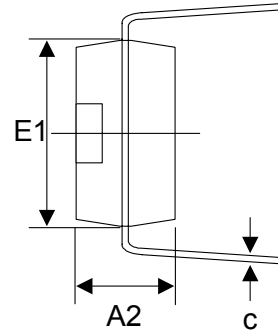
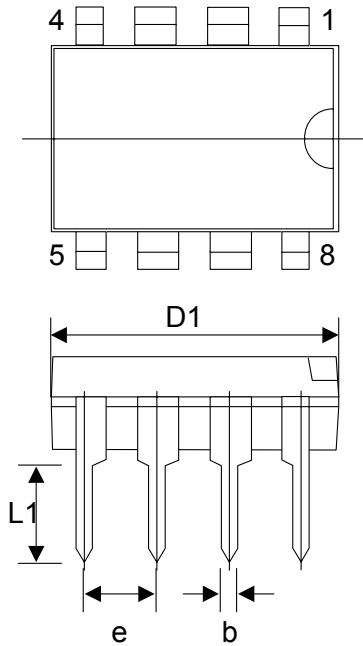
7.2.1. SOP 8



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	0.053	-	0.069
A ₁	0.004	-	0.010
b	-	0.016	-
D	0.189	-	0.196
E	0.150	-	0.157
e	-	0.050	-
H	0.228	-	0.244
L ₁	0.016	-	0.050
y	-	-	0.004

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7.2.2. PDIP 8



Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
374±10	250±4	130±5	130±15	18±2	10Typ	100Typ

All units are in mil. 1mil = 25.4µm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-8-300

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9. REVISION HISTORY

Date	Revision #	Description	Page
FEB. 01, 2008	1.2	1. Modify the diagram in section 6.	9
		2. Add Comparison table in section 6.1.	9
DEC. 03, 2007	1.1	1. Modify DC Characteristics in section 5.2.	5
		2. Modify the diagram in section 6.	9
JUL. 26, 2007	1.0	Original	14