DATA SHEET

GPY0050A

12-bit ADC with Microphone Preamplifier

Sep 16, 2014

Version 1.1

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12BITS ADC WITH MICROPHONE PREAMPLIFIER

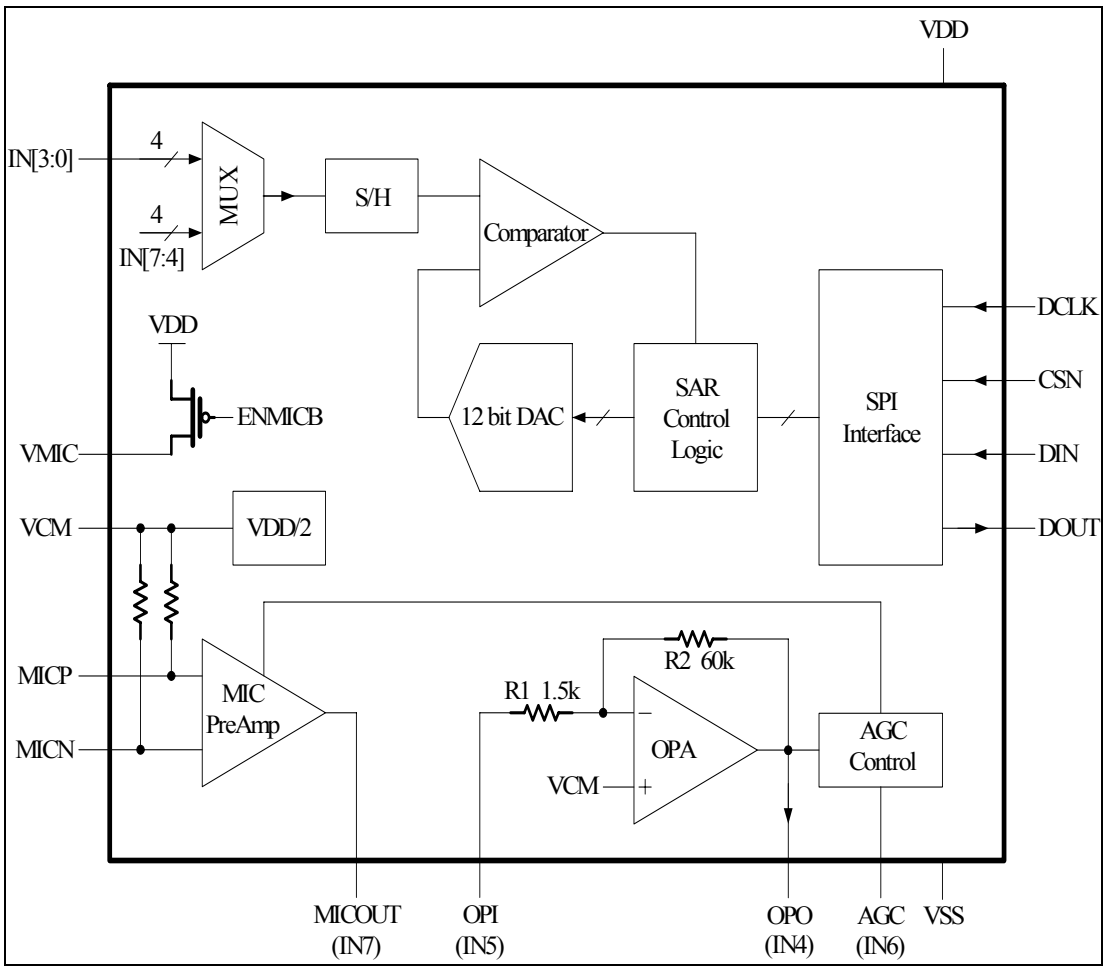
1. GENERAL DESCRIPTION

The GPY0050A is a 12-bit sampling Analog-to-Digital Converter (ADC) with a synchronous serial interface and differential microphone input preamplifier. The device contains an on-chip control register allowing control of ADC and microphone amplifier via the SPI interface.

2. FEATURES

- Wide working voltage: 2.2V – 5.5V
- SPI Serial Interface
- One 12-bit ADC (12-bit SAR ADC)
- ADC Sampling Up to 125KHz
- One Microphone Preamplifier with AGC

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

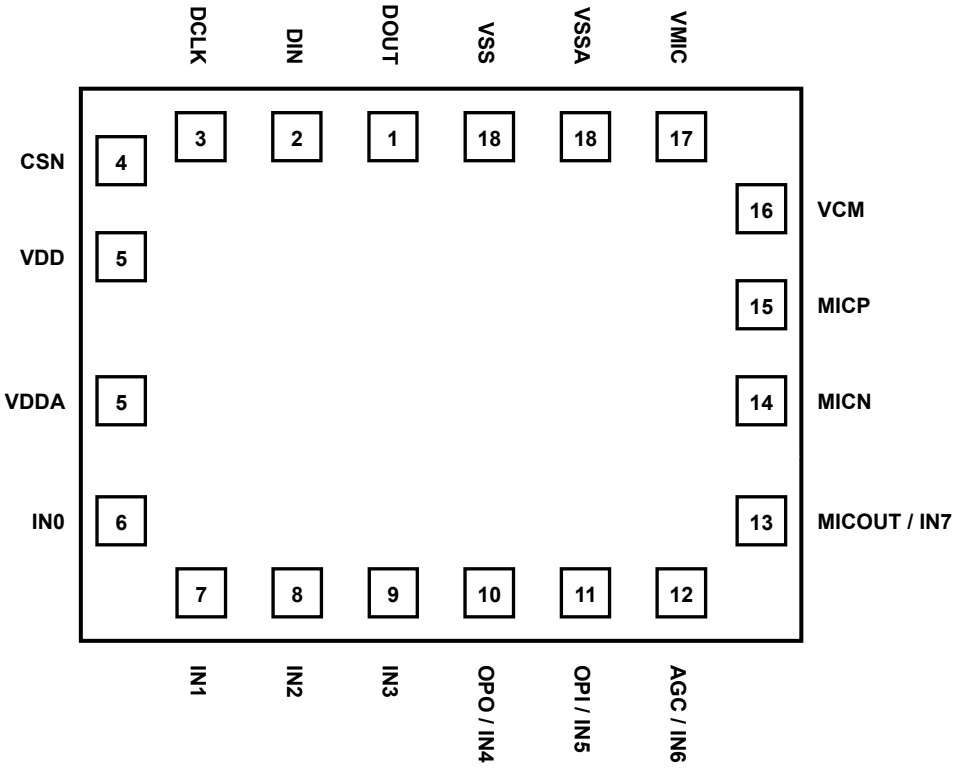
GPY0050A-HG08x (SSOP-20)

Mnemonic	PIN No.	Type	Description	Electrical Characteristics
DOUT	1	O	Serial data output. Data is shifted out on the falling edge of DCLK. This output is high impedance, when CSN is high.	-
DIN	2	I	Serial data input. If CSN is low, data is latched on the rising edge of DCLK.	-
DCLK	3	I	Data Clock input	-
CSN	4	I	Chip select. Active Low	-
VDD / VDDA	5 / 6	P	Power VDD	VDD=2.2V ~ 5.5V
IN0	7	I	ADC input channel 0	-
IN1	8	I	ADC input channel 1	-
IN2	9	I	ADC input channel 2	-
IN3	10	I	ADC input channel 3	-
OPO / IN4	11	O / I	OPA Output. / ADC input channel 4	-
OPI / IN5	12	I	OPA inverting input. / ADC input channel 5	-
AGC / IN6	13	O / I	AGC control pin. / ADC input channel 6	-
MICOUT / IN7	14	O / I	Microphone preamplifier output. / ADC input channel 7	-
MICN	15	I	Inverting input of the differential microphone signal	-
MICP	16	I	Non-inverting input of the differential microphone signal	-
VCM	17	O	VDD/2. MIC Preamplifier signal ground	VDD/2
VMIC	18	O	Power Switch for Microphone bias	-
VSSA / VSS	19 / 20	P	Power Ground	-

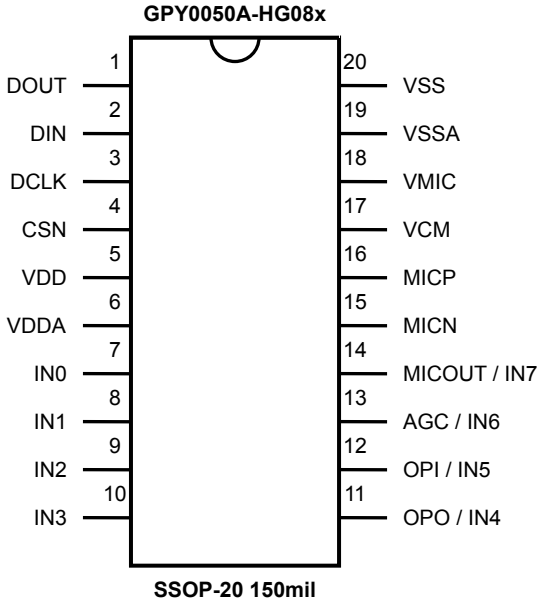
GPY0050A-HG01x (SSOP-16)

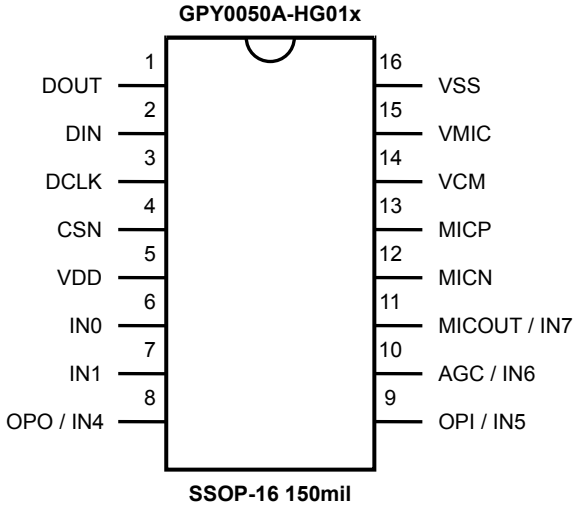
Mnemonic	PIN No.	Type	Description	Electrical Characteristics
DOUT	1	O	Serial data output. Data is shifted out on the falling edge of DCLK. This output is high impedance, when CSN is high.	-
DIN	2	I	Serial data input t. If CSN is low, data is latched on the rising edge of DCLK.	-
DCLK	3	I	Data Clock input	-
CSN	4	I	Chip select. Active Low	-
VDD	5	P	Power VDD	VDD=2.2V ~ 5.5V
IN0	6	I	ADC input channel 0	-
IN1	7	I	ADC input channel 1	-
IN2	-	I	ADC input channel 2	-
IN3	-	I	ADC input channel 3	-
OPO / IN4	8	O / I	OPA Output. / ADC input channel 4	-
OPI / IN5	9	I	OPA inverting input. / ADC input channel 5	-
AGC / IN6	10	O / I	AGC control pin. / ADC input channel 6	-
MICOUT / IN7	11	O / I	Microphone preamplifier output. / ADC input channel 7	-
MICN	12	I	Inverting input of the differential microphone signal	-
MICP	13	I	Non-inverting input of the differential microphone signal	-
VCM	14	O	VDD/2. MIC Preamplifier signal ground	VDD/2
VMIC	15	O	Power Switch for Microphone bias	-
VSS	16	P	Power Ground	-

4.1. PAD Assignment



4.2. Package Pin Assignment



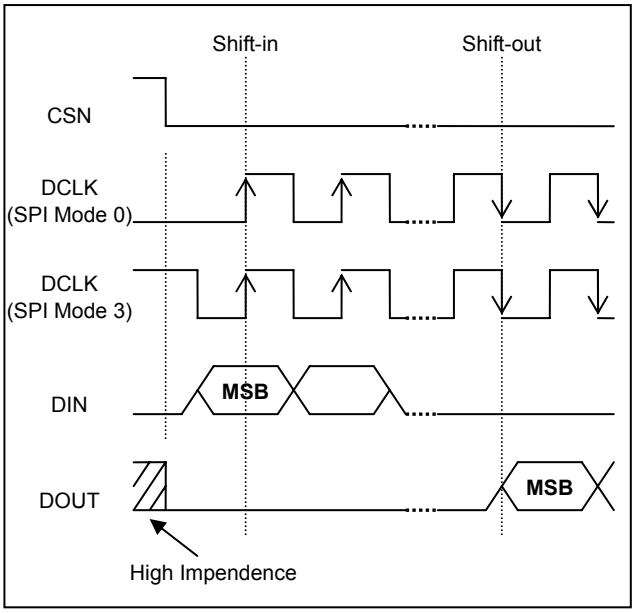


5. FUNCTIONAL DECRIPTIONS

5.1. SPI Serial Interface

The GPY0050A supports SPI Mode 0 and Mode 3 waveforms. When CSN is low, the DIN is latched on the rising of DCLK and DOUT is shifted out on the falling edge of DCLK. If CSN is high, it will disable SPI interface, set DOUT pin in high impedance state and maintain the register data. When the GPY0050A is power on, the power on reset (POR) will set all registers to default value.

The first command bit, the 'S' bit, must always be high and indicate the start of command input. The second bit, 'R/W' bit, controls Read or Write register. The next two bits (CMM_ADDR) select register address. The last 4 bits (CMD_DATA) is the data that will be written to register.



5.1.1. SPI Command Mode Setting

Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Function	S	R/W	CMD_ADDR		CMD_DATA			

Bit	Function	Type	Description	Condition
7	S	W	Start Bit. Control byte starts with first High bit on DIN.	
6	R/W	R/W	Read / Write signal. 0 = write 1 = read	
4-5	CMD_ADDR	R/W	Command Address	00 → ADC_CHSEL 01 → EN_CTRL 10 → Test Mode 11 → Test Mode
0-3	CMD_DATA	R/W	Command Data	

5.1.2. Command Mode Address Format

CMD_ADDR	Function	Type	Description
00	ADC_CHSEL	R/W	ADC channel select signals
01	EN_CTRL	R/W	ADC / MIC enable control signals.
10	Test Mode	R/W	Test mode

5.1.3. Command Mode Data Format

CMD_ADDR = 00：ADC_CHSEL

CMD_DATA	Function	Description	Conditions
[3:1]	ADC_CHSEL	ADC channel select signals.	111 = IN7 110 = IN6 101 = IN5 100 = IN4 011 = IN3 010 = IN2 001 = IN1 000 = IN0 (Default)
[0]	SFT_RST	Software reset	1 = Reset 0 = Active (Default)

Note: When microphone preamplifier is enabled (EN_MIC=1), ADC_CHSEL cannot be set IN5~IN7 channel.

CMD_ADDR = 01: EN_CTRL

CMD_DATA	Function	Description	Conditions
[3]	EN_ADBIAS	ADC and ADC bias enable signal.	1 = Enable 0 = Disable (Default)
[2]	MOD_ADC	ADC bit mode select signal.	1 = 10-bit mode 0 = 12-bit mode (Default)
[1]	EN_AGC	Microphone AGC Control	1 = Enable 0 = Disable (Default)
[0]	EN _MIC	Microphone enable signal.	1 = Enable 0 = Disable (Default)

5.1.4. SPI Timing

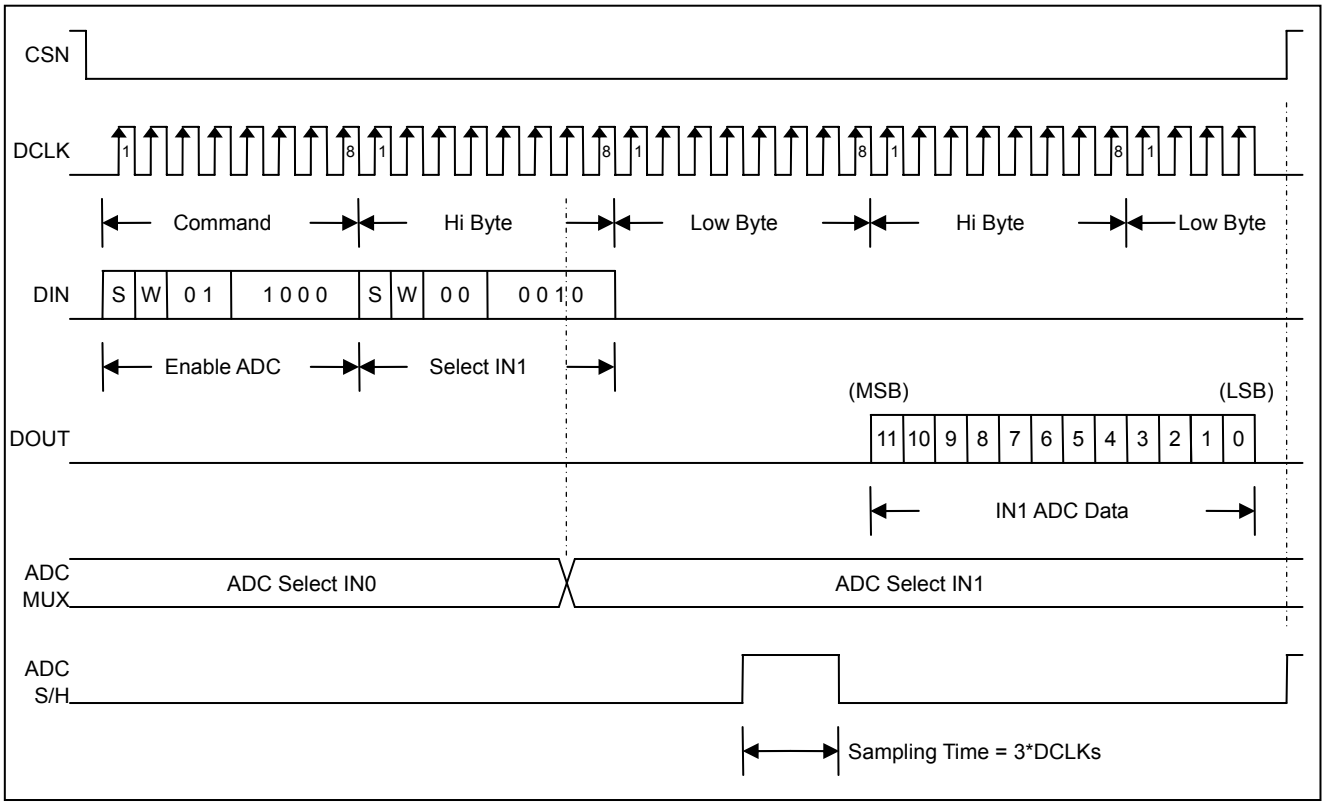


Figure 1. SPI Model 0 – ADC 12 bit Conversion Timing

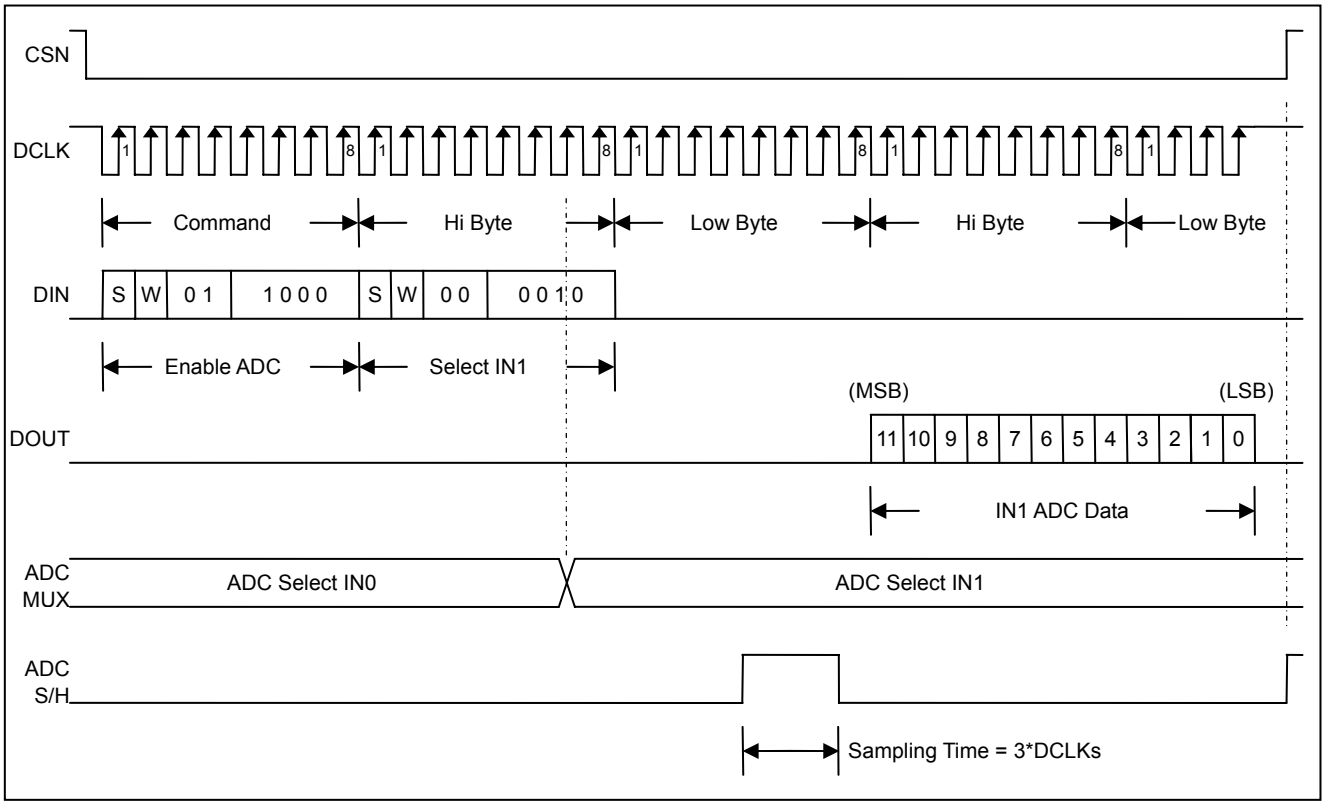


Figure 2. SPI Model 3 – ADC 12-bit Conversion Timing

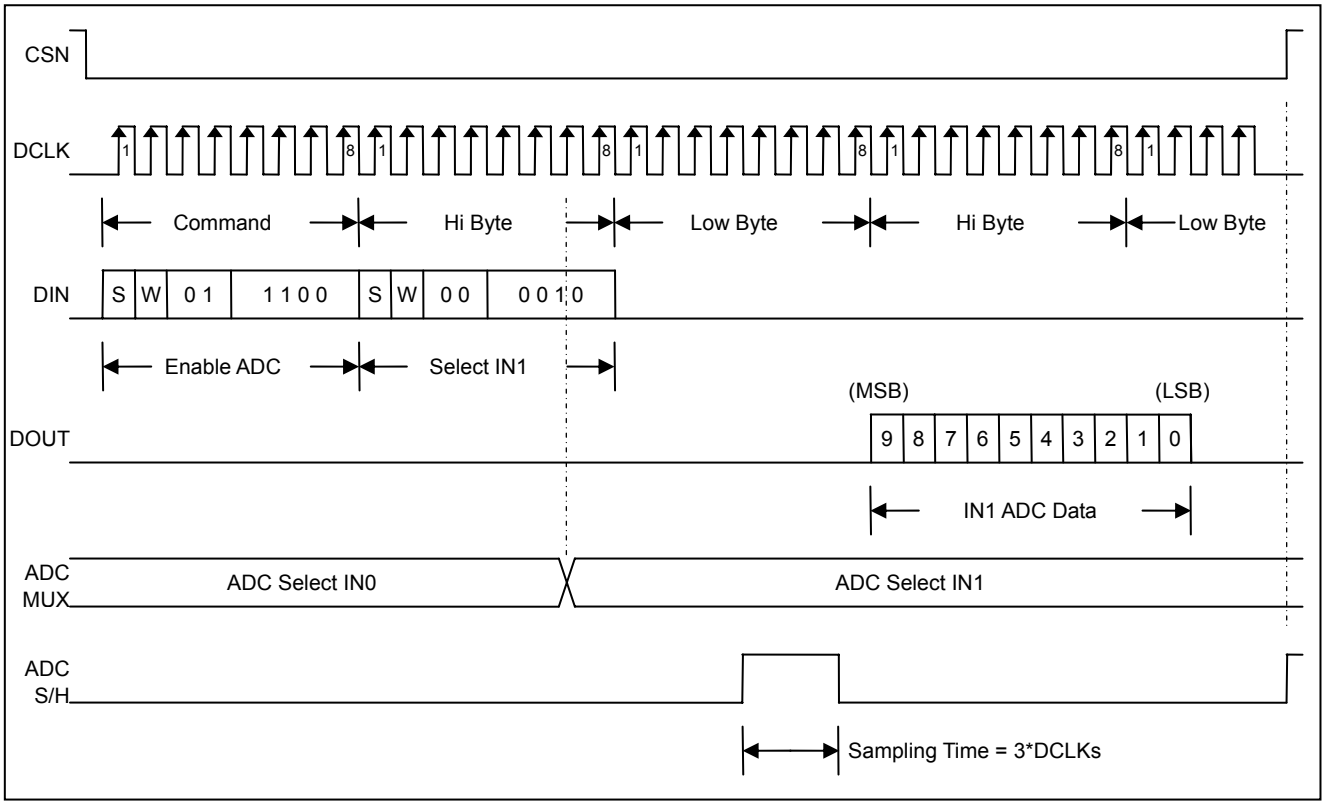


Figure 3. SPI Model 0 – ADC 10-bit Conversion Timing

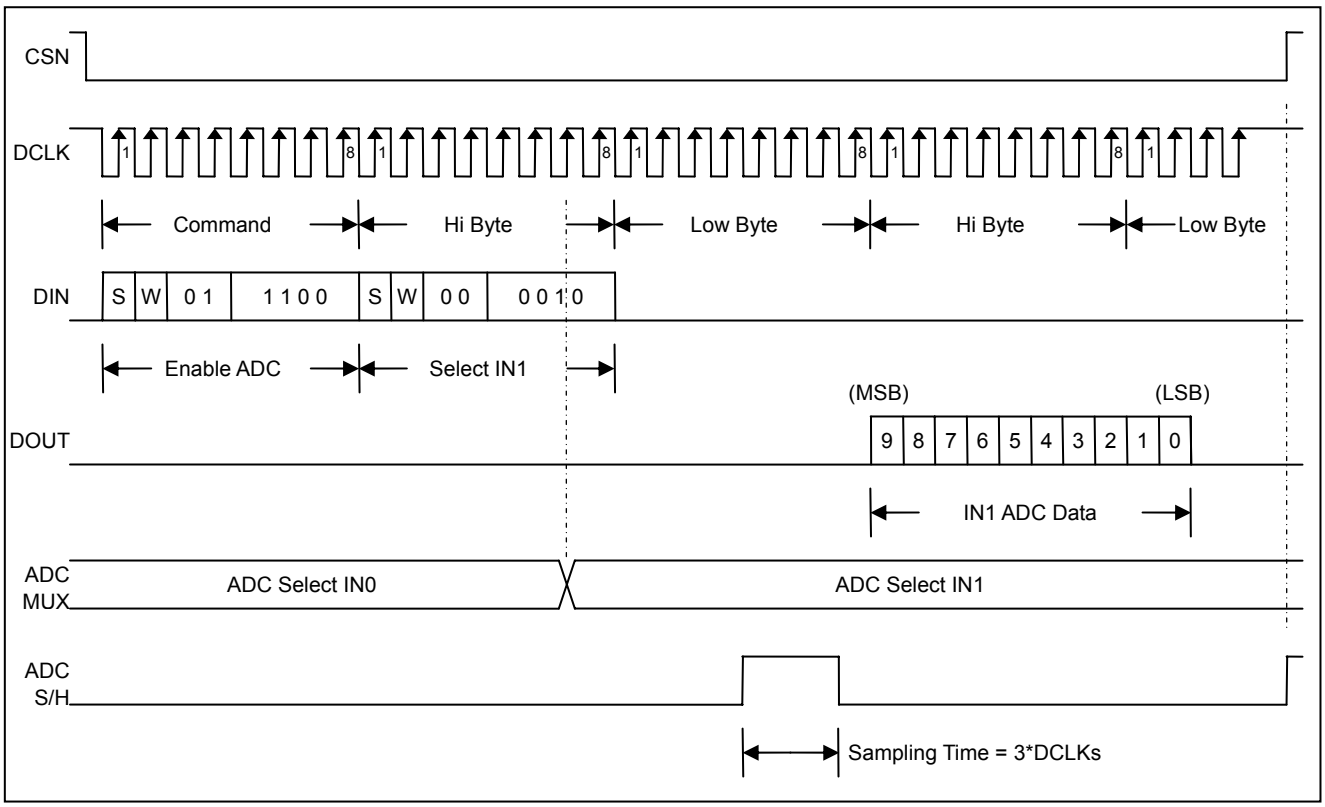


Figure 4. SPI Model 3 – ADC 10-bit Conversion Timing

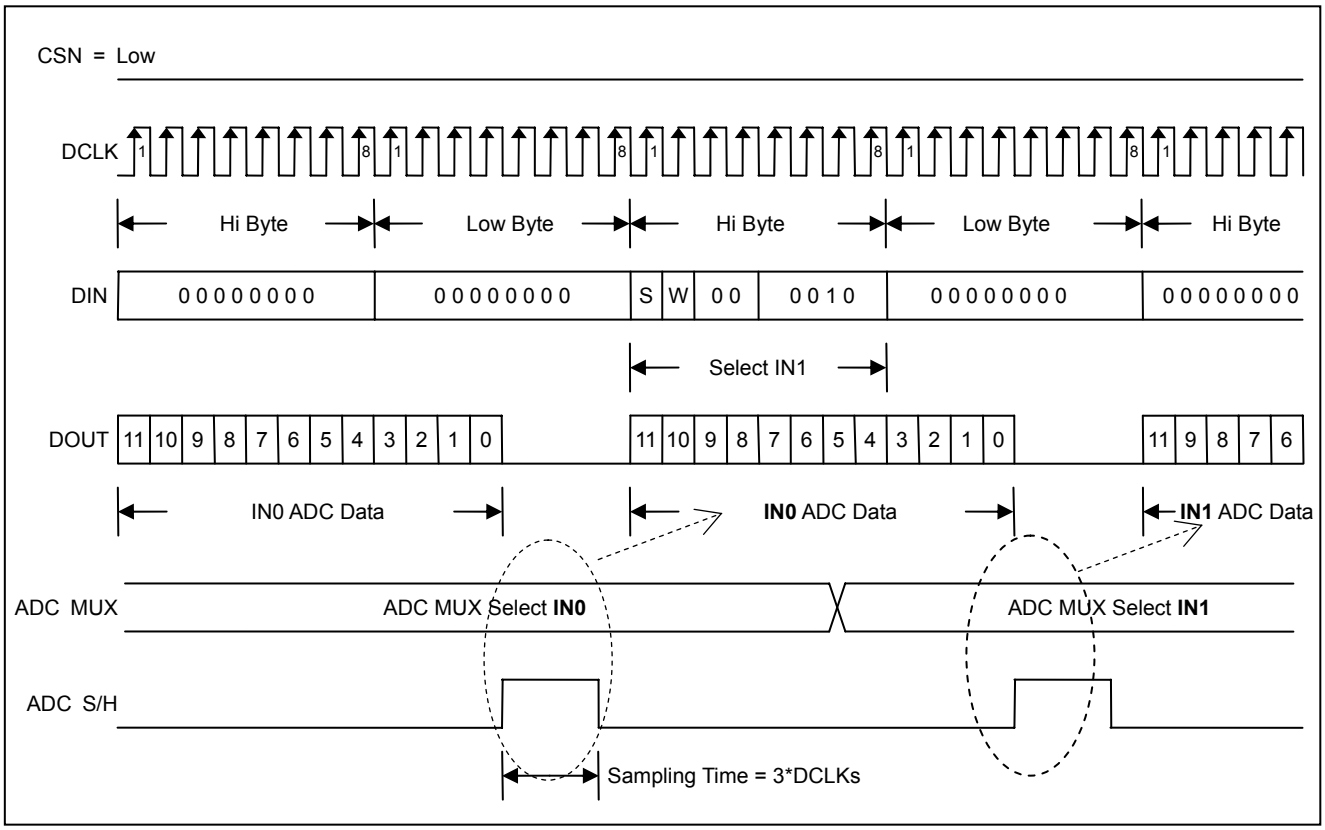


Figure 5. Channel switch during continuous ADC 12-bit conversion.

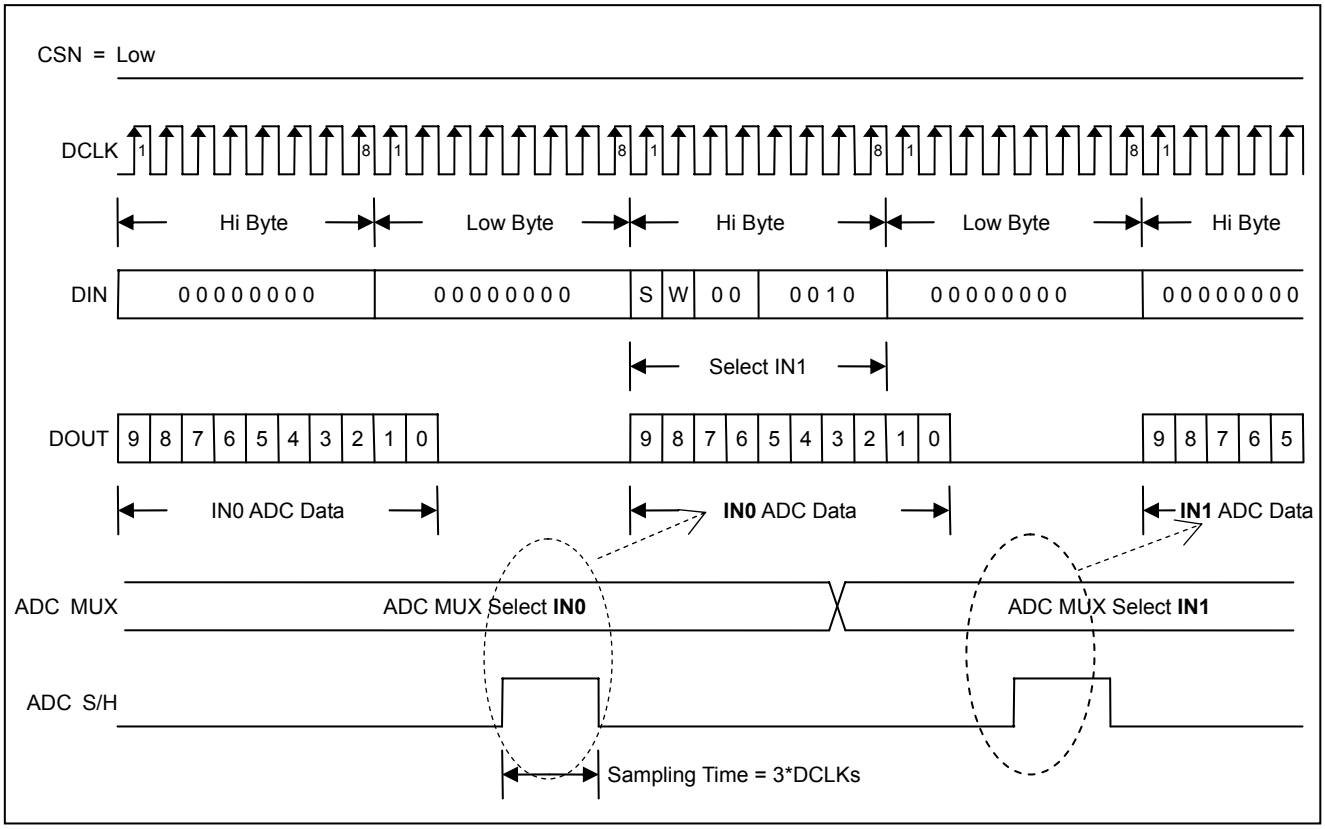


Figure 6. Channel switch during continuous ADC 10-bit conversion.

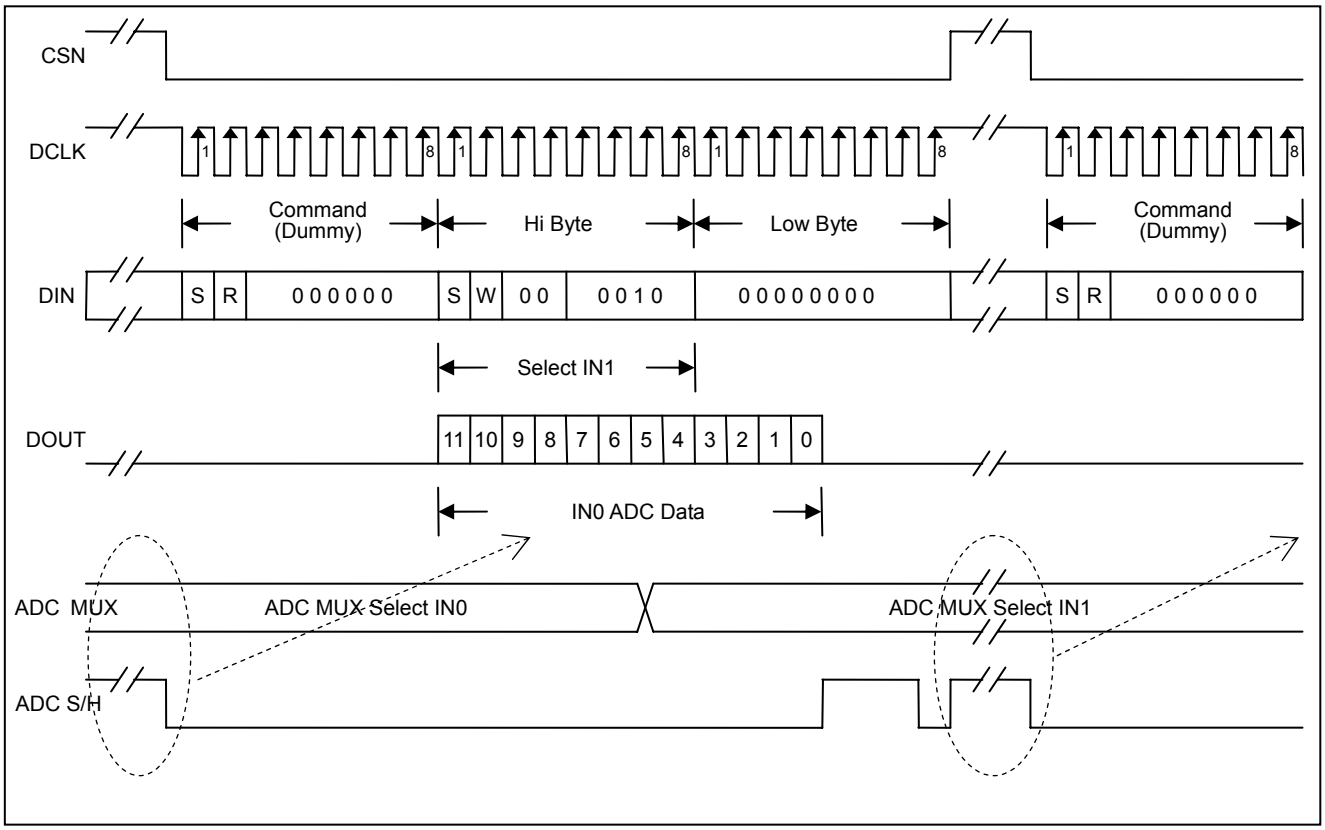


Figure 7. Channel switch during discontinuous ADC 12-bit conversion.

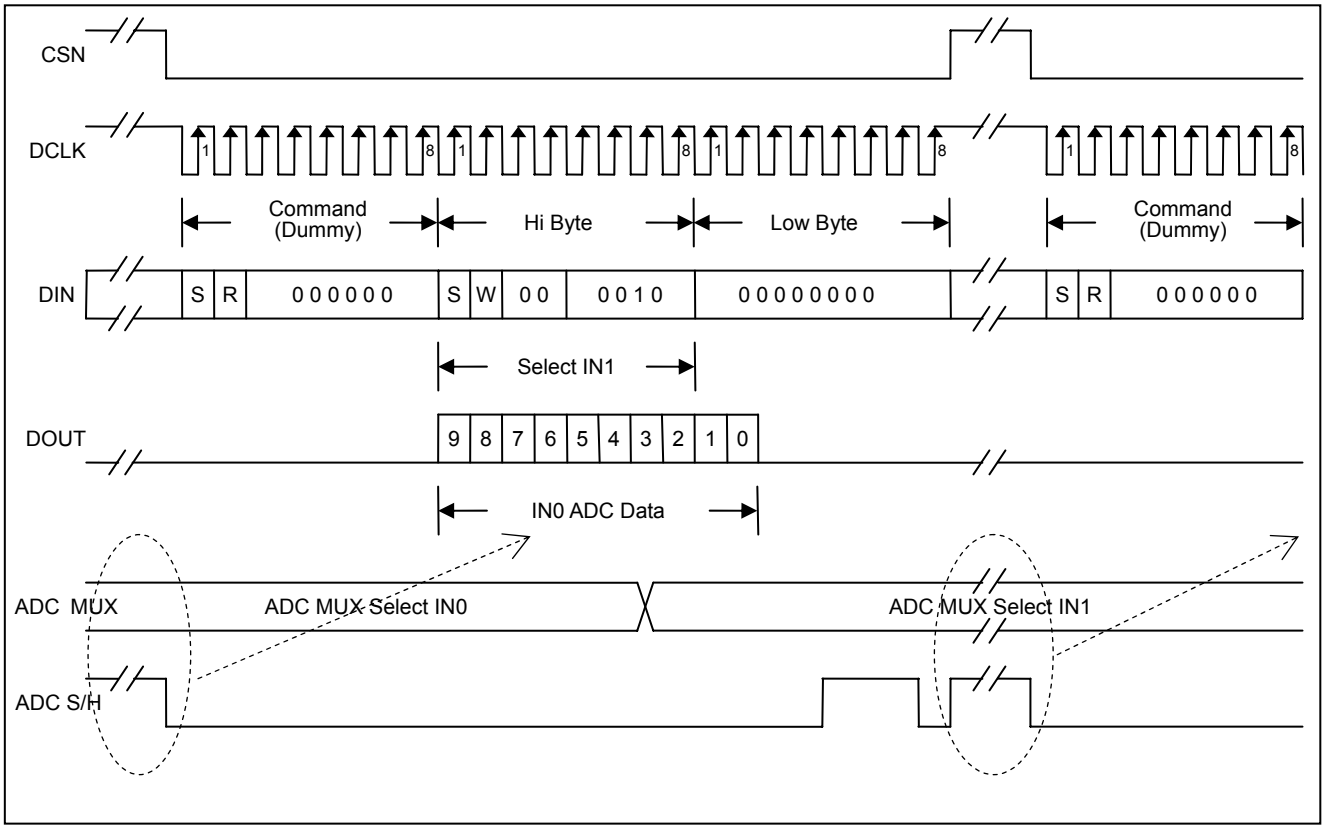


Figure 8. Channel switch during discontinuous ADC 10-bit conversion.

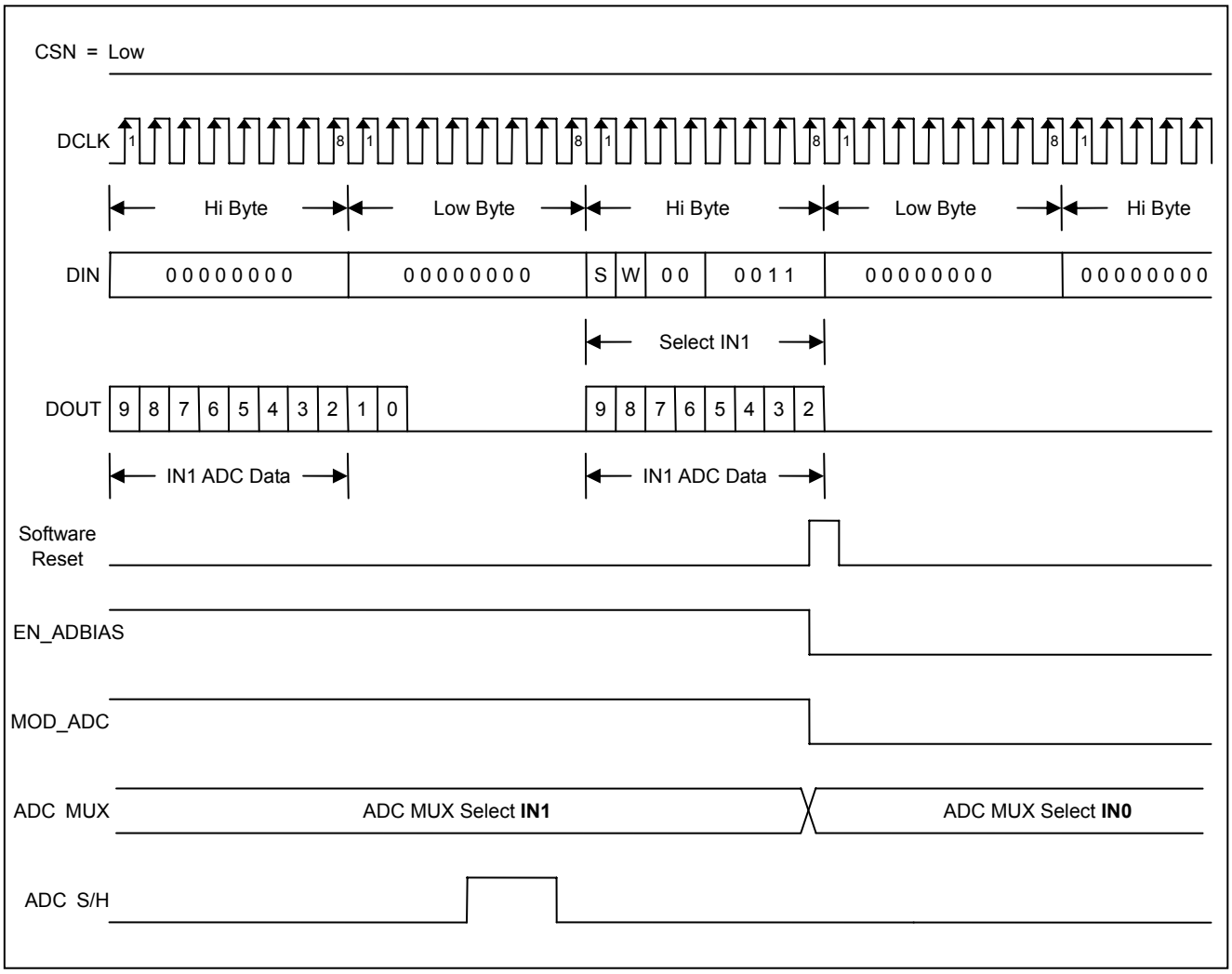


Figure 9. Software Reset Trigger.

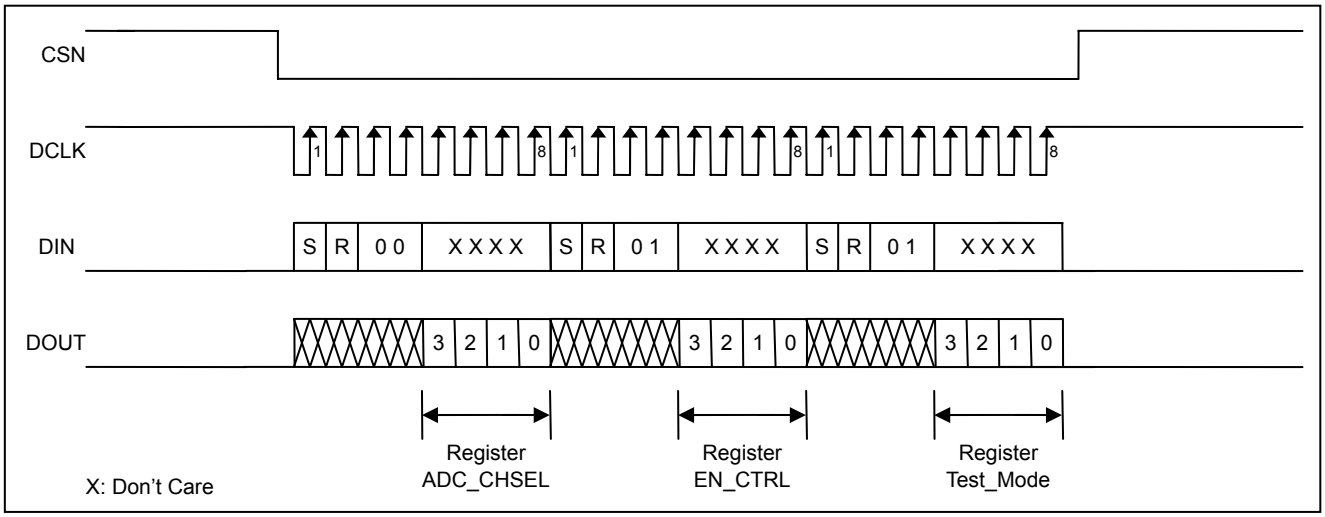


Figure 11. Control registers read-back.

5.2. Analog-to-Digital Converter

The GPY0050A ADC is a 12-bit Successive Approximation Register (SAR) ADC. The ADC provides 12-bit / 10-bit conversion mode operation and 8 analog input channels (see Figure 12). The converter digitizes the input signal form 0V to full-scale voltage (see Figure 13). The internal applied voltage reference value determines the full-scale input voltage range. The voltage reference of the GPY0050A is fixed to V_{DD}.

User can operate the ADC in continuing or discontinuing conversion mode by CSN pin. In continuing conversion mode, CSN pin is always kept low. The GPY0050A requires 16-DCLKs per conversion (see Figure 5 & 6).

Continuous Mode Sampling Rate = f_{DCLK} / 16

In discontinuing conversion mode, the ADC sampling and holding signal (ADC_S/H) can be controlled by CSN pin. The ADC will hold analog value on CSN falling edge, and need 24-DCLKs to finish conversion (see Figure 7 & 8). In discontinuing conversion mode, user can easily control sampling and holding time by CSN pin.

The ADC_CHSEL register is used to select ADC input channel (IN0 ~ IN7). The IN5 ~ IN7 pins are shared with microphone preamplifier block. Therefore, the MUX cannot be set to IN5 ~ IN7 channel, when microphone preamplifier is enabled.

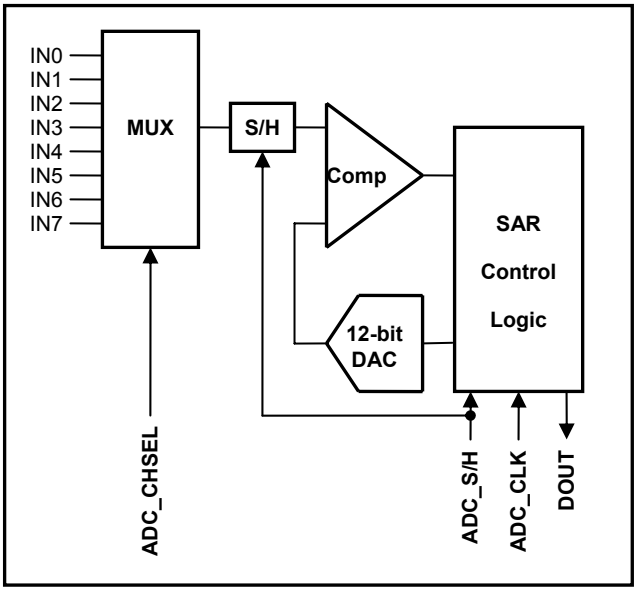


Figure 12. ADC Function Block Diagram

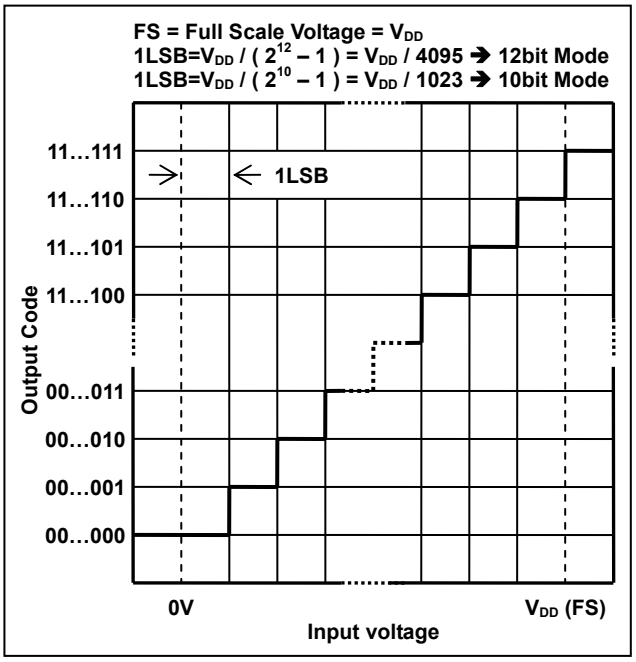


Figure 13. Ideal Input Voltage and Output Codes

5.3. Microphone Preamplifier

The GPY0050A Microphone Preamplifier consists of several distinct circuits: microphone bias switch (M1), first stage amplifier (MIC Preamplifier), second stage amplifier (OP-Amplifier) and AGC control circuitry, shown in Figure 14.

When register EN_MIC is set to '1', the internal switch M1 will be turned on and VMIC pin will be shorted to VDD. In order to reduce power noise, recommend RC time constant of (R_{VMIC}xC_{VMIC}) must be greater than 8ms and resistance of the R_{VMIC} must be less than 2kΩ.

The first stage microphone amplifier (MIC Preamplifier) is difference input preamplifier. The gain can be varied by the AGC. When AGC pin voltage rises, the MIC preamplifier will reduce the gain. If AGC function is turned off (EN_AGC='0'), the gain will be set to maximum value (Gain=15 @ VDD=3.3V).

The second stage amplifier consists of R1, R2 and OPA. The default gain is (1+R2/R1) = 41. Users can make a series resistance reduce the gain of second stage amplifier.

Gain of second stage amplifier = 1 + R2 / (R1+R_{OP1})

The AGC Control senses OPO pin output waveform. When "V_{OPO} > VDD – 0.3" or "V_{OPO} < 0.3", the AGC will pump C_{AGC} capacitor. The AGC voltage will rise to reduce gain of first stage amplifier until "V_{OPO} < VDD – 0.3" or "V_{OPO} > 0.3". In order to avoid the noise generated by the AGC Control, recommend capacitance of the C_{AGC} must be greater than 2.2uF and resistance of the R_{AGC} must be greater than 470kΩ.

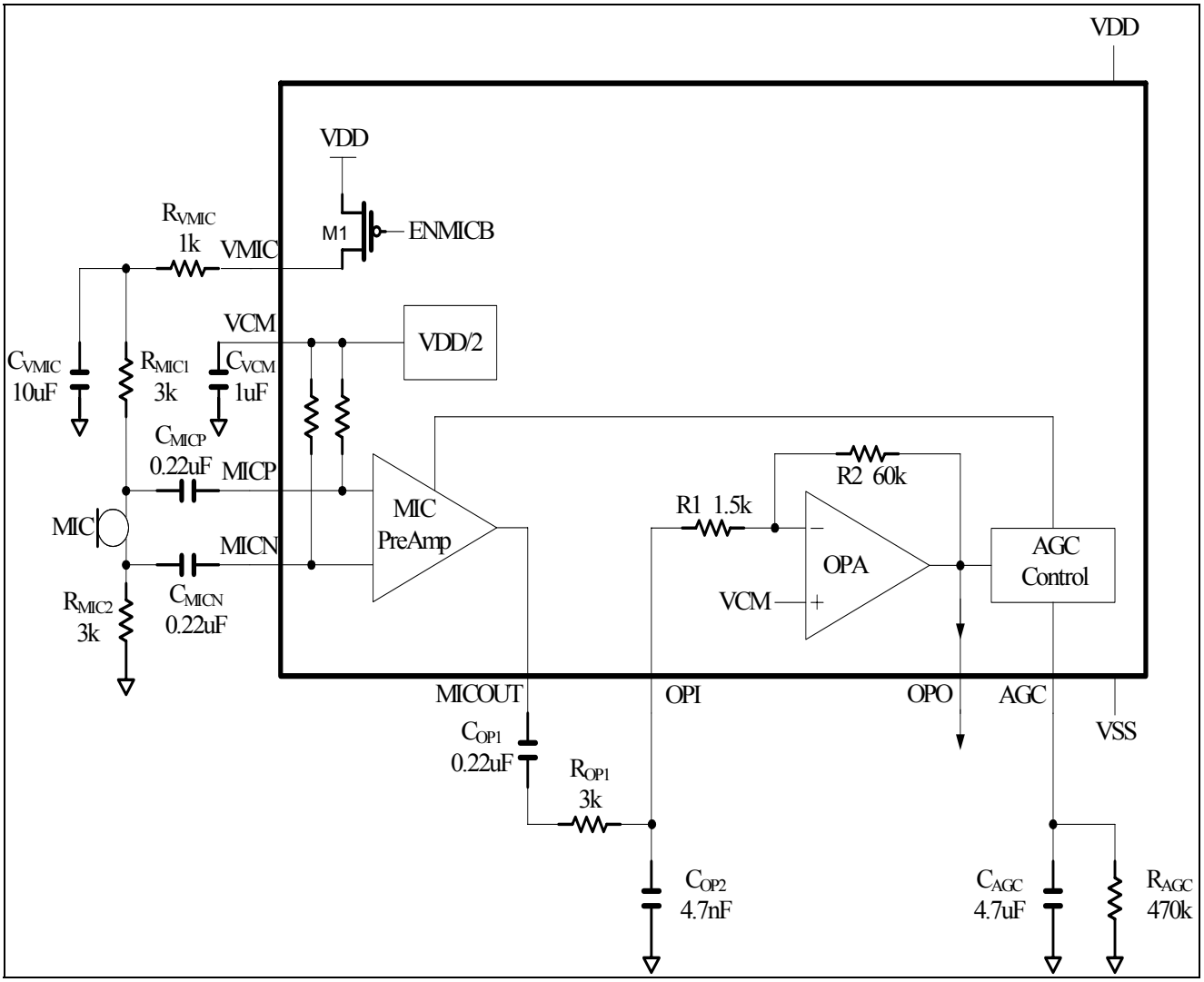


Figure 14. Microphone Preamplifier Block Diagram and Application Circuit

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating free-air Temperature Range	T_A	0℃ to + 60℃
Storage Temperature	T_{STO}	-50℃ to + 150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (V_{DD}=5.0V, T_A = 25°C)

Item	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Operation Voltage		V_{DD}	2.2	-	5.5	V
Shutdown Current		I_{STBY}	-	0.1	1.0	uA
Operating Current	V_{DD} = 5.0V	I_{DD}	-	2.2	3.5	mA
DCLK Frequency			-	-	2	MHz
ADC Conversion Time			-	-	16	DCLKs
ADC Acquisition Time			3	-	-	DCLKs
ADC Conversion Rate	DCLK/16	F_{CONV}		-	125	KHz
Resolution of ADC		RESO	-	-	12	bits
Signal-to-Noise Plus Distortion of ADC from Line In		SINAD	-	64	-	dB
Effective Number of Bit		ENOB	-	10.5	-	bits
Integral Non-Linearity of ADC		INL	-	±1.0	-	LSB
Differential Non-Linearity of ADC		DNL	-	±0.8	-	LSB
No Missing Code			-	12	-	bits
Microphone Input Impedance		R_{IN}	-	10	-	KΩ
Microphone AGC Gain	V_{IN}=15mV~300mV, C_{AGC}=47uF	Gain	6	-	40	dB
Microphone Total Harmonic Distortion	V_{IN}=20mV, f = 1.0KHz	THD+N	-	60	-	dB

7. APPLICATION CIRCUIT

The demo board circuit of the GPY0050A is shown in Figure 15. User can easily evaluate GPY0050A performance by the demo board. In order to reduce power noise from other device, suggest connecting Power and GND Line from power source, adding power filter for the GPY0050A and don't share power and ground line with other devices. (See Figure 16 & 17)

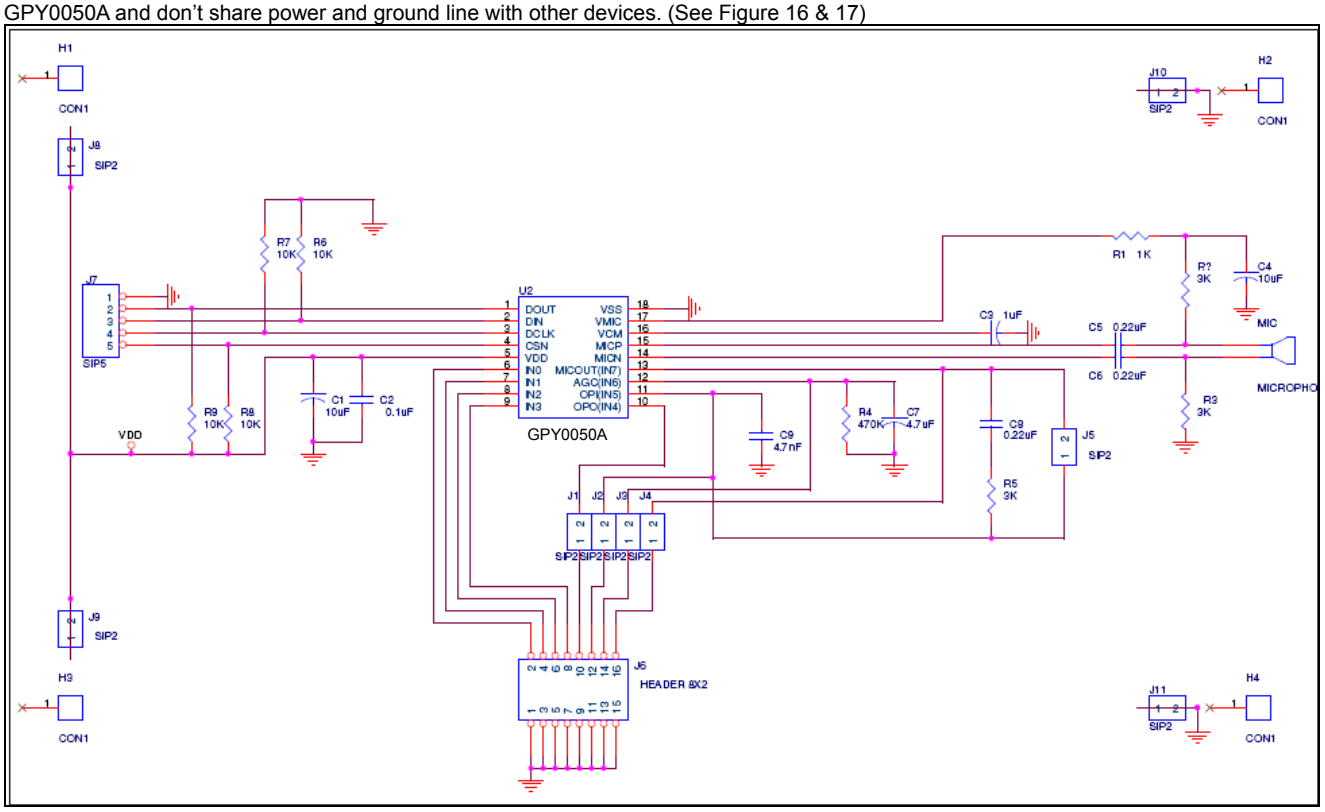


Figure 15. Demo Board Circuit of the GPY0050A

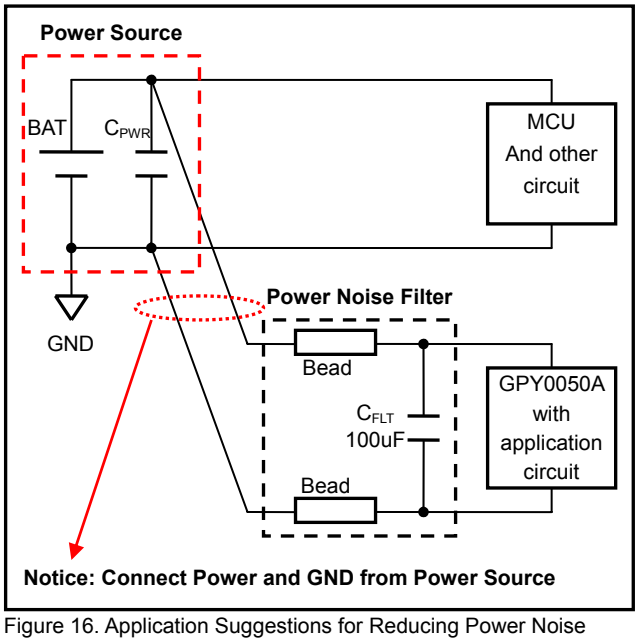


Figure 16. Application Suggestions for Reducing Power Noise

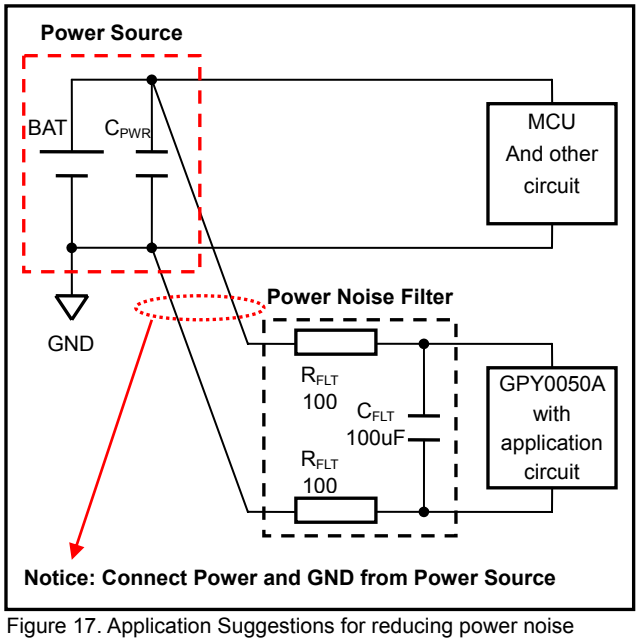


Figure 17. Application Suggestions for reducing power noise

8. PACKAGE/PAD LOCATIONS

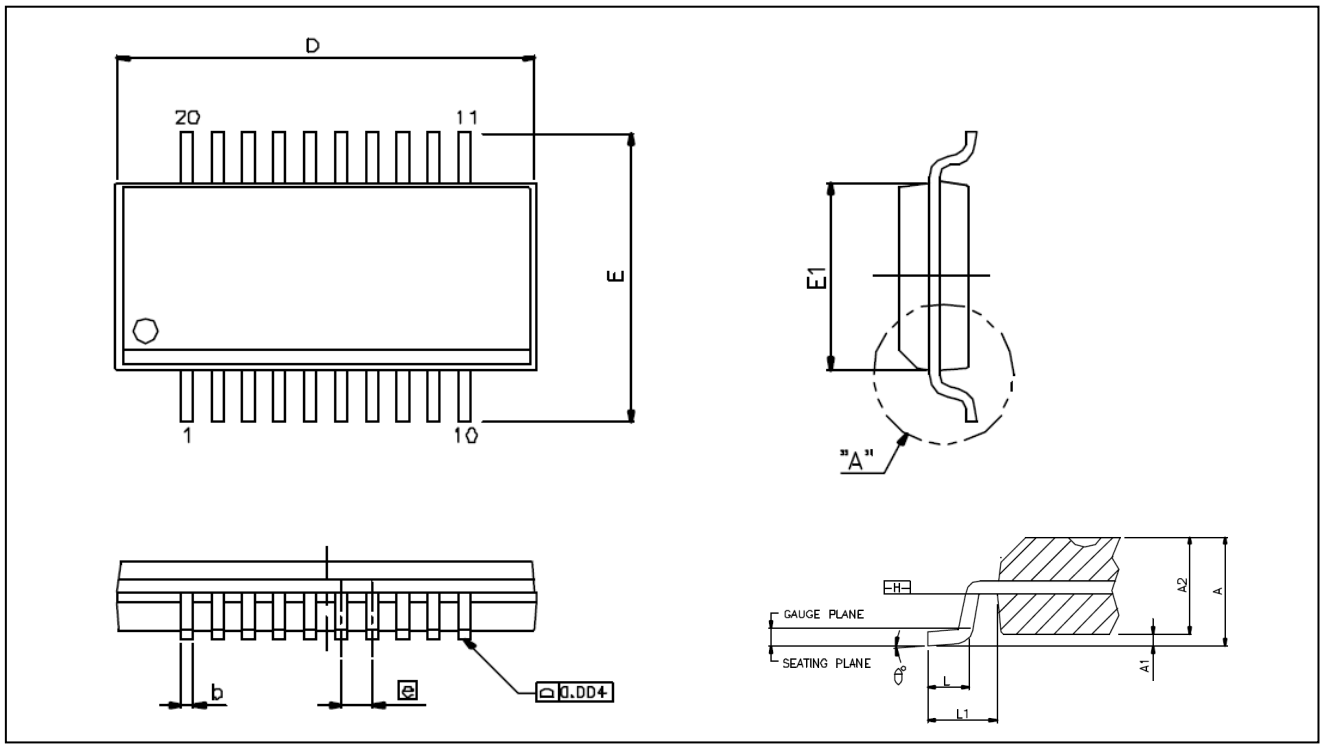
8.1. Ordering Information

Product Number	Package Type
GPY0050A - C	Chip form
GPY0050A - HG08x	Green Package - SSOP20 (150mil)
GPY0050A - HG01x	Green Package - SSOP16 (150mil)

Note: Package form number (x = 1 - 9, serial number).

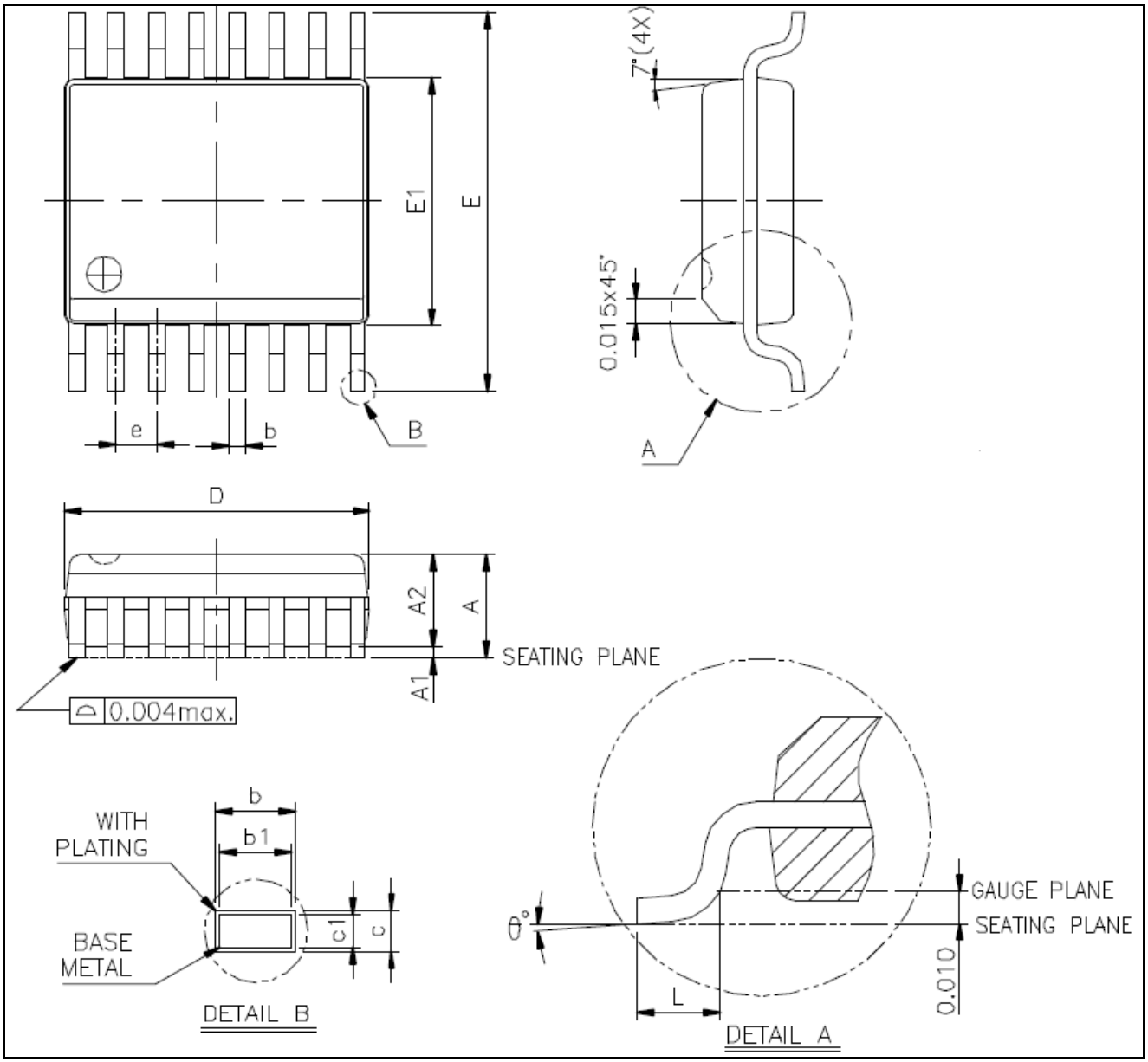
8.2. Package Information

8.2.1. SSOP 20



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	-	-	0.059
b	0.008	-	0.012
C	0.007	-	0.010
D	0.337	0.341-	0.344
E	0.291	0.236	0.244
E1	0.150	0.154	0.157
e	0.025 BASIC		
L	0.016	0.025	0.050
L1	0.014 BASIC		
θº	0	-	8

8.2.2. SSOP 16



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	0.053	-	0.069
A_1	0.004	-	0.010
b	0.008	-	0.012
b1	0.008	-	0.011
D	0.189	-	0.197
E	0.228	-	0.244
E_1	0.150	-	0.157
L	0.016	-	0.050
e	0.025 BASIC		
θº	0	-	8

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10. REVISION HISTORY

Date	Revision #	Description	Page
SEP. 16, 2014	1.1	1. Modify “SIGNAL DESCRIPTIONS” in section 4. 2. Modify “Pad Assignment” in section 4.1. 3. Modify “Package Pin Assignment” in section 4.2. 4. Modify “Ordering Information” in section 8.1. 5. Modify “Package Information” in section 8.2.	4 5 5 17 17
MAY 03, 2011	1.0	1. Modify “SPI Serial Interface” in section 5.1. 2. Add “Analog-to-Digital Converter” in section 5.2. 3. Add “Microphone Preamplifier” in section 5.3. 4. Modify “Application Circuit” in section 7.	6 13 14 16
AUG. 17, 2009	0.1	Original	18