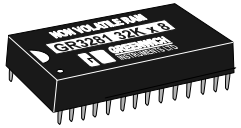
GR3281 (32K x 8)
NON-VOLATILE RAM

GREENWICH INSTRUMENTS LTD



DESCRIPTION

The GR3281 is a 32768 word by 8 bits (32K x 8) non-volatile CMOS Static Ram, fabricated from advanced silicon gate CMOS technology and a high reliability lithium power cell.

The pin-out of the GR3281 conforms to the JEDEC standards and is fully compatible with normal static RAM.

The power down circuit is fully automatic and is referenced at 4.5 volts. At this point the GR3281 is write protected by an internal inhibit function for Data Protection and the memory contents are retained by the lithium power source.

Power down is very fast, this being essential for data integrity, taking a maximum of 15 µS (15 microseconds) to power down from 5 volts to 0 volts. This is much faster than system power failure conditions. Therefore there are no special conditions required when installing the GR3281.

The GR3281 can, without external power, retain data almost indefinitely. The limiting factor will be the shelf life of the lithium cell, which is typically ten years. It is possible that this figure may be extended in view of the extremely light duty imposed upon the cell.

APPLICATION

When powered down, the GR3281 is transportable and data can be moved from system to system, this makes it ideal for program development, data collection in data loggers, program changes in process control, automation and robotics and user definable lookup tables, etc.

DISPOSAL INSTRUCTIONS

Do not dispose of non-volatile memory devices by incineration or crushing. Devices may be returned carriage paid to Greenwich Instruments Ltd., for disposal.

UK

Greenwich Instruments Ltd.,
Meridian House, Park Road,
Swanley, Kent. BR8 8AH
Tele: 08700 505 404
Fax: 08700 505 405

ABSOLUTE MAXIMUM RATINGS

Symbol	Min	Max	Units
Vdd	– 0.3	7.0	Volts
Vi/o	– 0.3	Vdd +0.3	Volts
Temp	– 20	+70	deg. C

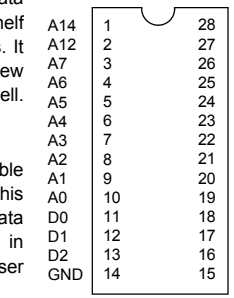
OPERATING CONDITIONS

Symbol	Min	Typ	Max	Unit
Vdd	4.75	5.0	5.5	Volts
Vin (1)	2.2			Volts
Vin (0)			0.8	Volts
Iin (any other pin)	– 1.0		+1.0	µA.
Vout (1)(Iout = –1mA)	2.4			Volts
Vout (0)(Iout = +2mA)			0.4	Volts
Idd (Active)		30		mA.
Idd (Deselected)		1.0		mA.
Tcycle			100	nS.
Cin (any pin)		10		pF

OPERATING MODE

$\overline{CE}$	$\overline{OE}$	$\overline{WR}$	MODE	OUTPUT	Idd
H	X	X	Unsel.	Hi-Z	Deselected
L	H	H	Unsel.	Hi-Z	Active
L	L	H	Read	Dout	Active
L	X	L	Write	Din	Active

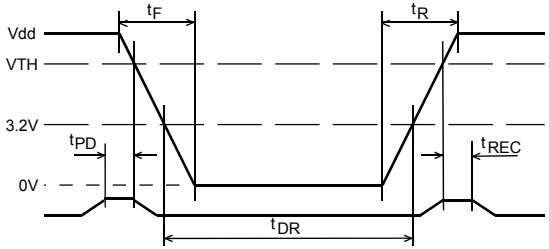
PIN CONNECTIONS



PIN DESIGNATIONS

Pin	Function
A0-A12	Address I/P`s
D0-D7	Data in/out
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WR}$	Write Enable
Vdd	+5Volt Power
GND	Ground

DATA RETENTION OPERATING CONDITIONS



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Vdd	Operating supply voltage	4.75	5.0	5.50	Volts
VTH	Data retention voltage		4.5		Volts
t_F	Vdd slew to 0V	15			µS
t_R	Vdd slew 0V to 5.0V	15			µS
t_{REC}	CE to O/P valid from power up			15	µS
t_{DR}	Data retention time		10		Years
t_{PD}	CE at Vin(1) before power down	0			µS

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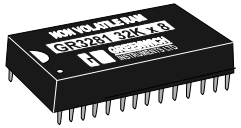

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Greenwich Instruments Ltd., are continually developing their products and reserve the right to alter specifications without prior notice. Standard Terms and Conditions of Sale apply.

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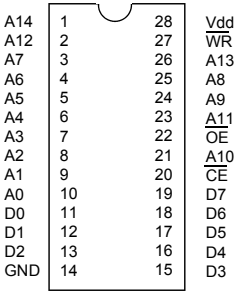
PIN CONNECTIONS



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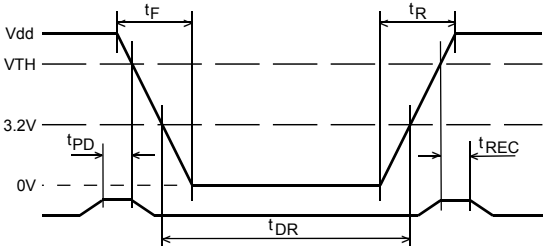

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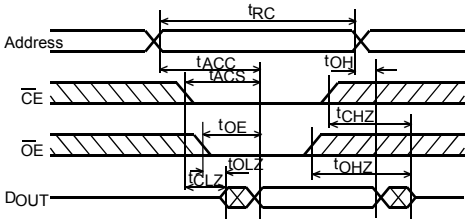
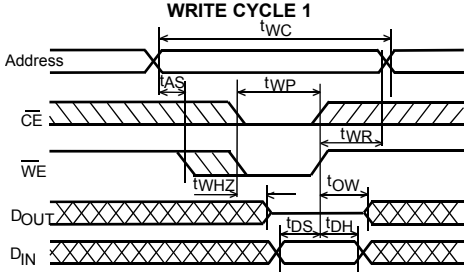
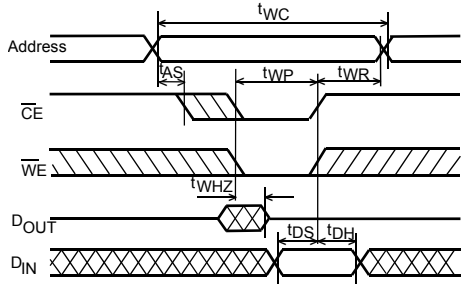
READ CYCLE



WRITE CYCLE 1



WRITE CYCLE 2



TIMING (nS-nano seconds)

	Read Cycle	100nS	
Symbol	**Parameter**	**Min**	**Max**
tRC	Read cycle time	100	
tACC	Access time		100
tACS	$\overline{CE}$ to output valid		100
tOE	$\overline{OE}$ to output valid		50
tCLZ	$\overline{CE}$ to output active	10	
tOLZ	$\overline{OE}$ to output active	10	
tOH	Output hold time	20	
tCHZ	$\overline{CE}$ to output disable		35
tOHZ	$\overline{OE}$ to output disable		35

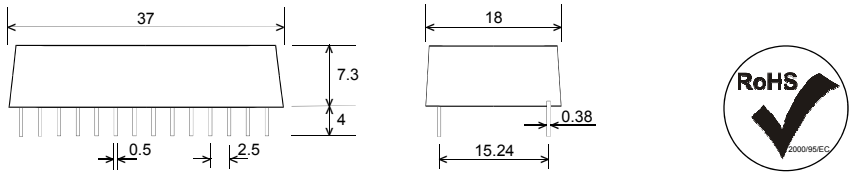
	Write Cycle	100nS	
Symbol	**Parameter**	**Min**	**Max**
tWC	Write cycle time	100	
tWP	Write pulse width	60	
tAS	Address setup time	0	
tWR	Write recovery time	0	
tWHZ	$\overline{WR}$ to output disable		35
tOW	Output active from $\overline{WR}$	10	
tDS	Data setup time	35	
tDH	Data HOLD TIME	0	

Notes
1. $\overline{WE}$ must be high during address transitions.
2. A Write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.
3. $\overline{WE}$ is high for a read cycle.

REPLACES

62256., 43256., 55257., etc.

DIMENSIONS (mm)



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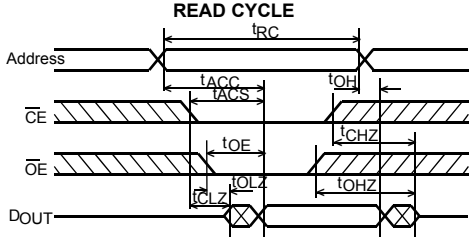

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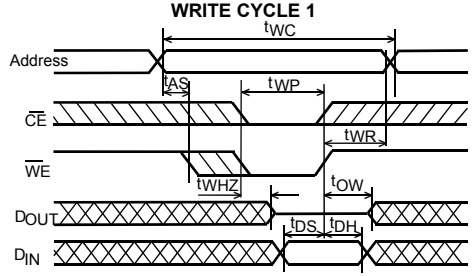
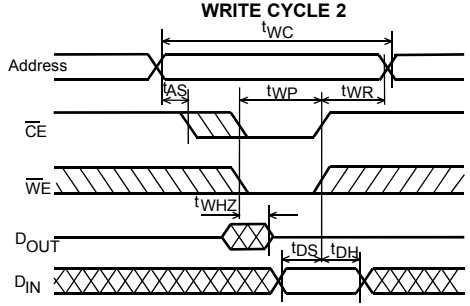


WRITE CYCLE 2



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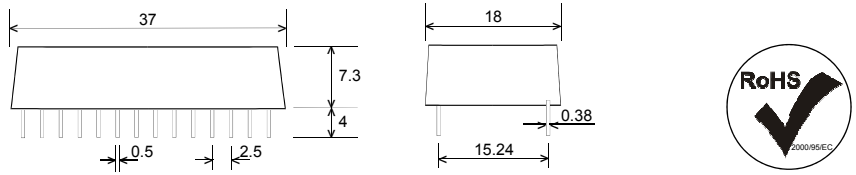

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ISSUE 4 OCT 2005