Power Factor Controller IC for High Power Factor

Features

- Low Startup Current
- Low Quiescent Current
- Under-Voltage Lockout with Hysteresis
- Zero Current Detector for Critical Conduction Mode
- Dynamic and Static Output Over-Voltage Protection
- Gate Output Maximum Voltage Clamped
- Internal Restart Timer
- 1% Internal Reference Voltage
- Internal Leading-Edge Blanking
- +/-500mA Totem Pole Output with Active Shut Down

Applications

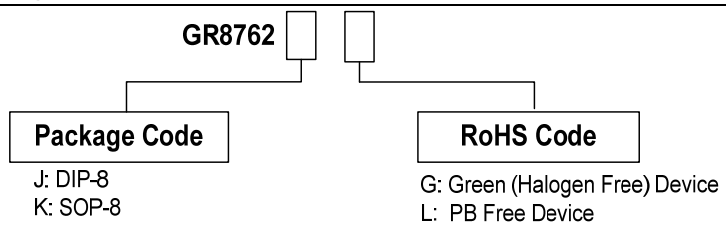
- Power Supply PFC Pre-Regulator
- LED Lighting Application
- Desktop PC
- Electronics Ballast for Fluorescent Lamp

Description

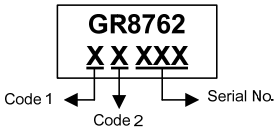
The GR8762 is a current-mode PFC controller operating in critical conduction mode. The sinusoidal current is taken from the single phase line supply and stabilized DC voltage is available at the output. The IC includes a highly liner multiplier which can reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even over a large load range.

The output voltage is controlled by an error amplifier and an internal voltage reference. An effective two-step (dynamic and static) OVP enables to safely handle over voltages either occurring at start-up or resulting from load disconnection. The totem-pole output stage capable of ±500mA driving capability is suitable for big MOSFET or IGBT. It is available in both 8-pin DIP and 8-pin SOP package.

Ordering and Marking Information



DIP-8/SOP-8



Code 1	8	9	A	B		G	H	I	J
Year	2008	2009	2010	2011		2016	2017	2018	2019
Code 2	1	2	3	4		9	A	B	C
Month	Jan.	Feb.	Mar.	Apr.		Sep.	Oct.	Nov.	Dec.

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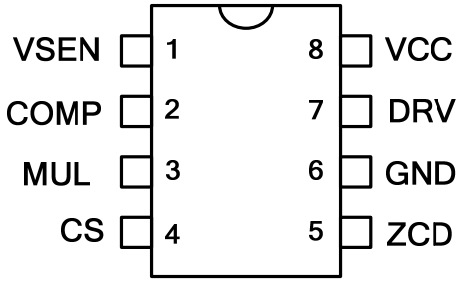
Pin Configuration

TOP VIEW



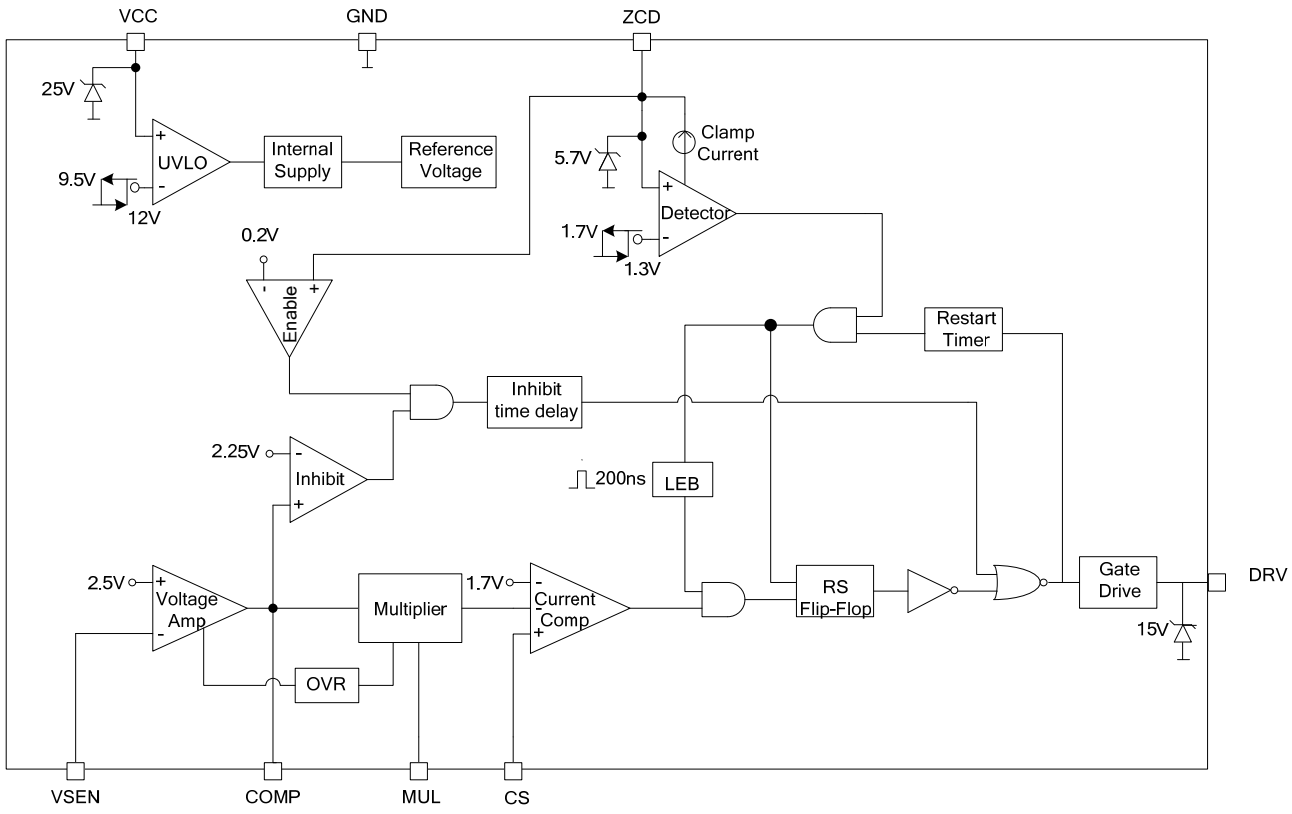
Pin Description

Pin	Symbol	Description
1	VSEN	Voltage error amplifier Inverting Input. VSEN is connected via a resistive divider to the boost converter output, With a capacitor connected to COMP, The internal error amplifier acts as an integrator.
2	COMP	Voltage error amplifier output. This is the first multiplier input. If the current flowing into this pin is exceeding an internal threshold, the multiplier output voltage is reduced to prevent the MOSFET from over-voltage damage.
3	MUL	Multiplier input, which is the second multiplier input and is connected via a resistive divider to the rectifier output voltage.
4	CS	Current sense input, which is connected to a sense resistor controlling the MOSFET source current .A leading edge blanking circuitry, suppresses voltage spits when turning the MOSFET on.
5	ZCD	Zero current detector input, which is connected to an auxiliary winding monitoring the zero crossing of the inductor current.
6	GND	Ground
7	DRV	Gate drive output, which is the output of a totem-pole circuitry for direct driving a MOSFET.
8	VCC	Positive voltage supply. If VCC exceeds the UVLO (on) threshold, the IC is switched on. When VCC falls below the UVLO (off) threshold, it is switched off and power consumption is very low. VCC is internally clamped to 28V.

Absolute Maximum Ratings

VCC supply + zener current ---------- 20mA
Voltage at Pin VSEN, MUL, CS, ZCD ---------- -0.3V~6.5V
Junction temperature ---------- 150℃
Operating ambient temperature ---------- -20℃ ~ 85℃
Storage temperature range ---------- -65℃ ~ 150℃
SOP-8 package thermal resistance ---------- 160℃/W
DIP-8 package thermal resistance ---------- 100℃/W
Power dissipation (SOP-8, at ambient temperature = 85℃) ---------- 400mW
Power dissipation (DIP-8, at ambient temperature = 85℃) ---------- 650mW
Lead temperature (All Pb free packages, soldering, 10sec) ---------- 260℃
ESD voltage protection (Human body model) ---------- 2 KV
ESD voltage protection (Machine model)---------- 200 V

Block Diagram



Electrical Characteristics (Ta = 25℃, Vcc = 12V, C_O=1nf, unless otherwise specified.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
VCC			10.5		22	V
Zener Voltage	I_{CC}+I_Z=20mA	V_Z	22	25	28	V
UVLO on Voltage		V_{CC-ON}	11	12	13	V
UVLO off Voltage		V_{CC-OFF}	8.5	9.5	10.5	V
VCC Hysteresis		V_{CC-HY}		2.5		V
SUPPLY CURRENT						
Startup Current		I_{CCL}		40	70	uA
Quiescent Current 1	I_{CCH} after turn on			2.5	3.8	mA
Operating Supply Current		I_{CC}		3.5	5.0	mA
Quiescent Current 2	During OVP(either static or dynamic or Vinv≤150mV)			1.7	2.2	mA
VOLTAGE ERROR AMPLIFIER						
Voltage Feedback Input Theshold		V_{FB}	2.465	2.5	2.535	V
Line Regulation	Vcc = 10.3V~22V	V_{FBLR}		2	5	mV
Input Bias Current	V_{INV}=0 to 3V				-1	uA
Voltage Gain		G_V	60	80		dB
Gain Bandwidth		G_{BW}		1		MHz
Source Current	V_{COMP}= 4V V_{SEN}=2.4V	$I_{COMPsrc}$	-2	-3.5	-5	mA
Sink Current	V_{COMP}= 4V V_{SEN}=2.6V	$I_{COMPsnk}$	2.5	4.5	5.5	mA
Upper Clamp Voltage	I_{SOURCE}= 0.5mA	V_{COMP_H}	4.5	5.0	5.5	V
Lower Clamp Voltage	I_{SINK}= 0.5mA	V_{COMP_L}	2.0	2.2	2.4	V
MULTIPLIER INPUT						
Input Bias Current	V_{VFF}= 0 to 4V	I_{MUL}			-1	uA
Dynamic Voltage Range of MUL		V_{MUL}	3.0			V
$\frac{\Delta V_{CS}}{\Delta V_{MUL}}$	V_{MUL}=0 to 0.5V V_{COMP}=Upper Clamp		1.65	1.9		V/V
K Gain	V_{MUL}=1V V_{COMP}=4V			0.6		1/V
OVER-VOLTAGE REGULATOR						
Threshold Current		I_{OVR}		30		uA

Hysteresis				20		uA
Static OVP Threshold			2.15	2.25	2.35	V

CURRENT SENSE COMPARATOR

Delay to Output		$T_{D(H-L)}$		200	350	nS
Current Sense Reference Clamp	V_{COMP}= Upper Clamp		1.6	1.7	1.8	V
Current Sense Offset	V_{MUL}= 0	$V_{CSoffset}$		30		mV
Leading Edge Blanking		T_{LEB}		200		nS

ZERO CURRENT DETECTOR

Upper Clamp Voltage	I_{ZCD}= 2.5mA		5.0	5.7	6.5	V
Lower Clamp Voltage	I_{ZCD}= -2.5mA		0.3	0.65	1.0	V
Upper Threshold Voltage Arming Voltage (positive-going edge)		V_{ZCDA}		1.7		V
Lower Threshold Voltage Arming Voltage (negative-going edge)		V_{ZCDT}		1.3		V
Source Current Capability		I_{ZCD_src}	-2.5		-5.5	mA
Sink Current Capability		I_{ZCD_sink}	2.5			mA
Disable Threshold		V_{ZCD_DIS}	150	200	250	mV
Restart Threshold		V_{ZCD_EN}	250		350	mV
Restart Current after Disable			30	75		uA

RESTART TIMER

Restart Time		T_{RES}	75	190	300	uS

GATE DRIVER

Dropout voltage	$I_{GD\ source}$ = 20mA			2.0	2.6	V
	$I_{GD\ source}$ = 200mA			5.5	6.5	V
	$I_{GD\ sink}$=200mA			1.3	2.0	V
Rising Time	Load=1nF	T_{RISE}		40	80	nS
Falling Time	Load=1nF	T_{FALL}		30	70	nS
Clamp		V_{CLAMP}	10	12	15	V
UVLO Saturation	VCC = 0 to VCC I_{sink}=2mA				3.5	V

Typical Performance Characteristics

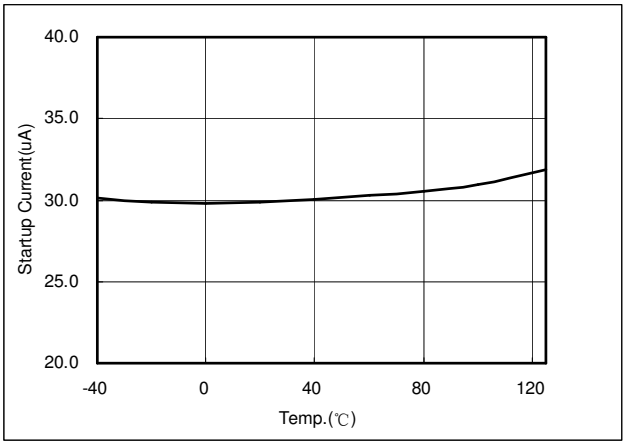


Fig. 1

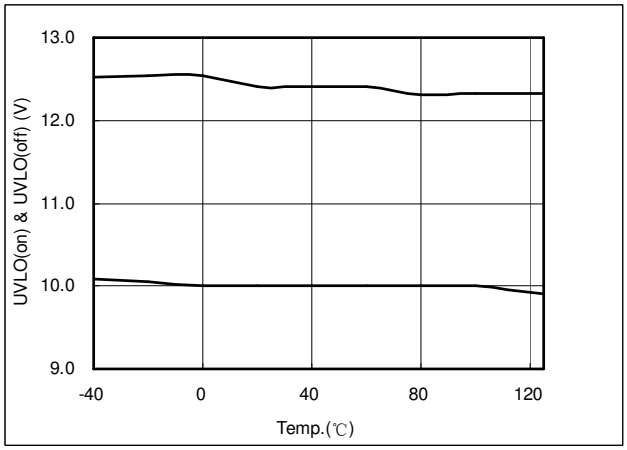


Fig. 2

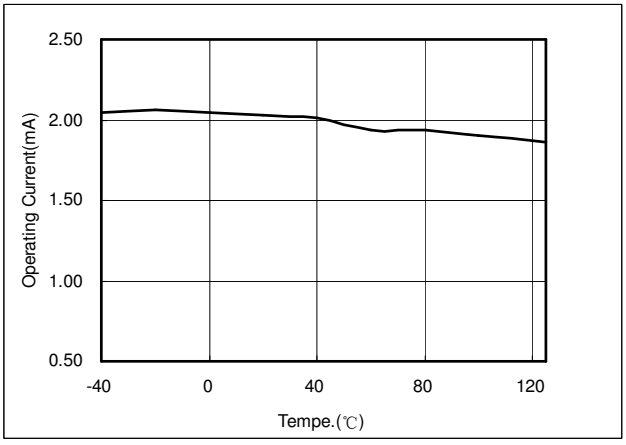


Fig. 3

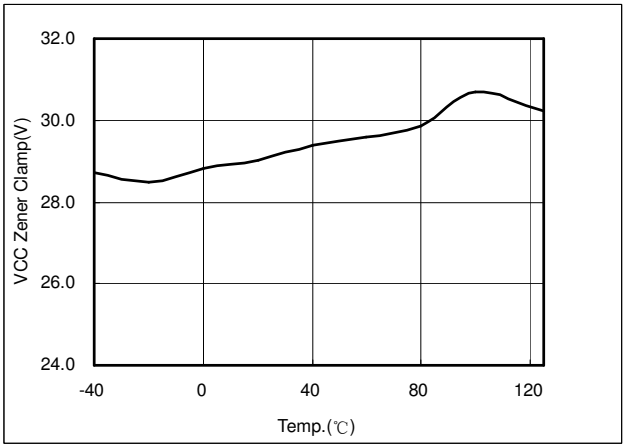


Fig. 4

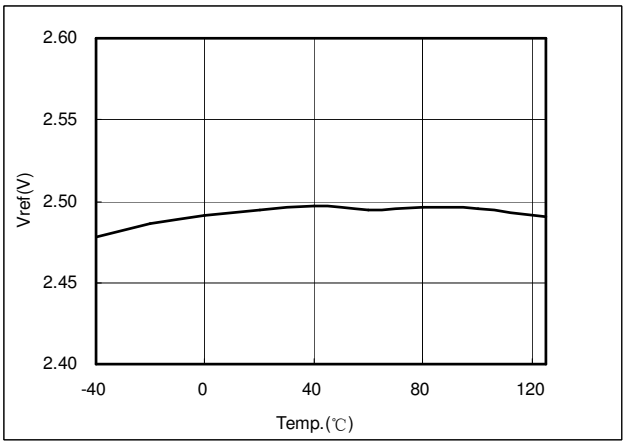


Fig. 5

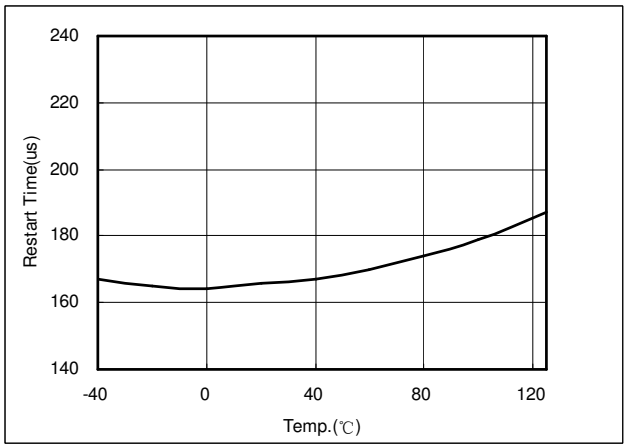


Fig. 6

Typical Performance Characteristics (Cont.)

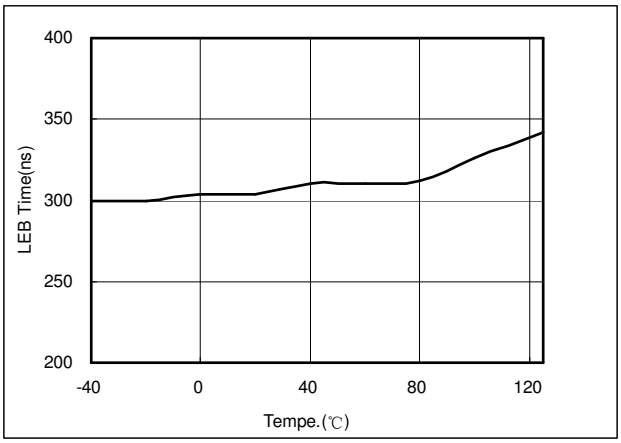


Fig. 7

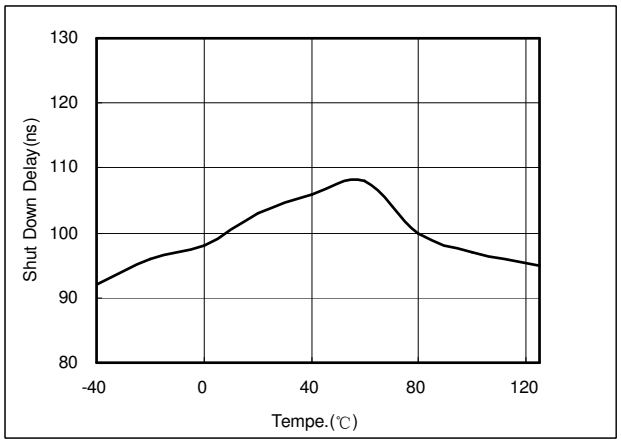


Fig. 8

Application Information

Overview

The GR8762 contains an one quadrant multiplier with a wide linear operating range, a voltage amplifier used in a feedback loop, an overvoltage regulator, a current sense comparator, a zero current detector, a PWM and logic circuit, a totem pole MOSFET driver, an internal voltage reference, a restart timer and under voltage lockout circuit.

Multiplier

The one quadrant multiplier has two inputs M1 and M2. The input M1 (MUL Pin) provides the information of the waveform of the input voltage. Its range is from 0 to 3.5V being referenced to ground. The input M2 (COMP Pin) is the voltage amplifier output, which provides the information of the DC output voltage. Both inputs are designed to achieve good linearity over a wide dynamic range to represent an AC line free from distortion.

Voltage Error Amplifier

With an external capacitor between the pins VSEN and COMP the voltage error amplifier forms an integrator. The integrator monitors the average output voltage over several line cycles. Typically the integrator's bandwidth is set below 20Hz in order to suppress the 100Hz ripple of the rectified line voltage. The non-inverting input is biased internally at 2.5V. The output is directly connected to the multiplier input.

The gate drive is disabled when VSEN voltage is less than 0.18V or COMP voltage is less than 2.2V.

Overvoltage Regulator

Because of the integrator's low bandwidth fast changes of the output voltage can't be regulated within an adequate time. Fast output changes occur during initial start-up, sudden load removal. While the integrator's differential input voltage remains zero.

During this fast changes, a peak current is flowing through the external capacitor into pin COMP. If this current exceeds an internal defined margin the overvoltage regulator circuit reduces the multiplier output voltage. As a result the on time of the MOSFET is reduced.

Current Sense Comparator

An external sense resistor transfers the source current of the MOSFET into a sense voltage. The multiplier output is compared with this sense voltage. The switch-on peak current of the MOSFET is blanked out via a leading edge blanking circuit with a blanking time of typically 300nS.

Zero Current Detector

The zero current detector senses the inductor current via an auxiliary winding and ensures that the next on-time of the MOSFET is initiated immediately when the inductor current has reached zero. This diminishes the reverse recovery losses of the boost converter diode. The MOSFET is switched off when the voltage drop of the sense resistor reaches the voltage level of the multiplier output. So the boost current waveform has a triangular shape and there are no dead-time gaps between the cycles. This leads to a continuous AC line current limiting the

peak current to twice of the average current.

To prevent false tripping, the zero current detector is designed as a Schmitt-Trigger with a hysteresis of 0.5V. An internal 5.7V clamp protects the input from overvoltage breakdown. An external resistor has to be used in series with the auxiliary winding to limit the current through the clamps.

Restart Timer

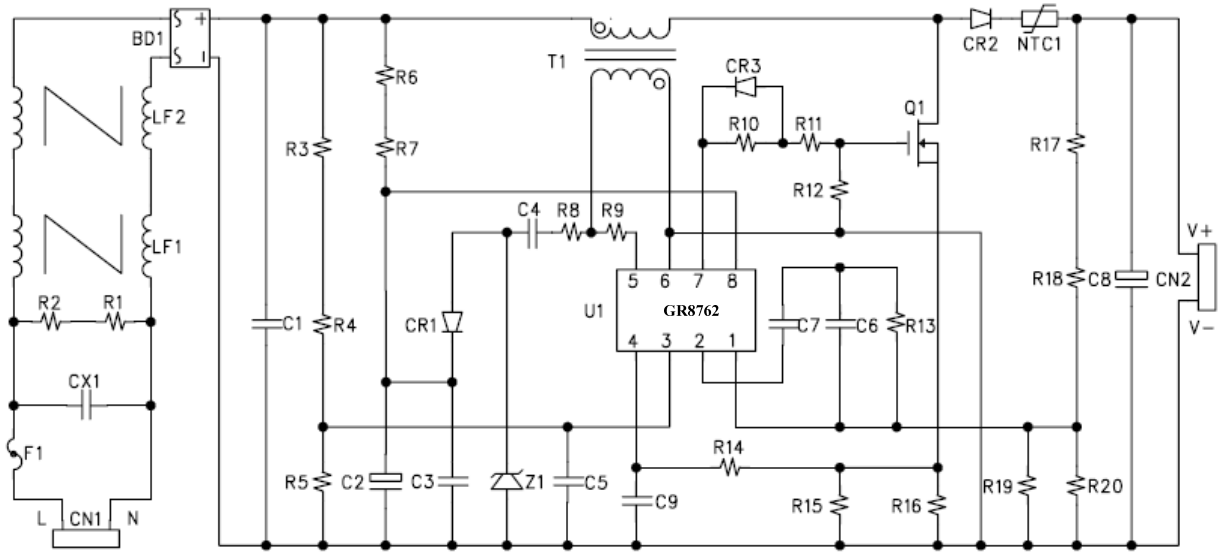
The restart timer function eliminates the need of a oscillator. The timer starts or restarts the GR8762 when the drive output has been off for more than 130us after the inductor current reaches zero.

Under-Voltage Lockout

An under voltage lockout circuit switches the IC on when VCC reaches the UVLO(ON) threshold and switches the IC off when VCC is falling below the UVLO(OFF) threshold. During start up the supply current is less than 40uA. An internal voltage clamp has been added to protect the IC from VCC overvoltage.

Typical Application Circuit

Pre-regulator Application



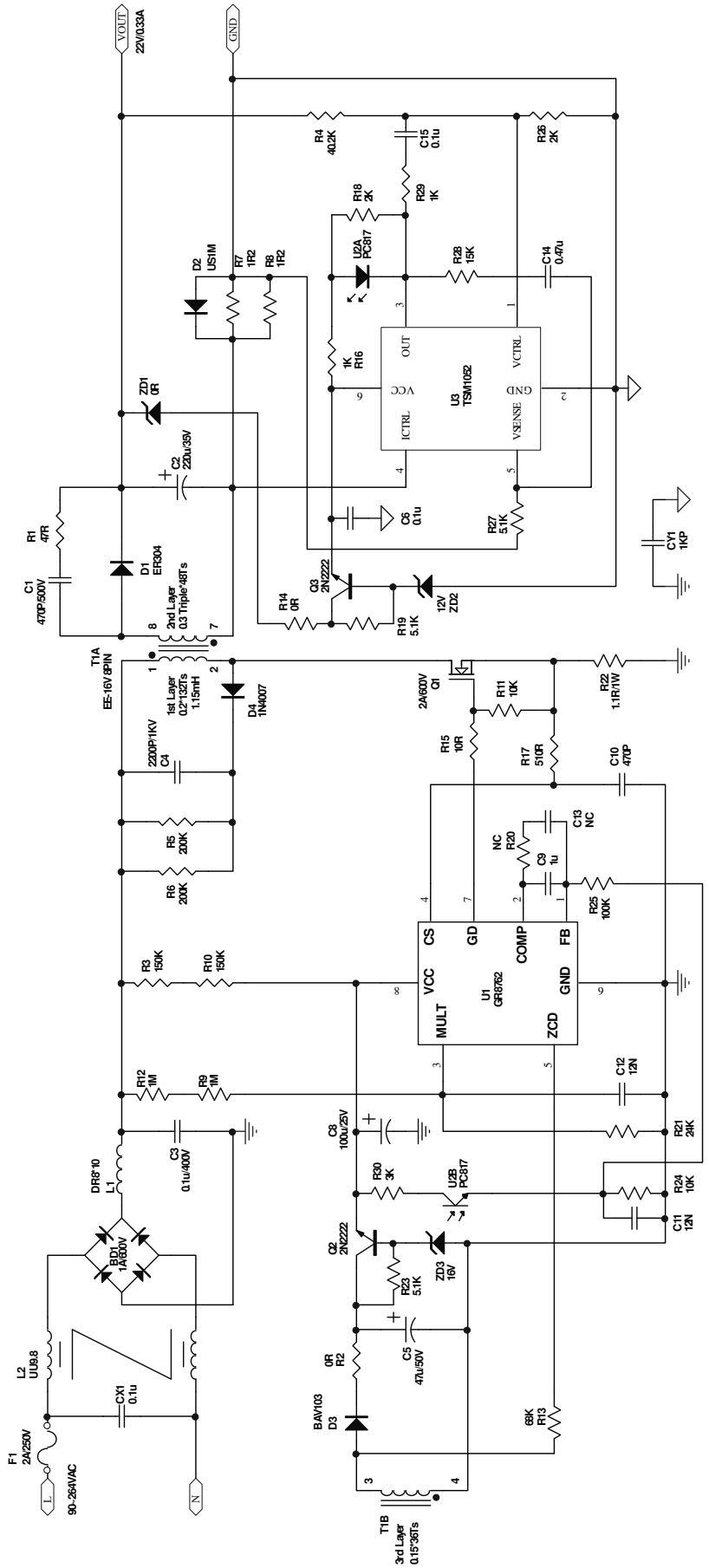
BOM List

No.	Part	Description	Q'ty.
1	BD1	PBL405 4A 600V	1
2	CN1, CN2	2/3 pin 3.96 180°,white	1
3	C1	474K 400V Pitch=15mm	1
4	C2	47uF 35V 6*12mm 105℃	1
5	C3	0805 104K 50V X7R	1
6	C4	103K 100V X7R	1
7	C5, C6	0805 103K 50V X7R	2
8	C7	0805 225K 50V X7R	1
9	C8	47uF/450V 22*26(max) 105℃	1
10	C9	NC	1
11	CX1	474K/275V	1
12	CR1	FR104 1A 400V	1
13	CR2	ER506 5A/800V DO-201	1
14	CR3	LL4148 DO-80	1
15	F1	4*8mm T3.15A/250V, fuse	1
16	HS1	15*10.5*25mm heat sink, Aluminum	1
17	LF1	T12*10*8c 0.7mH	1
18	LF2	T16*12*8c 15mH	1
19	NTC1	SCK2R55A	1
20	Q1	2SK2842 12A/500V TO-220	1
21	R1, R2, R3, R4	1206 1M 5%	4
22	R5	20K 0805 5%	1
23	R6, R7	1206 240K 5%	2
24	R8	100R 1206 5%	1
25	R9	39K 1206 5%	1
26	R10	33R 1206 5%	1
27	R11	0R 1206 5%	1
28	R12	100K 0805 5%	1
29	R13	4.7K 0805 5%	1
30	R14	0R 0805 5%	1
31	R15	0.27R 2WS 5%	1
32	R16	NC	0

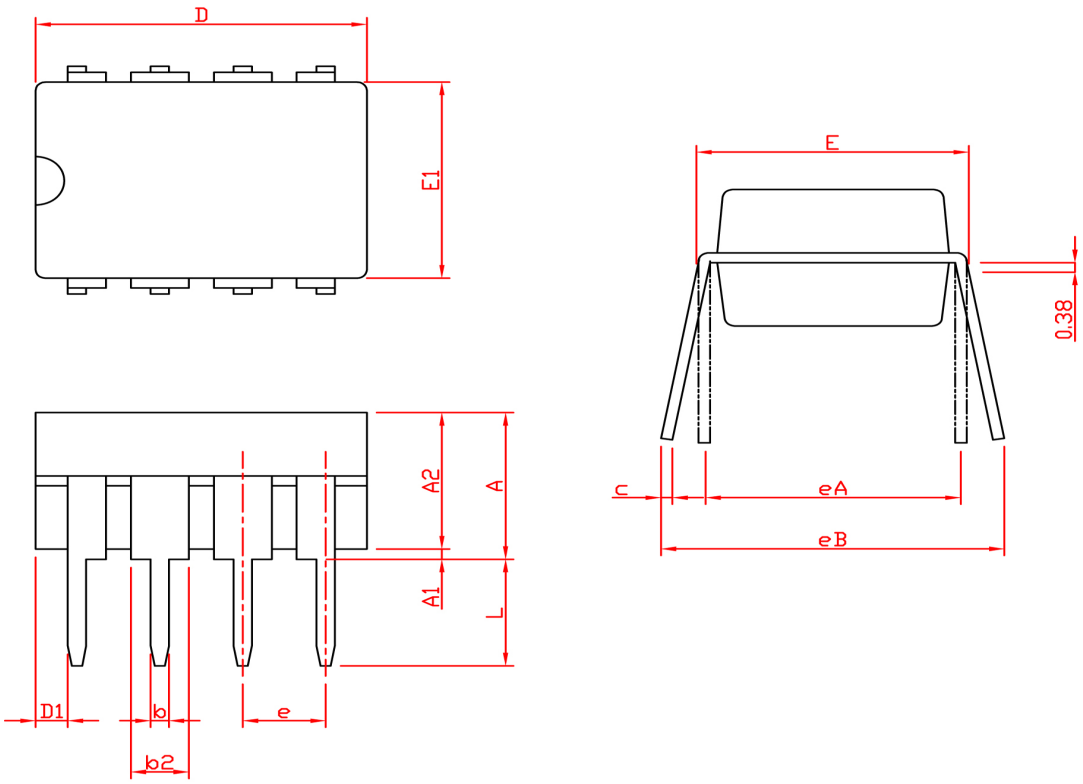
BOM List (Cont.)

No.	Part	Description	Q'ty.
33	R17, R18	330K 1206 1%	2
34	R19	4.3K 0805 1%	1
35	R20	91K 0805 1%	1
36	T1	PQ2620 0.7mH	1
37	U1	SOP-8 GR8762	1
38	Z1	18V 1W	1
39	PCB	CEM-1 2oz 1mm 110*56mm	1

LED Lighting Application



Package Information

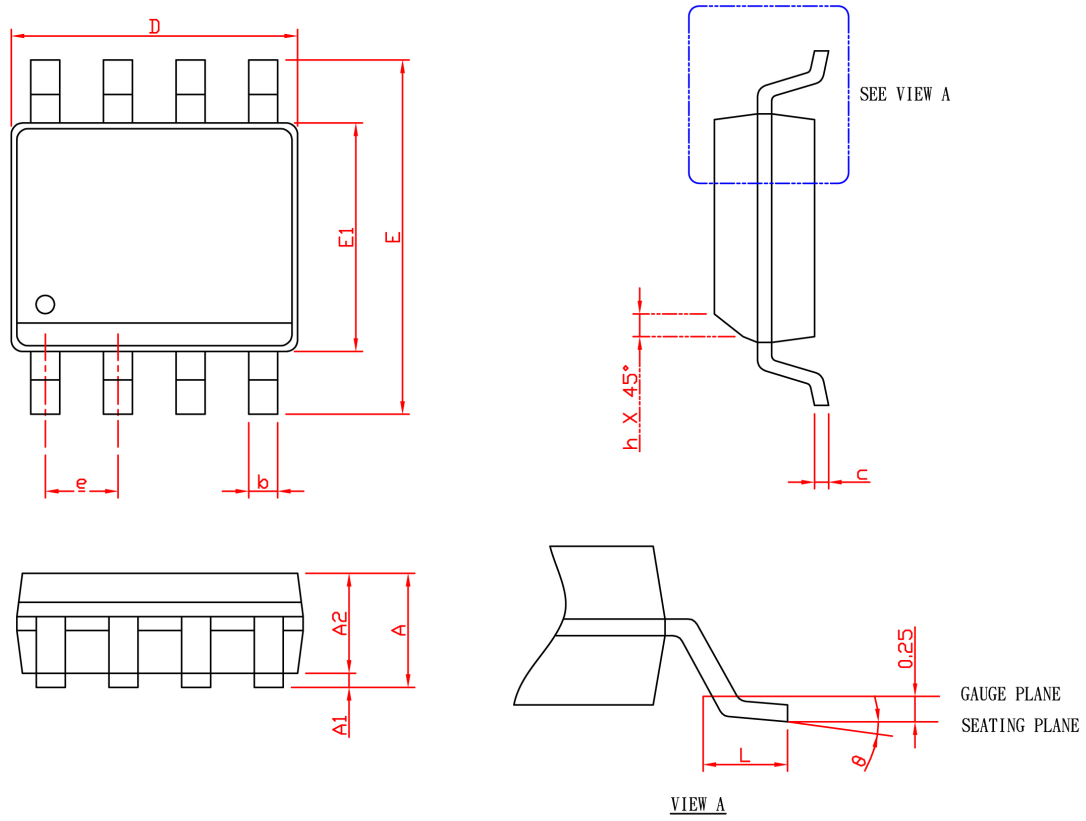


SYMBOL	DIP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
c	0.20	0.35	0.008	0.014
D	9.01	10.16	0.355	0.400
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
L	2.92	3.81	0.115	0.150

Note: 1. Followed from JEDEC MS-001 BA.

2. Dimension D, D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 10 mil.

Package Information



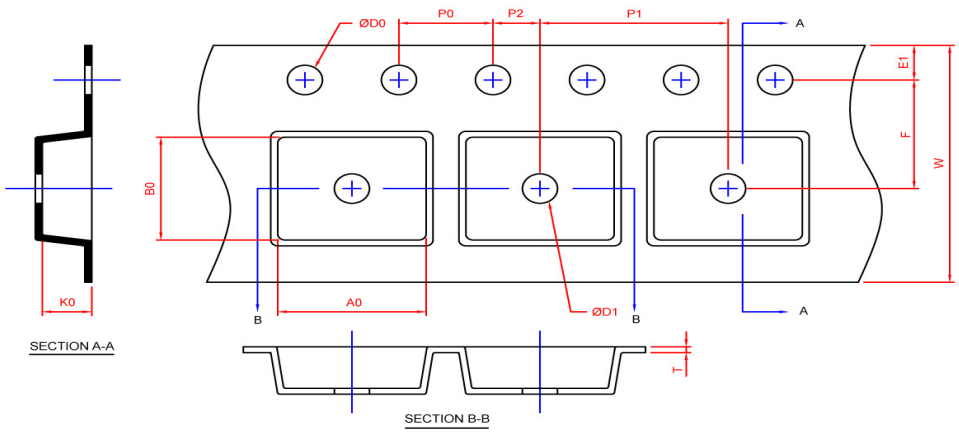
SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

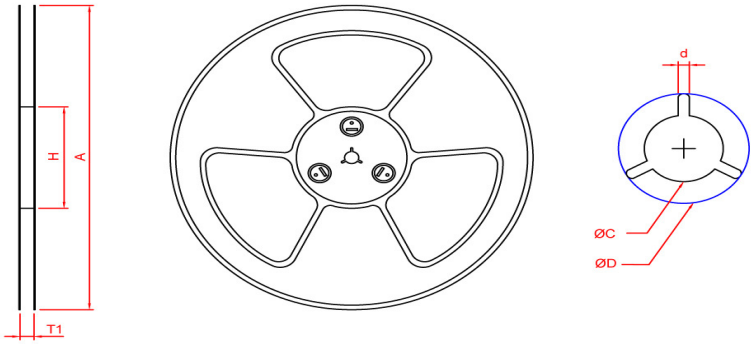
Note: 1. Followed from JEDEC MS-012 AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension “E1” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.0	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

(mm)

Devices Per Unit

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8	12	-	2500

Taping Direction Information

SOP-8