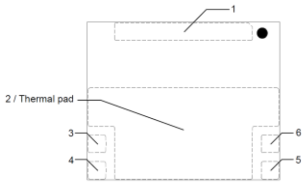
GS-065-060-5-B-A
Automotive 650 V GaN E-mode transistor
Datasheet

Features

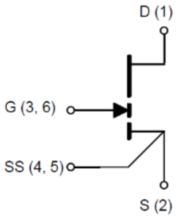
- AEC-Q101 and AutoQual+™ *(Enhanced-AEC-Q101)*
- 650 V enhancement mode power transistor
- Bottom-cooled, low inductance GaN*PX*® package
- $R_{DS(on)}$ = 25 mΩ
- $I_{DS(max)}$ = 60 A
- Ultra-low FOM
- Simple gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 / +10 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Reverse conduction capability
- Zero reverse recovery loss
- Small 11 x 9 mm^2 PCB footprint
- Dual gate pads for optimal board layout
- RoHS 3 (6+4) compliant

Package Outline

top view



Circuit Symbol



The thermal pad is internally connected to Source (pad 2) and substrate

Applications

- On Board Chargers
- Traction Drive
- DC-DC Converters
- Industrial Motor Drives
- Solar Inverters
- Bridgeless Totem Pole PFC

Description

The GS-065-060-5-B-A is an Automotive-grade 650 V enhancement mode GaN-on-Silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. GaN Systems innovates with industry leading advancements such as patented **Island Technology®** and **GaN*PX*®** packaging. **Island Technology®** cell layout realizes high-current die and high yield. **GaN*PX*®** packaging enables low inductance & low thermal resistance in a small package. The GS-065-060-5-B-A is a bottom-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Transient Drain-to-Source Voltage (Note 1)	$V_{DS(transient)}$	900	V
Gate-to-Source Voltage	V_{GS}	-10 to + 7	V
Gate-to-Source Voltage - transient (Note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case}= 25 °C)	I_{DS}	60	A
Continuous Drain Current (T_{case}= 100 °C)	I_{DS}	41	A
Pulse Drain Current (Pulse width 10 µs, V_{GS} = 6 V) (Note 2)	$I_{DS\ Pulse}$	120	A

(1) For ≤1 µs
(2) Defined by product design and characterization. Value is not tested to full current in production.

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	0.35	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

Ordering Information

Ordering code	Package type	Packing method	Qty	Reel Diameter	Reel Width
GS-065-060-5-B-A-TR	GaN*PX*® Bottom-Side Cooled	Tape-and-Reel	2000	13" (330 mm)	24mm
GS-065-060-5-B-A-MR	GaN*PX*® Bottom-Side Cooled	Mini-Reel	250	7" (180 mm)	24mm

Electrical Characteristics (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$V_{(BL)DSS}$	650			V	V_{GS} = 0 V, I_{DSS} ≤ 120 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		25	32	mΩ	V_{GS} = 6 V, T_J = 25 °C I_{DS} = 18 A
Drain-to-Source On Resistance	$R_{DS(on)}$		65		mΩ	V_{GS} = 6 V, T_J = 150 °C I_{DS} = 18 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	V_{DS} = V_{GS}, I_{DS} = 16.4 mA
Gate-to-Source Current	I_{GS}		320		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3		V	V_{DS} = 400 V, I_{DS} = 60 A
Drain-to-Source Leakage Current	I_{DSS}		4	120	µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		160		µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 150 °C
Internal Gate Resistance	R_G		1		Ω	f = 5 MHz, open drain
Input Capacitance	C_{ISS}		516		pF	V_{DS} = 400 V V_{GS} = 0 V f = 100 kHz
Output Capacitance	C_{OSS}		127		pF	
Reverse Transfer Capacitance	C_{RSS}		2.4		pF	
Effective Output Capacitance Energy Related (Note 3)	$C_{O(ER)}$		212		pF	V_{GS} = 0 V V_{DS} = 0 to 400 V
Effective Output Capacitance Time Related (Note 4)	$C_{O(TR)}$		338		pF	
Total Gate Charge	Q_G		14		nC	V_{GS} = 0 to 6 V V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		3.8		nC	
Gate-to-Drain Charge	Q_{GD}		4.1		nC	
Output Charge	Q_{OSS}		135		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	

(3) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

(4) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

Electrical Characteristics cont'd (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Turn-On Delay	$t_{D(on)}$		8.1		ns	V_{DD} = 400 V, V_{GS} = +6 V/-3 V I_{DS} = 20 A, $R_{G(on)}$ = 10 Ω, $R_{G(off)}$ = 2 Ω, L = 65 µH, L_P = 4 nH (Notes 5,6,7)
Rise Time	t_R		8.5		ns	
Turn-Off Delay	$t_{D(off)}$		9.8		ns	
Fall Time	t_F		7.7		ns	
Switching Energy during turn-on	E_{on}		117		µJ	
Switching Energy during turn-off	E_{off}		17.2		µJ	
Output Capacitance Stored Energy	E_{OSS}		17		µJ	V_{DS} = 400 V V_{GS} = 0 V, f = 100 kHz

(5) See Figure 16 for switching test circuit diagram.

(6) See Figure 17 for switching time definition waveforms.

(7) L_P = parasitic inductance.

Electrical Performance Graphs

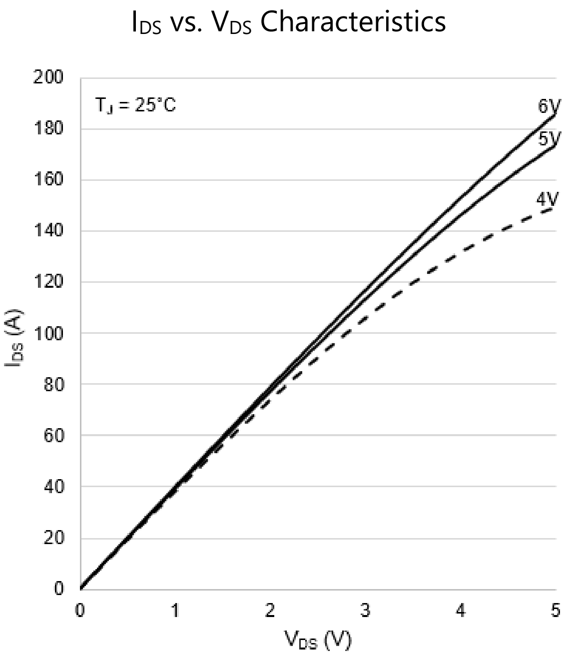


Figure 1: Typical I_{DS} vs. V_{DS} @ T_J = 25 ^{0}C

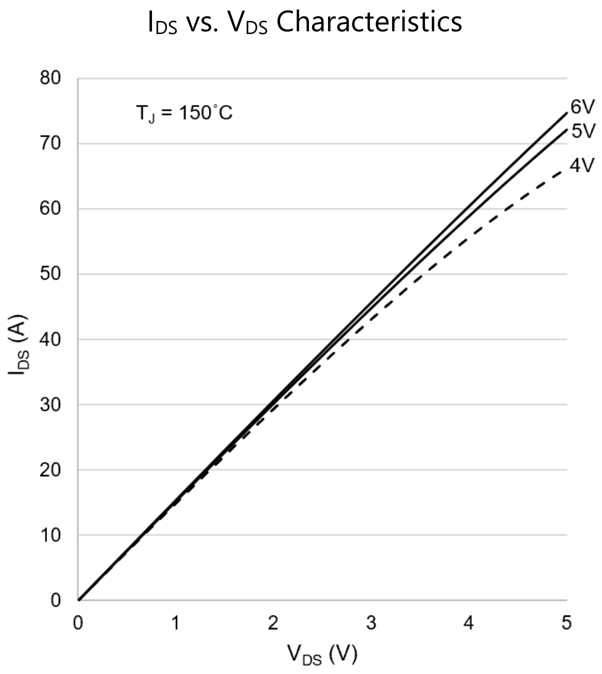


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 ^{0}C

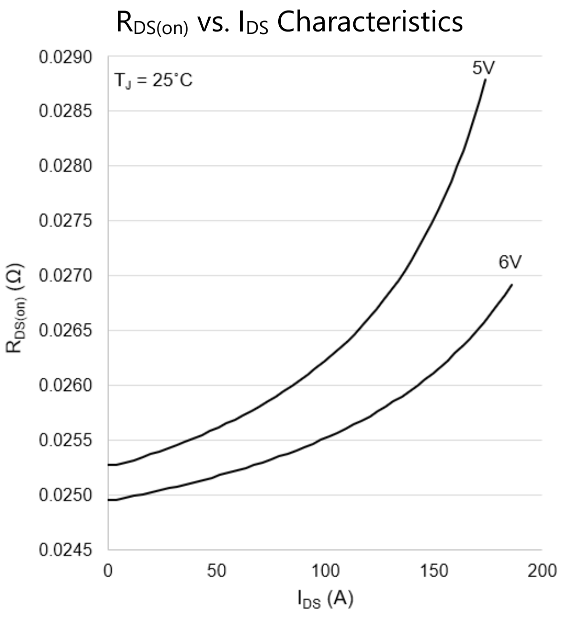


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 ^{0}C

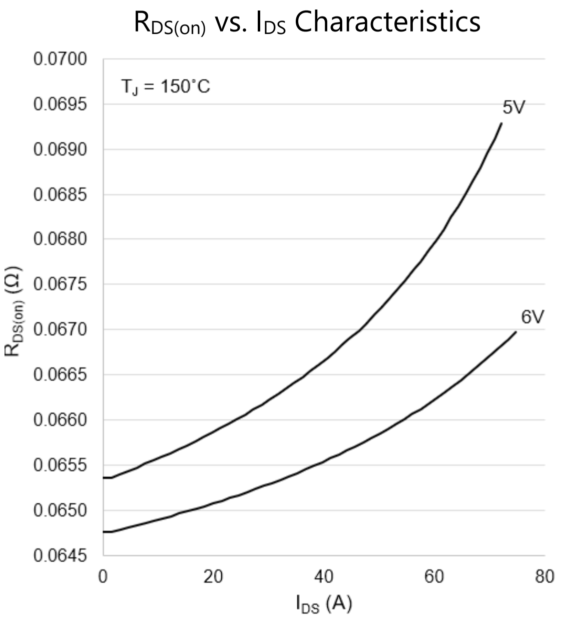


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150 ^{0}C

Electrical Performance Graphs

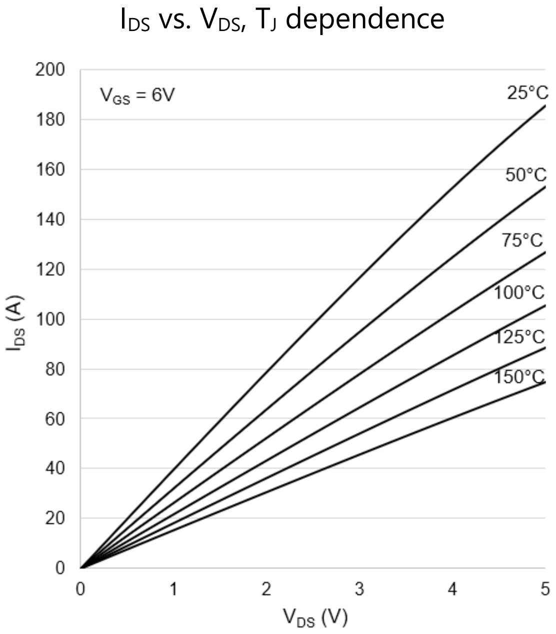


Figure 5: Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

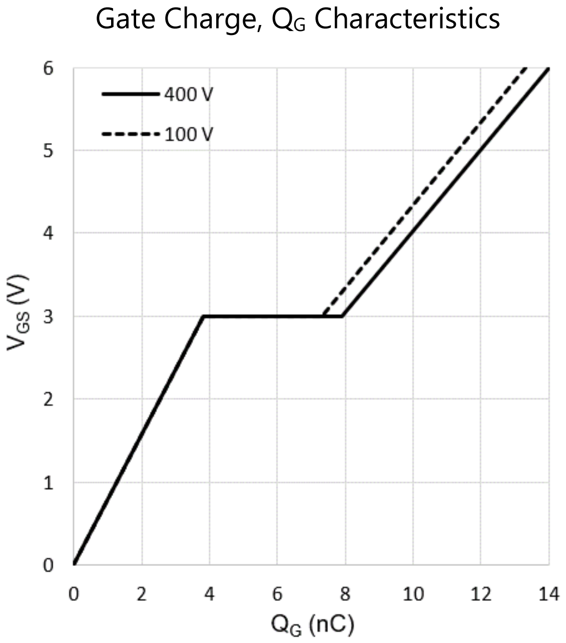


Figure 6: Typical V_{GS} vs. Q_G @ V_{DS}=100, 400V

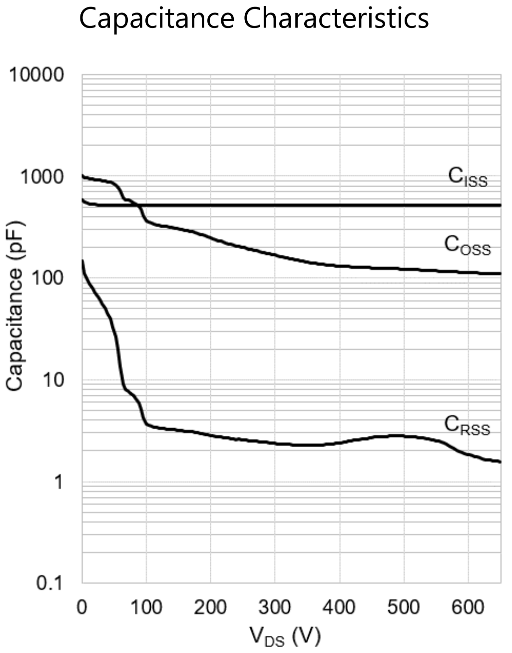


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

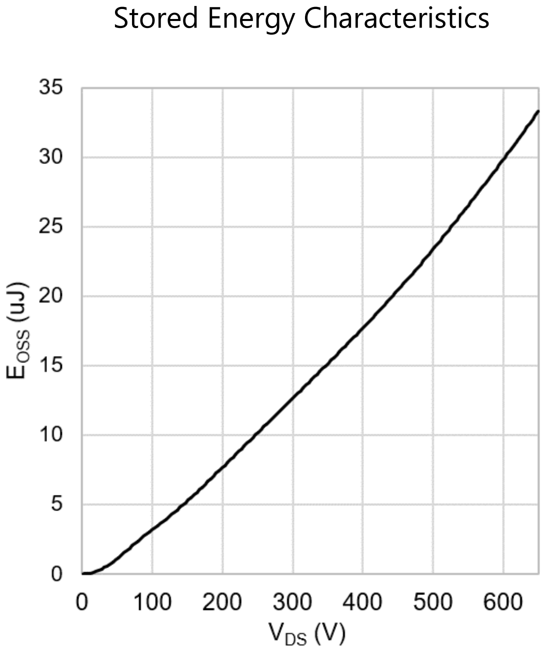


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

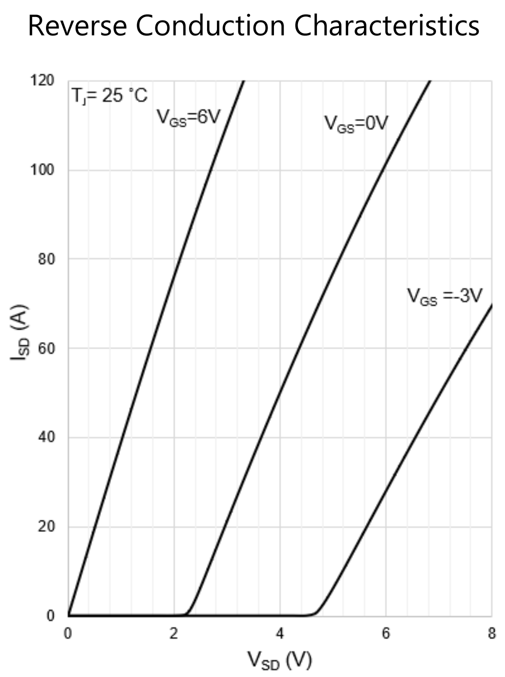


Figure 9: Typical I_{SD} vs. V_{SD} @ T_J = 25 °C

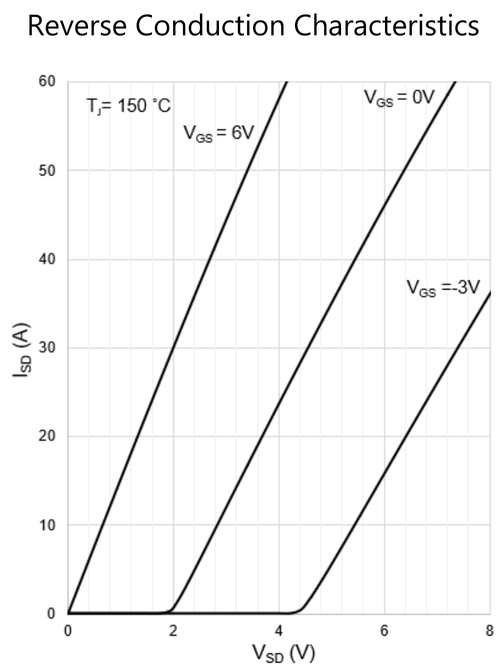


Figure 10: Typical I_{SD} vs. V_{SD} @ T_J = 150 °C

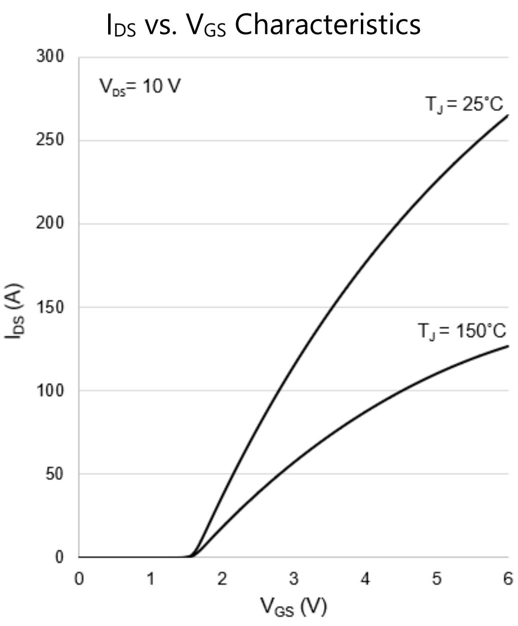


Figure 11: Typical I_{DS} vs. V_{GS}

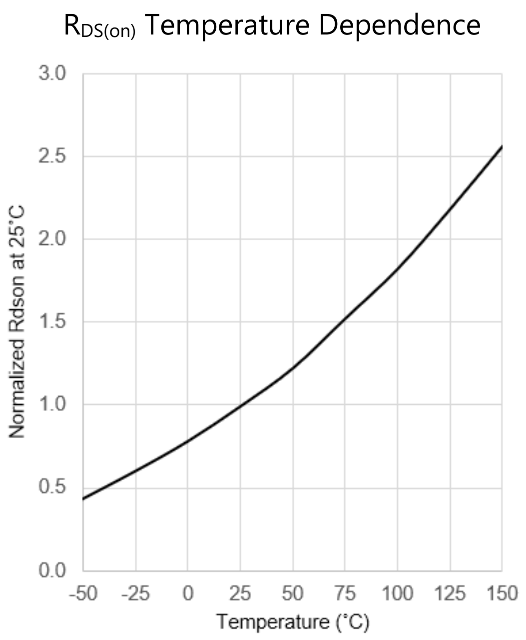


Figure12: Normalized $R_{DS(on)}$ as function of T_J

Thermal Performance Graphs

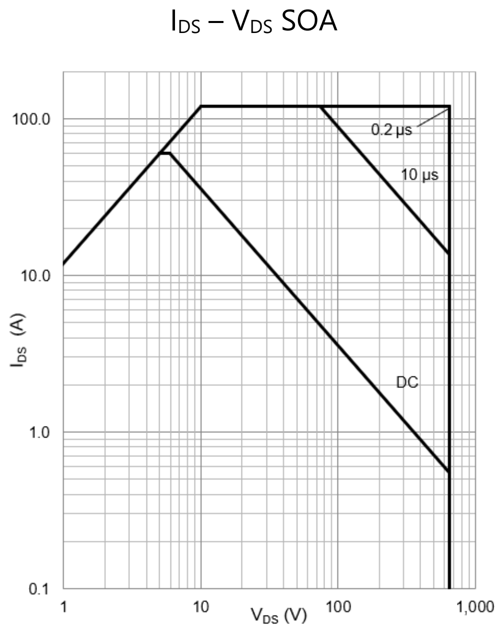


Figure 13: Safe Operating Area @ T_{case}=25°C

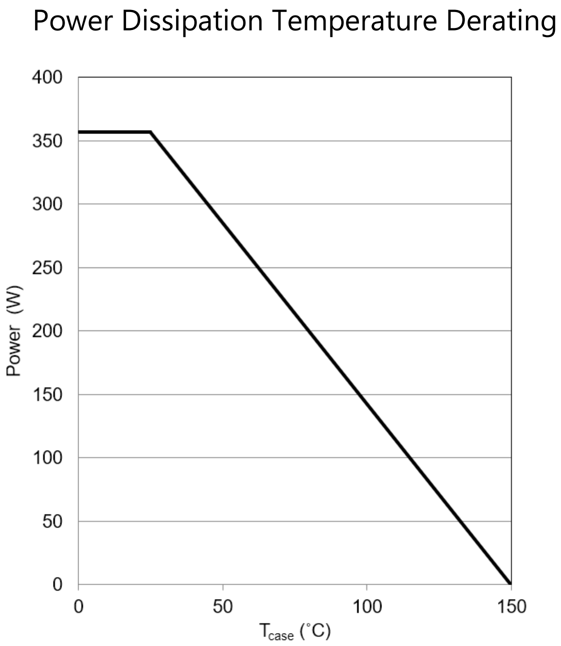


Figure 14: Power Derating vs. T_{case}

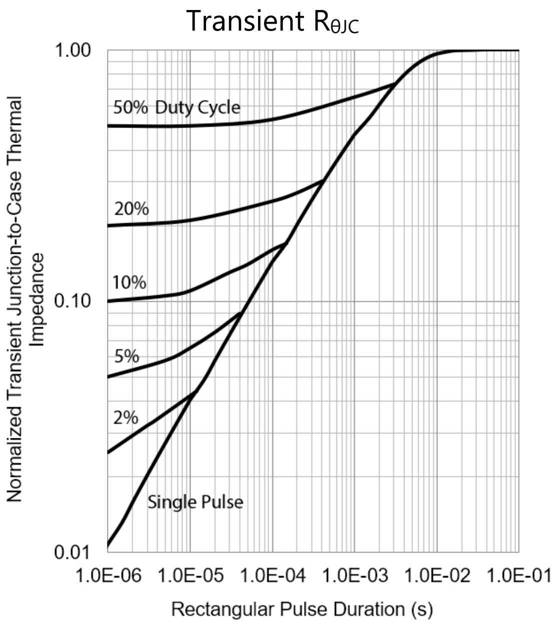


Figure 15: Transient Thermal Impedance
(1.00 = Nominal DC thermal impedance)

Test Circuits

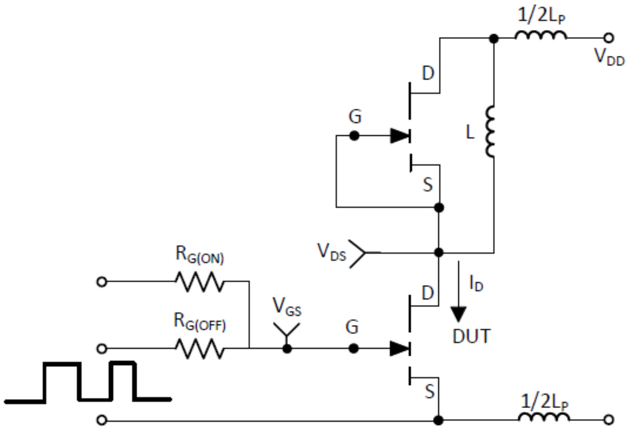


Figure 16: Switching Test Circuit

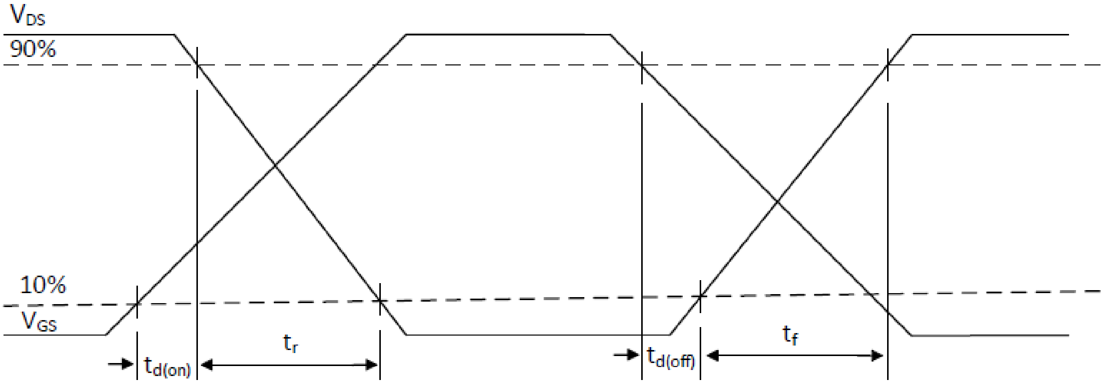


Figure 17: Switching Time Waveforms

Application Information

For more information, please refer to the application note entitled: "An Introduction to GaN Enhancement Mode HEMTs" at www.gansystems.com

Gate Drive

The recommended gate drive voltage range, V_{GS}, is 0 V to + 6 V for optimal $R_{DS(on)}$ performance. Also, the repetitive gate to source voltage, maximum rating, $V_{GS(AC)}$, is +7 V to -10 V. The gate can survive non-repetitive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias, typically V_{GS} = -3 V, ensures safe operation against the voltage spike on the gate, however it may increase reverse conduction losses if not driven properly. For more details, please refer to the gate driver application note "Gate Driver Circuit Design with GaN E-HEMTs" at www.gansystems.com

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note for more details.

A standard MOSFET driver can be used provided that it supports 6 V for gate drive and the UVLO is suitable for 6 V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Some non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive may not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Please see the gate driver application note for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

The dual gate drive pins are used to achieve balanced gate drive, especially useful in parallel GaN transistors operation. Both gate drive pins are internally connected to the gate, so only one needs to be connected. Connecting both may lead to timing improvements at very high frequencies. The two gates on the GS-065-060-5-B-A bottom-side cooled device are not designed to be used as a signal pass-through. When multiple devices are used in parallel, it is not recommended to use one gate connection to the other (on the same transistor) as a signal path for the gate drive to the next device. Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

Source Sensing

The package has two dedicated source sense pins. The GaNPX® packaging utilizes no wire bonds so the source connection is very low inductance. The dedicated source sense pins will further enhance performance by eliminating the common source inductance if a dedicated gate drive signal kelvin connection is created. This can be achieved connecting the gate drive signal from the driver to the gate pad and returning from the source sense pad to the driver ground reference.

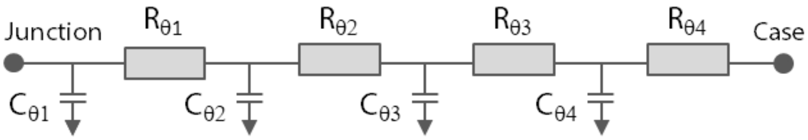
Thermal

The substrate is internally connected to the source/thermal pad on the bottom-side of the package. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under this pad will improve thermal performance by reducing the package temperature.

Thermal Modeling

RC thermal models are available to support detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This thermal model can be extended to the system level by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

RC thermal model:



RC breakdown of $R_{\Theta JC}$

R_θ (°C/W)	C_θ (W·s/°C)
$R_{\theta 1}$ = 0.008	$C_{\theta 1}$ = 1.8E-04
$R_{\theta 2}$ = 0.080	$C_{\theta 2}$ = 1.3E-03
$R_{\theta 3}$ = 0.222	$C_{\theta 3}$ = 9.5E-03
$R_{\theta 4}$ = 0.040	$C_{\theta 4}$ = 3.7E-03

For more detail, please refer to Application Note entitled “Modeling Thermal Behavior of GaN Systems’ GaN*PX*® Using RC Thermal SPICE Models” available at www.gansystems.com

Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.

Off-state condition ($V_{GS} \leq 0$ V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, V_{GD}, exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}+V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $V_{(BL)DSS}$, is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated $V_{(BL)DSS}$. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and does not change with negative gate voltage. GaN Systems tests devices in production with a 900 V Drain-to-source voltage pulse to insure blocking voltage margin.

Packaging and Soldering

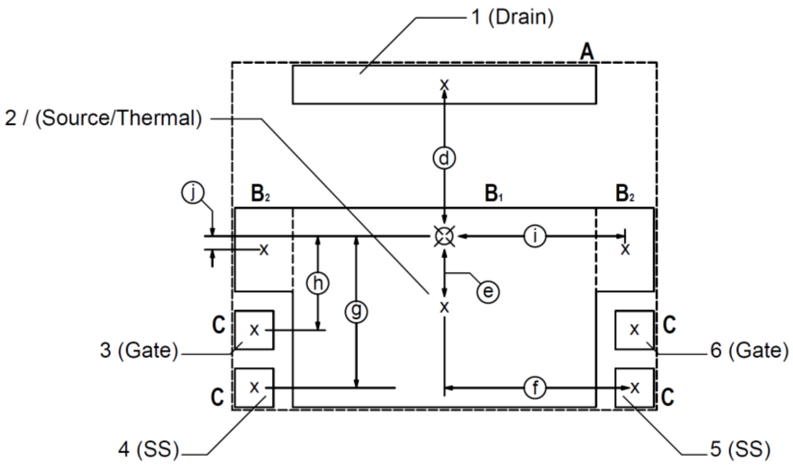
The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the GS-065-060-5-B-A device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

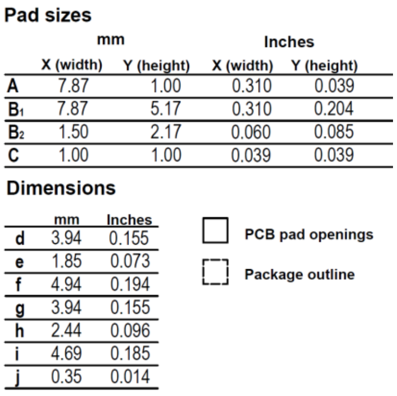
It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)
The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60-120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3°C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using “No-Clean” soldering paste and operating at high temperatures may cause a reactivation of the “No-Clean” flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the “No-Clean” paste residues. Avoid placing printed circuit board traces with high differential voltage to the source or drain directly underneath the bottom-cooled GS-065-060-5-B-A package on the PCB to avoid potential electro-migration and solder mask isolation issues during high temperature or/and voltage operation.

Recommended PCB Footprint





Pad sizes

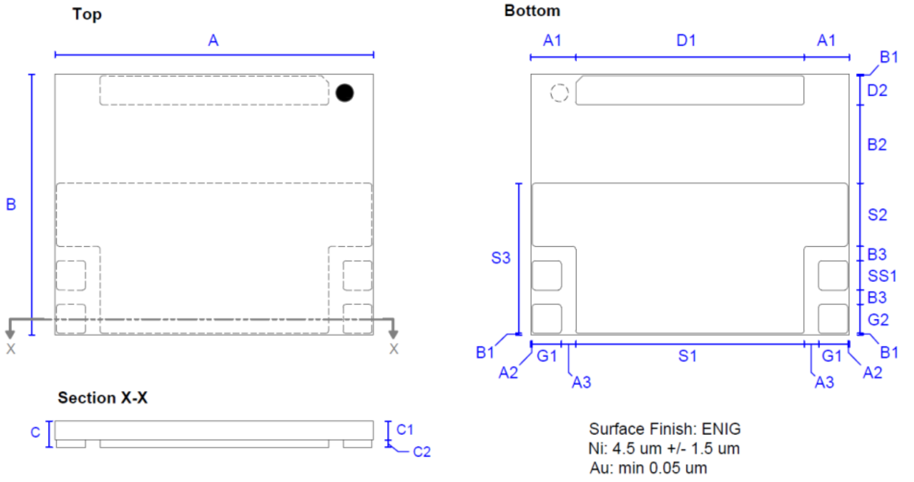
	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	7.87	1.00	0.310	0.039
B_1	7.87	5.17	0.310	0.204
B_2	1.50	2.17	0.060	0.085
C	1.00	1.00	0.039	0.039

Dimensions

	mm	Inches
d	3.94	0.155
e	1.85	0.073
f	4.94	0.194
g	3.94	0.155
h	2.44	0.096
i	4.69	0.185
j	0.35	0.014

☐ PCB pad openings
⬚ Package outline

Package Dimensions

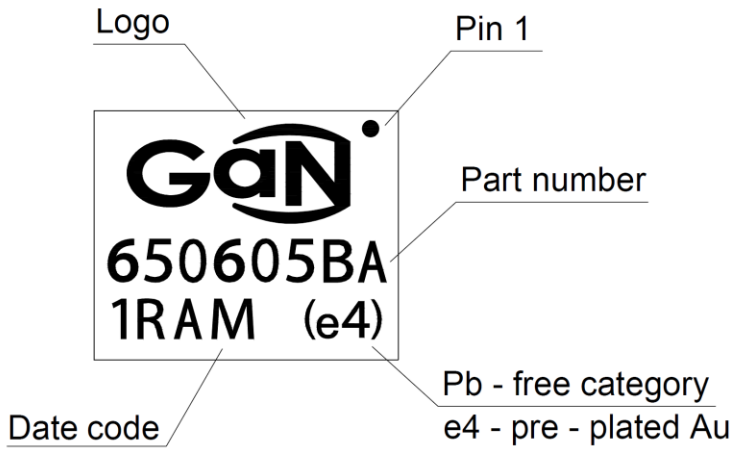


Surface Finish: ENIG
Ni: 4.5 um +/- 1.5 um
Au: min 0.05 um

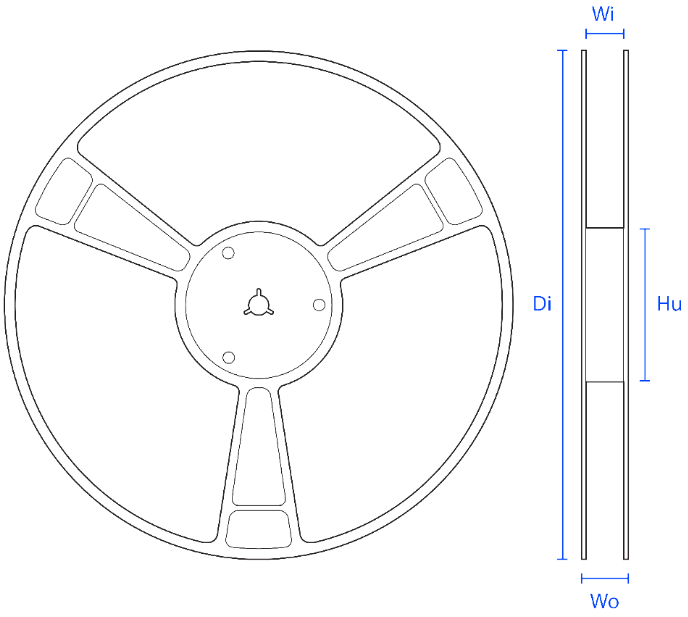
	mm	Inches*	
A	11.02	0.434	+/- 0.100 mm (0.004")
A1	1.58	0.062	+/- 0.050 mm (0.002")
A2	0.08	0.003	+/- 0.050 mm (0.002")
A3	0.50	0.020	
B	9.02	0.355	+/- 0.100 mm (0.004")
B1	0.08	0.003	+/- 0.050 mm (0.002")
B2	2.70	0.106	
B3	0.50	0.020	
C	0.63	0.025	+/- 0.09 mm (0.004")
C1	0.62	0.024	
C2	0.01	0.0004	
D1	7.87	0.310	
D2	1.00	0.039	
G1	1.00	0.039	
G2	1.00	0.039	
S1	7.87	0.310	
S2	2.17	0.085	
S3	5.17	0.204	
SS1	1.00	0.039	

*Inch measurements are approximate values

Part Marking

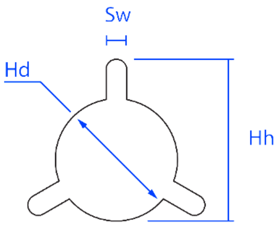


Tape and Reel Information

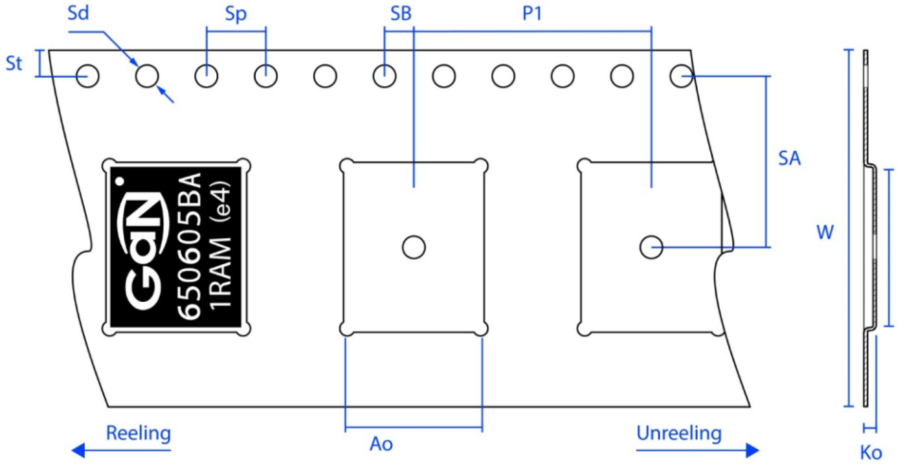


Dimensions (mm)

13 inch reel			7 inch reel		
	Min	Max		Min	Max
Di	328.5	331.5	**Di**	178.0	180.0
Wo		30.4	**Wo**	26.4	28.7
Wi	24.4	26.4	**Wi**	25.0	26.0
Hu	98.5	104.0	**Hu**	60.0	61.0
Hh	16.45	17.4	**Hh**	16.5	17.5
Sw	1.5	2.5	**Sw**	1.5	2.5
Hd	12.8	13.5	**Hd**	12.8	13.2



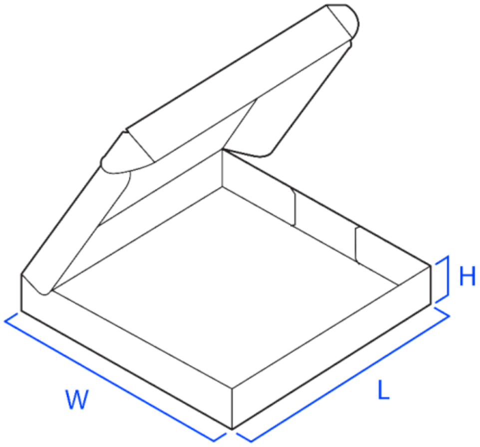
Note: Wo and Wi measured at hub



Dimensions (mm)

	Nominal	Tolerance
P1	16.00	+/- 0.1
W	24.00	+ 0.3 / - 0.1
Ko	1.14	+/- 0.1
Ao	9.48	+/- 0.1
Bo	11.43	+/- 0.1
Sp	4.00	+/- 0.02
Sd	1.50	+ 0.1 / - 0.0
St	1.75	+/- 0.1
SA	11.50	+/- 0.1
SB	2.00	+/- 0.1

Tape and Reel Box Dimensions



Outside dimensions (mm)

13 inch reel			7 inch reel		
	Min	**Max**		**Min**	**Max**
W	197.0	203.5	**W**	337.0	342.0
L	204.0	218.5	**L**		355.0
H		32.0	**H**	50.0	53.0

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