GENDA TECHNOLOGY LTD

Part No. :GS-GB1286420YFYJ/R

Customer :_____

Drawing No. :_____

Approved :_____

Date :_____

Approved:_____ Checked:_____ Prepared:_____

ADDRESS: Friendship Industrial Building 71 District , Baoan Shenzhen, P.R.China

TEL 86-755-2786 5012 FAX 86-755-2786 5217

CONTENTS

NO	*ITEM*	*PAGE*
1	COVER	1
2	CONTENTS	2
3	PRECAUTIONS FOR LCM	3
4	OPTICAL DEFINITIONS	5
5	GENERAL SPECIFICATIONS AND MECHANICAL DATA	6
6	BLOCK DIAGRAM	8
7	CHIP DEPICTION	8

3. PRECAUTIONS FOR LCM

3.1 Precautions in handling LCD Modules (hereinafter LCMs)

Genda' s LCMs have been assembled and accurately calibrated before delivery.

Please observe the following criteria when handling.

A. Do not subject the module to excessive shock.

B. Do not modify the tab on the metal holder.

C. Do not tamper with the printed circuit board.

D. Limit the soldering of the printed circuit board to I/O terminals only.

E. Do not touch the zebra strip nor modify its location.

3.2 Static electricity warning

Genda' s LCM uses CMOS LSI technology. Therefore, strict measures to avoid static electricity discharge are followed through all processes from manufacturing to shipping. When handling a LCM, take sufficient care to prevent static electricity discharge as you would any CMOS IC.

A. Do not take the LCM from its anti-static bag until it' s to be assembled.

LCM' s are individually packaged in bags specially treated to resist static electricity. When storing, keep the LCM packed in the original bags, or store them in a container processed to be resistant to static electricity, or in an electric conductive container.

B. Always use a ground strap when handling a LCM.

Always use a ground strap while working with the module, from the time it is taken out of the anti-static bag until it is assembled. If it is necessary to transfer the LCM, once it has been taken out of the bag, always place it in an electric conductive container. Avoid wearing clothes made of chemical fibers, the use of cotton or conductive treated fiber clothing is recommended.

C. Use a no-leak iron for soldering the LCM.

The soldering iron to be used for soldering the I/O terminals to the LCM are to be insulated or grounded at the iron tip.

D. Always ground electrical apparatuses required for assembly.

Electrical apparatuses required to assemble the LCM into a product, i.e. electrical screw drivers, are to be first grounded to avoid transmitting spike noises from the motor.

E.Assure that the work bench is properly grounded.

F. Peel off the LCM protective film slowly.

The module is attached with a film to protect the display surface from contamination, damage, adhesion of flux, etc. Peeling off this film abruptly could cause static electricity to be generated, so peel the tape slowly.

G. Pay attention to the humidity in the work area.

50~60% RH is recommended.

3.3 Precautions for the soldering of a LCM

The following procedures should be followed when soldering the LCM:

A. Solder only to the I/O terminal.

B. Use a no leakage soldering iron and pay particular attention to the following:

(1) Conditions for soldering I/O terminals

Temperature at iron tip: 280

Soldering time: 3~4 sec/terminal

Type of solder: Eutectic solder (rosin flux filled)

Note: (Avoid using flux, because it could penetrate the module and the module may get contaminated during cleaning.) Peel off protective film after soldering the I/O terminals. By following this procedure, the surface contamination caused by the dispersion of flux while soldering can be avoided.

(2) Removing the wiring

(When a lead wire, or a connector to the I/O terminal of the module is to be removed, remove it only after the solder at the connection has sufficiently melted since the I/O terminal is a through hole.) If it is forcefully removed, it could cause the terminal to break or peel. The recommended procedure is to use a suction-type solder remover. Caution: do not reheat the I/O terminal more than 3 times.

3.4 Long-term storage

If the correct method of storage is not followed, deterioration of the display material (polarizer) and oxidation of the I/O terminal plating may make the process of soldering difficult. Please comply with the following procedure.

A. Store in the shipping container.

B. If the shipping container is not available, place in anti-static bags and seal the opening.

C. Store the modules where they are not subjected to direct sunlight or a fluorescent lamp.

D.Store in a temperature range of 0 35 with low relative humidity.

3.5 Precautions in use of LCD modules

A. Do not give any external shock.

B. Do not wipe the surface with hard materials.

C. Do not apply excessive force on the surface.

D. Do not expose to direct sunlight or fluorescent light for a long time.

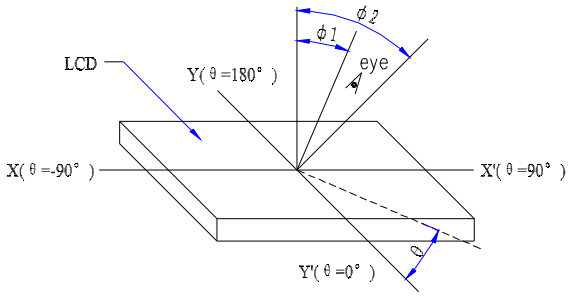
E. Avoid storage in high temperature and high humidity.

F. When storage for a long time at 40 or higher is required, R/H should be less than 60%.

G. Liquid in LCD is hazardous substance. Do not lick, swallow when the liquid is attached to your hands, skin, clothes etc. Wash it out thoroughly.

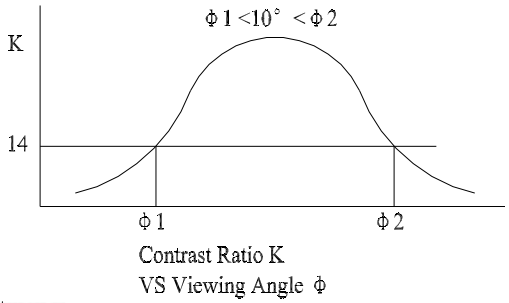
4. OPTICAL DEFINITIONS

4.1 Definition of angle and



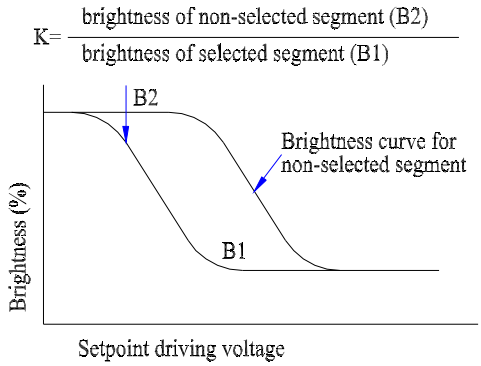
POSITIVE TYPE

4.2 Definition of viewing angle and 2



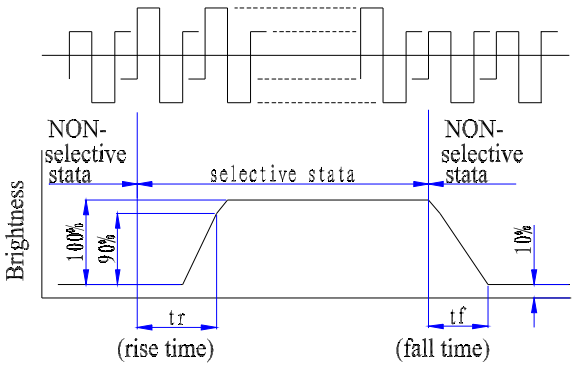
POSITIVE TYPE

4.3 Definition of contrast "K"



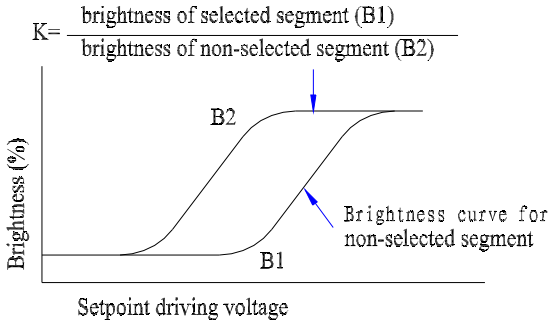
NEGATIVE TYPE

4.4 Definition of optical response

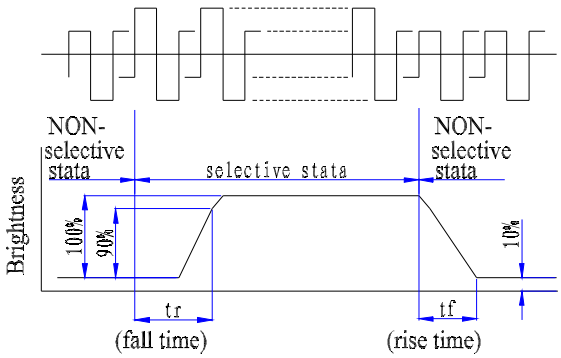


NEGATIVE TYPE

4.5 Definition of contrast "K"



4.6 Definition of optical response



5 General specifications and mechanical data

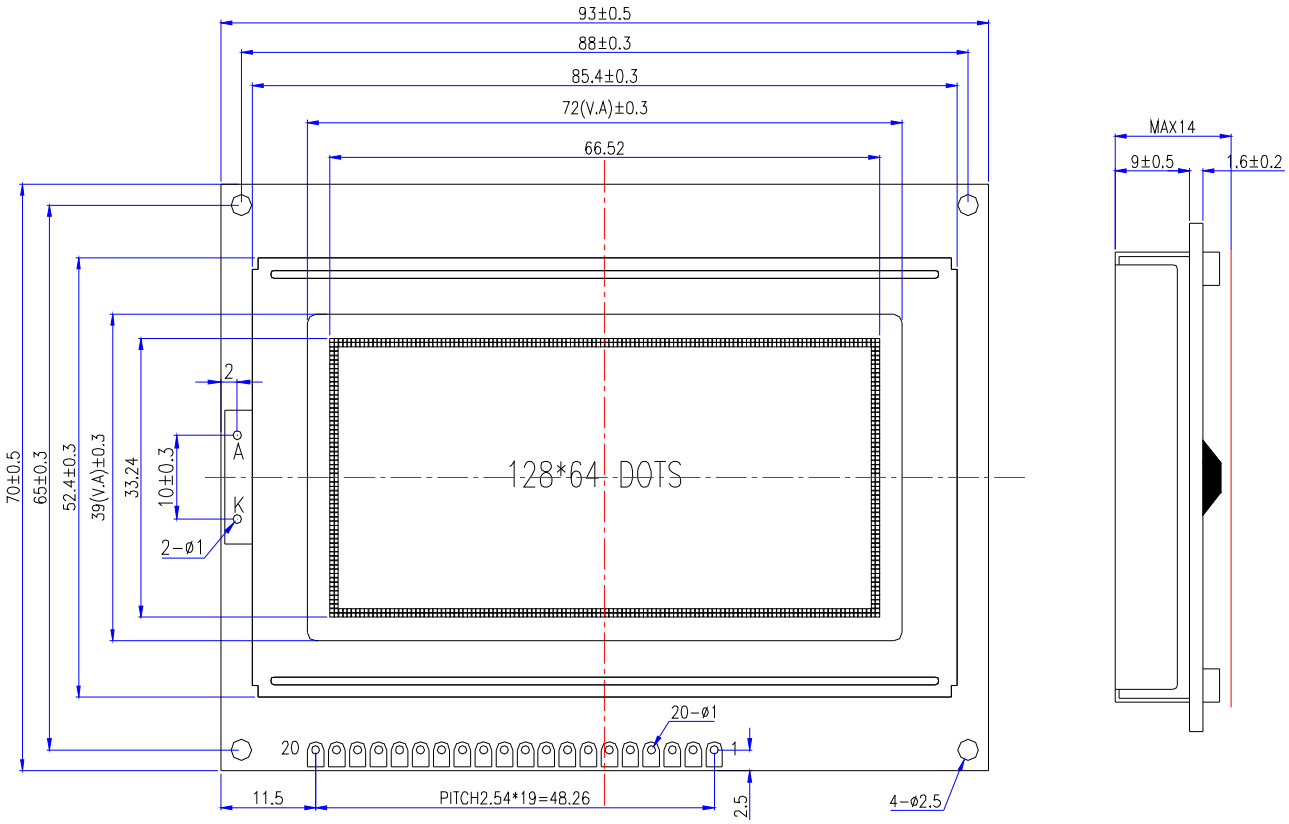
5.1 Mechanical data

ITEM	STANDARD VALUE	UNIT
NUMBER OF DOTS	128 x 64	DOTS
MODULE DIMENSION	93.0(W) x 70.0(H) x 14.0(T)	mm
EFFECTIVE DISPLAY AREA	66.52(W) x 33.24(H)	mm
DOT SIZE	0.48(W) x 0.48(H)	mm
DOT PITCH	0.52(W) x 0.52 (H)	mm
OPERATING TEMP	-20~70	
STORAGE TEMP	-30~80	
DUTY	1/64	
VIEWING DIRECTION	6 O' clock	
BACK LIGHT	LED BACKLIGHT/YELLOW-GREEN, BOTTOM	
LCD TYPE	STN, YELLOW-GREEN MODE, TRANSFLECTIVE/POSITIVE	

5.2 Electrical Characteristics

ITEM	SYM	CONDITION	MIN.	TYP.	MAX.	UNIT
Power supply voltage for circuit	VDD-VSS	——	4.5	5.0	5.5	V
Power supply current for LCM	IDD	VDD-VSS=5.0V	—	3.5	5.0	mA
Recommended LCD driving voltage	VDD-V0 Φ=10°	Ta=50	—	10.0	—	V
		Ta=25	—	10.5	—	V
		Ta=0	—	11.0	—	V
Power supply voltage for B/L	VLED-VSS	Ta=25	—	4.1	—	V
Power supply current for B/L	ILED	VLED=4.2V	—	480	700	mA

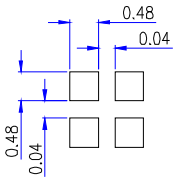
5.3 Dimensional outline



NOTES:

1. DISPLAY TYPE : 128X64 DOTS,1/64 DUTY,1/9 BIAS.VOP=10.5V.
   STN, YELLOW-GREEN MODE, TRANSFLECTIVE/POSITIVE.
2. DRIVER: NT7107 and NT7108 OR EQUIVALENT
3. VIEWING DIRECTION: 6 O'CLOCK.
4. OPERATING TEMP: -20°C ~ 70°C.
5. STORAGE TEMP: -30°C ~ 80°C.
6. LED BACKLIGHT: YELLOW-GREEN ,BOTTOM
7. Unmarked Tolerance: ±0.5mm.

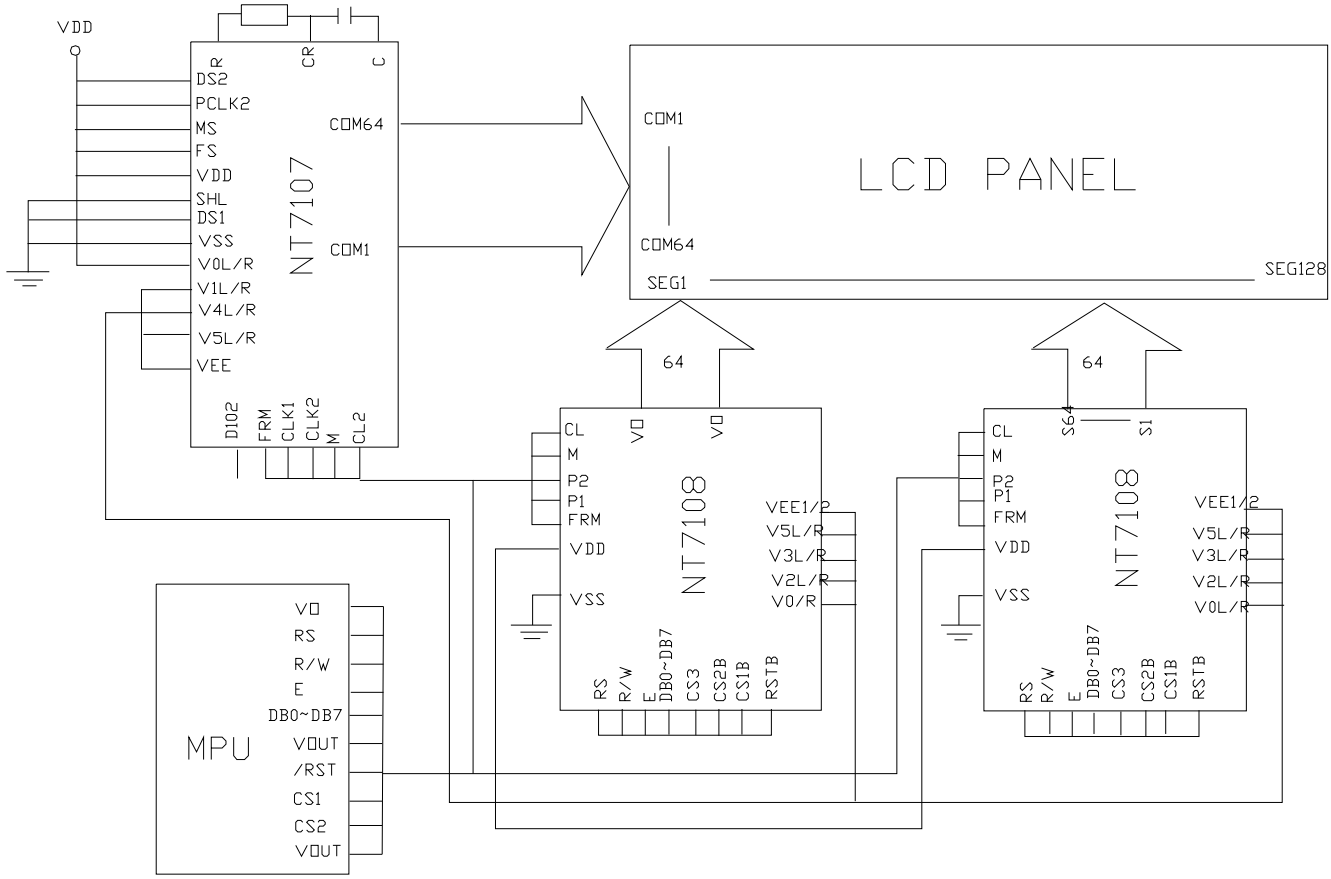
DISPLAY PATTERN



Pin Connections:

Pin NO.	Signal
1	VSS
2	VDD
3	V0
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	/CS1
16	/CS2
17	RST
18	VOUT
19	LED+
20	LED-

6 Block diagram



7 CHIP DEPICTION

7.1 NT7107

INTRODUCTION

The NT7107 is a LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device provides 64 shift registers and 64 out put drivers. It generates the timing signal to control the NT7108. The NT7107 is fabricated by low power CMOS high woltage process technology. And is composed of the liquid crystal display system in combination with the NT7108(64 channel segment driver).

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating voltage	V_{DD}	-0.3 to +7.0	V	(1)
Supply voltage	V_{EE}	V_{DD}-19.0 to VDD+0.3		(4)
Driver supply voltage	V_B	-0.3 to V_{DD}+0.3		(1),(2)
	V_{LCD}	V_{EE}-0.3 to V_{DD}+0.3		(3),(4)
Operating temperature	T_{OPR}	-30 to +85	℃	-
Storage temperature	T_{STG}	-55 to +125		-

NOTES:

1. Based on Vss=0V
2. Applies to input terminals and I/O terminals at high impedance. (Except V0L(R), V1L(R), V4L(R) and V5L(R))
3. Applies to V0L(R), V1L(R), V4L(R) and V5L(R).
4. Voltage level: $V_{DD} \geqq$ V0L=V0R $\geqq$ V1L=V1R $\geqq$ V4L=V4R $\geqq$ V5L=V5R $\geqq V_{EE}$.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{DD}=+5.0V, Vss=0V, $|V_{DD}-V_{EE}|$=8~17V, TA=-30 ~+85℃)

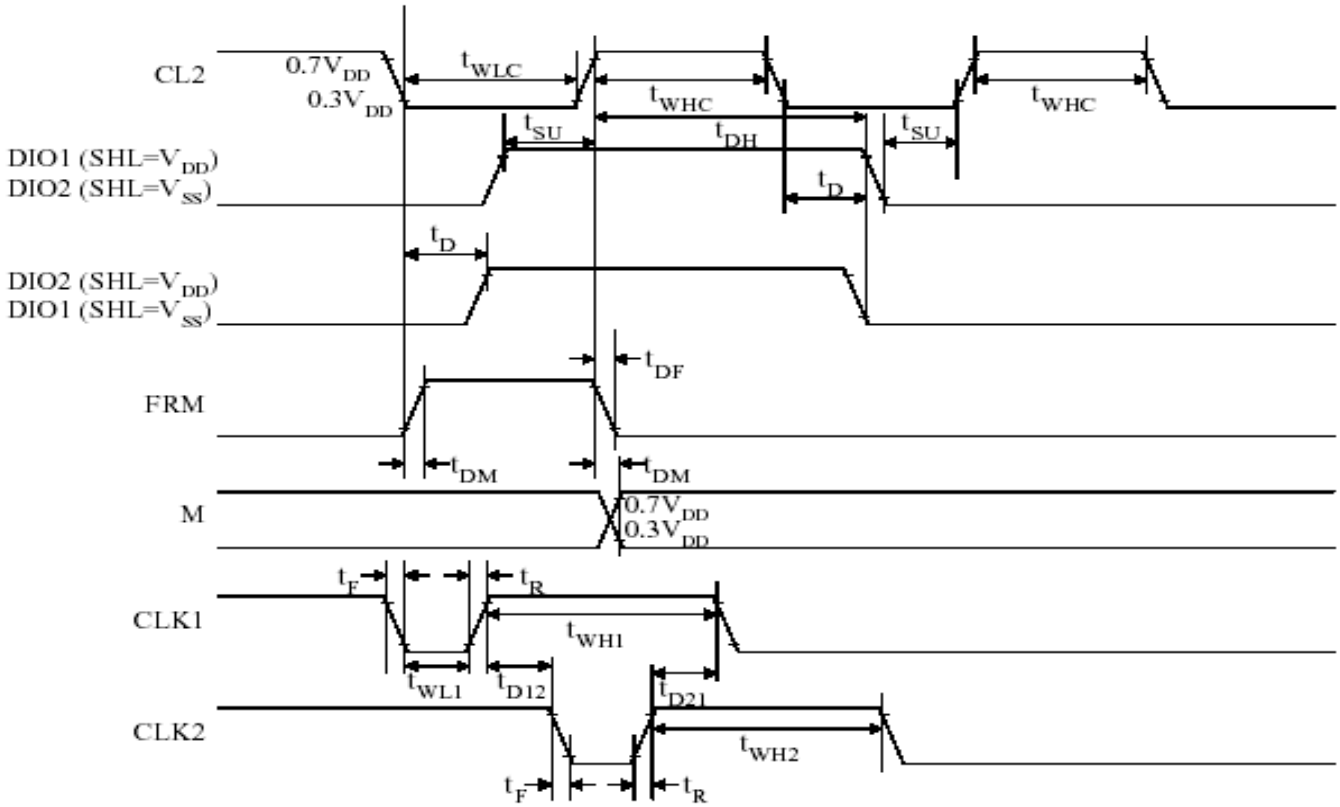
Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage		V_{DD}	-	2.7	-	5.5	V	
Input Voltage	High	V_{IH}	-	0.7V_{DD}	-	V_{DD}		(1)
	Low	V_{IL}	-	V_{SS}	-	0.3V_{DD}		
Output Voltage	High	V_{OH}	I_{OH}=-0.4mA	V_{DD}-0.4	-	-		(2)
	Low	V_{OL}	I_{OL}=0.4mA	-	-	0.4		
Input leakage current		I_{LKG}	$V_{IN}=V_{DD}-V_{SS}$	-1.0	-	1.0	μA	(1)
OSC frequency		f_{OSC}	Rf=47KΩ±2%	315	450	585	kHz	
On resistance (V_{DIV} - C_i)		R_{ON}	$V_{DD}-V_{EE}$=17V Load current = ±150 μA	-	-	1.5	KΩ	
Operating current		I_{DD1}	Master mode; 1/128duty	-	-	1.0	mA	(3)
		I_{DD2}	Slave mode; 1/128 duty	-	-	200	μA	(4)
Supply current		I_{EE}	Master mode; 1/128 duty	-	-	100		(5)
Operating Frequency		f_{OP1}	Master mode; External clock	50	-	600	kHz	
		f_{OP2}	Slave mode	0.5	-	1500		

NOTES:

1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the input state.
2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the Output State.
3. This value is specified at about the current flowing through Vss. Internal oscillation circuit: Rf = 47kΩ, Each terminal of DS1, DS2, FS, SHL and MS is connected to V_{DD} and out is no load.
4. This value is specified at about the current flowing through Vss. Each terminal of DS1, DS2, FS, SHL, PCLK2 and CR is connected to V_{DD}, and MS is connected to Vss. CL2, M, DIO1 is external clock.
5. This value is specified at the current flowing through V_{EE}. Don connect to V_{LCD} (V1-V5).

AC CHARACTERISTICS (V_{DD}=5V 10%,TA=-30~+85)

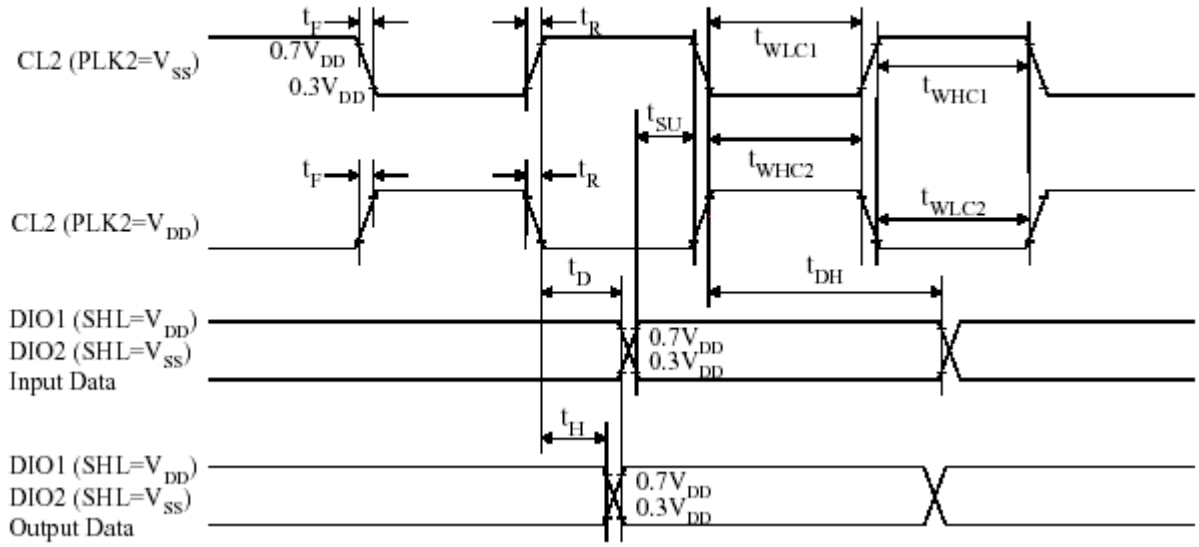
Master Mode (MS=V_{DD},PCLK2= V_{DD})



Master Mode

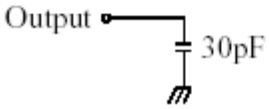
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Data setup time	t_{SU}	20	-	-	μs
Data hold time	t_{DH}	40	-	-	
Data delay time	t_D	5	-	-	
FRM delay time	t_{DF}	-2	-	2	
M delay time	t_{DM}	-2	-	2	
CL2 low level width	t_{WLC}	35	-	-	
CL2 high level width	t_{WHC}	35	-	-	
CLK1 low level width	t_{WL1}	700	-	-	ns
CLK2 low level width	t_{WL2}	700	-	-	
CLK1 high level width	t_{WH1}	2100	-	-	
CLK2 high level width	t_{WH2}	2100	-	-	
CLK1-CLK2 phase difference	t_{D12}	700	-	-	
CLK2-CLK1 phase difference	t_{D21}	700	-	-	
CLK1,CLK2 rise/fall time	t_R/ t_F	-	-	150	

Slave Mode (MS=V_{SS})



Characteristic	Symbol	Min.	Typ.	Max.	Unit	Note
CL2 low level width	t_{WLC1}	450	-	-	ns	PCLK2=V_{SS}
CL2 high level width	t_{WHC1}	150	-	-		PCLK2=V_{SS}
CL2 low level width	t_{WLC2}	150	-	-		PCLK2=V_{DD}
CL2 high level width	t_{WHC2}	450	-	-		PCLK2=V_{DD}
Data setup time	t_{SU}	100	-	-		
Date hold time	t_{DH}	100	-	-		
Data delay time	t_D	-	-	200		(NOTE)
Output data hold time	t_H	10	-	-		
CL2 rise/fall time	t_R/ t_F	-	-	30		

NOTE: Connect load CL = 30pF

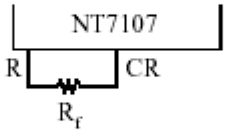


FUNCTIONAL DESCRIPTION

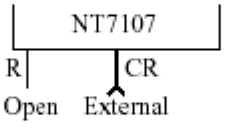
RC Oscillator

The RC Oscillator generates CL2, M, FRM of the NT7107, and CLK1 and CLK1 of the NT7108 by the oscillation resister R and internal capacitor C. When selecting the master/slave mode, the oscillation circuit is as following:

Master Mode: In the master mode, use these terminals as shown below.

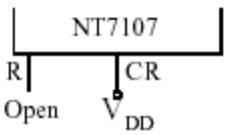


Internal Oscillation(Rf=47kΩ)



External Clock

Slave Mode: In the slave mode, stop the oscillator as shown below.



Timing Generation Circuit

It generates CL2, M, FRM, CLK1 and CLK2 by the frequency from the oscillation circuit.

Selection of Master/Slave (M/S) Mode

When MS is H, it generates CL2, M, FRM, CLK1 and CLK2 internally.

When MS is L, it operates by receiving M and CL2 from the master device.

Frequency Selection (FS)

To adjust FRM frequency by 70Hz, the oscillation frequency should be as follows:

FS	Oscillation Frequency
H	f_{OSC}=430kHz
L	f_{OSC}=215kHz

In the slave mode, it is connected to V_{DD}.

Duty Selection (DS1, DS2)

It provides various duty selections according to DS1 and DS2.

DS1	DS2	Duty
L	L	1/48
	H	1/64
H	L	1/96
	H	1/128

Data Shift & Phase Select Control

Phase Selection

It is a circuit to shift data on synchronization of rising edge, or falling edge of the CL2 according to PCLK2.

PCLK2	Phase Selection
H	Data shift on rising edge of CL2
L	Data shift on falling edge of CL2

Data shift Direction Selection

When MS is connected to V_{DD}, DIO1 and DIO2 terminal is only output.

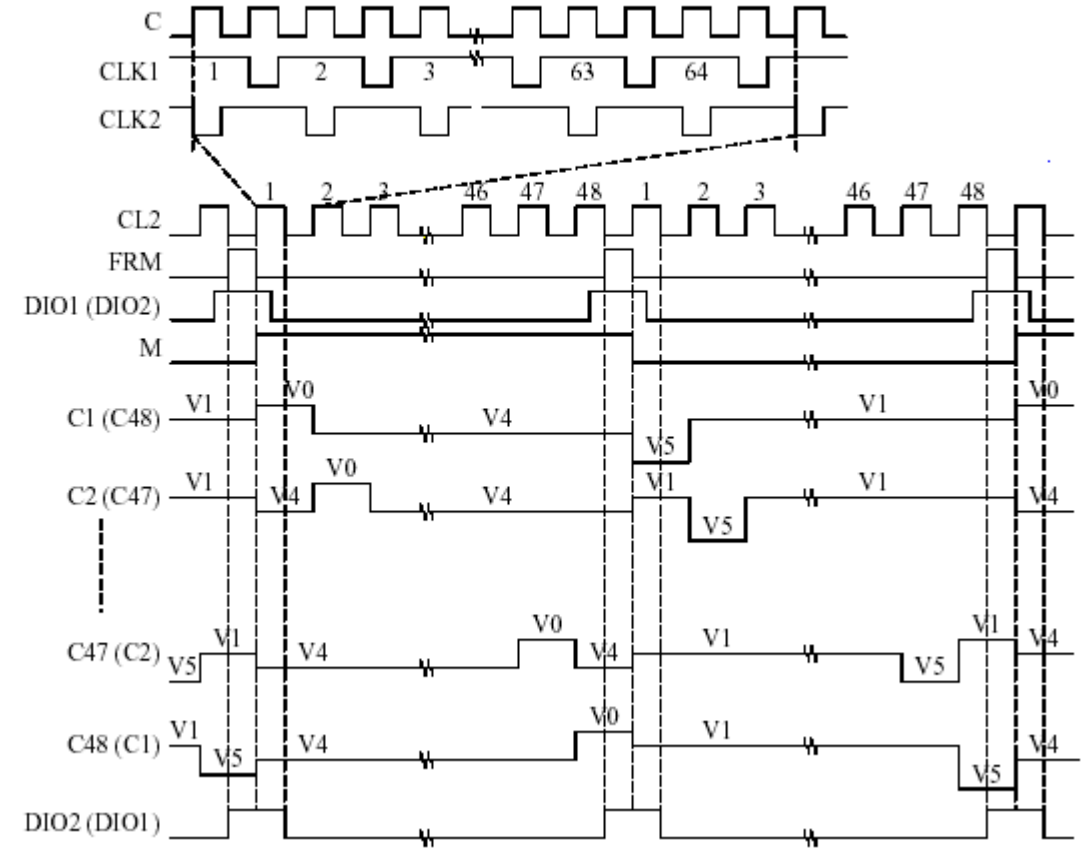
When MS is connected to Vss, it depends on the SHL.

MS	SHL	DIO1	DIO2	Direction of Data
H	H	Output	Output	C1→ C64
	L	Output	Output	C64 → C1
L	H	Input	Output	DIO1 → C1 → C64 → DIO2
	L	Output	Input	DIO2 → C64 → C1 → DIO1

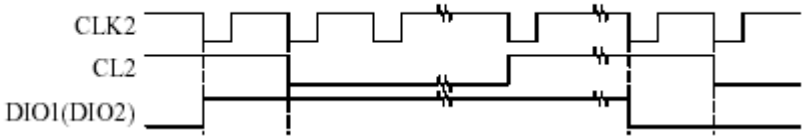
TIMING DIAGRAM

1/48 DUTY TIMING (MASTER MODE)

Condition: DS1=L, DS2=L, SHL=H (L), PCLK2=H

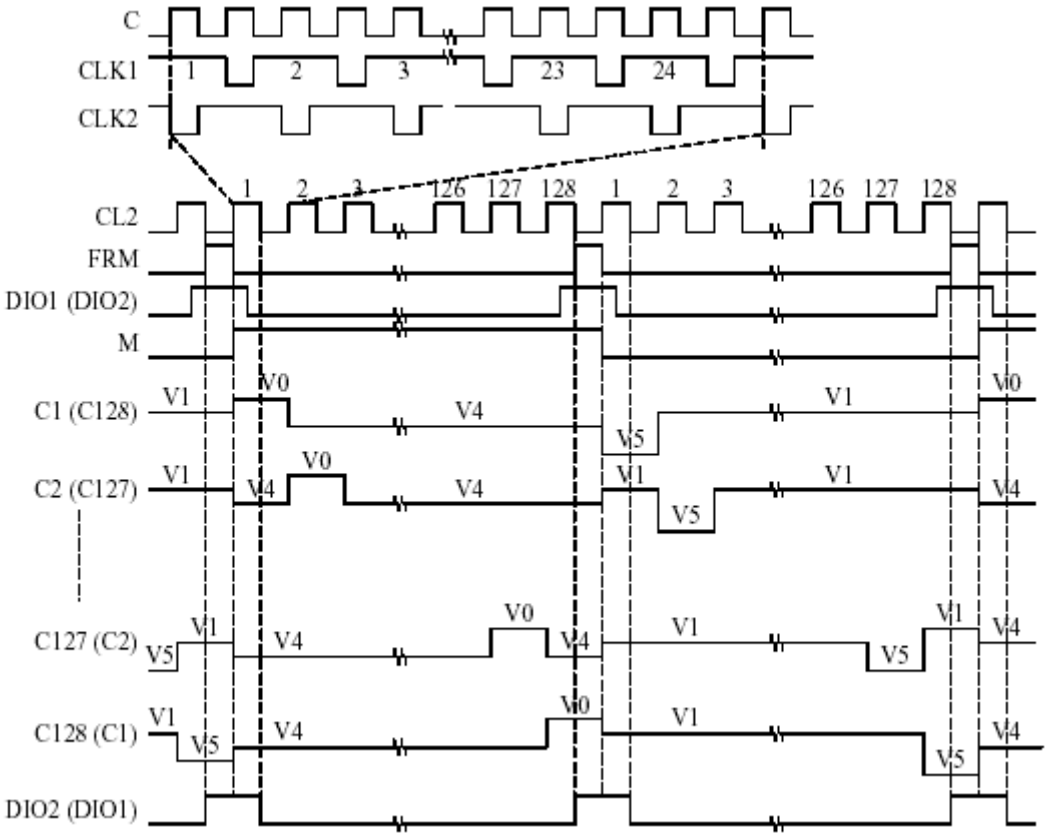


Relation of CL2 and DIO1(DIO2)

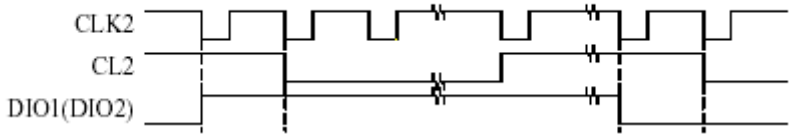


1/128 DUTY TIMING (MASTER MODE)

Condition: DS1=H,DS2=H,SHL=H(L),PCLK2=H

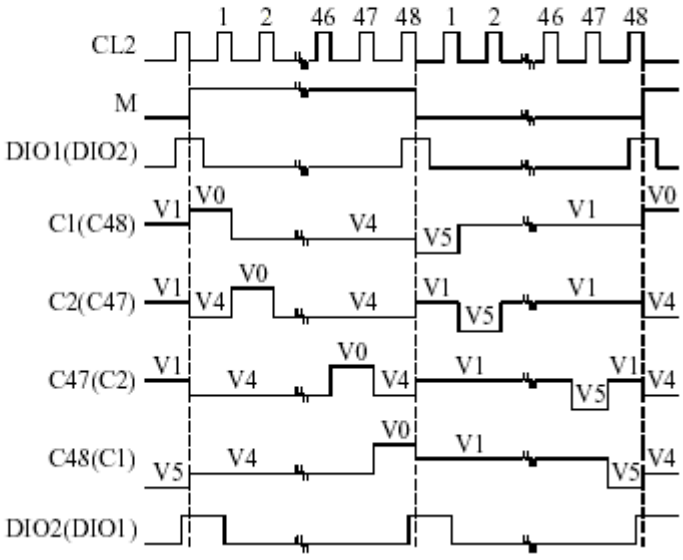


Relation of CL2 and DIO1(DIO2)

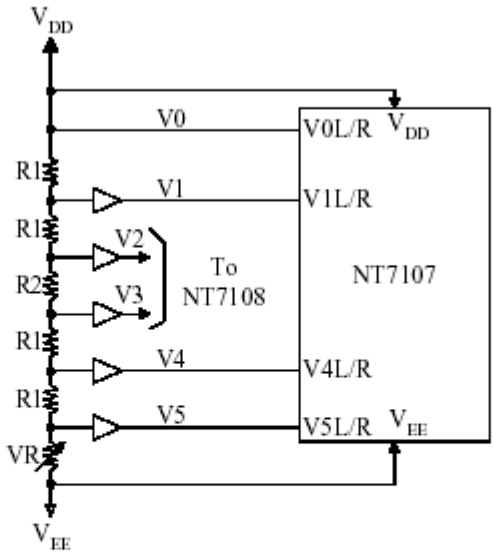


1/48 DUTY TIMING (SLAVE MODE)

Condition: SHL=H (L), PCLK2=L



POWER DRIVER CIRCUIT



Relation of Duty & Bias

Duty	Bias	RDIV
1/48	1/8	R2=4R1
1/64	1/9	R2=5R1
1/96	1/11	R2=7R1
1/128	1/12	R2=8R1

When duty factor is 1/48, the value of R1 & R2 should satisfy.
R1/(4R1 + R2)=1/8 ;
R1=3kΩ , R2=12kΩ

7.2 NT7108

INTRODUCTION the NT7108 is a LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device consists of the display RAM, 64 bits data latch, 64 bit drivers and decoder logic. It has the internal display RAM for storing the display data transferred form a 8 bit micro controller and generates the dot matrix liquid crystal driving signals corresponding to stored data. The NT7108 composed of the liquid crystal display system in combination with the NT7107.

OPERATING PRINCIPLES AND METHODS

I/O BUFFER

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B-CS3.

INPUT REGISTER

Input register is provided to interface with MPU, which is different operating frequency. Input register stores the data temporarily before writing it into display RAM. When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register, then into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

OUTPUT REGISTER

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H, RS=L, status data (busy check) can read out. To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

RESET

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU.

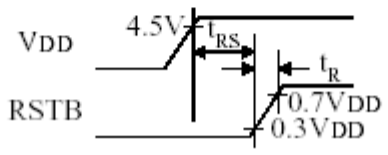
When RSTB becomes low, following procedure is occurred.

- Display off
- Display start line register become set by 0. (Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4=0 (clear RSTB) and DB7=0 (ready) by status read instruction. The Conditions of power supply at initial power up are shown in table 2.

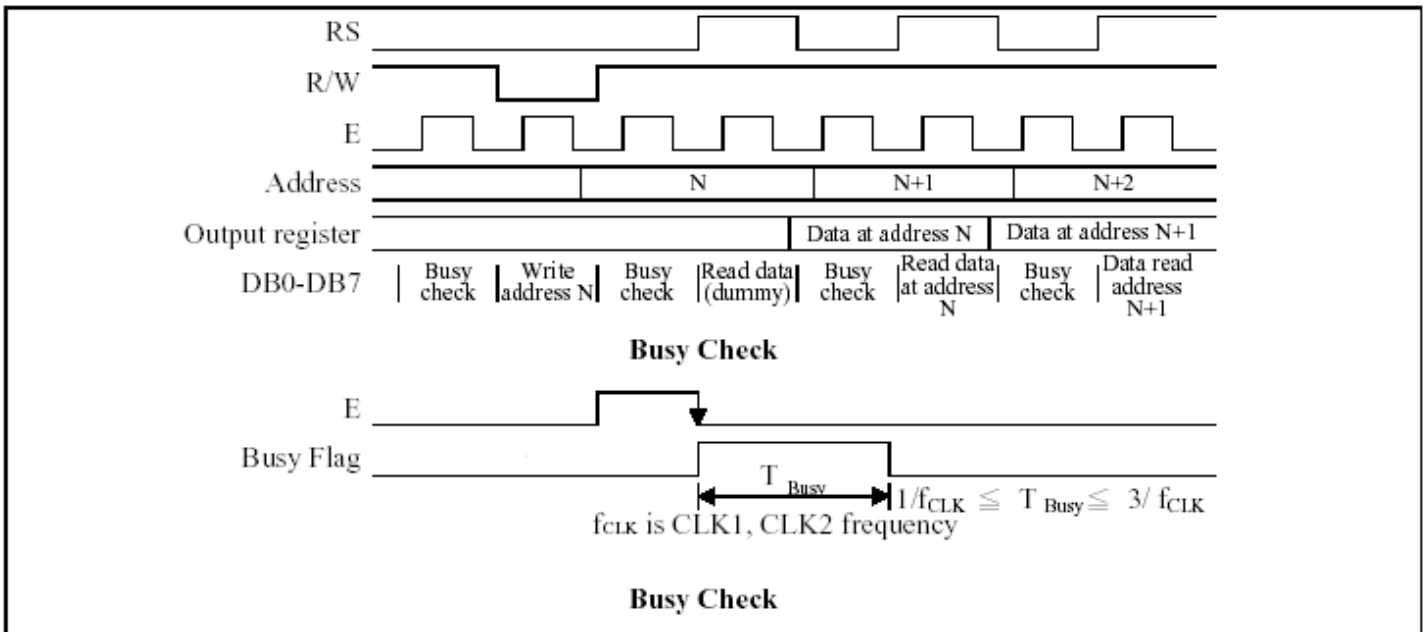
Table 2. Power Supply Initial Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Reset time	tRS	1.0	-	-	μs
Rise time	tR	-	-	200	ns



Busy Flag

Busy Flag indicates the NT7108 is operating or no operating. When busy flag is high, NT7108 is in internal operating. When busy flag is low, NT7108 can accept the data or instruction. DB7 indicates busy flag of the NT7108.



Display ON / OFF Flip-Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non-selective voltage appears on segment output terminals. When flip-flop is set (logic high), non-selective voltage appears on segment output terminals regardless of display RAM data. The display on/off flip-flop can changes status by instruction. The display data at all segments disappear while RSTB is low. The status of the flip-flop is output to DB5 by status read instruction. The display on/off flip-flop synchronized by CL signal.

X Page Register

X page register designates pages of the internal display data RAM. Count function is not available. An address is set by instruction.

Y Address Counter

An Address is set by instruction and is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write data 1. The other way, off state, writes 0.

Display data RAM address and segment output can be controlled by ADC signal.

- ADC=H → Y-address 0:S1-Y address 63:S64
- ADC=L → Y-address 0:S64-Y address 63:S1

ADC terminal connects the VDD or Vss.

Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display. Bit data (DB<0.5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter. It is used for scrolling of the liquid crystal display screen.

DISPLAY CONTROL INSTRUCTION

The display control instructions control the internal state of the NT7108. Instruction is received from MPU to NT7108 for the display control. The following table shows various instructions.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display on/off	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L:OFF, H:ON
Set address (Y address)	L	L	L	H	Y address (0-63)						Sets the Y address in the Y address counter.
Set page (X address)	L	L	H	L	H	H	H	Page (0-7)			Sets the X address at the X address register.
Display Start line (Z address)	L	L	H	H	Display start line (0-63)						Indicates the display data RAM displayed at the top of the screen.
Status read	L	H	Busy	L	On/ Off	Reset	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset
Write display data	H	L	Write data								Writes data (DB0: 7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read display data	H	H	Read data								Reads data (DB0: 7) from display data RAM to the data bus.

DISPLAY ON/OFF

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

SET ADDRESS (Y ADDRESS)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address (AC0-AC5) of the display data RAM is set in the Y address counter. An address is set by instruction and increased by 1 automatically by read or write operations of display data.

SET PAGE (X ADDRESS)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

X address (AC0-AC2) of the display data RAM is set in the X address register. Writing or reading to or from MPU is executed in this specified page until the next page is set.

DISPLAY START LINE (Z ADDRESS)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

Z address (AC0-AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen. When the display duty cycle is 1/64 or others (1/32-1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

STATUS READ

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY

  When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.

  When BUSY is 0, the Chip is ready to accept any instructions.

- ON/OFF

  When ON/OFF is 1, the display is OFF.

  When ON/OFF is 0, the display is ON.

- RESET

  When RESET is 1, the system is being initialized.

  In this condition, no instructions except status read can be accepted.

  When RESET is 0, initializing has finished and the system is in usual operation condition.

WRITE DISPLAY DATA

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Writes data (D0-D7) into the display data RAM. After writing instruction, Y address is increased by 1automatically.

READ DISPLAY DATA

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Reads data (D0-D7) from the display data RAM. After reading instruction, Y address is increased by 1 automatically.

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating voltage	V_{DD}	-0.3 to +7.0	V	(1)
Supply voltage	V_{EE}	V_{DD}-19.0 to V_{DD} +0.3		(4)
Driver supply voltage	V_B	-0.3 to V_{DD} +0.3		(1),(3)
	V_{LCD}	V_{EE}-0.3 to V_{DD} +0.3		(2)
Operating temperature	T_{OPR}	-30 to +85	℃	
Storage temperature	T_{STG}	-55 to +125		

NOTES:

1. Based on Vss=0V
2. Applies the same supply voltage to V_{EE1} and V_{EE2}. $V_{LCD}=V_{DD}-V_{EE}$.
3. Applies to M, FRM, CL, RSTB, ADC, CLK1, CLK2, CS1B, CS2B, CS3, E, R/W, RS and DB0-DB7.
4. Applies to V0L(R), V2L(R), V3L(R) and V5L(R).

Voltage level: $V_{DD} \geqq V0L=V0R \geqq V2L=V2R \geqq V3L=V3R \geqq V5L=V5R \geqq V_{EE}$.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{DD}=5.0V, Vss=0V, V_{DD}-V_{EE}=8 to 17V, Ta=-30℃ to +85℃)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating Voltage	V_{DD}	-	2.7	-	5.5	V	
Input high Voltage	V_{IH1}	-	0.7V_{DD}	-	V_{DD}		(1)
	V_{IH2}	-	2.0	-	V_{DD}		(2)
Input low Voltage	V_{IL1}	-	0	-	0.3V_{DD}		(1)
	V_{IL2}	-	0	-	0.8		(2)
Output high voltage	V_{OH}	I_{OH}=-200 μA	2.4	-	-		(3)
Output low voltage	V_{OL}	I_{OL}=1.6mA	-	-	0.4		(3)
Input leakage current	I_{LKG}	V_{IN}=Vss-V_{DD}	-1.0	-	1.0	μA	(4)
Three-state(off) input current	I_{TSL}	V_{IN}=Vss-V_{DD}	-5.0	-	5.0		(5)
Driver input leakage current	I_{DIL}	V_{IN}=V_{EE}-V_{DD}	-2.0	-	2.0		(6)
Operating current	I_{DD1}	During display	-	-	100		(7)
	I_{DD2}	During access Access cycle = 1 MHz	-	-	500		(7)
On resistance	R_{ON}	V_{DD}-V_{EE}=15V I_{LOAD}= ±0.1mA	-	-	7.5	kΩ	(8)

NOTES:

1. CL,FRM,M RSTB,CLK1,CLK2
2. CS1B,CS2B,CS3,E,R/W,RS,DB0~DB7
3. DB0-DB7
4. Except DB0~DB7
5. DB0-DB7 at high impedance
6. VOL(R),V2L(R),V5L(R)
7. 1/64 duty,fclk=250KHz,frame frequency=70HZ,output:no load
8. VDD-VEE=15.5V

V0L(R)> V2L(R)=V_{DD}-2/7(V_{DD}- V_{EE})> V3L(R)= V_{EE}+2/7(V_{DD}- V_{EE})> V5L(R)

AC CHARACTERISTICS (V_{DD}=+5V±10%, Vss=0V, Ta=-30℃ to +85℃)

Clock Timing

Characteristic	Symbol	Min	Type	Max	Unit
CLK1, CLK2 cycle time	tCY	2.5	-	20	μs
CLK1 "low" level width	tWL1	625	-	-	ns
CLK2 "low" level width	tWL2	625	-	-	
CLK1 "high" level width	tWH1	1875	-	-	
CLK2 "high" level width	tWH2	1875	-	-	
CLK1-CLK2 phase difference	tD12	625	-	-	
CLK2-CLK1 phase difference	tD21	625	-	-	
CLK1, CLK2 rise time	tR	-	-	150	
CLK1, CLK2 fall time	tF	-	-	150	

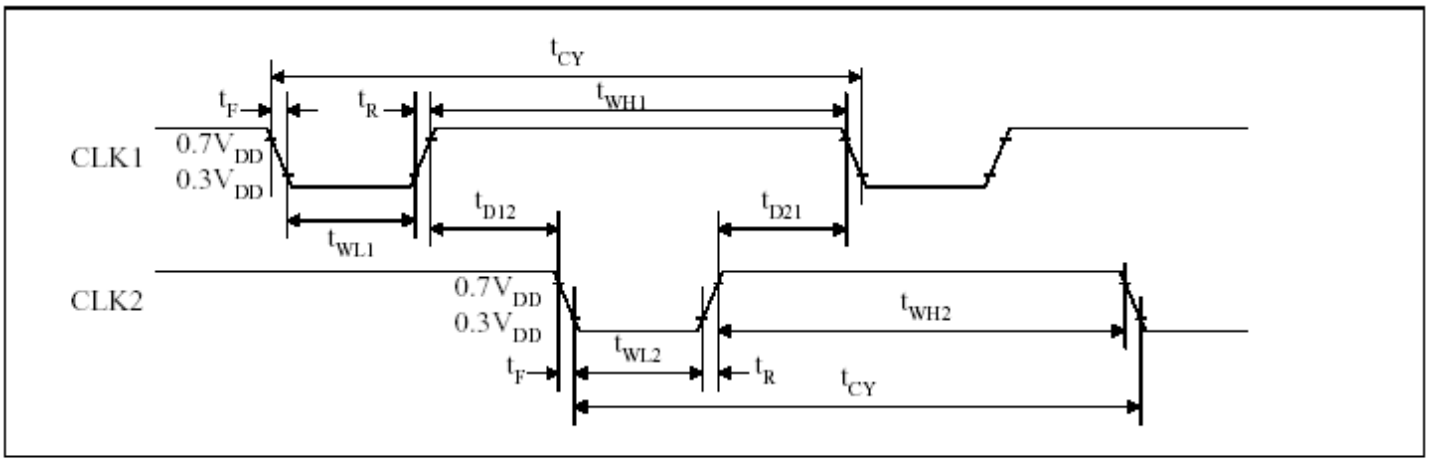


Figure 1. External Clock Waveform

Display Control Timing

Characteristic	Symbol	Min	Type	Max	Unit
FRM delay time	tDF	-2	-	2	μs
M delay time	tDM	-2	-	2	
CL "low" level width	tWL	35	-	-	
CL "high" level width	tWH	35	-	-	

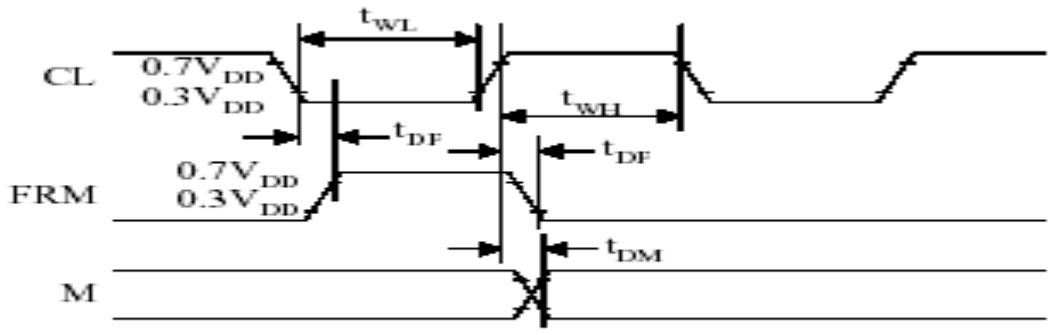


Figure 2. Display Control Waveform

MPU Interface

Characteristic	Symbol	Min	Type	Max	Unit
E cycle	tC	1000	-	-	ns
E high level width	tWH	450	-	-	
E low level width	tWL	450	-	-	
E rise time	tR	-	-	25	
E fall time	tF	-	-	25	
Address set-up time	tASU	140	-	-	
Address hold time	tAH	10	-	-	
Data set-up time	tDSU	200	-	-	
Data delay time	tD	-	-	320	
Data hold time (write)	tDHW	10	-	-	
Data hold time (read)	tDHR	20	-	-	

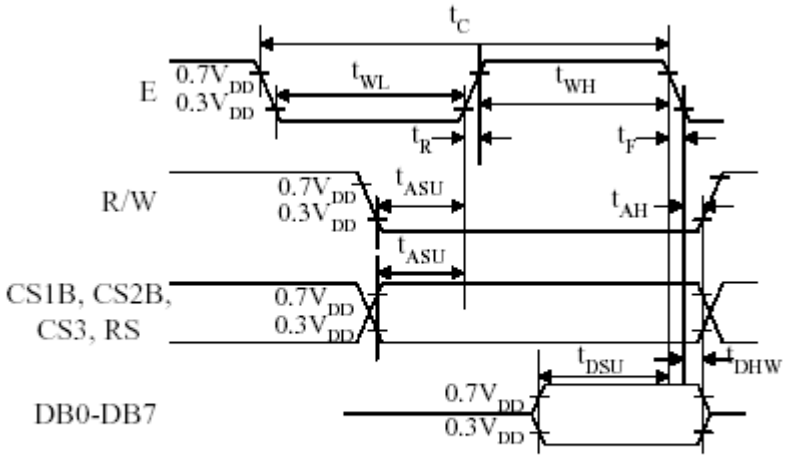


Figure 3. MPU Write Timing

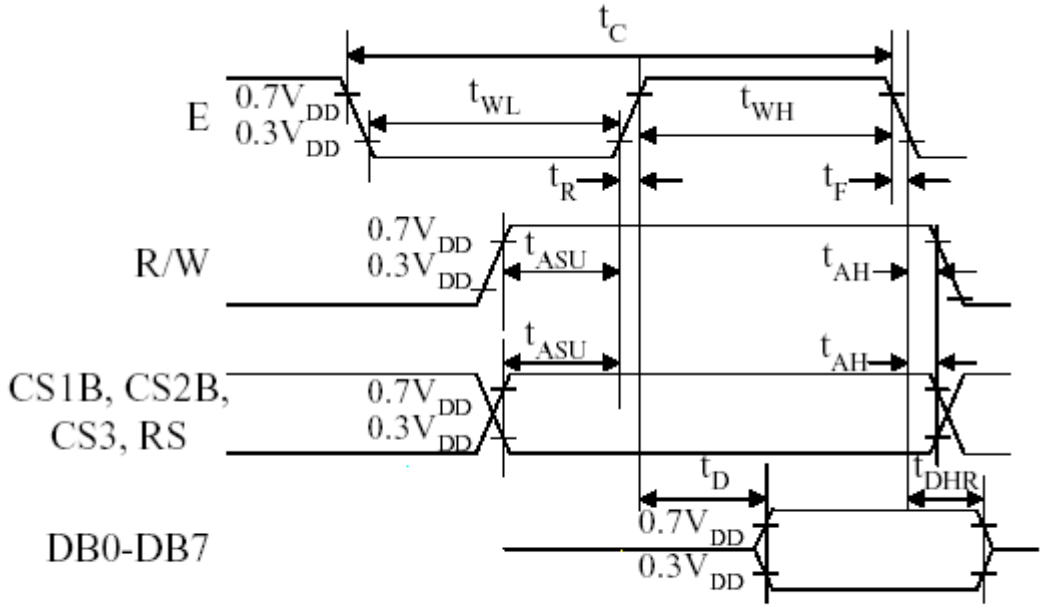


Figure 4. MPU Read Timing

TIMING DIAGRAM (1/64 DUTY)