GENDA TECHNOLOGY (SHEN ZHEN) LTD

Part No. : GS-GB1286433YFYJ-C/R

Customer :_____

Drawing No. :_____

Approved :_____

Date :_____

Approved:_____ Checked:_____ Prepared:_____

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CONTENTS

3. GENERAL SPECIFICATIONS

This individual specification is general specifications.

4. PRECAUTIONS FOR LCM

4.1 Precautions in handling LCD Modules (hereinafter LCMs)

Genda's LCMs have been assembled and accurately calibrated before delivery.

Please observe the following criteria when handling.

A. Do not subject the module to excessive shock.

B. Do not modify the tab on the metal holder.

C. Do not tamper with the printed circuit board.

D. Limit the soldering of the printed circuit board to I/O terminals only.

E. Do not touch the zebra strip nor modify its location.

4.2 Static electricity warning

Genda's LCM uses CMOS LSI technology. Therefore, strict measures to avoid static electricity discharge are followed through all processes from manufacturing to shipping. When handling a LCM, take sufficient care to prevent static electricity discharge as you would any CMOS IC.

A. Do not take the LCM from its anti-static bag until it's to be assembled.

LCM's are individually packaged in bags specially treated to resist static electricity. When storing, keep the LCM packed in the original bags, or store them in a container processed to be resistant to static electricity, or in an electric conductive container.

B. Always use a ground strap when handling a LCM.

Always use a ground strap while working with the module, from the time it is taken out of the anti-static bag until it is assembled. If it is necessary to transfer the LCM, once it has been taken out of the bag, always place it in an electric conductive container. Avoid wearing clothes made of chemical fibers, the use of cotton or conductive treated fiber clothing is recommended.

C. Use a no-leak iron for soldering the LCM.

The soldering iron to be used for soldering the I/O terminals to the LCM are to be insulated or grounded at the iron tip.

D. Always ground electrical apparatuses required for assembly.

Electrical apparatuses required to assemble the LCM into a product, i.e. electrical screw drivers, are to be first grounded to avoid transmitting spike noises from the motor.

E. Assure that the work bench is properly grounded.

F. Peel off the LCM protective film slowly.

The module is attached with a film to protect the display surface from contamination, damage, adhesion of flux, etc. Peeling off this film abruptly could cause static electricity to be generated, so peel the tape slowly.

G. Pay attention to the humidity in the work area.

50~60% RH is recommended.

4.3 Precautions for the soldering of a LCM

The following procedures should be followed when soldering the LCM:

A. Solder only to the I/O terminal.

B. Use a no leakage soldering iron and pay particular attention to the following:

(1) Conditions for soldering I/O terminals

Temperature at iron tip: 280℃ + 10℃

Soldering time: 3~4 sec/terminal

Type of solder: Eutectic solder (rosin flux filled)

Note: (Avoid using flux, because it could penetrate the module and the module may get contaminated during cleaning.) Peel off protective film after soldering the I/O terminals. By following this procedure, the surface contamination caused by the dispersion of flux while soldering can be avoided.

(2) Removing the wiring

(When a lead wire, or a connector to the I/O terminal of the module is to be removed, remove it only after the solder at the connection has sufficiently melted since the I/O terminal is a through hole.) If it is forcefully removed, it could cause the terminal to break or peel. The recommended procedure is to use a suction-type solder remover. Caution: do not reheat the I/O terminal more than 3 times.

4.4 Long-term storage

If the correct method of storage is not followed, deterioration of the display material (polarizer) and oxidation of the I/O terminal plating may make the process of soldering difficult. Please comply with the following procedure.

A. Store in the shipping container.

B. If the shipping container is not available, place in anti-static bags and seal the opening.

C. Store the modules where they are not subjected to direct sunlight or a fluorescent lamp.

D. Store in a temperature range of 0℃ - 35℃ with low relative humidity.

4.5 Precautions in use of LCD modules

A. Do not give any external shock.

B. Do not wipe the surface with hard materials.

C. Do not apply excessive force on the surface.

D. Do not expose to direct sunlight or fluorescent light for a long time.

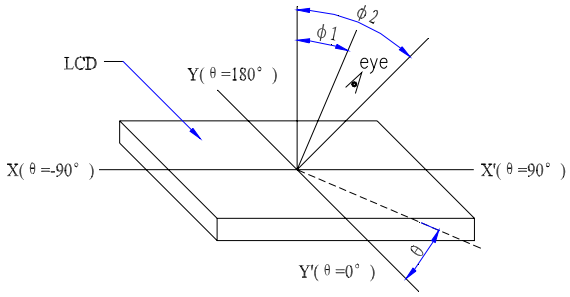
E. Avoid storage in high temperature and high humidity.

F. When storage for a long time at 40℃ or higher is required, R/H should be less than 60%.

G. Liquid in LCD is hazardous substance. Do not lick, swallow when the liquid is attached to your hands, skin, clothes etc. Wash it out thoroughly.

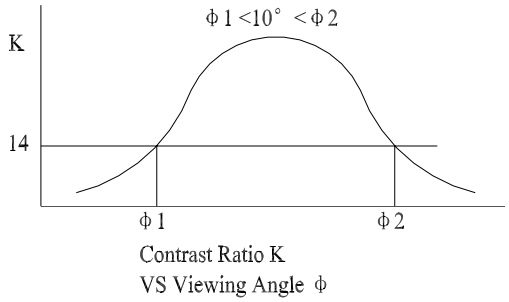
5. OPTICAL DEFINITIONS

5.1 Definition of angle θ and ϕ



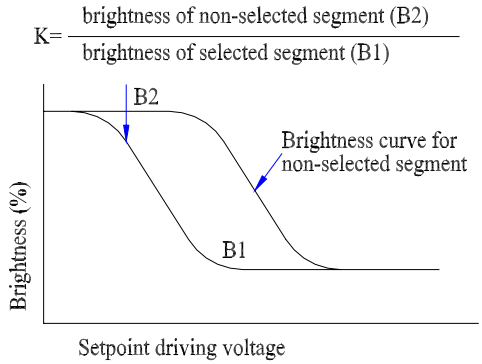
POSITIVE TYPE

5.2 Definition of viewing angle ϕ1 and ϕ2



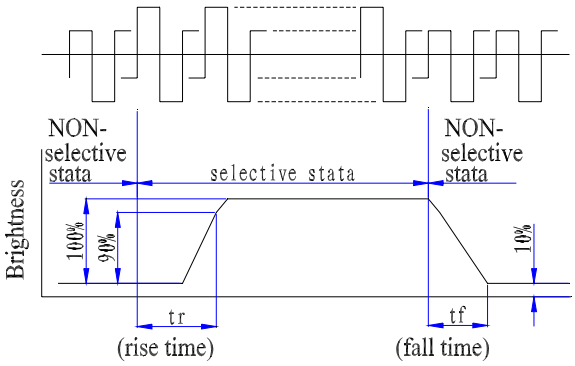
POSITIVE TYPE

5.3 Definition of contrast "K"



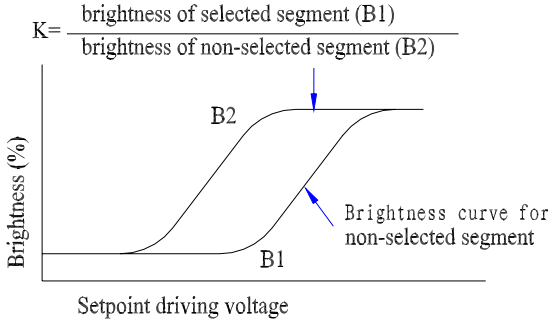
NEGATIVE TYPE

5.4 Definition of optical response

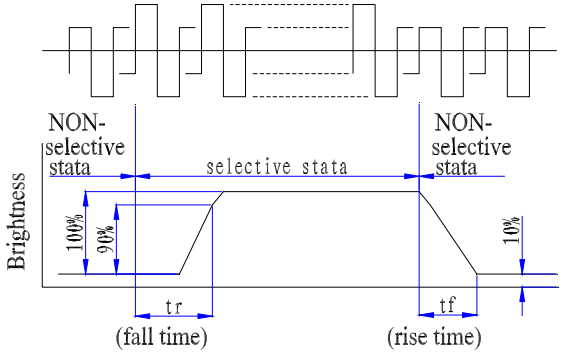


NEGATIVE TYPE

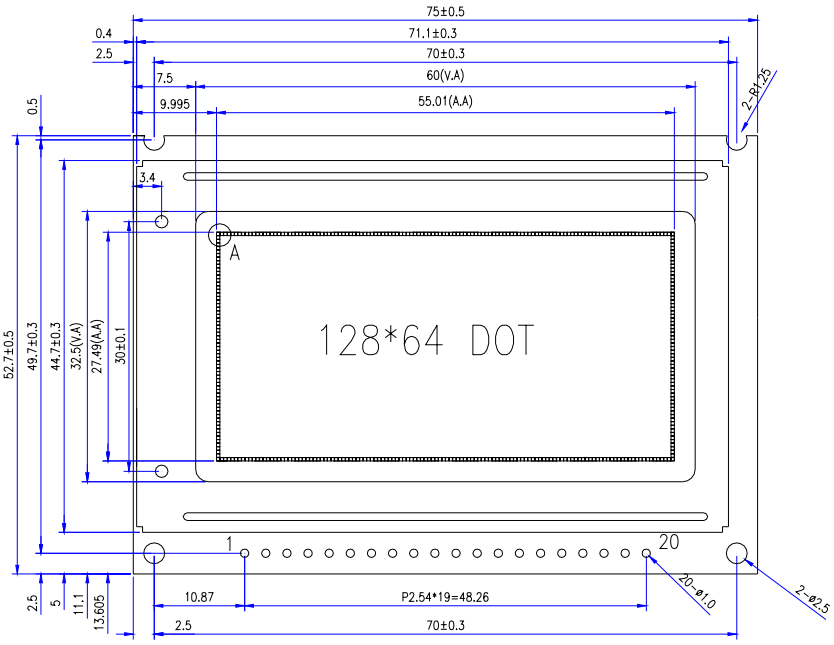
5.5 Definition of contrast "K"

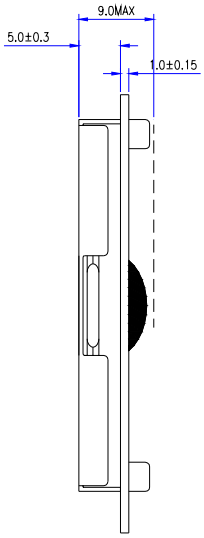


4.6 Definition of optical response



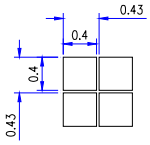
6.DIMENSIONAL OUTLINE





PIN CONNECTION:

PIN	SIGNAL
1	VDD
2	VSS
3	V0
4	DB0
5	DB1
6	DB2
7	DB3
8	DB4
9	DB5
10	DB6
11	DB7
12	/CS1
13	/CS2
14	/RST
15	R/W
16	D/I
17	E
18	VEE
19	A
20	K



"A" DISPLY PATTERN

NOTES:

1. DISPLAY TYPE: STN, YELLOW-GREEN MODE, TRANSFLECTIVE/POSITIVE
2. DRIVE METHOD: 1/64DUTY,1/9BIAS,VDD=5.0V,VOP=10.5V
3. VIEWING DIRECTION: 6 O'CLOCK
4. DRIVER: SBN0064G AND SBN6400G
5. OPERATING TEMP: -25°C~70°C
6. STORAGE TEMP: -30°C~80°C
7. BACKLIGHT TYPE: YELLOW-GREEN,EDGE,A-K=5.0V.
8. UNMARKED TOLERANCE: ±0.5mm.
9. ENVIRONMENT REQUEST.

VERSION	MODIFYCONTENT
03	更改IC品牌并升级模组料号
02	更改复位、偏压电路
--	更改为环保
01	更改温度和16PIN信号名称

CUSTOMER APVL		DATE	
DRAWN	SCALE	TITLE	MODULE
DFTG CHK	UNIT mm		
ENGR CHK		MODEL	GS-GB1286433YFYJ-C/R
APPROVAL	GENDA TECHNOLOGY LTD	DWG NO	03
		PAGE	1/10

7.MECHANICAL DATA

ITEM	STANDARD VALUE	UNIT
LCM SIZE	75*52.7*9.0MAX	mm
EFFECTIVE DISPLAY AREA	55.01*27.49	mm
OPERATING TEMP	-25~70	℃
STORAGE TEMP	-30~80	℃
DUTY	1/64	
VIEWING DIRECTION	6 O'CLOCK	
BACKLIGHT	YELLOW-GREEN	
LCD TYPE	STN YELLOW-GREEN MODE, TRANSFLECTIVE/POSITIVE	
DRIVER	SBN0064G AND SBN6400G	

8. ELECTRICAL ABSOLUTE RATING

Item	Std,value	UNIT	NOTE
Power Supply For LCM	5	V	
Power Supply For LCD	10.5	V	

9.CHIP DEPICTION

SBN6400G INTRODUCTION

The SBN6400G is a LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device provides 64 shift registers and 64 out put drivers. It generates the timing signal to control the SBN0064G. The SBN6400G is fabricated by low power CMOS high voltage process technology. And is composed of the liquid crystal display system in combination with the SBN0064G(64 channel segment driver).

Absolute maximum rating

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS}, unless otherwise specified; T_{amb} = −20 to +75 °C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	voltage on the V_{DD} pin(pad)	−0.3	+7.0	Volts
V_{EE}	Negative voltage on the V_{EE} pin(pad)	V_{DD}-16		Volts
V_{LCD} (note 2)	LCD bias voltage, V_{LCD}=V0-V5		13	Volts
V_I	input voltage on any pin with respect to V_{SS}	−0.3	V_{DD} + 0.3	Volts
P_D	power dissipation		200	mW
T_{stg}	storage temperature range	−55	+125	°C
T_{amb}	operating ambient temperature range	-30	+ 85	°C
Tsol (note 3)	soldering temperature/time at pin		260 °C, 10 Second	

Notes

1. The following applies to the Absolute Maximum Rating:
   a) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.
   b) The SBN6400G includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge (ESD). However, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
   c) Parameters are valid over operating temperature range, unless otherwise specified.
   d) All voltages are with respect to V_{SS}, unless otherwise noted.
2. The condition V_{DD}(V0)≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 must always be met.
3. QFP-type packages are sensitive to moisture of the environment, please check the drypack indicator on the tray package before soldering. Exposure to moisture longer than the rated drypack level may lead to cracking of the plastic package or broken bonding wiring inside the chip.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS}, unless otherwise specified; T_{amb} = −20 to +75 °C.

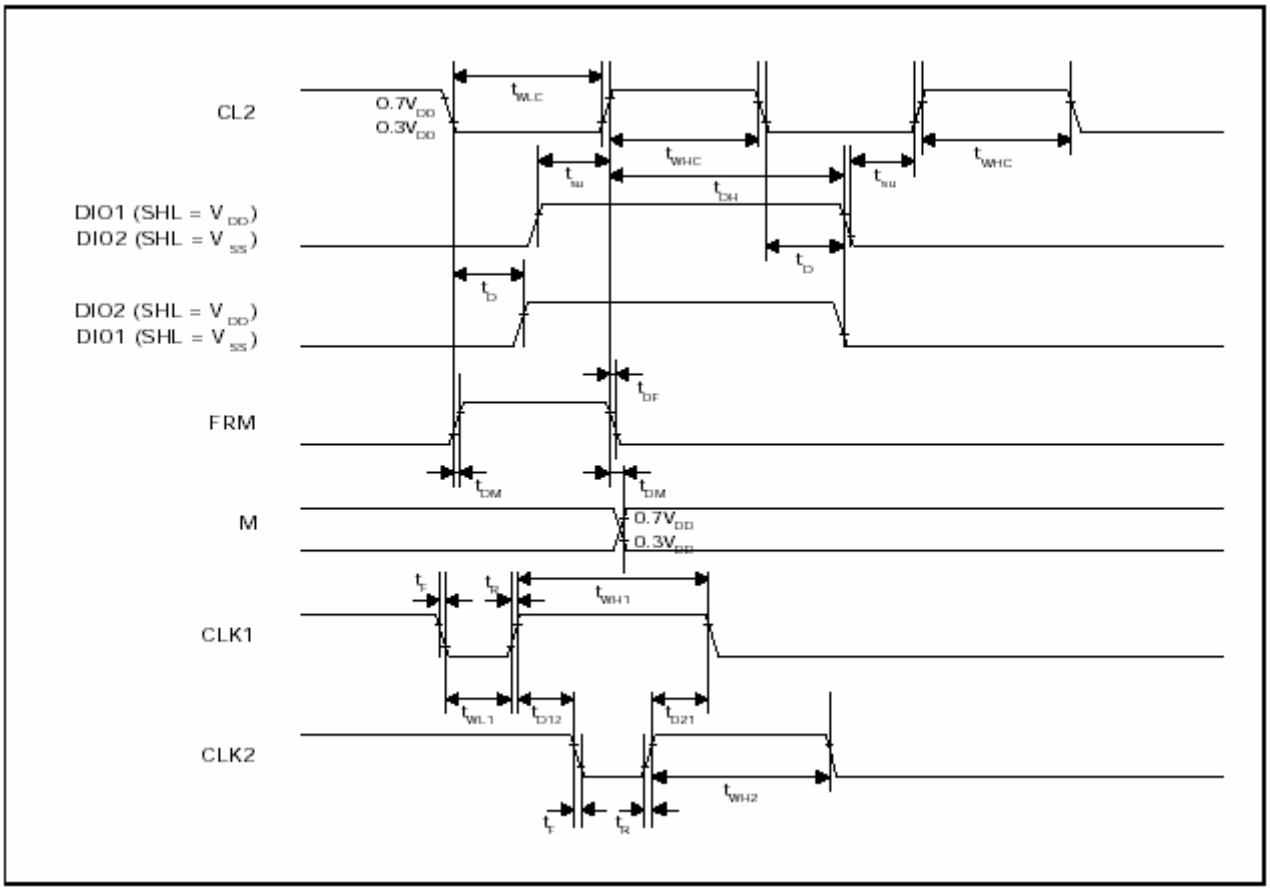
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage for logic		2.7	5.0	5.5	V
V_{LCD}	LCD bias voltage V_{LCD}= V0(V_{DD})-V5	Note 1.			13	V
V_{NEG}	V_{NEG}=V_{DD}-V_{EE}				16	V
V_{IL}	LOW level input voltage	Note 2.	0		0.8	V
V_{IH}	HIGH level input voltage	Note 2.	V_{DD}-2.2		V_{DD}	V
V_{OL}	LOW level output voltage of output terminals, at I_{OL}=1.6 mA.	Note 3	0.0		0.3	V
V_{OH}	HIGH level output voltage of output terminals, at I_{OH}=-200μA.	Note 3.	V_{DD} – 0.3		V_{DD}	V
I_{LKG}	Leakage current of input pins(pads)	for all inputs			0.2	μA
I_{STBY}	Standby current at V_{DD}=5 volts	Note 4			3.0	μA
$I_{DD(1)}$	Operating current for master mode with 1/128 display duty cycle	Note 5			960	μA
$I_{DD(2)}$	Operating current for slave mode with 1/128 display duty cycle	Note 6			180	μA
I_{EE}	Operating current measured at the V_{EE} pin(pad)	Note 7			90	μA
C_{in}	Input capacitance of all input pins			5.0	8.0	pF
R_{ON}	LCD driver ON resistance	Note 8			1.5	KΩ

Notes:

1. LCD bias voltage V_{LCD} is V0 - V5. V0 should always be connected to VDD.
2. For all input pins (pads), FS, DS1,DS2, CR, SHL, MS, and PSEL. Also, for all I/Os, DIO1, DIO2, M, and CL when they are used as inputs.
3. For all output pins (pads), CLK1, CLK2, and FRM. Also, for all I/Os, DIO1, DIO2, M, and CL when they are used as outputs
4. Conditions for the measurement: CR=V_{DD}, measured at the V_{DD} pin.
5. This value is measured at the V_{DD} pin (pad). The condition for the measurement is as follows:
   a) R_f=33K, C_f=20 pF,
   b) Display duty cycle=1/128 (DS1=DS2=1),
   c) Master mode (M/$\overline{S}$=1), and FS=SHL=PSEL=1, and
   d) COM0~COM63 were left open.
6. This value is measured at the V_{DD} pin (pad). The condition for the measurement is as follows:
   a) Display duty cycle=1/128 (DS1=DS2=1), Slave mode (M/$\overline{S}$=0), and FS=SHL=PSEL=CR=1,
   b) CL, M, and DIO1 are from the master, and
   c) COM0~COM63 were left open.
7. The condition for the measurement is the same as those described in Note 5, except that the value is measured at the V_{EE} pin(pad).
8. This measurement is for the transmission high-voltage PMOS or NMOS of COM0~COM63. Please refer to Section 12, Pin Circuits, for detailed schematic of these drivers. The measurement is for the case when the voltage differential between the source and the drain of the high voltage PMOS or NMOS is 0.1 volts.

AC CHARACTERISTICS (V_{DD} = 5V ± 10%, Tamb = -20°C to +75°C)

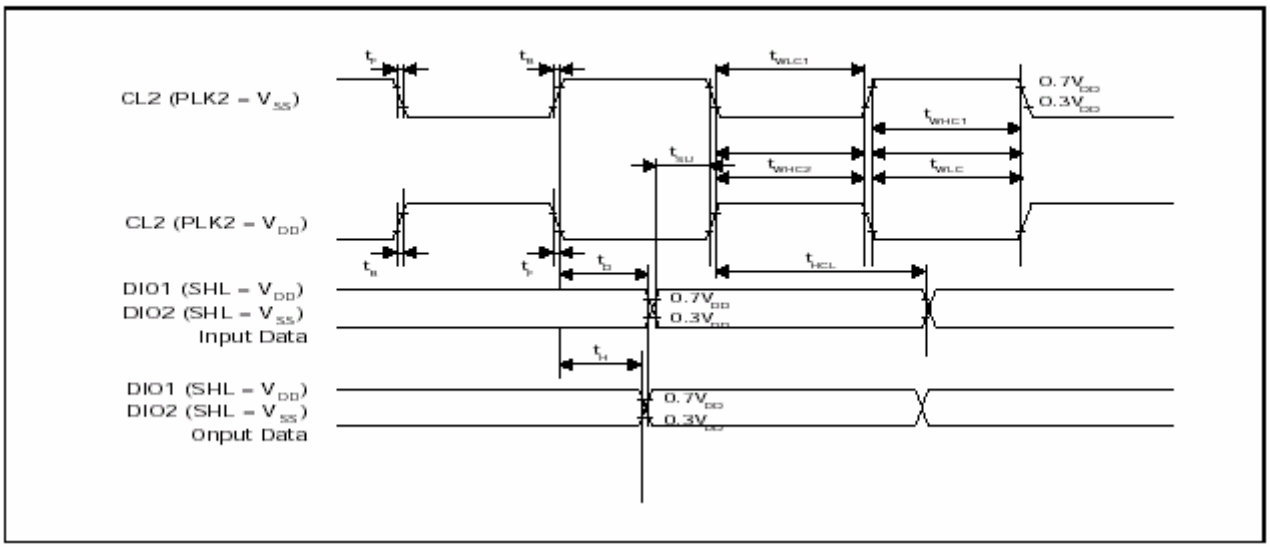
Master Mode (MS = V_{DD}, PCLK2 = V_{DD}, Cf = 20pF, Rf = 33kΩ)



Master Mode

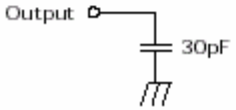
Characteristic	Symbol	Min	Typ	Max	Unit
Data setup time	t_{SU}	20	-	-	μs
Data hold time	t_{DH}	40	-	-	
Data delay time	t_D	5	-	-	
FRM delay time	t_{DF}	-2	-	2	
M delay time	t_{DM}	-2	-	2	
CL2 low level width	t_{WLC}	35	-	-	
CL2 high level width	t_{WHC}	35	-	-	
CLK1 low level width	t_{WL1}	700	-	-	ns
CLK2 low level width	t_{WL2}	700	-	-	
CLK1 high level width	t_{WH1}	2100	-	-	
CLK2 high level width	t_{WH2}	2100	-	-	
CLK1-CLK2 phase difference	t_{D12}	700	-	-	
CLK2-CLK1 phase difference	t_{D21}	700	-	-	
CLK1, CLK2 rise/fall time	t_R/t_F	-	-	150	

Slave Mode (MS = V_{SS})



Characteristics	Symbol	Min	Typ	Max	Unit	Note
CL2 low level width	t_{WLC1}	450	-	-	ns	PCLK2 = V_{SS}
CL2 high level width	t_{WHC1}	150	-	-	ns	PCLK2 = V_{SS}
CL2 low level width	t_{WLC2}	150	-	-	ns	PCLK2 = V_{DD}
CL2 high level width	t_{WHL}	450	-	-	ns	PCLK2 = V_{DD}
Data setup time	t_{SU}	100	-	-	ns	
Data hold time	t_{DH}	100	-	-	ns	
Data delay time	t_D	-	-	200	ns	(NOTE)
Output data hold time	t_H	10	-	-	ns	
CL2 rise/fall time	t_R/t_F	-	-	30	ns	

NOTE: Connect load CL = 30pF



SBN0064G INTRODUCTION

The SBN0064G is a LCD driver LSI with 64 channel output for dot matrix liquid crystal graphic display systems. This device consists of the display RAM, 64 bit data latch, 64 bit drivers and decoder logic. It has the internal display RAM for storing the display data transferred from a 8 bit micro controller and generates the dot matrix liquid crystal driving signals corresponding to stored data. The SBN0064G composed of the liquid crystal display system in combination with the SBN6400G (64 channel common driver).

OPERATING PRINCIPLES AND METHODS

I/O BUFFER

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B-CS3.

INPUT REGISTER

Input register is provided to interface with MPU, which is different operating frequency. Input register stores the data temporarily before writing it into display RAM. When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register, then into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

OUTPUT REGISTER

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H, RS=L, status data (busy check) can read out. To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

RESET

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU.

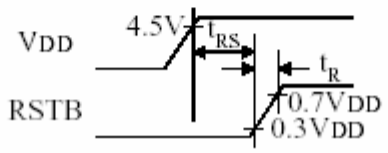
When RSTB becomes low, following procedure is occurred.

- Display off
- Display start line register become set by 0. (Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4=0 (clear RSTB) and DB7=0 (ready) by status read instruction. The Conditions of power supply at initial power up are shown in table 2.

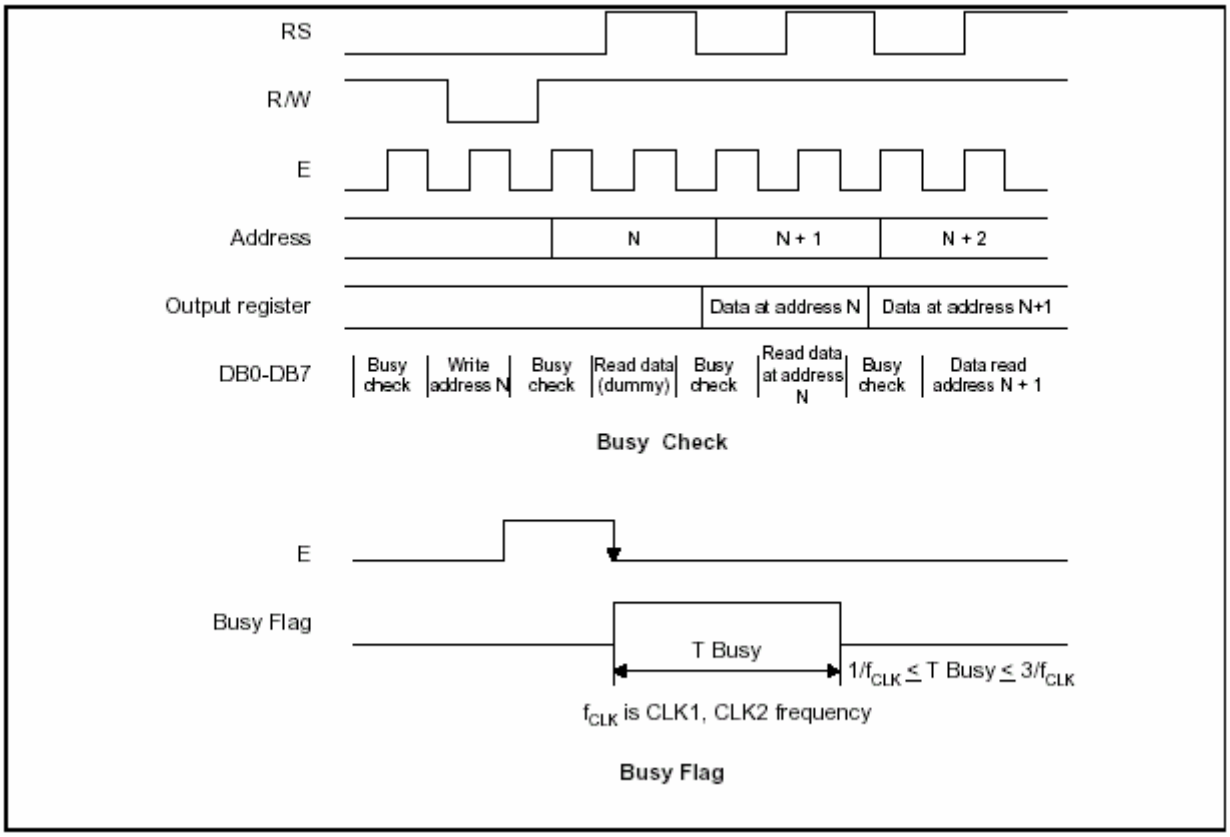
Table 2. Power Supply Initial Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Reset time	t_{RS}	1.0	-	-	μs
Rise time	t_R	-	-	200	ns



Busy Flag

Busy Flag indicates that SBN0064G is operating or no operating. When busy flag is high, SBN0064G is in internal operating. When busy flag is low, SBN0064G can accept the data or instruction. DB7 indicates busy flag of the SBN0064G.



Display ON / OFF Flip-Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non-selective voltage appears on segment output terminals. When flip-flop is set (logic high), non-selective voltage appears on segment output terminals regardless of display RAM data. The display on/off flip-flop can changes status by instruction. The display data at all segments disappear while RSTB is low. The status of the flip-flop is output to DB5 by status read instruction. The display on/off flip-flop synchronized by CL signal.

X Page Register

X page register designates pages of the internal display data RAM. Count function is not available. An address is set by instruction.

Y Address Counter

An Address is set by instruction and is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write data 1. The other way, off state, writes 0.

Display data RAM address and segment output can be controlled by ADC signal.

- ADC=H → Y-address 0:S1-Y address 63:S64
- ADC=L → Y-address 0:S64-Y address 63:S1

ADC terminal connects the VDD or Vss.

Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display. Bit data (DB<0.5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter. It is used for scrolling of the liquid crystal display screen.

DISPLAY CONTROL INSTRUCTION

The display control instructions control the internal state of the NT7108. Instruction is received from MPU to NT7108 for the display control. The following table shows various instructions.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display on/off	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L:OFF, H:ON
Set address (Y address)	L	L	L	H	Y address (0-63)						Sets the Y address in the Y address counter.
Set page (X address)	L	L	H	L	H	H	H	Page (0-7)			Sets the X address at the X address register.
Display Start line (Z address)	L	L	H	H	Display start line (0-63)						Indicates the display data RAM displayed at the top of the screen.
Status read	L	H	Busy	L	On/ Off	Reset	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset
Write display data	H	L	Write data								Writes data (DB0: 7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read display data	H	H	Read data								Reads data (DB0: 7) from display data RAM to the data bus.

DISPLAY ON/OFF

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

SET ADDRESS (Y ADDRESS)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address (AC0-AC5) of the display data RAM is set in the Y address counter. An address is set by instruction and increased by 1 automatically by read or write operations of display data.

SET PAGE (X ADDRESS)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

X address (AC0-AC2) of the display data RAM is set in the X address register. Writing or reading to or from MPU is executed in this specified page until the next page is set.

DISPLAY START LINE (Z ADDRESS)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

Z address (AC0-AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen. When the display duty cycle is 1/64 or others (1/32-1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

STATUS READ

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY

  When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.

  When BUSY is 0, the Chip is ready to accept any instructions.

- ON/OFF

  When ON/OFF is 1, the display is OFF.

  When ON/OFF is 0, the display is ON.

- RESET

  When RESET is 1, the system is being initialized.

  In this condition, no instructions except status read can be accepted.

  When RESET is 0, initializing has finished and the system is in usual operation condition.

WRITE DISPLAY DATA

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Writes data (D0-D7) into the display data RAM. After writing instruction, Y address is increased by 1automatically.

READ DISPLAY DATA

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Reads data (D0-D7) from the display data RAM. After reading instruction, Y address is increased by 1 automatically.

Absolute maximum rating

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	voltage on the V_{DD} pin(pad)	–0.3	+7.0	volt
V_{EE}	voltage on the V_{EE} pin(pad)	V_{DD} - 16		
V_{LCD} (note 2)	LCD bias voltage, V_{LCD}=V0-V5		13	
V_I	input voltage on any pin with respect to V_{SS}	–0.3	V_{DD} + 0.3	
P_D	power dissipation		200	mW
T_{stg}	storage temperature range	–55	+125	°C
T_{amb}	operating ambient temperature range	-30	+ 85	°C
Tsol (note 3)	soldering temperature/time at pin		260 °C, 10 Second	

Notes

1. The following applies to the Absolute Maximum Rating:
   a) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.
   b) The SBN0064G includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge (ESD). However, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
   c) Parameters are valid over operating temperature range unless otherwise specified.
   d) All voltages are with respect to V_{SS}, unless otherwise noted.
2. The condition V_{DD}(V0)≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 must always be met.
3. QFP-type packages are sensitive to moisture of the environment, please check the drypack indicator on the tray package before soldering. Exposure to moisture longer than the rated drypack level may lead to cracking of the plastic package or broken bonding wiring inside the chip.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS}, unless otherwise specified; T_{amb} = −20 to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage for logic		2.7	5.0	5.5	V
V_{NEG}	$V_{NEG}=V_{DD}-V_{EE}$				16	V
V_{LCD}	LCD bias voltage V_{LCD}= V0(V_{DD})-V5	Note 1.			13	V
V_{IL}	LOW level input voltage	For all inputs	0		0.8	V
V_{IH}	HIGH level input voltage	For all inputs	V_{DD}-2.2		V_{DD}	V
V_{OL}	LOW level output voltage of DB0~7 at I_{OL}=1.6 mA.		0.0		0.3	V
V_{OH}	HIGH level output voltage of DB0~7 at I_{OH}=-200μA.		V_{DD} – 0.3		V_{DD}	V
I_{LKG}	Leakage current of input pins	for all inputs			0.2	μA
I_{STBY}	Stand-by current at V_{DD}=5 volts	Note 2			3.0	μA
$I_{DD(1)}$	Operating current for display-only operation	Note 3			100	μA
$I_{DD(2)}$	Operating current for display and microcontroller access at t_{CYC}=1 MHz	Note 4			500	μA
C_{in}	Input capacitance of all input pins			5.0	8.0	pF
R_{ON}	LCD driver ON resistance	Note 5		5.0	7.5	KΩ

Notes:

1. LCD bias voltage V_{LCD} is V0 - V5. V0 should always be connected to VDD.
2. Conditions for the measurement: CLK1=CLK2=V_{DD}, measured at the V_{DD} pin.
3. This value is measured when the microcontroller does not perform any READ/WRITE operation to the chip and the chip is only performing display operation, with the following condition: 1/64 duty, $F_{CLK1,CLK2}$=250 KHz, frame frequency= 70Hz, and no loading for SEG0~63.
4. This values is measured when the microcontroller continuously performs READ/WRITE operation to the chip and the chip is also performing display operation with the following condition: 1/64 duty, $F_{CLK1,CLK2}$=250 KHz, frame frequency= 70Hz, and no loading for SEG0~63.
5. This measurement is for the transmission high-voltage PMOS or NMOS of SEG0~SEG63. Please refer to Section 16 for these driver circuit. The measurement is for the case when the voltage differential between the source and the drain of the high voltage PMOS or NMOS is 0.1 volts.

AC CHARACTERISTICS (V_{DD} = 5V ± 10%, Tamb = -20°C to +75°C)

Clock Timing

Characteristic	Symbol	Min	Type	Max	Unit
CLK1, CLK2 cycle time	tCY	2.5	-	20	μs
CLK1 "low" level width	tWL1	625	-	-	ns
CLK2 "low" level width	tWL2	625	-	-	
CLK1 "high" level width	tWH1	1875	-	-	
CLK2 "high" level width	tWH2	1875	-	-	
CLK1-CLK2 phase difference	tD12	625	-	-	
CLK2-CLK1 phase difference	tD21	625	-	-	
CLK1, CLK2 rise time	tR	-	-	150	
CLK1, CLK2 fall time	tF	-	-	150	

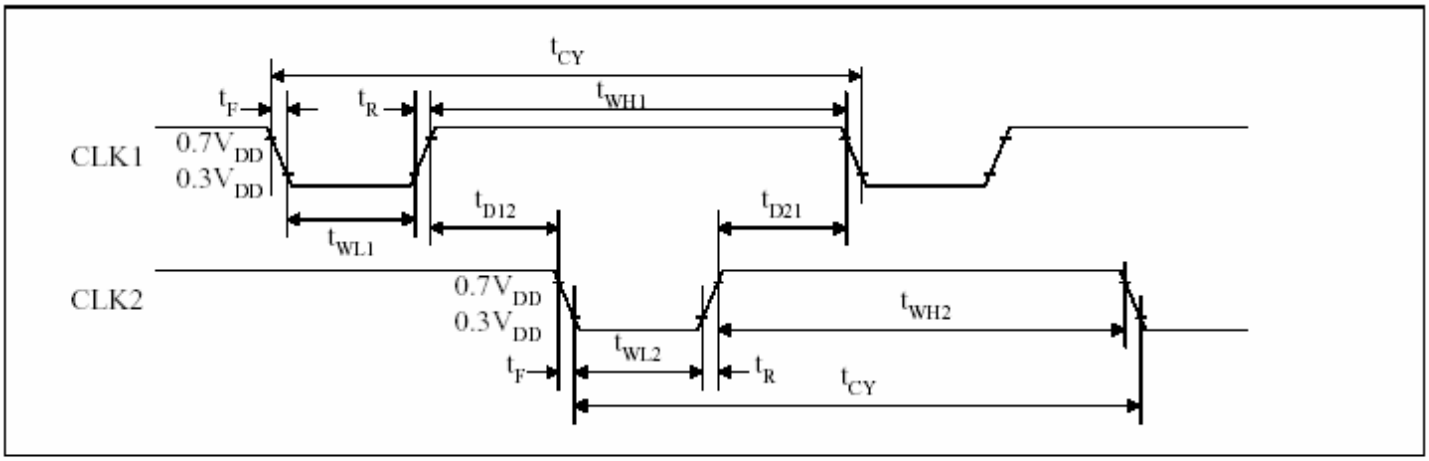


Figure 1. External Clock Waveform

Display Control Timing

Characteristic	Symbol	Min	Type	Max	Unit
FRM delay time	tDF	-2	-	2	μs
M delay time	tDM	-2	-	2	
CL "low" level width	tWL	35	-	-	
CL "high" level width	tWH	35	-	-	

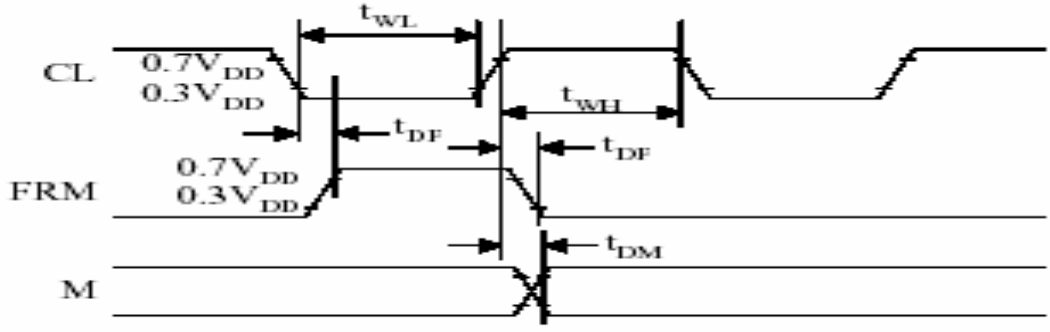


Figure 2. Display Control Waveform

MPU Interface

Characteristic	Symbol	Min	Type	Max	Unit
E cycle	t_C	1000	-	-	ns
E high level width	t_{WH}	450	-	-	
E low level width	t_{WL}	450	-	-	
E rise time	t_R	-	-	25	
E fall time	t_F	-	-	25	
Address set-up time	t_{ASU}	140	-	-	
Address hold time	t_{AH}	10	-	-	
Data set-up time	t_{DSU}	200	-	-	
Data delay time	t_D	-	-	320	
Data hold time (write)	t_{DHW}	10	-	-	
Data hold time (read)	t_{DHR}	20	-	-	

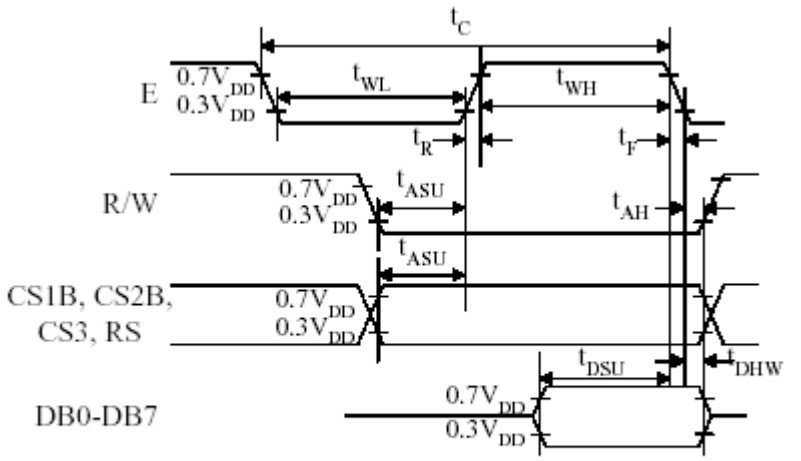


Figure 3. MPU Write Timing

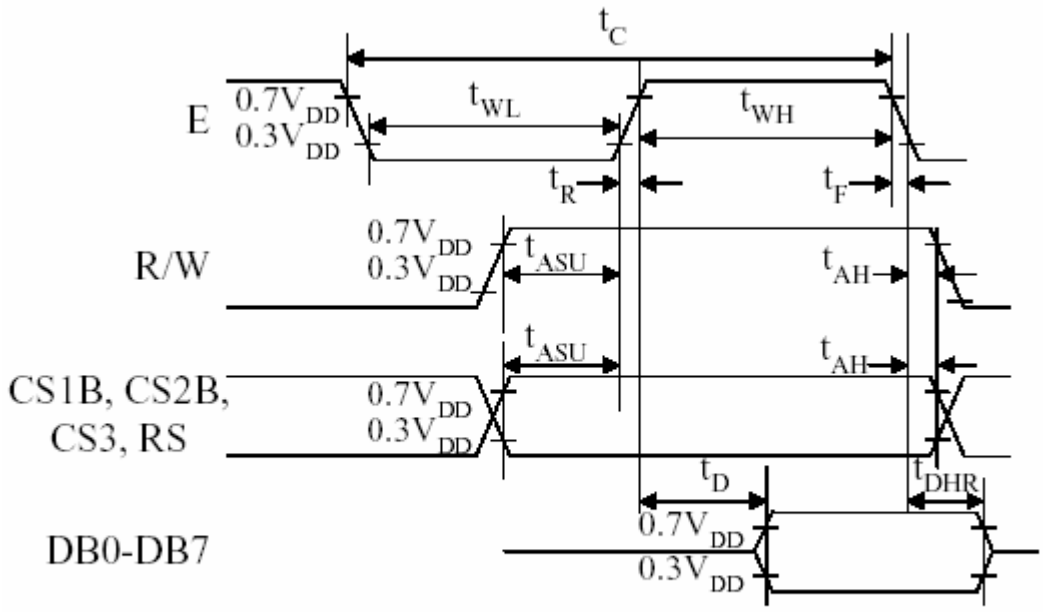
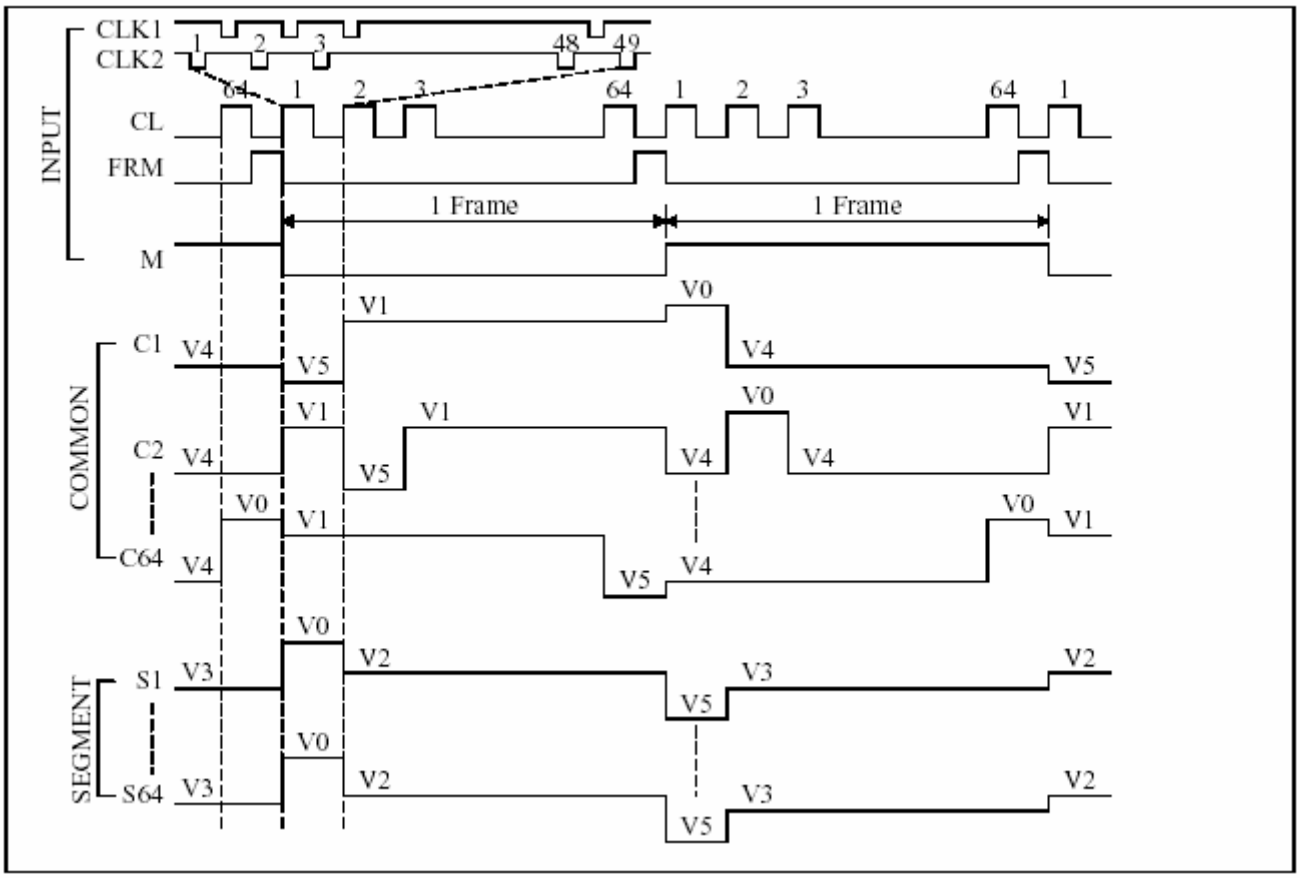
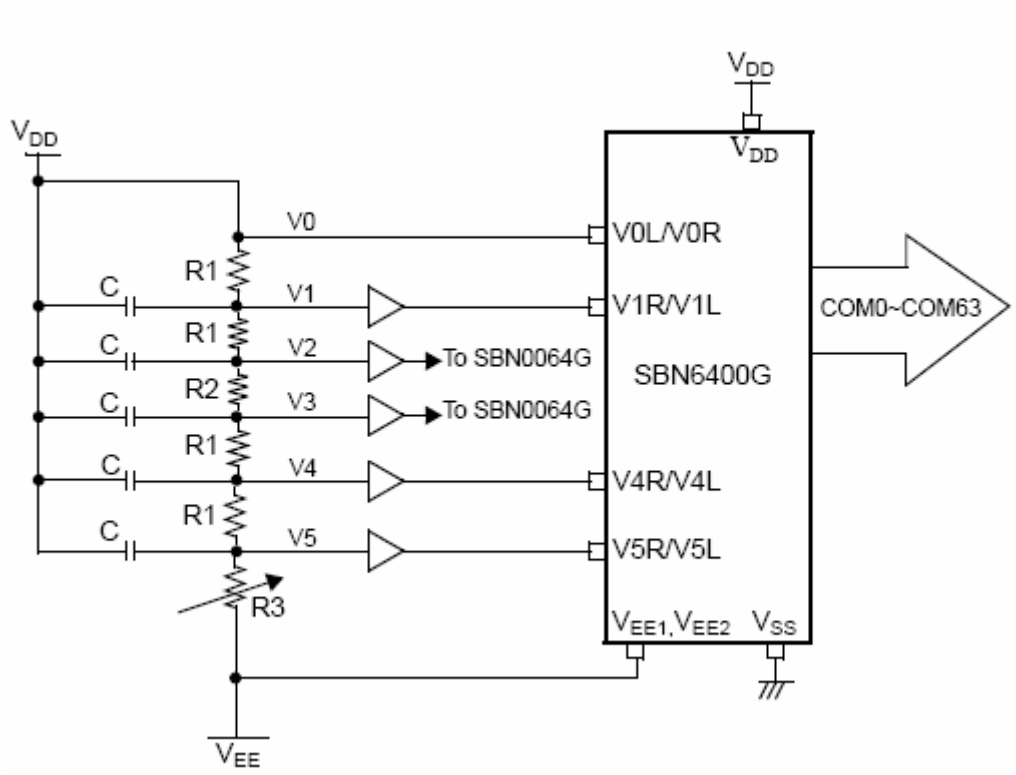


Figure 4. MPU Read Timing

TIMING DIAGRAM (1/64 DUTY)



LCD BIAS AND COMMON OUTPUT VOLTAGE



Duty	CL period	Bias	Resistor ladder
1/48	64 x CLK2	1/8	R2= 4 x R1
1/64	48 x CLK2	1/9	R2= 5 x R1
1/96	32 x CLK2	1/11	R2= 7 x R1
1/128	24 x CLK2	1/12	R2= 8 x R1

10.LED BACKLIGHT ELECTRO-OPTICAL CHARACTERISTIC

The module **GS-GB1286433YFYJ-C/R** has YELLOW-GREEN LED BACKLIGHT, we can prepare all types LED B/L of our customer'request.

ELECTRICAL/OPTICAL CHARACTERISTICS(T=25℃):

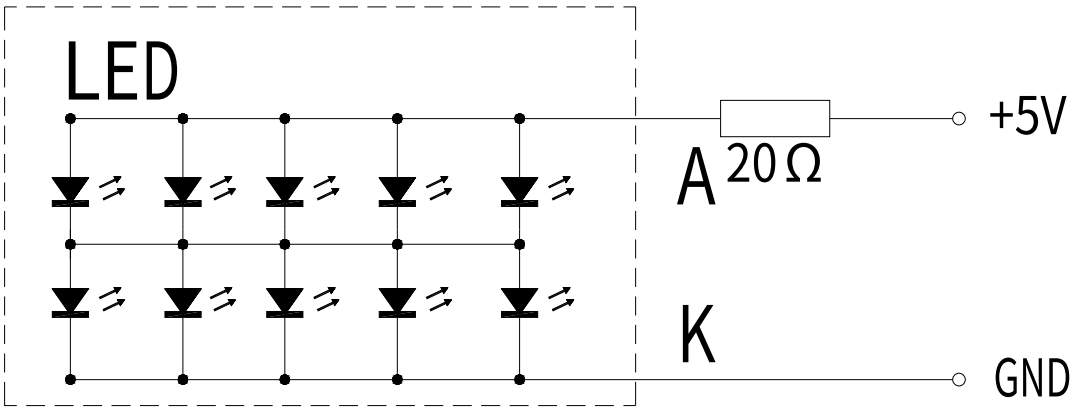
ITEM	MIN.	TYPE	MAX.	UNIT	CONDITION
Forward Voltage	4.0	4.2	4.4	V	
Forward Current	-	50	100	mA	5V
Power Dissdipation			440	mW	5V
Luminance	55	70	-	cd/m^2	5V
Wave length Range	569	572	575	nm	Yellow/Green
Operating Temp Range	-30		75	℃	
Storage Temp Range	-40		80	℃	

备注：亮度值为图示5个测试点的平均值，

亮度偏差为±30%,均匀度≥70%

颜色偏绿

符合ROHS标准



测试电路

11.CHECKING STANDARD

11.1 Inspection level：检验标准

Sampling procedure: General inspection levels Ⅱ and single sampling plans for normal inspection of ISO2859.

抽样方案：按 ISO2859 的一般检验水准Ⅱ级方案进行单次抽样。

Item 不良类别	Indication 说明	AQL
Major Nonconformity (MA) 严重不良	Function 功能不全	0.4
	Size 尺寸不符	
Minor Nonconformity (MI) 次要不良	Effects on LCD appearance but not on function 不影响产品功能但对外观有影响	1.0

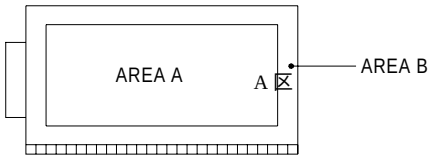
11.2 The area of LCD：LCD 区域定义

Viewing area：The uncovered area after assembling frame.

可视区(A 区)：装外框后 LCD 所显露的区域

Non-viewing area：Covered area after assembling frame.

非可视区（B 区）：装外框后 LCD 被遮盖的区域



11.3 Inspection condition： 外观检查条件

11.3.1 The inspection should be done under 40W fluorescent light and visual inspection distance is 30cm.

须在 40W 的日光灯下，目测距离 30cm 检查

11.3.2 Back-Lights or reflective boards should be adopted for inspecting transmissive LCDs.

透射性的 LCD 检验时，下面需有背光源或反光板

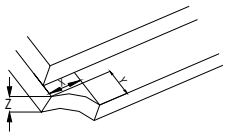
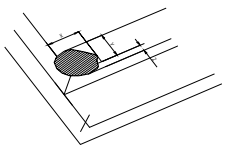
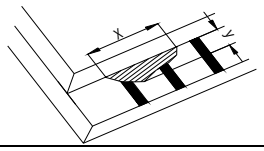
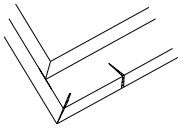
11.3.3 The visual direction should be viewing angle range 目检范围按视角范围检测

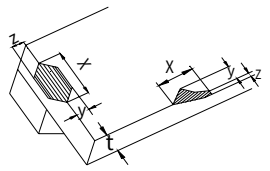
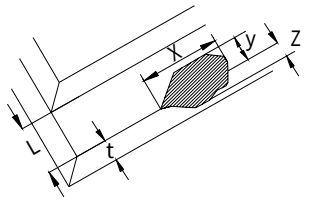
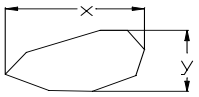
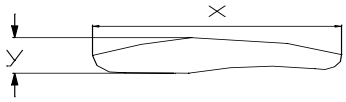
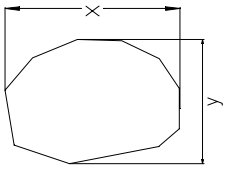
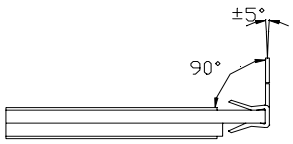
11.3.4 This kind of situation will be judged qualificatory one that defection of product in B area won't effect customer's assembly and product quality

原则上 B 区域的不良不影响客户装配与产品品质时判为良品.

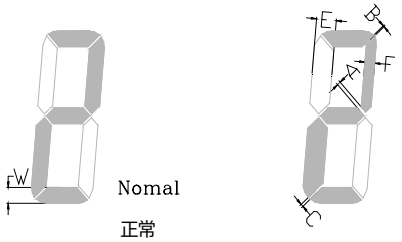
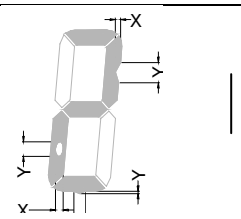
11.4 Appearance Standard：外观标准

11.4.1 Appearance Nonconformity 外观不良

Item 项目		Figure 示意图	Criteria 判断标准	MA / MI
Glass Nonconformity 玻璃不良	Glass Corner Breakage 角破损		1、X≤3mm and don't touch pin X≤3mm 和不达到 PIN 的引线 2、Y out of seal resin Y 不进入框线 3、Z ignore ACC Z 不计 接收	MI
			1、X≤1/8 Length of LCD side X≤1/8 边长 2、Y out of area A Y 不进入可视区 3、Z≤t Z don't touch seal resin ACC Z≤t Z 不到达框线 接收	
	Extra Glass Ledge 突出		1、 X ignore X 不计 2、 Y≤1/3 Length of conductor ACC Y≤1/3 PIN 长 接收	MI
Glass Nonconformity 玻璃破损	Crack 裂缝		Any crack any where REJ 任何区域有裂痕 拒收	MA

Glass Nonconfor m-ity 玻璃不良	Glass Side Breakage 边破损		1、 X≤1/4 Length of LCD side X≤1/4 边长 2、Y out of area A Y不进入可视区 3、Z≤t Z don't touch seal resin ACC Z≤t 不到达框线 接收	MI
			1、 X≤ 1/4 Length of LCD side X≤ 1/4 LCD边长 2、 Y≤1/3L (L: Length of conductor) Y≤1/3 PIN宽 3、Z≤t don't touch seal resin ACC Z≤t 不到达框线 接收	MI
Color Variation 彩虹			At most 2-color samples are acceptable but have no color difference in the brightest state. ACC 无明显两色之分 接收	MI
Point Like flaw 点状不良			Φ= (X+Y) /2 Φ≤0.25mm ACC Distance between 2 spots>5mm 接收 Φ= (X+Y) /2 Φ≤0.25mm 两点间距 > 5mm	MI
Scratching Line 线状刮伤			X≤ 6mm y≤ 0.08mm ACC X≤ 6mm y≤ 0.08mm 接收	MI
Polarizer Nonconfor m-ity 偏光片 不良	Deflectie Sticking 贴歪		According to the tolerance specified in engineering drawing. ACC 符合工程图要求的公差 接收	MI
	Faulty Sticking 贴错		REJ 拒收	MA
	Air Bubble 气泡		Φ= (X+Y) / 2 Size (mm) 尺寸 / Qty allowed 允许个数 0.2<Φ≤0.5 / 2 Distance between 2 spots>5mm 两点间距>5mm Ignore if out of viewing area. 可视区外忽略不计	MI
Electrode & pin Nonconfor m-ity 电极与 PIN 脚不良	Pin Length PIN长		Non-conformity with engineering drawing REJ 与工程图不符 拒收	MA
	Pin Deflec- tion PIN歪斜		Deviation exceeds 5 degree REJ 偏差>5⁰ 拒收 According to the tolerance specified in engineering drawing 若工程图有规定范围，则依图面规格	MI
	Pin body With resin PIN上有胶		REJ 拒收	MI
	Deflectin Frame Lines 切斜		Deviation between two ends exceeds 0.25mm REJ 两端相差 0.25mm 拒收	MI

11.4.2 Electro-optical Nonconformity：电性不良

Item 项目	Figure 示意图	Criteria 判断标准	
Open Circuit 断路		REJ 拒收	MA
Short Circuit 短路		REJ 拒收	MA
Cross Display 交叉显示		Refer to specimen 以样片为准	MI
Trans Formation Of Segment 图形变形		1、Segment 笔段 (E-W) ≤W/3，(W-F) ≤W/3，(E-F) ≤ 0.3mm W: Width of design W 指设计宽度 2、Segment Interval 笔段间距 (A-C) ≤C/3，(C-B) ≤C/3，(A-B) ≤0.25mm C: Width of design C 指设计宽度 ACC 接收	MA
Pin Holes And Cracks In Segment 多、缺亮		ϕ= (X+Y) /2 ϕ≤0.3mm Distance between 2 spots＞5mm 两点间距＞5mm ACC 接收	MI
After Image Fade-out 鬼影、字淡		Refer to specimen , but pressure difference less than 0.2 volt under the same visual angle ACC 参考样片，但在同一视角下电压偏差≤0.2V 接收	MI